A Quantitative Analytical Model of Paralleled SiC MOSFETs for Calculating Unbalanced Switching Currents and Energy

Jianwei Lv, Cai Chen, *Member, IEEE*, Yiyang Yan, Baihan Liu, *Graduate Student Member, IEEE*,
Zexiang Zheng, and Yong Kang, *Fellow, IEEE*

***Abstract*—Uneven dynamic currents between paralleled silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) can cause unbalanced switching losses, challenging the circuit reliability. Therefore, it is essential to quantitatively evaluate unbalanced dynamic currents during circuit design and application. However, the existing calculation methods face challenges in modeling or are time-consuming in circuits with paralleled MOSFETs. To address these issues, this article presents an analytical model to calculate the unbalanced switching currents and switching energy, which is applicable to circuits with any parallel number (n) and easier to use than Spice simulation method. To address the challenge of the high circuit order, the power and driving circuits are decoupled and modeled, reducing the equation order to $3n-1$. To handle the numerous parasitic mutual inductances, the inductance matrices are used for modeling. Moreover, the nonlinear die parameters and their temperature dependence are considered to guarantee accuracy. The accuracy of the presented model is verified by experiments. The model-calculated waveforms fit the tested results well. Under various switching speeds, load currents, and die temperatures, the model can accurately predict the dynamic current differences and unbalanced switching energy, with calculation errors lower than 8% for the current differences and 11% for the switching energy.**

***Index Terms*—Analytical switching model, multichip sic power modules, paralleled sic metal-oxide-semiconductor field-effect transistors (MOSFETS) , silicon carbide (SiC) MOSFET , unbalanced dynamic currents.**

I. INTRODUCTION

Due to the high switching speed, high efficiency, and high thermal performance, silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) have been widely used in many applications [1], [2], [3], [4]. However, because of the immature manufacturing technique, the maximum current rating of a SiC MOSFETs bare die is generally lower than 150 A. Therefore, paralleled devices or dies are often used to enlarge the current capacity [5]. Unbalanced dynamic and static currents between paralleled SiC MOSFETs can cause unbalanced losses, leading to unbalanced junction temperatures. To ensure stability and security, the current capacity of paralleled SiC MOSFETs is usually derated. Moreover, the solder layer of the die with a higher junction temperature will degrade earlier, further increasing its temperature and shortening the device's lifetime [6], [7]. Therefore, when designing and applying circuits with paralleled SiC MOSFETs, merely evaluating the total losses on the switch is insufficient. It is also necessary to quantitatively evaluate the unbalanced currents and the resulting unbalanced losses on the paralleled MOSFET dies. In this way, the maximum losses on a single die can be obtained and used for design. The unbalanced static currents are caused by the unbalanced parasitic inductances and conduction resistances ($R_{\mathrm{ds(ON)}}$) in the paralleled power branches, which are easy to analyze and calculate [6]. However, due to the complex switching transients, the mechanisms of unbalanced dynamic currents are more complicated, making quantitative analysis difficult [8], [9]. Especially under light loads or high switching frequencies, the switching losses may be much larger than the conduction losses [10], [11]. It is of great significance to accurately calculate the unbalanced dynamic currents and switching energy of parallel SiC MOSFETs.

Dynamic current sharing mechanisms have been investigated in many research [6], [12], [13], [14], [15], [16], [17], [18], [19]. Sadik et al. [12], Helong et al. [13], Lim et al. [14], and Haihong et al. [15] found that in circuits without Kelvin-source connections, the unbalanced dynamic currents are mainly caused by unbalanced threshold voltages (V_{th}) and parasitic common-source inductances. In [6], [16], and [17], it is found that the unbalanced dynamic currents are caused by unbalanced threshold voltages and parasitic power-source inductances in Kelvin-source connected circuits. The unbalanced drain and driving inductances have little effect. Ge et al. [18] and Lv et al. [19] further considered the influences of parasitic mutual inductances. It is found that the parasitic power-driving mutual inductances and the drain-source mutual inductances also have a significant impact. These works reveal the factors that affect unbalanced dynamic currents. During design and manufacturing processes, the differences in die characteristics can be well limited by chip screening [16]. However, the unbalanced parasitic

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The authors are with the State Key Laboratory of High Density Electrical Energy Conversion, Huazhong University of Science and Technology, Wuhan 430074, China (e-mail: jianweil@hust.edu.cn; caichen@hust.edu.cn; yanyiyang@hust.edu.cn; loubeckham@hust.edu.cn; zzx_huster@hust.edu.cn; ykang@mail.hust.edu.cn).

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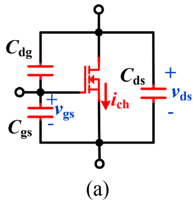


(a) (b) (c)

Fig. 1. Equivalent circuit models of SiC MOSFETs. (a) Equivalent circuit model. (b) Circuit model in saturation and cut-off regions. (c) Circuit model in Ohim region.

self and mutual inductances will still cause unbalanced dynamic currents, which is difficult to absolutely balance, especially in power modules. Hence, it is necessary to establish quantitative models to evaluate the unbalanced dynamic currents under the unbalanced circuit layouts, where the nonlinear MOSFET parameters have to be considered to guarantee accuracy [20]. In the existing current sharing research, many parameters are simplified, and the nonlinearities of the MOSFETs are neglected to analyze the parameter influences clearly. Therefore, the established theoretical models cannot be used for quantitative analysis.

To calculate MOSFET switching transients and switching energy accurately, researchers established many quantitative switching models. They can be divided into three categories according to the MOSFET models: 1) physical models, 2) behavioral models, and 3) analytical models.

Physical models build two-dimensional (2-D) or 3-D models of MOSFETs based on the semiconductor theory. The models are solved by finite element numerical calculations. Combined with the circuits outside the MOSFET, high-precision results can be obtained, and internal physical processes can be analyzed [21], [22]. However, the MOSFET physical structure and parameters are needed, which is usually not available. Moreover, the models are solved by finite-element numerical method, which is time-consuming [20], especially when multiple MOSFETs are paralleled.

Behavioral models establish circuit equations based on the MOSFETs' equivalent circuit, as shown in Fig. 1(a), where the characteristic expressions of the components are obtained by physical equations or curve fitting. The circuit equations are usually solved by simulation software [23], [24]. Behavioral models can be solved faster than physical models with high accuracy. It is widely used to build MOSFET Spice models. Currently, Spice circuit simulation is the main method to calculate the unbalanced dynamic currents between paralleled SiC MOSFETs, where the parasitic self and mutual inductances are obtained by electromagnetic simulations [17]. However, this method has some shortcomings. First, the partial inductance matrix of the circuit needs to be imported into the simulation software. The corresponding circuit symbol needs to be established based on the same pin order as the spice file of the inductance matrix. When the parallel number is large, the symbol has many pins, making its creation process cumbersome. When the parallel number changes, the symbol needs to be recreated [25]. Second, it is not easy to modify the internal parameters of the sealed inductance spice model during simulation. Thus, it is difficult to investigate the influences of the inductances individually by simulation. Moreover, it cannot provide insight into the switching processes. Third, it often suffers from convergence problems due to the numerous nonlinear parameters of the paralleled MOSFETs. It is time-consuming to calculate a large number of operating points [26]. Moreover, the construction process of MOSFET Spice models is complicated, with many curve fitting and Spice editing processes. High-precision curve fitting is challenging. When the die characteristics change, the curves need to be refitted, and when the fitting accuracy is insufficient, further modifications to the fitting functions are needed [27]. Though the Spice models of many commercial MOSFETs are provided, the parameters of the models may be different from those of the actual MOSFETs due to different die batches. Furthermore, parameter corrections of the official Spice models are inconvenient due to their complicated fitting functions.

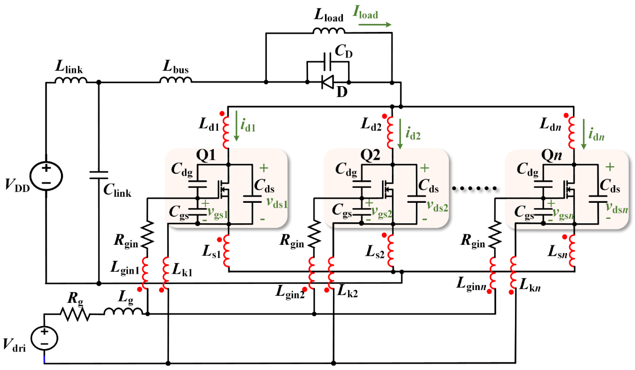


Fig. 2. Typical circuit model with n paralleled MOSFETs.

Compared to physical and behavioral models, analytical models based on simplified MOSFET equivalent circuits are more convenient and helpful. They are based on the analytical equations constructed in different time intervals, where the MOSFETs are simplified to the model in Fig. 1(b) and (c) according to different working regions. Analytical models are able to overcome the drawbacks of physical and behavioral models. They can be solved faster without convergence problems, and are easier to incorporate with circuit and MOSFET parameters and massive calculating points [28]. Nayak and Hatua [29], Alexakis et al. [30], Rodríguez et al. [31], and Wang et al. [32] established analytical models to calculate switching energy. To obtain closed-loop expressions, many parameters are simplified or neglected, influencing the calculating accuracy. To improve the accuracy, Xie et al. [20] and Wu et al. [33] established and solved the state differential equations of each time interval. In this way, all of the parasitic inductances and the nonlinear parameters can be included, and precise transient waveforms can be obtained. However, the analytical models are based on circuits with a single MOSFET. In circuits with multiple paralleled MOSFETs, the circuit order is much higher, and the circuit parameter number is large due to the parasitic mutual inductances between any two of the branches. This makes it challenging to establish and solve the differential equations. For example, the order of the circuit with n paralleled MOSFETs, as shown in Fig. 2, is $5n$, and the parasitic inductance number is $4n^2 - n + 3$.

To calculate the unbalanced dynamic currents and switching energy and address the above issues, this article presents a novel analytical switching model of paralleled SiC MOSFETs, which can be used in circuits with any parallel number. The contributions are as follows.

1) The analytical model of paralleled SiC MOSFETs is presented for the first time. All of the parasitic self and mutual inductances, the nonlinear MOSFET parameters, and their temperature dependence are considered. Thus, high accuracy is achieved.
2) The power and driving circuits are separated by simplification to achieve decoupled modeling between the two circuits. In this way, the maximum circuit order is reduced to $3n-1$. Moreover, the inductance matrices are directly used to establish the model, to include and handle all the parasitic inductances. The challenges of high circuit order and numerous circuit parameters encountered by the existing analytical models are addressed.
3) Compared to Spice simulation, the presented model can be calculated quickly without convergence problems. When investigating the influences of the parasitic inductances, they can be directly changed by modifying the inductance matrices. Moreover, the postprocessing is more convenient. Thus, it is more suitable for batch calculations. The model eliminates the cumbersome simulation modeling and high-precision curve fitting processes of Spice simulation and is compatible with different circuit parameters and parallel numbers. When the parallel number or die parameters change, it is only needed to update the parameter inputs without the complex remodeling process, making it easier to use.

The rest of this article is organized as follows. In Section II, the SiC MOSFET's and diode's equivalent circuit models are given. On this basis, the quantitive analytical model is established in Section III. The calculation method is also presented. Then, the accuracy of the model is verified in Section IV by a SiC power module, where four MOSFETs are paralleled as one switch. Finally, Section V concludes this article.

II. Equivalent Circuit Models of SiC MOSFET and Diode

To establish the analytical model, the equivalent circuit models of SiC MOSFETs and diodes are first given in this section. A SiC MOSFET can be equivalent to an idea MOSFET with three junction capacitances, as shown in Fig. 1(a). C_{ds} is the drain-source capacitance, C_{dg} is the drain-gate capacitance, and C_{gs} is the gate-source capacitance. The channel current i_{ch} of the idea MOSFET is determined by the gate-source voltage v_{gs} and the drain-source voltage v_{ds}, as shown in Fig. 3, which is called the output characteristic. Based on the different regions in the output characteristic, the MOSFET can be divided into three working states.

1) When $v_{\mathrm{gs}} \leq V_{\mathrm{th}}$, the MOSFET channel is cut OFF. The channel current i_{ch} is equal to 0.

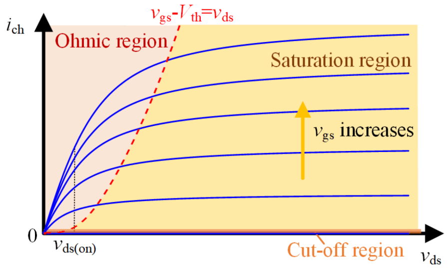
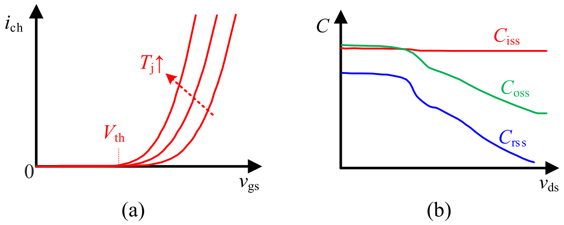


Fig. 3. Output characteristic of SiC MOSFETs.



(a) (b)

Fig. 4. (a) Transfer characteristic and (b) junction capacitances of SiC MOSFETs.

2) When $0 < v_{\mathrm{gs}} - V_{\mathrm{th}} \leq v_{\mathrm{ds}}$, the channel works in the saturation region, where i_{ch} approximately does not change with v_{ds}.

In the cut off and saturation regions, the ideal MOSFET can be equivalent to a current source controlled by v_{gs}, as shown in Fig. 1(b). The cut off and the saturation regions are collectively defined as the controlled region. The relationship between i_{ch} and v_{gs} is shown in Fig. 4(a), which is called the transfer characteristic. It can be seen from Fig. 4(a) that after v_{gs} reaches the threshold voltage V_{th}, i_{ch} increases with v_{gs} increases. The i_{ch} under the same v_{gs} increases with the increased temperature T_{j}, and V_{th} decreases with the increased T_{j}. The relationship between i_{ch} and v_{gs} can be expressed by

$$i_{\mathrm{ch}}(v_{\mathrm{gs}}, T_{\mathrm{j}}) = g_{\mathrm{m}}(v_{\mathrm{gs}}, T_{\mathrm{j}}) \cdot (v_{\mathrm{gs}} - V_{\mathrm{th}}(T_{\mathrm{j}})) \tag{1}$$

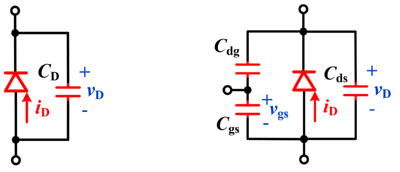
where $g_{\mathrm{m}}(v_{\mathrm{gs}}, T_{\mathrm{j}})$ is the transconductance and varies with v_{gs} or T_{j}. The nonlinearity of the transfer characteristic and its temperature dependence are considered in the presented model to achieve high accuracy.

3) When $v_{\mathrm{gs}} - V_{\mathrm{th}} > v_{\mathrm{ds}} > 0$, the MOSFET works in the ohmic region and can be equivalent to a resistor, as shown in Fig. 1(c). The value of the resistance is determined by v_{gs}, v_{ds}, and T_{j} as

$$R_{\mathrm{ds(on)}}(v_{\mathrm{ds}}, v_{\mathrm{gs}}, T_{\mathrm{j}}) = \frac{v_{\mathrm{ds}}}{i_{\mathrm{ch}}(v_{\mathrm{ds}}, v_{\mathrm{gs}}, T_{\mathrm{j}})} = \frac{v_{\mathrm{ds}}}{f(v_{\mathrm{ds}}, v_{\mathrm{gs}}, T_{\mathrm{j}})} \tag{2}$$

where f is the function that describes the output characteristic in the ohmic region. The nonlinearity and temperature dependence of the ohmic-region output characteristic are also considered.

The junction capacitances are usually given as the input capacitance C_{iss}, the output capacitance C_{oss}, and the reverse capacitance C_{rss}. Their relationships with C_{ds}, C_{gd}, and C_{gs} are



(a) (b)

Fig. 5. Equivalent models of (a) SiC Diodes and (b) SiC MOSFETs working in third quadrant.

expressed by

$$\begin{cases} C_{\mathrm{gd}} = C_{\mathrm{rss}} \\ C_{\mathrm{ds}} = C_{\mathrm{oss}} - C_{\mathrm{rss}} \\ C_{\mathrm{gs}} = C_{\mathrm{iss}} - C_{\mathrm{rss}} \end{cases} . \tag{3}$$

Fig. 4(b) shows the junction capacitances under logarithmic coordinates. They are also nonlinear and decrease as v_{ds} increases. To guarantee accuracy, the nonlinear junction capacitances are also considered in the model.

The freewheeling diode can be equivalent to a diode with its junction capacitance C_{D}, as shown in Fig. 5(a). The diode current i_{d} can be expressed by

$$i_{\mathrm{D}}(v_{\mathrm{D}}, T_{\mathrm{j}}) = \begin{cases} 0, v_{\mathrm{D}} < -V_{\mathrm{D0}}(T_{\mathrm{j}}) \\ \frac{-v_{\mathrm{D}} - V_{\mathrm{D0}}(T_{\mathrm{j}})}{R_{\mathrm{D}}(T_{\mathrm{j}})}, v_{\mathrm{D}} > -V_{\mathrm{D0}}(T_{\mathrm{j}}) \end{cases} \tag{4}$$

where $R_{\mathrm{D}}(T_{\mathrm{j}})$ is the equivalent resistance and $V_{\mathrm{D0}}(T_{\mathrm{j}})$ is the turn-ON threshold voltage [20]. They are related to the die temperature T_{j}. The junction capacitance C_{D} is also nonlinear and decreases as v_{D} increases. If SiC MOSFETs are used as the freewheeling diodes, they can also be equivalent to a diode with the junction capacitances, as shown in Fig. 5(b). The junction capacitors can be equivalent to a single capacitor $C_{\mathrm{D}} = C_{\mathrm{dg}}C_{\mathrm{gs}}/(C_{\mathrm{dg}} + C_{\mathrm{gs}}) + C_{\mathrm{ds}}$ as the circuit in Fig. 5(a). During switching transients, v_{gs} is clamped to zero or negative, and C_{dg} is usually much lower than C_{gs} in a wide v_{ds} range. Thus, $C_{\mathrm{D}} \approx C_{\mathrm{dg}} + C_{\mathrm{ds}} = C_{\mathrm{oss}}$. The nonlinearity of C_{D} and the temperature dependence of R_{D} and V_{D0} are also considered.

III. ANALYTICAL SWITCHING MODEL FOR CALCULATING UNBALANCED DYNAMIC CURRENTS AND SWITCHING ENERGY

The analytical switching model for calculating the unbalanced dynamic currents and switching energy is presented in this section. The circuit model is presented first, and simplified to separate the power and driving circuits. Second, based on the simplified circuit model, decoupled modeling between the two circuits and, thus, reduced equation order is achieved, and the differenced dynamic currents are calculated. Combining the calculated differenced currents and the average currents, the total unbalanced switching currents and energy are obtained.

A. Circuit Model and Switching Waveforms

Based on the equivalent model of SiC MOSFETs, the typical double-pulse test (DPT) circuit with n paralleled MOSFETs is shown in Fig. 2 and used for analysis and modeling. In a practical circuit, the branches closed to the paralleled MOSFETs are complexly connected and magnetic coupled. Their parasitic self and mutual inductances are all equivalent into the paralleled branches, as shown by the red inductances in Fig. 2. The self-inductances are depicted as the drain inductances $L_{\mathrm{d}1}{\sim}L_{\mathrm{d}n}$, the power-source inductances $L_{\mathrm{s}1}{\sim}L_{\mathrm{s}n}$, the gate inductances $L_{\mathrm{gin}1}{\sim}L_{\mathrm{gin}n}$, and the driving-source inductances $L_{\mathrm{k}1}{\sim}L_{\mathrm{k}n}$. There are mutual inductances between any two of the paralleled branches. $M_{\mathrm{d}jl}$ represents the mutual inductances between the j_{th} and l_{th} drain branches. $M_{\mathrm{s}jl}$, $M_{\mathrm{g}jl}$, and $M_{\mathrm{k}jl}$ have similar definitions. $M_{\mathrm{d}jgl}$ is the drain-gate mutual inductance between the j_{th} drain branch and l_{th} gate branch. $M_{\mathrm{s}jgl}$, $M_{\mathrm{d}jkl}$, $M_{\mathrm{s}jkl}$, $M_{\mathrm{d}jsl}$, and $M_{\mathrm{g}jkl}$ have similar definitions. The positive directions of the magnetic couplings are defined as the red dots. For the bus branches and driving branches that have no magnetic coupling with the paralleled branches, the parasitic inductances are defined as L_{link}, L_{bus}, and L_{g}. The circuit model also contains the bus voltage source V_{DD}, the bus capacitor C_{link}, the load inductance L_{load}, the gate resistors R_{g} and R_{gin}, and the driving voltage source V_{dri}.

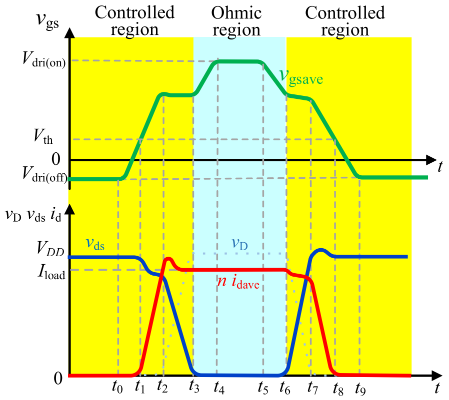


Fig. 6. Switching waveforms of the DPT circuit.

The typical switching waveforms of the circuit are shown in Fig. 6, where v_{gsave}, v_{ds}, i_{dave} are the average values of $v_{\mathrm{gs}1}{\sim}v_{\mathrm{gs}n}$, $v_{\mathrm{ds}1}{\sim}v_{\mathrm{ds}n}$, $i_{\mathrm{d}1}{\sim}i_{\mathrm{d}n}$, respectively. I_{load} is the load current. $V_{\mathrm{dri(ON)}}$ and $V_{\mathrm{dri(OFF)}}$ are the high and low driving voltages, respectively. During t_0–t_4, the MOSFETs are turned ON. The turn-ON period can be divided into three intervals.

1) During t_0–t_1, v_{gs} begin to increase under $V_{\mathrm{dri(ON)}}$. The MOSFETs work in the cut-off region.
2) During t_1–t_3, v_{gs} go above V_{th}. The MOSFETs work in the saturation region. The drain currents i_{d} increase, and the diode current i_{D} is reduced, as v_{gs} rise. When i_{dave} reaches I_{load} at t_2, i_{D} is reduced to 0. Then, v_{ds} begins to reduce fast, and v_{D} is increased.
3) During t_3–t_4, v_{gs} continue to increase, and the MOSFETs work in the ohmic region. During $t_5{\sim}t_9$, the MOSFETs are turned OFF.

This period can also be divided into three intervals.

1) During t_5–t_6, v_{gs} begin to decrease under $V_{\mathrm{dri(OFF)}}$. The MOSFETs work in the ohmic region. At t_6, the MOSFETs enter the saturation region.
2) During t_6–t_8, the MOSFETs work in the saturation region. v_{ds} is quickly increased, and i_{ch} and i_{d} decrease as v_{gs} decreases.

3) After t_8, v_{gs} are reduced below V_{th}. The MOSFETs go into the cut-off region.

During t_0–t_3 and t_6–t_9, the MOSFETs work in the controlled region, where the channel currents are controlled by v_{gs}. The MOSFETs are modeled by Fig. 1(b). During t_3–t_6, they work in the ohmic region and are modeled by Fig. 1(c).

B. Simplified Circuit Model

The order of the nonsimplified circuit in Fig. 2 is $5n$. To establish the model with reduced order and concise form, the circuit model needs to be simplified first. The following assumptions and equivalences are made during the turn-ON (t_0–t_4) and the turn-OFF transients (t_5–t_9).

1) v_{gs} of the MOSFETs can be expressed by

$$v_{\mathrm{gs}} = \frac{1}{C_{\mathrm{iss}}}\int\left(i_{\mathrm{g}} + C_{\mathrm{dg}}\frac{\mathrm{d}v_{\mathrm{ds}}}{\mathrm{d}t}\right)\mathrm{d}t. \tag{5}$$

Hence, as for the driving circuits, the change of v_{gs} are caused by the charge and discharge of C_{iss} through the gate currents i_{g}. Moreover, the effects of $C_{\mathrm{dg}}\mathrm{d}v_{\mathrm{ds}}/\mathrm{d}t$ are equivalent to the current sources i_{c} controlled by v_{ds}, which can be expressed as

$$i_{\mathrm{c}} = -C_{\mathrm{dg}}\mathrm{d}v_{\mathrm{ds}}/\mathrm{d}t. \tag{6}$$

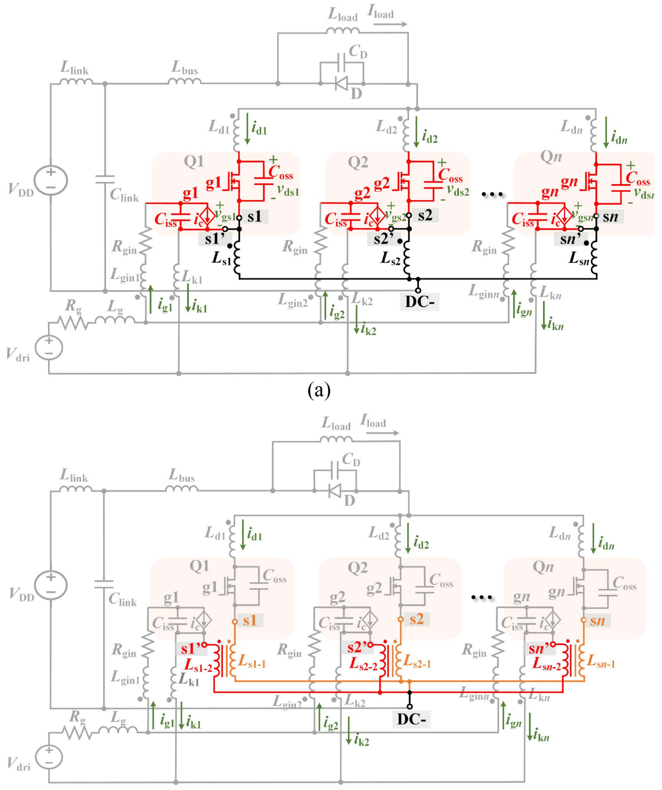
As for the power loop, during the switching transients, the drain-source voltages v_{ds} are mainly borne by the drain-gate capacitances C_{dg} and C_{ds} in a wide v_{ds} range, and C_{gs} is considered a short circuit. Then, the circuit model is equivalent to Fig. 7(a). The simplified MOSFET models are shown by red color.

2) The black part in Fig. 7(a) has $2n+1$ external connection points: s1∼sn, s1'∼sn', and dc-. Taking dc- as the zero potential point, the potentials of other points can be expressed as

$$\boldsymbol{v}_{\mathrm{s}} = \boldsymbol{v}_{\mathrm{s}}' = \boldsymbol{L}_{\mathrm{s}}(\dot{\boldsymbol{i}}_{\mathrm{d}} + \dot{\boldsymbol{i}}_{g} - \dot{\boldsymbol{i}}_{k}) + \boldsymbol{M}_{\mathrm{ds}}\,\dot{\boldsymbol{i}}_{\mathrm{d}} + \boldsymbol{M}_{\mathrm{gs}}\,\dot{\boldsymbol{i}}_{g} - \boldsymbol{M}_{\mathrm{ks}}\,\dot{\boldsymbol{i}}_{k} \tag{7}$$

where $\boldsymbol{v}_{\mathrm{s}} = [v_{\mathrm{s}1}\ v_{\mathrm{s}2}\ \ldots\ v_{\mathrm{s}n}]^{\mathrm{T}}$, $\boldsymbol{v}_{\mathrm{s}}' = [v_{\mathrm{s}1}'\ v_{\mathrm{s}2}'\ \ldots\ v_{\mathrm{s}n}']^{\mathrm{T}}$, $\boldsymbol{i}_{\mathrm{d}} = [i_{\mathrm{d}1}\ i_{\mathrm{d}2}\ \ldots\ i_{\mathrm{d}n}]^{\mathrm{T}}$, $\boldsymbol{i}_{\mathrm{g}} = [i_{\mathrm{g}1}\ i_{\mathrm{g}2}\ \ldots\ i_{\mathrm{g}n}]^{\mathrm{T}}$, $\boldsymbol{i}_{\mathrm{k}} = [i_{\mathrm{k}1}\ i_{\mathrm{k}2}\ \ldots\ i_{\mathrm{k}n}]^{\mathrm{T}}$, and $\boldsymbol{L}_{\mathrm{s}}$, $\boldsymbol{M}_{\mathrm{ds}}$, $\boldsymbol{M}_{\mathrm{gs}}$, $\boldsymbol{M}_{\mathrm{ks}}$ are the parasitic inductance matrices, whose definitions are depicted in Section A of Appendix. Based on (7), the circuit model can be equivalent to Fig. 7(b), where the power-source inductance of j_{th} MOSFET – $L_{\mathrm{s}j}$ – is equivalent to a full-coupled inductor. In this way, the power loop and driving loop are separated. The values of $L_{\mathrm{s}j-1}$ and $L_{\mathrm{s}j-2}$ are both equal to $L_{\mathrm{s}j}$. The magnetic couplings of $L_{\mathrm{s}j-1}$ or $L_{\mathrm{s}j-2}$ with other branches are the same as that of $L_{\mathrm{s}j}$. The voltage potentials of s1∼sn and s1'∼ sn' still satisfy (7).

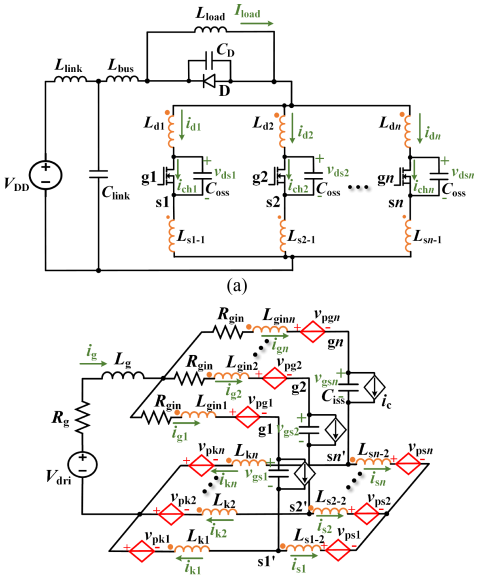
3) Compared with the currents in the power loop, the currents in the driving loop are much smaller. Therefore, the induced voltages in the power loop generated by the driving-loop currents through the mutual inductances are ignored. The power loop in Fig. 7(b) is simplified into Fig. 8(a), where there are mutual inductances between $L_{\mathrm{d}1}\sim L_{\mathrm{d}n}$ and $L_{\mathrm{s}1\text{-}1}\sim L_{\mathrm{s}n-1}$. The driving loop in Fig. 7(b) is simplified into Fig. 8(b), where there are mutual inductances between $L_{\mathrm{gin}1}\sim L_{\mathrm{gin}\,n}$, $L_{\mathrm{k}1}\sim L_{\mathrm{k}n}$, and $L_{\mathrm{s}1\text{-}2}\sim L_{\mathrm{s}n-2}$.



(a)

(b)

Fig. 7. Equivalent dynamic circuit models. (a) Circuit with simplified MOSFET models. (b) Circuit with equivalent power-source full-coupled inductors.



(a)

(b)

Fig. 8. Simplified circuit models. (a) Power circuit. (b) Driving circuit.

The induced voltages in the driving loop generated by $i_{\mathrm{d}1}\sim i_{\mathrm{d}n}$ through the power-driving mutual inductances are equivalent to controlled voltage sources. $v_{\mathrm{pg}1}\sim v_{\mathrm{pg}n}$ represent the induced voltages in the gate branches through the power-gate mutual inductances. $v_{\mathrm{pk}1}\sim v_{\mathrm{pk}n}$ represent that in the driving-source branches caused by power-driving source mutual inductances. $v_{\mathrm{ps}1} \sim v_{\mathrm{ps}n}$ represent the induced voltages on $L_{\mathrm{s1\text{-}2}} \sim L_{\mathrm{s}n-2}$. The controlled voltages can be expressed as

$$\begin{cases} \boldsymbol{v}_{\mathrm{pg}} = \boldsymbol{M}_{\mathrm{pg}}\, \dot{\boldsymbol{i}}_{\mathrm{d}} \\ \boldsymbol{v}_{\mathrm{pk}} = \boldsymbol{M}_{\mathrm{pk}}\, \dot{\boldsymbol{i}}_{\mathrm{d}} \\ \boldsymbol{v}_{\mathrm{ps}} = (\boldsymbol{M}_{\mathrm{ds}} + \boldsymbol{L}_{\mathrm{s}})\, \dot{\boldsymbol{i}}_{\mathrm{d}} \end{cases} \tag{8}$$

where $\boldsymbol{v}_{\mathrm{pg}} = [v_{\mathrm{pg}1}\ v_{\mathrm{pg}2}\ \ldots\ v_{\mathrm{pg}n}]^{\mathrm{T}}$, $\boldsymbol{v}_{\mathrm{pk}} = [v_{\mathrm{pk}1}\ v_{\mathrm{pk}2}\ \ldots\ v_{\mathrm{pk}n}]^{\mathrm{T}}$, $\boldsymbol{v}_{\mathrm{ps}} = [v_{\mathrm{ps}1}\ v_{\mathrm{ps}2}\ \ldots\ v_{\mathrm{ps}n}]^{\mathrm{T}}$; $\boldsymbol{M}_{\mathrm{pg}}$ is the mutual inductance matrix between the power and the gate branches, and $\boldsymbol{M}_{\mathrm{pk}}$ is the mutual inductance matrix between the power and the driving-source branches. They can be expressed by

$$\begin{cases} \boldsymbol{M}_{\mathrm{pg}} = \boldsymbol{M}_{\mathrm{dg}} + \boldsymbol{M}_{\mathrm{sg}} \\ \boldsymbol{M}_{\mathrm{pk}} = \boldsymbol{M}_{\mathrm{dk}} + \boldsymbol{M}_{\mathrm{sk}} \end{cases} \tag{9}$$

where $\boldsymbol{M}_{\mathrm{dg}}$, $\boldsymbol{M}_{\mathrm{sg}}$, $\boldsymbol{M}_{\mathrm{dk}}$, and $\boldsymbol{M}_{\mathrm{sk}}$ are the mutual inductance matrices between the drain, power-source, gate, and driving-source branches, respectively. Their definitions are also given in Section A of Appendix. Based on the simplified circuit models, the model calculating the current differences is established. Combining with the average dynamic current and voltage, the unbalanced switching currents and energy are obtained.

C. Model of the Induced Voltages

The key to calculating the dynamic current differences is to calculate the v_{gs} differences. In the driving circuit in Fig. 8(b), the sources V_{dri}, i_{c}, and the common values (average values) of $v_{\mathrm{pg}1} \sim v_{\mathrm{pg}n}$ and $v_{\mathrm{pk}1} \sim v_{\mathrm{pk}n}$ will induce unbalanced v_{gs} only when the parasitic inductances of the paralleled driving branches are unbalanced. It is proven that in SiC power modules or circuits with small sizes, the differences in the driving inductances are small, and the unbalanced driving inductances do not induce unbalanced dynamic currents [6], [17], [19]. Thus, the influences of these sources on the v_{gs} differences are all neglected. It is supposed that they only influence the average gate current i_{gave} and the average gate-source voltage v_{gsave}. Moreover, since the power source branches are Y-connected, the common values (average values) of $v_{\mathrm{ps}1} \sim v_{\mathrm{ps}n}$ do not induce any currents, which are also neglected. Therefore, it can be concluded that the unbalanced v_{gs} and i_{g} are mainly induced by the unbalanced values of $v_{\mathrm{pg}1} \sim v_{\mathrm{pg}n}$, $v_{\mathrm{pk}1} \sim v_{\mathrm{pk}n}$, and $v_{\mathrm{ps}1} \sim v_{\mathrm{ps}n}$, which can be expressed as

$$\begin{cases} \Delta\boldsymbol{v}_{\mathrm{pg}} = \boldsymbol{v}_{\mathrm{pg}} - v_{\mathrm{pgave}}\boldsymbol{I}_1 = \boldsymbol{P}_1 \cdot \boldsymbol{v}_{\mathrm{pg}} = \boldsymbol{P}_1 \cdot \boldsymbol{M}_{\mathrm{pg}}\, \dot{\boldsymbol{i}}_{\mathrm{d}} \\ \Delta\boldsymbol{v}_{\mathrm{pk}} = \boldsymbol{v}_{\mathrm{pk}} - v_{\mathrm{pkave}}\boldsymbol{I}_1 = \boldsymbol{P}_1 \cdot \boldsymbol{v}_{\mathrm{pk}} = \boldsymbol{P}_1 \cdot \boldsymbol{M}_{\mathrm{pk}}\, \dot{\boldsymbol{i}}_{\mathrm{d}} \\ \Delta\boldsymbol{v}_{\mathrm{ps}} = \boldsymbol{v}_{\mathrm{ps}} - v_{\mathrm{psave}}\boldsymbol{I}_1 = \boldsymbol{P}_1 \cdot \boldsymbol{v}_{\mathrm{ps}} = \boldsymbol{P}_1 \cdot (\boldsymbol{L}_{\mathrm{s}} + \boldsymbol{M}_{\mathrm{ds}})\, \dot{\boldsymbol{i}}_{\mathrm{d}} \end{cases} \tag{10}$$

where $\Delta\boldsymbol{v}_{\mathrm{pg}} = [\Delta v_{\mathrm{pg}1}\ \Delta v_{\mathrm{pg}2}\ \ldots\ \Delta v_{\mathrm{pg}n}]^{\mathrm{T}}$, $\Delta\boldsymbol{v}_{\mathrm{pk}} = [\Delta v_{\mathrm{pk}1}\ \Delta v_{\mathrm{pk}2}\ \ldots\ \Delta v_{\mathrm{pk}n}]^{\mathrm{T}}$, and $\Delta\boldsymbol{v}_{\mathrm{ps}} = [\Delta v_{\mathrm{ps}1}\ \Delta v_{\mathrm{ps}2}\ \ldots\ \Delta v_{\mathrm{ps}n}]^{\mathrm{T}}$ are the unbalanced values of the induced voltages. v_{pgave}, v_{pkave}, and v_{psave} are the average values of the voltages. The average voltages, $\boldsymbol{P}_1$, and $\boldsymbol{I}_1$ are expressed by

$$\begin{cases} v_{\mathrm{pgave}} = \frac{1}{n}\boldsymbol{I}_2 \cdot \boldsymbol{v}_{\mathrm{pg}} \\ v_{\mathrm{pkave}} = \frac{1}{n}\boldsymbol{I}_2 \cdot \boldsymbol{v}_{\mathrm{pk}} \\ v_{\mathrm{psave}} = \frac{1}{n}\boldsymbol{I}_2 \cdot \boldsymbol{v}_{\mathrm{ps}} \\ \boldsymbol{P}_1 = (\boldsymbol{E} - \frac{1}{n}\boldsymbol{I}_3) \\ \boldsymbol{I}_1 = [11\ldots1]^{\mathrm{T}} \end{cases} \tag{11}$$

where

$$\begin{cases} \boldsymbol{E} = \begin{bmatrix} 1 & 0 & \cdots & 0 \\ 0 & 1 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & 1 \end{bmatrix}, \boldsymbol{I}_2 = \begin{bmatrix} 1 & 1 & \cdots & 1 \end{bmatrix}, \\ \boldsymbol{I}_3 = \begin{bmatrix} 1 & 1 & \cdots & 1 \\ 1 & 1 & \cdots & 1 \\ \vdots & \vdots & \ddots & \vdots \\ 1 & 1 & \cdots & 1 \end{bmatrix}. \end{cases} \tag{12}$$

D. Model of the Driving Circuit

To solve the v_{gs} differences under $\Delta\boldsymbol{v}_{\mathrm{pg}}$, $\Delta\boldsymbol{v}_{\mathrm{pk}}$, and $\Delta\boldsymbol{v}_{\mathrm{ps}}$, the state differential equations of the driving circuit are established. The circuit order is only $3n - 1$, which is lower than that of the nonsimplified circuit in Fig. 5. $\Delta v_{\mathrm{gs}1} \sim \Delta v_{\mathrm{gs}n}$, $\Delta i_{\mathrm{g}1} \sim \Delta i_{\mathrm{g}n}$, $\Delta i_{\mathrm{k}1} \sim \Delta i_{\mathrm{k}n-1}$ are chosen as the state variables.

Under the unbalanced values of the induced voltages, the Kirchhoff's voltage law (KVL) equation of the gate and driving-source branches in Fig. 8(b) can be written as

$$\begin{aligned} &(R_{\mathrm{g}}\boldsymbol{I}_3 + \boldsymbol{R}_{\mathrm{gin}})\Delta\boldsymbol{i}_{\mathrm{g}} + (L_{\mathrm{g}}\boldsymbol{I}_3 + \boldsymbol{L}_{\mathrm{gin}} - \boldsymbol{M}_{\mathrm{gk}})\,\Delta\dot{\boldsymbol{i}}_{\mathrm{g}} \\ &\quad + (\boldsymbol{L}_{\mathrm{k}} - \boldsymbol{M}_{\mathrm{kg}})\,\Delta\dot{\boldsymbol{i}}_{k} + (\boldsymbol{M}_{\mathrm{sg}} - \boldsymbol{M}_{\mathrm{sk}})\,\Delta\dot{\boldsymbol{i}}_{\mathrm{s}} = \Delta\boldsymbol{v}_{\mathrm{pk}} \\ &\quad - \Delta\boldsymbol{v}_{\mathrm{pg}} - \Delta\boldsymbol{v}_{\mathrm{gs}} \end{aligned} \tag{13}$$

where $\Delta\boldsymbol{v}_{\mathrm{gs}} = [\Delta v_{\mathrm{gs}1}\ \Delta v_{\mathrm{gs}2}\ \ldots\Delta v_{\mathrm{gs}n}]^{\mathrm{T}}$ is the vector of the unbalanced values of $v_{\mathrm{gs}1} \sim v_{\mathrm{gsn}}$. $\Delta\boldsymbol{i}_{\mathrm{g}} = [\Delta i_{\mathrm{g}1}\ \Delta i_{\mathrm{g}2}\ \ldots\Delta i_{\mathrm{g}n}]^{\mathrm{T}}$, $\Delta\boldsymbol{i}_{\mathrm{k}} = [\Delta i_{\mathrm{k}1}\ \Delta i_{\mathrm{k}2}\ \ldots\Delta i_{\mathrm{k}n}]^{\mathrm{T}}$, and $\Delta\boldsymbol{i}_{\mathrm{s}} = [\Delta i_{\mathrm{s}1}\ \Delta i_{\mathrm{s}2}\ \ldots\Delta i_{\mathrm{s}n}]^{\mathrm{T}}$ are the vectors of the unbalanced currents. $\boldsymbol{R}_{\mathrm{gin}}$ is the matrix of the internal gate resistances, and $\boldsymbol{L}_{\mathrm{gin}}$, $\boldsymbol{L}_{\mathrm{k}}$, $\boldsymbol{M}_{\mathrm{gk}}$, $\boldsymbol{M}_{\mathrm{kg}}$, $\boldsymbol{M}_{\mathrm{sg}}$, and $\boldsymbol{M}_{\mathrm{sk}}$ are the parasitic inductance matrices of the driving circuit, which are defined in Section A of Appendix.

Applying KVL to the driving-source and power-source branches, there are

$$\begin{aligned} &(\boldsymbol{L}_{\mathrm{s}} + \boldsymbol{M}_{\mathrm{sk}})\,\Delta\dot{\boldsymbol{i}}_{\mathrm{s}} + (\boldsymbol{M}_{\mathrm{gs}} + \boldsymbol{M}_{\mathrm{gk}})\,\Delta\dot{\boldsymbol{i}}_{\mathrm{g}} + (-\boldsymbol{M}_{\mathrm{ks}} - \boldsymbol{L}_{\mathrm{k}})\,\Delta\dot{\boldsymbol{i}}_{k} \\ &\quad + \Delta\boldsymbol{v}_{\mathrm{pk}} + \Delta\boldsymbol{v}_{\mathrm{ps}} = \frac{1}{n}\boldsymbol{I}_3((\boldsymbol{L}_{\mathrm{s}} + \boldsymbol{M}_{\mathrm{sk}})\,\Delta\dot{\boldsymbol{i}}_{\mathrm{s}} \\ &\quad + (\boldsymbol{M}_{\mathrm{gs}} + \boldsymbol{M}_{\mathrm{gk}})\,\Delta\dot{\boldsymbol{i}}_{\mathrm{g}} - (\boldsymbol{M}_{\mathrm{ks}} + \boldsymbol{L}_{\mathrm{k}})\,\Delta\dot{\boldsymbol{i}}_{k} \\ &\quad + \Delta\boldsymbol{v}_{\mathrm{pk}} + \Delta\boldsymbol{v}_{\mathrm{ps}}). \end{aligned} \tag{14}$$

The current differences in the driving circuit satisfy

$$\Delta\boldsymbol{i}_{\mathrm{g}} - \Delta\boldsymbol{i}_{\mathrm{s}} = \Delta\boldsymbol{i}_{\mathrm{k}} \tag{15}$$

$$\boldsymbol{I}_2\Delta\boldsymbol{i}_{\mathrm{s}} = 0. \tag{16}$$

The relationship between Δv_{gs} and Δi_{g} can be expressed as

$$\Delta\dot{\boldsymbol{v}}_{\mathrm{gs}} = \frac{1}{C_{\mathrm{iss}}}\Delta\boldsymbol{i}_{\mathrm{g}}. \tag{17}$$

By (15), (13) can be rewritten as

$$\boldsymbol{L}_{\mathrm{g1}}\,\Delta\dot{\boldsymbol{i}}_{\mathrm{g}} + \boldsymbol{L}_{\mathrm{k1}}\,\Delta\dot{\boldsymbol{i}}_{k} = -\boldsymbol{R}_{\mathrm{g}}\Delta\boldsymbol{i}_{\mathrm{g}} - \Delta\boldsymbol{v}_{\mathrm{pg}} + \Delta\boldsymbol{v}_{\mathrm{pk}} - \Delta\boldsymbol{v}_{\mathrm{gs}} \tag{18}$$

where

$$\begin{cases}\boldsymbol{L}_{\mathrm{g1}} = L_{\mathrm{g}}\boldsymbol{I}_3 + \boldsymbol{L}_{\mathrm{g}} + \boldsymbol{M}_{\mathrm{sg}} - \boldsymbol{M}_{\mathrm{gk}} - \boldsymbol{M}_{\mathrm{sk}}\\ \boldsymbol{L}_{\mathrm{k1}} = \boldsymbol{L}_{\mathrm{k}} - \boldsymbol{M}_{\mathrm{kg}} - \boldsymbol{M}_{\mathrm{sg}} + \boldsymbol{M}_{\mathrm{sk}}\\ \boldsymbol{R}_{\mathrm{g}} = R_{\mathrm{g}}\boldsymbol{I}_3 + \boldsymbol{R}_{\mathrm{gin}}.\end{cases} \tag{19}$$

By (15), (14) can be rewritten as

$$\boldsymbol{P}_1\boldsymbol{L}_{\mathrm{g2}}\,\Delta\dot{\boldsymbol{i}}_{\mathrm{g}} - \boldsymbol{P}_1\boldsymbol{L}_{\mathrm{k2}}\,\Delta\dot{\boldsymbol{i}}_{k} = -\boldsymbol{P}_1\Delta\boldsymbol{v}_{\mathrm{pk}} - \boldsymbol{P}_1\Delta\boldsymbol{v}_{\mathrm{ps}} \tag{20}$$

where

$$\begin{cases}\boldsymbol{L}_{\mathrm{g2}} = \boldsymbol{L}_{\mathrm{s}} + \boldsymbol{M}_{\mathrm{gs}} + \boldsymbol{M}_{\mathrm{gk}} + \boldsymbol{M}_{\mathrm{sk}}\\ \boldsymbol{L}_{\mathrm{k2}} = \boldsymbol{L}_{\mathrm{s}} + \boldsymbol{M}_{\mathrm{ks}} + \boldsymbol{L}_{\mathrm{k}} + \boldsymbol{M}_{\mathrm{sk}}\end{cases}. \tag{21}$$

By (15) and (16), it can be derived that

$$\boldsymbol{I}_2\Delta\boldsymbol{i}_{\mathrm{g}} = \boldsymbol{I}_2\Delta\boldsymbol{i}_{\mathrm{k}}. \tag{22}$$

Combining (20) and (22), (23) can be derived

$$\boldsymbol{L}_{\mathrm{g3}}\,\Delta\dot{\boldsymbol{i}}_{\mathrm{g}} - \boldsymbol{L}_{\mathrm{k3}}\,\Delta\dot{\boldsymbol{i}}_{\mathrm{k}} = -\boldsymbol{T}\Delta\boldsymbol{v}_{\mathrm{pk}} - \boldsymbol{T}\Delta\boldsymbol{v}_{\mathrm{ps}} \tag{23}$$

where

$$\begin{cases}\boldsymbol{L}_{\mathrm{g3}} = \begin{bmatrix}\boldsymbol{P}_2\cdot\boldsymbol{P}_1\cdot\boldsymbol{L}_{\mathrm{g2}}\\ \begin{bmatrix}1 & 1 & \cdots & 1\end{bmatrix}\end{bmatrix}, \boldsymbol{L}_{\mathrm{k3}} = \begin{bmatrix}\boldsymbol{P}_2\cdot\boldsymbol{P}_1\cdot\boldsymbol{L}_{\mathrm{k2}}\\ \begin{bmatrix}1 & 1 & \cdots & 1\end{bmatrix}\end{bmatrix}\\ \boldsymbol{T} = \begin{bmatrix}\boldsymbol{P}_2\cdot\boldsymbol{P}_1\\ \begin{bmatrix}0 & 0 & \cdots & 0\end{bmatrix}\end{bmatrix}, \boldsymbol{P}_2 = \begin{bmatrix}1 & 0 & \cdots & 0 & 0\\ 0 & 1 & \cdots & 0 & 0\\ \vdots & \vdots & \ddots & 0 & 0\\ 0 & 0 & \cdots & 1 & 0\end{bmatrix}\end{cases}. \tag{24}$$

Then, it can be solved by (18) and (23) that

$$\begin{cases}\Delta\dot{\boldsymbol{i}}_{\mathrm{g}} = -{\boldsymbol{L}_{\mathrm{g4}}}^{-1}\Delta\boldsymbol{v}_{\mathrm{gs}} - {\boldsymbol{L}_{\mathrm{g4}}}^{-1}\boldsymbol{R}_{\mathrm{g}}\Delta\boldsymbol{i}_{\mathrm{g}} - {\boldsymbol{L}_{\mathrm{g4}}}^{-1}\Delta\boldsymbol{v}_{\mathrm{pg}}\\ +{\boldsymbol{L}_{\mathrm{g4}}}^{-1}(\boldsymbol{E} - \boldsymbol{L}_{\mathrm{k1}}{\boldsymbol{L}_{\mathrm{k3}}}^{-1}\boldsymbol{T})\Delta\boldsymbol{v}_{\mathrm{pk}} - {\boldsymbol{L}_{\mathrm{g4}}}^{-1}\boldsymbol{L}_{\mathrm{k1}}{\boldsymbol{L}_{\mathrm{k3}}}^{-1}\boldsymbol{T}\Delta\boldsymbol{v}_{\mathrm{ps}}\\ \Delta\dot{\boldsymbol{i}}_{\mathrm{k}} = -{\boldsymbol{L}_{\mathrm{k3}}}^{-1}\boldsymbol{L}_{\mathrm{g3}}{\boldsymbol{L}_{\mathrm{g4}}}^{-1}\Delta\boldsymbol{v}_{\mathrm{gs}} - {\boldsymbol{L}_{\mathrm{k3}}}^{-1}\boldsymbol{L}_{\mathrm{g3}}{\boldsymbol{L}_{\mathrm{g4}}}^{-1}\boldsymbol{R}_{\mathrm{g}}\Delta\boldsymbol{i}_{\mathrm{g}}\\ -{\boldsymbol{L}_{\mathrm{k3}}}^{-1}\boldsymbol{L}_{\mathrm{g3}}{\boldsymbol{L}_{\mathrm{g4}}}^{-1}\Delta\boldsymbol{v}_{\mathrm{pg}}\\ +({\boldsymbol{L}_{\mathrm{k3}}}^{-1}\boldsymbol{L}_{\mathrm{g3}}{\boldsymbol{L}_{\mathrm{g4}}}^{-1}(E - \boldsymbol{L}_{\mathrm{k1}}{\boldsymbol{L}_{\mathrm{k3}}}^{-1}\boldsymbol{T}) + {\boldsymbol{L}_{\mathrm{k3}}}^{-1}\boldsymbol{T})\Delta\boldsymbol{v}_{\mathrm{pk}}\\ -({\boldsymbol{L}_{\mathrm{k3}}}^{-1}\boldsymbol{L}_{\mathrm{g3}}{\boldsymbol{L}_{\mathrm{g4}}}^{-1}\boldsymbol{L}_{\mathrm{k1}}{\boldsymbol{L}_{\mathrm{k3}}}^{-1}\boldsymbol{T} - {\boldsymbol{L}_{\mathrm{k3}}}^{-1}\boldsymbol{T})\Delta\boldsymbol{v}_{\mathrm{ps}}\end{cases} \tag{25}$$

where

$$\boldsymbol{L}_{\mathrm{g4}} = \boldsymbol{L}_{\mathrm{g1}} + \boldsymbol{L}_{\mathrm{k1}}{\boldsymbol{L}_{\mathrm{k3}}}^{-1}\boldsymbol{L}_{\mathrm{g3}}. \tag{26}$$

Then, based on (17) and (25), the state differential equation can be written as

$$\dot{\boldsymbol{X}} = \boldsymbol{A}\cdot\boldsymbol{X} + \boldsymbol{B}\cdot\boldsymbol{F} \tag{27}$$

where $\boldsymbol{X} = [\Delta v_{\mathrm{gs1}}\ \ldots\ \Delta v_{\mathrm{gs}\,n}\ \Delta i_{\mathrm{g1}}\ \ldots\ \Delta i_{\mathrm{g}\,n}\ \Delta i_{\mathrm{k1}}\ \ldots\ \Delta i_{\mathrm{k}(n-1)}]^{\mathrm{T}}$ are the state variables. $\boldsymbol{F} = [\Delta v_{\mathrm{pg1}} \ldots \Delta v_{\mathrm{pg}\,n}\ \Delta v_{\mathrm{pk1}} \ldots \Delta v_{\mathrm{pk}\,n}\ \Delta v_{\mathrm{ps1}} \ldots \Delta v_{\mathrm{ps}\,n}]^{\mathrm{T}}$ are the excitations. $\boldsymbol{A}$ and $\boldsymbol{B}$ are the coefficient matrices and are expressed by (28) shown at the bottom of this page. Based on (10), the induced voltages can be obtained, and then $\Delta\boldsymbol{v}_{\mathrm{gs}}$ can be calculated using the state equation

E. Model of the Power Circuit

The power circuit model is established separately from the driving circuit.

1) During t_0–t_3 or t_6–t_9, the MOSFETs work in the controlled region. The channel currents $\boldsymbol{i}_{\mathrm{ch}} = [i_{\mathrm{ch1}}\ i_{\mathrm{ch2}} \ldots i_{\mathrm{ch}\,n}]^{\mathrm{T}}$ are obtained by the nonlinear transfer characteristic using $\boldsymbol{v}_{\mathrm{gs}} = [v_{\mathrm{gs1}}\ v_{\mathrm{gs2}} \ldots\ v_{\mathrm{gs}\,n}]^{\mathrm{T}}$ and $\boldsymbol{T}_{\mathrm{j}} = [T_{\mathrm{j1}}\ T_{\mathrm{j2}} \ldots T_{\mathrm{j}\,n}]^{\mathrm{T}}$, where $\boldsymbol{v}_{\mathrm{gs}}$ is calculated by

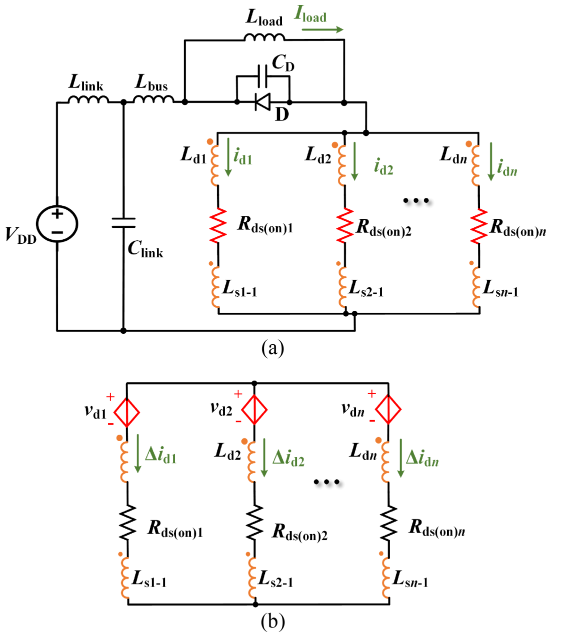
$$\boldsymbol{v}_{\mathrm{gs}} = v_{\mathrm{gsave}}\boldsymbol{I}_1 + \Delta\boldsymbol{v}_{\mathrm{gs}}. \tag{29}$$

The unbalanced value of the channel currents $\Delta\boldsymbol{i}_{\mathrm{ch}} = [\Delta i_{\mathrm{ch1}}\ \Delta i_{\mathrm{ch2}} \ldots \Delta i_{\mathrm{ch}\,n}]^{\mathrm{T}}$ are

$$\Delta\boldsymbol{i}_{\mathrm{ch}} = \boldsymbol{i}_{\mathrm{ch}} - i_{\mathrm{chave}}\boldsymbol{I}_1 = \boldsymbol{P}_1\cdot\boldsymbol{i}_{\mathrm{ch}} \tag{30}$$

where i_{chave} is the average channel current. Since the voltages on the paralleled MOSFETs are approximately equal [12], the currents on the paralleled C_{oss} are supposed to be equal. Thus,

$$\begin{cases}\boldsymbol{A} = \begin{bmatrix}\boldsymbol{0} & \frac{1}{C_{\mathrm{iss}}}\boldsymbol{E} & \boldsymbol{0}\\ -{\boldsymbol{L}_{\mathrm{g4}}}^{-1} & -{\boldsymbol{L}_{\mathrm{g4}}}^{-1}\boldsymbol{R}_{\mathrm{g}} & \boldsymbol{0}\\ -\boldsymbol{P}_2{\boldsymbol{L}_{\mathrm{k3}}}^{-1}\boldsymbol{L}_{\mathrm{g3}}{\boldsymbol{L}_{\mathrm{g4}}}^{-1} & -\boldsymbol{P}_2{\boldsymbol{L}_{\mathrm{k3}}}^{-1}\boldsymbol{L}_{\mathrm{g3}}{\boldsymbol{L}_{\mathrm{g4}}}^{-1}\boldsymbol{R}_{\mathrm{g}} & \boldsymbol{0}\end{bmatrix}\\ \boldsymbol{B} = \begin{bmatrix}\boldsymbol{0} & \boldsymbol{0} & \boldsymbol{0}\\ -{\boldsymbol{L}_{\mathrm{g4}}}^{-1} & {\boldsymbol{L}_{\mathrm{g4}}}^{-1}(\boldsymbol{E} - \boldsymbol{L}_{\mathrm{k1}}{\boldsymbol{L}_{\mathrm{k3}}}^{-1}\boldsymbol{T}) & -({\boldsymbol{L}_{\mathrm{g4}}}^{-1}\boldsymbol{L}_{\mathrm{k1}}{\boldsymbol{L}_{\mathrm{k3}}}^{-1}\boldsymbol{T})\\ -\boldsymbol{P}_2{\boldsymbol{L}_{\mathrm{k3}}}^{-1}\boldsymbol{L}_{\mathrm{g3}}{\boldsymbol{L}_{\mathrm{g4}}}^{-1} & \boldsymbol{P}_2({\boldsymbol{L}_{\mathrm{k3}}}^{-1}\boldsymbol{L}_{\mathrm{g3}}{\boldsymbol{L}_{\mathrm{g4}}}^{-1}(\boldsymbol{E} - \boldsymbol{L}_{\mathrm{k1}}{\boldsymbol{L}_{\mathrm{k3}}}^{-1}\boldsymbol{T}) + {\boldsymbol{L}_{\mathrm{k3}}}^{-1}\boldsymbol{T}) & \begin{matrix}-\boldsymbol{P}_2({\boldsymbol{L}_{\mathrm{k3}}}^{-1}\boldsymbol{L}_{\mathrm{g3}}{\boldsymbol{L}_{\mathrm{g4}}}^{-1}\boldsymbol{L}_{\mathrm{k1}}{\boldsymbol{L}_{\mathrm{k3}}}^{-1}\boldsymbol{T}\\ -{\boldsymbol{L}_{\mathrm{k3}}}^{-1}\boldsymbol{T})\end{matrix}\end{bmatrix}.\end{cases} \tag{28}$$



(a)

(b)

Fig. 9. Power circuit models in the ohmic region. (a) Simplified model. (b) Simplified model for the unbalanced currents.

$\Delta\boldsymbol{i}_{\mathrm{d}} = [\Delta i_{\mathrm{d1}}\ \Delta i_{\mathrm{d2}} \ldots \Delta i_{\mathrm{d}n}] = \Delta\boldsymbol{i}_{\mathrm{ch}}$. By (30), the unbalanced drain currents are obtained as

$$\boldsymbol{i}_{\mathrm{d}} = i_{\mathrm{dave}}\boldsymbol{I}_1 + \Delta\boldsymbol{i}_{\mathrm{ch}} = i_{\mathrm{dave}}\boldsymbol{I}_1 + \boldsymbol{P}_1\boldsymbol{i}_{\mathrm{ch}}. \tag{31}$$

By the driving circuit model, $\Delta\boldsymbol{v}_{\mathrm{gs}}$ can be obtained. The gate-source voltage $\boldsymbol{v}_{\mathrm{gs}}$ is obtained by (29), $\boldsymbol{i}_{\mathrm{ch}}$ is obtained by the transfer characteristic, and $\boldsymbol{i}_{\mathrm{d}}$ is calculated by (31). v_{gsave}, i_{chave}, and i_{dave} can be obtained by calculating the average switching transient.

2) During t_3–t_4 and t_5–t_6, the MOSFETs work in the ohmic region. The effect of C_{oss} is neglected. Thus, the power circuit is simplified into Fig. 9(a), where $R_{\mathrm{ds(ON)}1}$~$R_{\mathrm{ds(ON)}n}$ are the resistances of the MOSFETs. They are given by (2), where $\boldsymbol{i}_{\mathrm{ch}}$ is obtained by the ohmic-region output characteristic using $\boldsymbol{v}_{\mathrm{gs}}$, v_{ds}, and $\boldsymbol{T}_{\mathrm{j}}$. $\boldsymbol{v}_{\mathrm{gs}}$ is calculated by (29). And the average drain-source voltage v_{ds} is used, which is obtained by calculating the average switching transient. When only considering the unbalanced currents, the circuit is simplified into Fig. 9(b), where the effects of the common values of i_{d1}~$i_{\mathrm{d}n}$ are equivalent to the controlled voltages $\boldsymbol{v}_{\mathrm{d}} = [v_{\mathrm{d1}}\ v_{\mathrm{d2}} \ldots v_{\mathrm{d}n}]^{\mathrm{T}}$, expressed by

$$\boldsymbol{v}_{\mathrm{d}} = (\boldsymbol{L}_{\mathrm{d}} + \boldsymbol{L}_{\mathrm{s}} + \boldsymbol{M}_{\mathrm{ds}} + \boldsymbol{M}_{\mathrm{sd}})\,\dot{i}_{\mathrm{dave}}\,\boldsymbol{I}_1 + \boldsymbol{R}_{\mathrm{ds(on)}} i_{\mathrm{dave}}\boldsymbol{I}_1 \tag{32}$$

where $\boldsymbol{L}_{\mathrm{d}}$ is the drain inductance matrix defined in Section A of Appendix, and $\boldsymbol{R}_{\mathrm{ds(ON)}}$ is expressed as

$$\boldsymbol{R}_{\mathrm{ds(on)}} = \begin{bmatrix} R_{\mathrm{ds(on)1}} & 0 & \cdots & 0 \\ 0 & R_{\mathrm{ds(on)2}} & \cdots & 0 \\ \vdots & \vdots & \ddots & 0 \\ 0 & 0 & \cdots & R_{\mathrm{ds(on)n}} \end{bmatrix}. \tag{33}$$

The circuit equation of Fig. 9(b) can be written as

$$\begin{aligned} &\boldsymbol{v}_{\mathrm{d}} + (\boldsymbol{L}_{\mathrm{d}} + \boldsymbol{L}_{\mathrm{s}} + \boldsymbol{M}_{\mathrm{ds}} + \boldsymbol{M}_{\mathrm{sd}})\,\Delta\dot{\boldsymbol{i}}_{\mathrm{d}} + \boldsymbol{R}_{\mathrm{ds(on)}}\Delta\boldsymbol{i}_{\mathrm{d}} \\ &= \frac{1}{n}\boldsymbol{I}_3((\boldsymbol{v}_{\mathrm{d}} + (\boldsymbol{L}_{\mathrm{d}} + \boldsymbol{L}_{\mathrm{s}} + \boldsymbol{M}_{\mathrm{ds}} + \boldsymbol{M}_{\mathrm{sd}})\,\Delta\dot{\boldsymbol{i}}_{\mathrm{d}} \\ &+ \boldsymbol{R}_{\mathrm{ds(on)}}\Delta\boldsymbol{i}_{\mathrm{d}})) \end{aligned} \tag{34}$$

$$\begin{bmatrix} 1 & 1 & \cdots & 1 \end{bmatrix} \Delta\boldsymbol{i}_{\mathrm{d}} = 0. \tag{35}$$

Combining (34) and (35), it can be derived that

$$\boldsymbol{L}_{\mathrm{ds}}\,\Delta\dot{\boldsymbol{i}}_{\mathrm{d}} = -\boldsymbol{R}_{\mathrm{ds}}\Delta\boldsymbol{i}_{\mathrm{d}} - \boldsymbol{T}\boldsymbol{v}_{\mathrm{d}} \tag{36}$$

where

$$\begin{cases} \boldsymbol{L}_{\mathrm{ds}} = \begin{bmatrix} \boldsymbol{P}_2\boldsymbol{P}_1(\boldsymbol{L}_{\mathrm{d}} + \boldsymbol{L}_{\mathrm{s}} + \boldsymbol{M}_{\mathrm{ds}} + \boldsymbol{M}_{\mathrm{sd}}) \\ \begin{bmatrix} 1 & 1 & \cdots & 1 \end{bmatrix} \end{bmatrix} \\ \boldsymbol{R}_{\mathrm{ds}} = \begin{bmatrix} \boldsymbol{P}_2\boldsymbol{P}_1\boldsymbol{R}_{\mathrm{ds(on)}} \\ \begin{bmatrix} 0 & 0 & \cdots & 0 \end{bmatrix} \end{bmatrix} \end{cases}. \tag{37}$$

Choosing Δi_{d1}~$\Delta i_{\mathrm{d}(n-1)}$ as the state variables, the state equation of the simplified power circuit in the ohmic region is derived by (36) and (37) as

$$\dot{\boldsymbol{Y}} = \boldsymbol{C}\cdot\boldsymbol{Y} + \boldsymbol{D}\cdot\boldsymbol{v}_{\mathrm{d}} \tag{38}$$

where $\boldsymbol{Y} = [\Delta i_{\mathrm{d1}}\ \Delta i_{\mathrm{d2}} \ldots \Delta i_{\mathrm{d}(n-1)}]^{\mathrm{T}}$, and $\boldsymbol{C}$ and $\boldsymbol{D}$ are expressed as

$$\begin{cases} \boldsymbol{C} = -\boldsymbol{P}_2{\boldsymbol{L}_{\mathrm{ds}}}^{-1}\boldsymbol{R}_{\mathrm{ds}}\boldsymbol{P}_3 \\ \boldsymbol{D} = -\boldsymbol{P}_2{\boldsymbol{L}_{\mathrm{ds}}}^{-1}\boldsymbol{T} \end{cases} \tag{39}$$

where

$$\boldsymbol{P}_3 = \begin{bmatrix} 1 & 0 & \cdots & 0 \\ 0 & 1 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & 1 \\ -1 & -1 & \cdots & -1 \end{bmatrix}. \tag{40}$$

$\boldsymbol{v}_{\mathrm{d}}$ is calculated by (32), then $\Delta\boldsymbol{i}_{\mathrm{d}}$ can be obtained by solving (38), and then $\boldsymbol{i}_{\mathrm{d}}$ and $\boldsymbol{i}_{\mathrm{ch}}$ can be obtained by

$$\begin{cases} \boldsymbol{i}_{\mathrm{d}} = i_{\mathrm{dave}}\boldsymbol{I}_1 + \Delta\boldsymbol{i}_{\mathrm{d}} \\ \boldsymbol{i}_{\mathrm{ch}} = i_{\mathrm{chave}}\boldsymbol{I}_1 + \Delta\boldsymbol{i}_{\mathrm{d}} \end{cases}. \tag{41}$$

F. Analytical Model and Calculation Method

By the above models, the analytical model for calculating the unbalanced dynamic currents is shown in Fig. 10. The unbalanced power-driving mutual inductances, drain-source mutual inductances, or power-source inductances cause unbalanced induced voltages, causing unbalanced $\boldsymbol{v}_{\mathrm{gs}}$, and then inducing unbalanced $\boldsymbol{i}_{\mathrm{d}}$. The current $\boldsymbol{i}_{\mathrm{d}}$, in turn, influences the unbalanced induced voltages.

The calculation flowchart is shown in Fig. 11. First, the parameter values are given as inputs, including the MOSFET characteristic curves, the diode parameters, and the circuit parameters. The MOSFET characteristics can be obtained by the datasheet or by experimental tests. The circuit parasitic matrices can be obtained

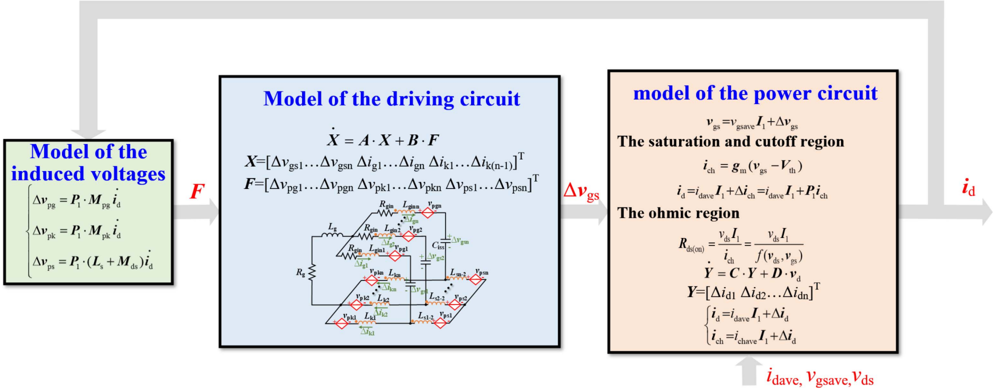


Fig. 10. Analytical model for calculating the unbalanced dynamic currents.

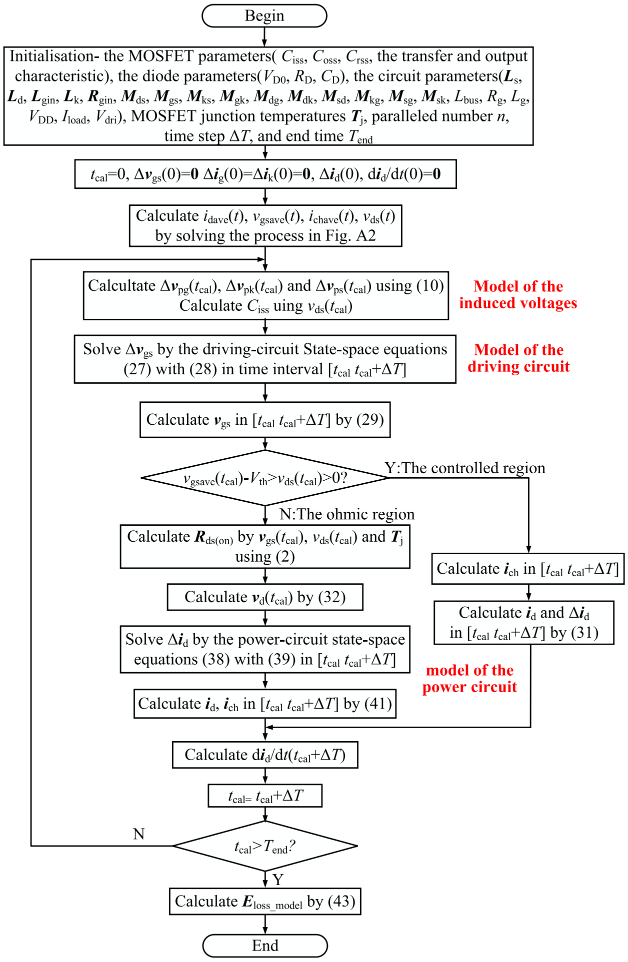


Fig. 11. Calculation flowchart of the analytical model.

by electromagnetic simulation. Second, the initial values are given, where $\Delta \boldsymbol{i}_d(0)$ is given by

$$\Delta i_{dj}(0) = \frac{\frac{1}{R_{ds(on)j}}}{\frac{1}{R_{ds(on)1}} + \frac{1}{R_{ds(on)2}} + \cdots + \frac{1}{R_{ds(on)n}}} \cdot n i_{dave}(0) - i_{dave}(0). \tag{42}$$

$\Delta i_{dj}(0)$ is the j_{th} element of $\Delta \boldsymbol{i}_d(0)$. During the turn-ON period, $\Delta i_{dj}(0) = 0$, since $i_{dave}(0) = 0$. During the turn-OFF period, $i_{dave}(0) = I_{load}/n$, and $\Delta i_{dj}(0)$ is determined by the initial $R_{ds(ON)1} \sim R_{ds(ON)n}$. Then, the average switching transient is calculated to obtain v_{gsave}, i_{chave}, i_{dave}, and v_{ds} for the subsequent calculation. An analytical model is used for the average calculation, which is detailed in Appendix. The average model is based on the modeling method in [20] and [33] with high calculating precision. The average waveforms can also be obtained by experiments if the actual circuit is available. Finally, the presented dynamic current sharing model is calculated by time stepping. The time step is much lower than the switching time.

During each time step $[t_{cal}, t_{cal}+\Delta T]$, the unbalanced induced voltages $\Delta \boldsymbol{v}_{pg}(T_{cal})$, $\Delta \boldsymbol{v}_{pk}(T_{cal})$, $\Delta \boldsymbol{v}_{ps}(T_{cal})$, and C_{iss} are calculated first, where C_{iss} is obtained by linearly interpolating the $C_{iss}(v_{ds})$ curve data using the latest calculated $v_{ds}(T_{cal})$. Then, the state (27) is calculated to obtain $\Delta \boldsymbol{v}_{gs}$ and $\boldsymbol{v}_{gs}$. The unbalanced induced voltages and C_{iss} are considered constant in this time step. Hence, the coefficients and excitation matrices of the state equation are constant, making it easy and fast to solve. Then, $\boldsymbol{i}_d$ and $\boldsymbol{i}_{ch}$ are calculated using the power circuit model. When solving the power circuit model, the working region is judged first. Different models are used for different working regions

1) When the MOSFETs work in the controlled region, $\boldsymbol{i}_{ch}$ is obtained by performing two- 2-D linear interpolation on the curve data of the transfer characteristic $i_{ch}(v_{gs}, T_j)$ using the calculated $\boldsymbol{v}_{gs}$ waveform in this time step and $\boldsymbol{T}_j$. Then, $\boldsymbol{i}_d$ is obtained by (31) using the calculated $\boldsymbol{i}_{ch}$.
2) When the MOSFETs work in the ohmic region, first, the curve data of the ohmic-region output characteristic $i_{ch}(v_{ds}, v_{gs}, T_j)$ is linearly interpolated using $v_{ds}(T_{cal})$, $\boldsymbol{T}_j$, and the latest calculated $\boldsymbol{v}_{gs}(T_{cal})$ to obtain $\boldsymbol{i}_{ch}(T_{cal})$. Then, $\boldsymbol{i}_{ch}(T_{cal})$ is divided by $v_{ds}(T_{cal})$ to obtain the resistance $\boldsymbol{R}_{ds(ON)}(T_{cal})$ of the paralleled dies for calculation in this time step. Then, $\boldsymbol{v}_d(T_{cal})$ is calculated by (32). $\Delta \boldsymbol{i}_d$ is calculated by solving (38), and $\boldsymbol{i}_d$ is obtained by (41). $\boldsymbol{R}_{ds(ON)}$ and $\boldsymbol{v}_d$ are also considered constant to ensure fast solution and convergence of the state equation.

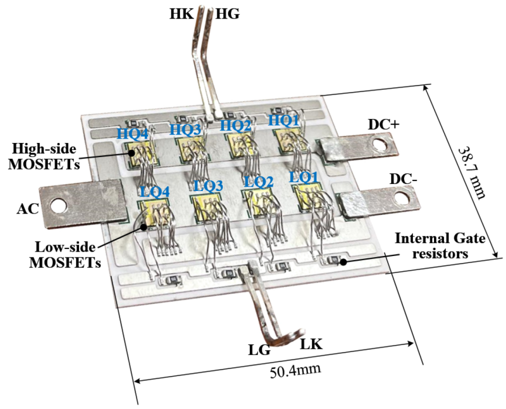


Fig. 12. Experimental power module.

Finally, $\mathrm{d}\Delta\boldsymbol{i}_{\mathrm{d}}/\mathrm{d}t(t_{\mathrm{cal}}+\Delta T)$ is calculated for solving the unbalanced induced voltages of the next time step. By reinterpolating the curve data of the die characteristics within each time step, their nonlinearities are involved. By interpolating the curve data under different temperatures using $\boldsymbol{T}_{\mathrm{j}}$, the temperature dependence of the die parameters is included.

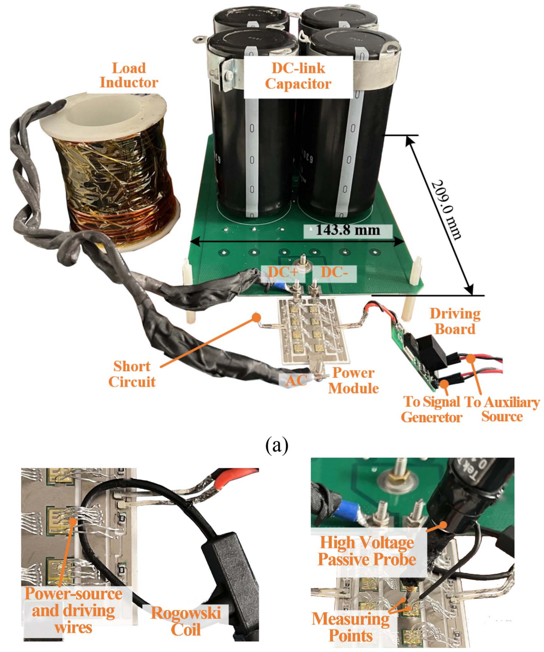
When the calculation is finished, the unbalanced switching energy $\boldsymbol{E}_{\mathrm{loss\_model}} = [\boldsymbol{E}_{\mathrm{loss1\_model}}\ \boldsymbol{E}_{\mathrm{loss2\_model}}\ \ldots\ \boldsymbol{E}_{\mathrm{lossn\_model}}]^{\mathrm{T}}$ are calculated by

$$\boldsymbol{E}_{\mathrm{loss-model}} = \int_{0}^{T_{\mathrm{end}}} \boldsymbol{i}_{\mathrm{d}} v_{\mathrm{ds}} \mathrm{d}t. \tag{43}$$

The calculation program is established in MATLAB and solved by cyclic calculations of the state equations and expressions according to the flowchart in Fig. 11. The ready-made linear interpolating function and state equation solving function in MATLAB are used. Moreover, the calculation program is suitable for different parallel numbers, circuit parameters, and die temperatures. When used in different circuits, it is only needed to update the chip characteristic curves, junction temperatures, and parasitic inductance matrices.

IV. EXPERIMENTAL VERIFICATION

In this section, the presented model is verified by experiments based on the SiC power module shown in Fig. 12. The module layout is designed based on the commercial modules from ROHM [34]. 8 ROHM S4661 (1200 V/13 mΩ) SiC MOSFETs are used, where four MOSFETs are paralleled in each switch. Moreover, there are 10 Ω gate resistors soldered on the substrate and connected to each MOSFET to dampen the oscillations between the paralleled dies. Under 2 Ω, 4.1 Ω, and 6 Ω external R_{g}, the current rise and fall times are 43 ns–78 ns and 32 ns–63 ns, which are reasonable for high-capacity SiC power modules. The test circuit of the power module is shown in Fig. 13, where the bill of the components is shown in Table I. A 120 A Rogowski coil is used to test the drain currents of LQ1–LQ4. The coil is simultaneously placed on the MOSFETs' power-source and driving bonding wires, as shown in Fig. 13(b), to obtain the drain currents directly. As for the high-side MOSFETs, the driving and power-source wires are on different sides. Due to the low area and the fragile driving wires, it is hard to place the coil on all the bonding wires to measure the high-side drain currents. Therefore, the experimental tests are based on the situation where the low-side MOSFETs are used as the main switch, whose drain currents are easy to measure. The i_{d} waveforms of LQ1–LQ4 are obtained by four repeated tests under the same conditions using one coil. In this way, the measurement errors caused by coil differences are avoided. The v_{ds} waveforms are tested directly on the MOSFET dies by a 1000 V passive voltage probe from Tektronix, as shown in Fig. 13(c). Though the accuracy of the voltage probe is limited under several volts, the test errors have little impact on the tested switching energy and the experimental verifications. Since the module is not encapsulated to facilitate the measurements, the dc bus voltage is 400 V to prevent partial discharge. The equivalent test circuit diagram is shown in Fig. 14. The black components in Fig. 14 are the parameters inside the power module, where there are magnetic couplings between the parasitic inductances. The blue parts are the outside circuits. In addition, there are current coupling effects caused by the common branch currents between the parallel



(a)

(b) (c)

Fig. 13. Test setups. (a) DPT test rig. (b) Measurement method of drain currents. (c) Measurement method of drain-source voltage v_{ds}.

TABLE I
COMPONENT LIST OF THE TEST CIRCUIT

Part		Specifications
Gate driver IC		IXDN630YI from IXYS with 30 A Peak current
Gare driver power supply		MGJ2D051802SC from muRata with 2 W and 18 V&-2.5 V dual outputs
L_{load}		70 μH air-cored inductor
C_{link}	C_{dec}	2220Y6300105KETWS2 630 V/1 μF ceramic capacitors from Knowles Syfer. Ten paralleled branches, Two series-connected capacitors in each branch.
	C_{bulk}	LNX2J102MSEG 630 V/1000 μF from Nichicon. Two paralleled branches, Two series-connected capacitors in each branch.

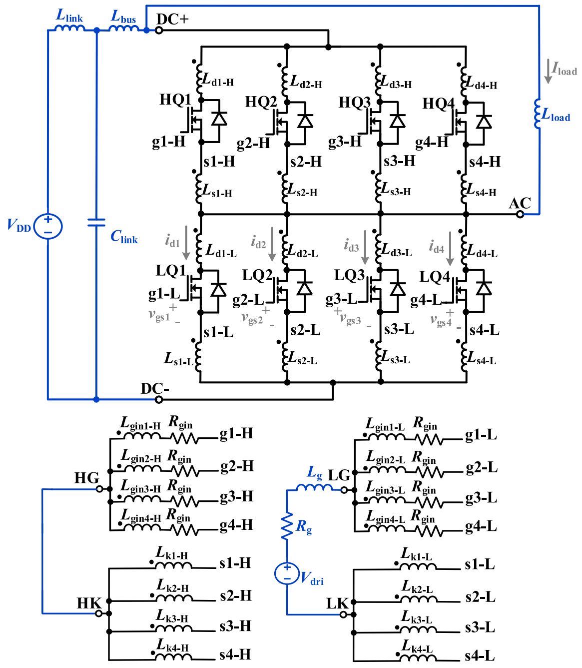


Fig. 14. Equivalent circuit diagram of the DPT circuit.

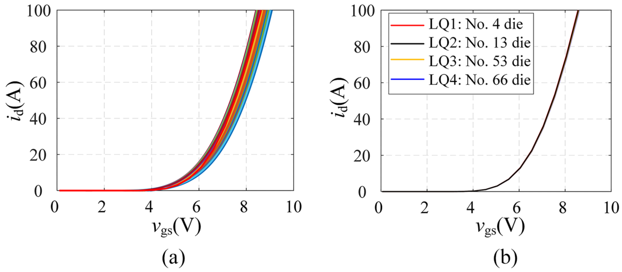
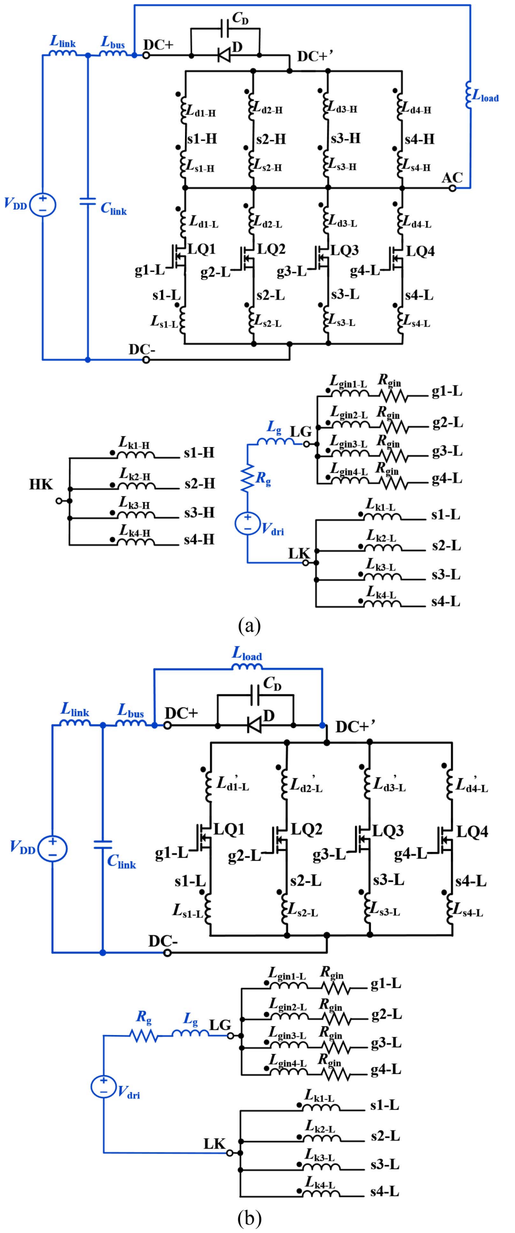


Fig. 15. Transfer curves of the tested dies. (a) Transfer curves of the 70 tested dies. (b) Transfer curves of the selected LQ1–LQ4.

chips, which is equivalent to parts of the parasitic inductances and mutual inductances in Fig. 14. The low-side MOSFETs are used as the main switch. The high-side driving terminals (HG and HK) are shorted, and the driving board is connected to the low-side driving terminals (LG and LK). The load inductance is connected to the dc+ and ac terminals.

Before module manufacturing, the transfer curves of 70 dies are tested by Agilent B1505A and screened to ensure the consistency of the paralleled dies. The results are shown in Fig. 15(a). The transfer curves of the selected LQ1–LQ4 are shown in Fig. 15(b), which overlap with each other.

A. Circuit Parasitic Parameter Values



(a)

(b)

Fig. 16. Equivalent models of the test circuit. (a) Circuit with simplified freewheeling diodes. (b) Circuit after parasitic inductace equivalence.

The parasitic inductance values need to be given first. As for the circuit in Fig. 14, supposing the voltages on the freewheeling diodes are equal, HQ1–HQ4 can be moved outside the paralleled branches and equivalent to a single diode, as shown in Fig. 16(a). V_{D0} of the diode takes the average value of the paralleled dies. C_{D} and R_{D} takes the paralleled values. Moving the connection point of the load inductor from ac to dc+', and equivalenting the parasitic inductances from dc+' to the drains of LQ1–LQ4 into four paralleled inductances ($L_{\text{d1-L}}$'$\sim L_{\text{d4-L}}$'), the circuit is equivalent to Fig. 16(b). The circuit is the same as the typical circuit in Fig. 2 and is used for calculating. The parasitic inductance values are obtained by Q3D simulation, which is precise and convenient [18], [19], [20]. During the simulation, the high-side dies are shorted, the electrodes of the low-side dies are set to sources, and the terminals (dc+, dc-, LG, and LK) are set to sinks. Then, four nets ($L_{\mathrm{d}}, L_{\mathrm{s}}, L_{\mathrm{k}}, L_{\mathrm{g}}$) with excitations are generated, as shown in Fig. 17. The parasitic inductances in Fig. 16(b) are directly solved based on this simulation setup. Based on the simulation, the current coupling effects are included. Fig. 18 shows the parasitic inductances under different frequencies. As shown in Fig. 18, as the frequency increases, the absolute values of the

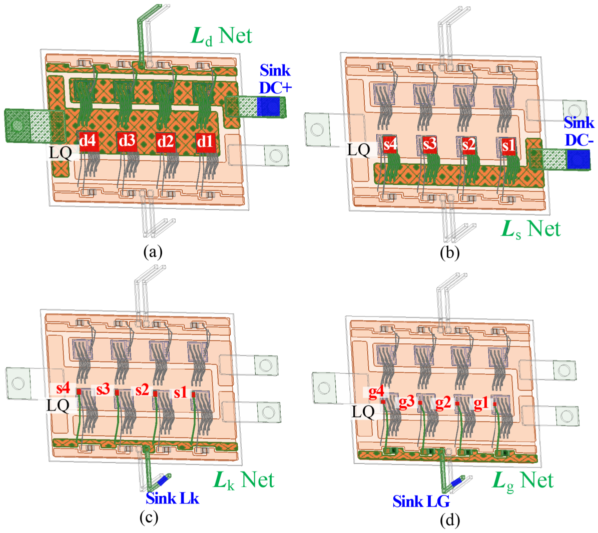


Fig. 17. Q3D simulation nets. (a) L_d net. (b) L_s net. (c) L_k net. (d) L_g net.

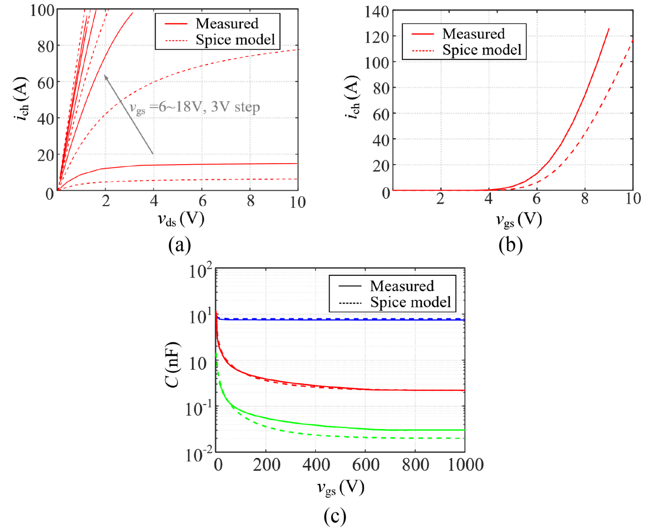


Fig. 19. MOSFET characteristics from measurements and Spice model. (a) Ohmic-region output characteristic. (b) Transfer characteristic. (c) Junction capacitances.

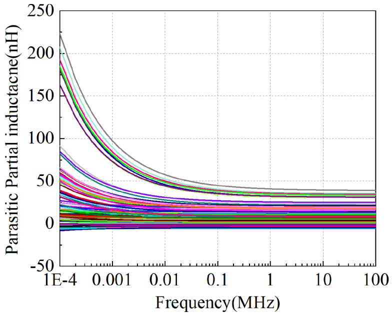


Fig. 18. Parasitic inductances under different frequencies.

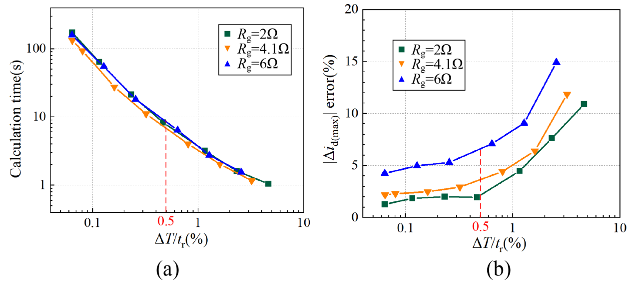


Fig. 20. Calculation times and errors under different time steps ΔT. (a) Calculation times. (b) Calculation errors of the maximum current differences.

parasitic inductances gradually decrease due to the changes in the skin and proximity effects. When the frequency is higher than 1 MHz, because of the little variations in these two effects, the parasitic inductances change little with frequency. During the switching transients of the SiC power module, the current rise and fall times are in the range of tens of nano seconds, corresponding to an equivalent frequency range of a few MHz to tens of MHz, where the inductances remain nearly constant with frequency [9]. Thus, the inductances on 10 MHz are used for model calculation. The parasitic inductances of the outside circuits are also obtained by Q3D simulations, where $L_{\text{bus}} = 6.65$ nH and $L_g = 38.1$ nH.

B. Experimental Results Under Room Temperature

Under room temperature, the measured average ohmic-region output characteristic curves, transfer characteristic curve, and junction capacitances of LQ1–LQ4 are shown in Fig. 19, where the curves of the die Spice model provided by the manufacturer are compared. The parameters of the Spice model are different from the measured practical values, which may be due to the different die batches. This will reduce the accuracy of Spice simulations. Based on the circuit parasitic inductances and the tested MOSFET parameters, the presented model is solved.

Fig. 20(a) shows the model-calculation times under different time steps ΔT during the turn-ON period, when $I_{\text{load}} = 230$ A. Fig. 20(b) shows the influence of ΔT on the calculation errors of the maximum current differences $|\Delta i_{d(\max)}|$ ($= |\max(i_{d1} - i_{d4})|$). It can be seen that the larger the time step ΔT, the shorter the calculation time but the larger the calculation errors. The time steps equal to 0.5% of the current rise or fall time are used for calculation, which can simultaneously ensure fast calculation speed and high calculation accuracy. In practical applications, the current rise and fall times can be obtained from the die/module datasheet, and the required calculation time step can be determined proportionally. Alternatively, obtain the results quickly with a large time step, read the switching time according to the calculated waveforms, and then readjust the time step to 0.5% of the current rise or fall time to get a higher precision.

Under the same conditions, the model calculated, LTSpice simulated, and experimentally tested waveforms are shown in Figs. 21–23. In the LTSpice simulation, the die Spice model provided by the manufacturer and the same parasitic inductances are used. Figs. 21–23 show the results when $R_g = 2\ \Omega$, 4.1 Ω, and 6 Ω, respectively. It can be concluded that the turn-ON currents on LQ1–LQ4 decrease in sequence, and their turn-OFF

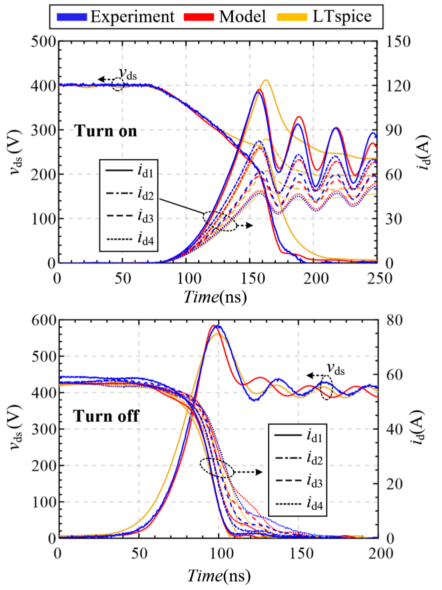


Fig. 21. Turn-ON and turn-OFF waveforms when $R_g = 2\ \Omega$ and $I_{load} = 230$ A.

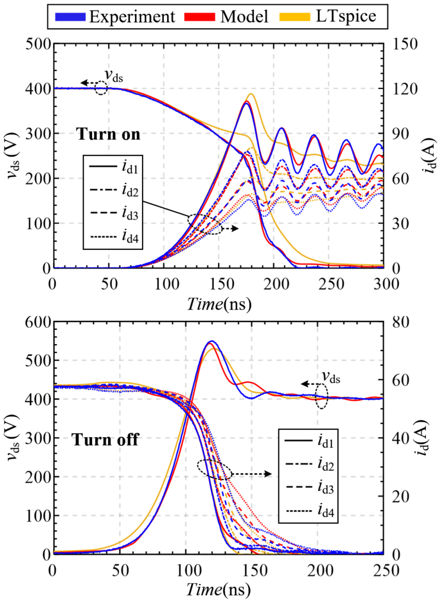


Fig. 22. Turn-ON and turn-OFF waveforms when $R_g = 4.1\ \Omega$ and $I_{load} = 230$ A.

currents increase in sequence. The model-calculated waveforms match the tested waveforms well. However, the errors of the simulated waveforms are large, especially when $R_g = 2\ \Omega$ and $4.1\ \Omega$. The deviations of the simulation results are caused by the nonaccurate parameters of the MOSFET Spice model.

Table II summarizes the tested, model calculated, and Spice simulated maximum unbalanced currents ($\Delta i_{d1(max)} \sim \Delta i_{d4(max)}$) during the turn-ON and turn-OFF periods. The maximum unbalanced current $\Delta i_{dj(max)}$ on the j_{th} MOSFET represents the maximum deferences between i_{dj} and i_{dave}, and can be expressed as

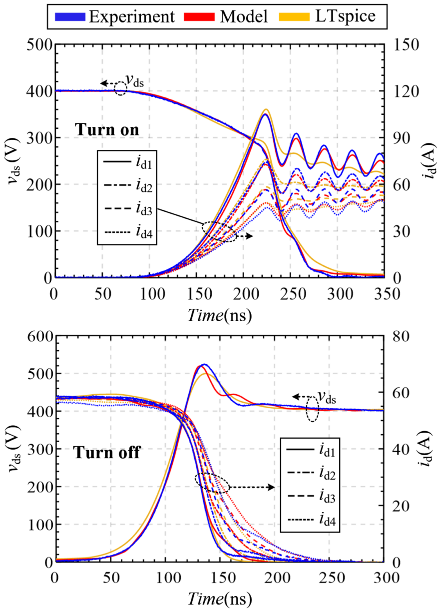


Fig. 23. Turn-ON and turn-OFF waveforms when $R_g = 6\ \Omega$ and $I_{load} = 230$ A.

$$\Delta i_{dj(max)} = \begin{cases} \max(\Delta i_{dj}) = \max(i_{dj} - i_{dave}), \text{if} \Delta i_{dj} > 0 \\ -\max(|\Delta i_{dj}|) = -\max(|i_{dj} - i_{dave}|), \text{if} \Delta i_{dj} < 0 \end{cases} . \tag{44}$$

Since $\Delta i_{d1(max)} \sim \Delta i_{d4(max)}$ do not appear at the same time, their sums are not equal to 0. The errors of the model calculated results are defined as

$$\text{error} = |(\Delta i_{dj(max)\_mod} - \Delta i_{dj(max)\_exp})/(I_{load}/n)| \tag{45}$$

where $\Delta i_{dj(max)\_mod}$ is the calculated value and $\Delta i_{dj(max)\_exp}$ is the tested value. The errors of the simulated results are defined in the same way. Under different gate resistances, the errors of the calculated turn-ON maximum unbalanced currents are within 8%, and the errors of the turn-OFF results are within 6%. The errors of the simulated turn-ON and turn-OFF results are below 8% and 5%, respectively. Both the presented model and LTSpice simulation can predict dynamic current differences well.

Table III shows the errors of the calculated and simulated v_{ds} waveforms relative to the tested results. Since the accuracy at a single point does not reflect the accuracy of the entire v_{ds} waveform, we define the errors of the calculated v_{ds} waveforms as

$$\text{error} = \frac{1}{T_{end}} \int_0^{T_{end}} |v_{ds\_model} - v_{ds\_exp}| dt \tag{46}$$

where v_{ds_model} and v_{ds_exp} are the model-calculated and tested v_{ds} waveforms, respectively. The definition contains the error information of all points in the calculated v_{ds} waveforms. The same definition is used for the simulated errors. As shown in Table III, the maximum error of the model-calculated results is 6.40 V during the turn-ON transients and 12.6 V during the turn-OFF transients. The maximum turn-ON and turn-OFF errors

TABLE II
MAXIMUM UNBALANCED CURRENTS ON THE PARALLELED MOSFETS ($I_{\text{LOAD}} = 230$ A)

R_g (Ω)	MOSFET	Turn-ON					Turn-OFF				
		experiment value (A)	model		LTspice		experiment value (A)	model		LTspice	
			value (A)	error	value (A)	error		value (A)	error	value (A)	error
2	LQ1	38.8	41.7	4.98%	43.0	7.22%	-11.0	-10.7	0.515%	-11.7	1.22%
	LQ2	6.70	2.21	7.72%	3.80	4.98%	-4.14	-3.06	1.86%	-3.53	1.05%
	LQ3	-15.8	-17.0	2.06%	-17.8	3.44%	3.79	4.20	0.705%	4.71	1.58%
	LQ4	-28.4	-26.8	2.75%	-29.9	2.58%	10.8	9.46	2.30%	10.0	1.30%
4.1	LQ1	34.6	38.4	6.60%	38.2	6.19%	-11.4	-10.9	0.894%	-11.4	0%
	LQ2	6.02	2.49	6.07%	3.59	4.18%	-4.04	-2.79	2.15%	-3.12	1.58%
	LQ3	-13.6	-15.7	3.59%	-15.5	3.32%	3.97	4.25	0.482%	4.56	1.01%
	LQ4	-27.1	-25.1	3.28%	-26.3	1.34%	11.6	9.25	4.041%	9.53	3.56%
6	LQ1	35.3	34.5	1.32%	35.5	0.399%	-11.6	-10.5	1.82%	-11.2	0.705%
	LQ2	4.25	2.11	3.67%	3.39	1.48%	-4.19	-2.60	2.73%	-3.00	2.05%
	LQ3	-13.6	-14.0	0.690%	-14.4	1.37%	4.59	4.07	0.889%	4.50	0.163%
	LQ4	-25.6	-22.6	5.21%	-24.5	1.92%	12.0	8.73	5.59%	9.26	4.68%

TABLE III
ERRORS OF THE MODEL-CALCULATED AND LTSPICE-SIMULATED VOLTAGE WAVEFORMS ($I_{\text{LOAD}} = 230$ A)

R_g (Ω)	Turn-ON		Turn-OFF	
	Model error (V)	LTspice error (V)	Model error (V)	LTspice error (V)
2	6.40	24.0	12.6	21.9
4.1	3.12	22.1	9.81	14.2
6	3.34	8.12	7.26	12.3

TABLE IV
SWITCHING ENERGY ON THE PARALLELED MOSFETS ($I_{\text{LOAD}} = 230$ A)

R_g (Ω)	MOSFET	Turn-ON					Turn-OFF				
		experiment value (mJ)	Model		LTspice		experiment value (mJ)	Model		LTspice	
			value (mJ)	error	value (mJ)	error		value (mJ)	error	value (mJ)	error
2	LQ1	1.05	1.08	3.37%	1.42	35.4%	0.544	0.513	5.56%	0.618	13.6%
	LQ2	0.747	0.818	9.54%	0.997	33.6%	0.647	0.637	1.39%	0.732	13.1%
	LQ3	0.595	0.630	5.97%	0.768	29.2%	0.765	0.759	0.707%	0.843	10.3%
	LQ4	0.513	0.513	0.0877%	0.640	24.7%	0.885	0.862	2.500%	0.936	5.74%
4.1	LQ1	1.49	1.49	0.238%	1.96	31.7%	0.808	0.798	1.15%	0.898	11.2%
	LQ2	1.11	1.07	4.36%	1.41	26.9%	0.957	0.977	2.05%	1.04	8.61%
	LQ3	0.866	0.847	2.18%	1.11	28.4%	1.101	1.14	3.63%	1.16	5.64%
	LQ4	0.692	0.730	5.51%	0.940	36.0%	1.28	1.28	0.115%	1.26	1.22%
6	LQ1	2.08	2.00	3.62%	2.29	10.2%	1.07	0.98	8.07%	1.08	0.829%
	LQ2	1.55	1.48	4.70%	1.68	8.39%	1.23	1.20	2.71%	1.23	0.245%
	LQ3	1.22	1.21	1.11%	1.35	10.1%	1.44	1.39	3.12%	1.38	4.23%
	LQ4	1.00	1.06	5.97%	1.15	15.2%	1.65	1.55	5.68%	1.49	9.37%

of the simulated results are large, which are 24.0 V and 21.9 V, respectively.

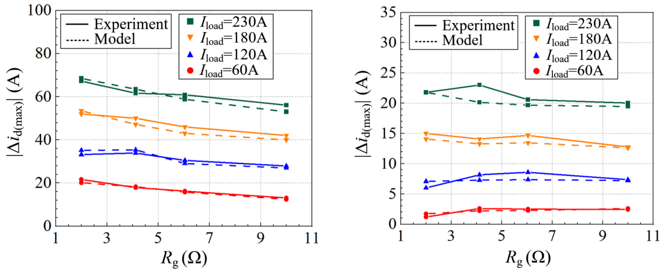
Table IV shows the tested, model-calculated, and Spice-simulated unbalanced switching energy during the turn-ON and turn-OFF periods. The switching energy of the j_{th} MOSFET is defined as

$$E_{\text{loss}j} = \int_0^{T_{\text{end}}} i_{\text{d}j} v_{\text{ds}} \mathrm{d}t. \tag{47}$$

Since the i_{ch} waveforms cannot be measured in the experiments, i_{d} is used here for switching energy calculation. The errors of the model-calculated switching energy are defined as

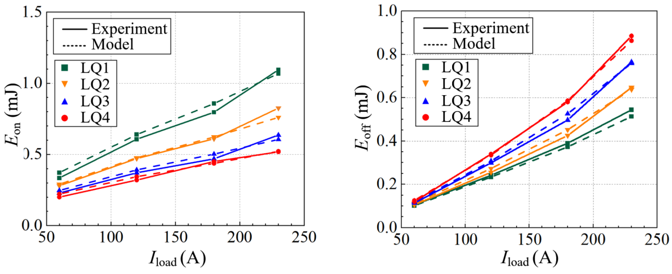
$$\text{error} = |(E_{\text{loss}j\_\text{model}} - E_{\text{loss}j\_\text{exp}})/(E_{\text{loss}j\_\text{exp}})| \tag{48}$$

where $E_{\text{loss}j\_\text{model}}$ is the calculated value and $E_{\text{loss}j\_\text{exp}}$ is the tested value. The errors of the simulated energy are defined in the same way. It can be concluded that the turn-ON switching energy on LQ1–LQ4 decrease in sequence, and the turn-OFF switching energy increase in sequence. Under different gate resistances, the errors of the calculated turn-ON switching energy are within 10%, and the errors of the calculated turn-OFF switching energy are within 9%. It can be concluded that the presented model predicts unbalanced switching energy well. As for the simulated results, the errors of the turn-ON switching energy are higher than 8% and reach 36% on LQ4 under 4.1 Ω R_g. This is because of the large errors in the simulated turn-ON voltage waveforms. The errors of the simulated turn-OFF switching energy are relatively small, and the maximum value is 13.6%. It can be concluded that the errors of the Spice simulated waveforms and switching energy are large due to the errors in the die parameters of the Spice model. If the die parameters can be modified based on the measured curves, Spice simulation can also achieve high calculation accuracy [28]. However, the output characteristic in the spice model is expressed by a complex multidimensional



(a) (b)

Fig. 24. Maximum current differences under different gate resistances and load currents. (a) Turn-ON results. (b) Turn-OFF results.



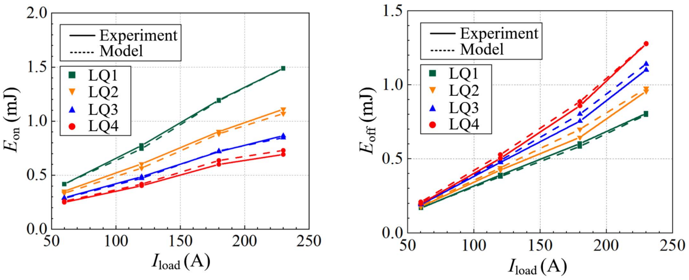
(a) (b)

Fig. 25. Turn-ON and turn-OFF switching energy on the paralleled MOSFETs under different load currents when $R_g = 2\ \Omega$. (a) Turn-ON results. (b) Turn-OFF results.

fitting function, and the parameters' specific physical meanings are unclear. Thus, modifying the complex fitting curve in the spice model is difficult. Compared to Spice simulation, the presented model is calculated directly by inputting the tested die characteristics without the model modification process.

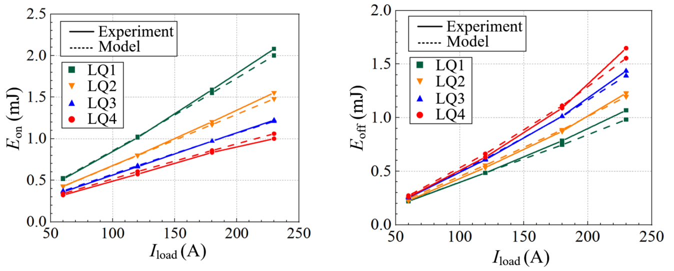
Under different I_{load} and gate resistances, the maximum current differences $|\Delta i_{\text{d(max)}}|$ $(= |\max(i_{\text{d1}} - i_{\text{d4}})|)$ are shown in Fig. 24. The presented model can accurately calculate the current differences under different conditions. The maximum error of the turn-ON and turn-OFF results is lower than 8%. Fig. 24 also shows that the current differences increase as the load current increases. However, they only slightly decrease with the increased R_g during the turn-ON transients, and almost do not change with R_g during the turn-OFF transients. This is because under an increased R_g, the switching time increases, and the current slope decreases. The unbalanced induced voltages in the driving circuit are reduced, but the effect time is increased. The two effects cancel each other out, making the change of the current differences small.

The turn-ON and turn-OFF switching energy under different I_{load} and R_g are shown in Figs. 25 –27, which shows the results when $R_g = 2\ \Omega$, 4.1 Ω, and 6 Ω, respectively. The model-calculated results fit the tested results well. The maximum error during the turn-ON and turn-OFF periods is lower than 11%. The switching energy and their differences increase with the increased I_{load}. To further verify the model accuracy, the total turn-ON and turn-OFF switching energy results when $R_{\text{g\_ON}} = 4.1\ \Omega$, $R_{\text{g\_OFF}} = 2\ \Omega$ are shown in Fig. 28(a), and the results when $R_{\text{g\_ON}} = 6\ \Omega$, $R_{\text{g\_OFF}} = 2\ \Omega$ are shown in Fig. 28(b). The



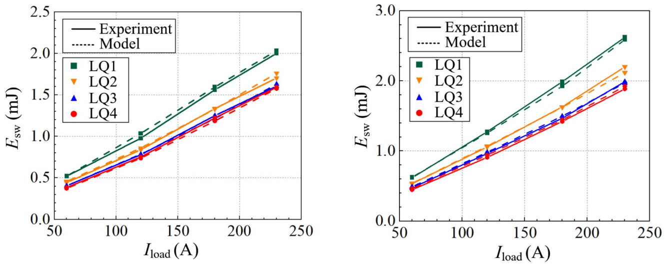
(a) (b)

Fig. 26. Turn-ON and turn-OFF switching energy on the paralleled MOSFETs under different load currents when $R_g = 4.1\ \Omega$. (a) Turn-ON results. (b) Turn-OFF results.



(a) (b)

Fig. 27. Turn-ON and turn-OFF switching energy on the paralleled MOSFETs under different load currents when $R_g = 6\ \Omega$. (a) Turn-ON results. (b) Turn-OFF results.



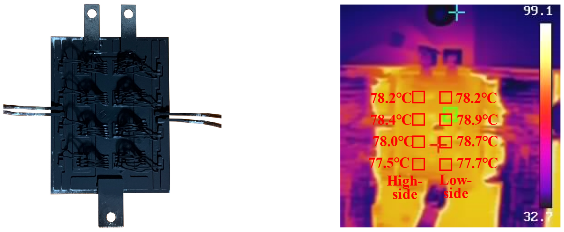
(a) (b)

Fig. 28. Total switching energy on the paralleled MOSFETs when (a) $R_{\text{g\_on}} = 4.1\ \Omega$, $R_{\text{g\_OFF}} = 2\ \Omega$, and (b) $R_{\text{g\_ON}} = 6\ \Omega$, $R_{\text{g\_OFF}} = 2\ \Omega$.

model still has high accuracy, with a maximum error of 5.7%. Thus, it can be concluded that the model can accurately predict the maximum switching energy on the paralleled MOSFETs.

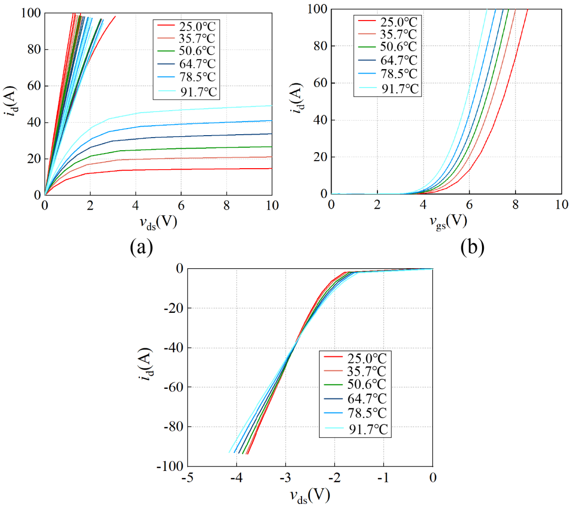
C. *Experimental Results Under Higher Temperatures*

First, to perform accurate calculation, the ohmic-region output and transfer curves under different temperatures are measured using Agilent B1505A. Because the dies are already soldered on the direct bonded copper (DBC), the parameters of a single die cannot be individually tested. Since the dies are screened before soldering, their characteristic differences are ignored. Thus, the entire switch with four paralleled dies is measured, and the measured currents are divided by four to obtain the characteristic curves of a single die. The module is attached to a hot plate with silicon thermal grease, and the die temperatures are checked by an infrared thermal imager. To accurately monitor the die



(a) (b)

Fig. 29. (a) Power moduel with black paint. (b) Temperature distribution under 100 °C heat plate temperature.



(a) (b) (c)

Fig. 30. Measured characteristic curves under different junction temperatures. (a) Ohmic-region output characteristic. (b) Transfer characteristic. (c) Third quadrant characteristic.

temperatures, the power module is covered with black paint to avoid the influence of reflected lights, as shown in Fig. 29(a). The temperature distribution is depicted in Fig. 29(b), when the hot plate temperature is 100 °C. The maximum temperature difference on LQ1–LQ4 is only 1.7%. Therefore, this heating method can ensure the consistency of the temperatures between the paralleled dies, and the die characteristic curves are tested accurately. Giving different temperatures, the measured curves of the low-side dies are shown in Fig. 30(a)–(b). The measured third quadrant characteristic curves of the high-side freewheeling dies are shown in Fig. 30(c). The calculations of the presented model under different junction temperatures are based on these measured curves.

DPT tests are performed to obtain the switching waveforms and energy under elevated temperatures. The test setup under the higher, balanced temperatures is shown in Fig. 31. The module is also attached to the hot plate. The temperature distribution is also tested by the infrared thermal imager. The signal test methods are the same as the experiments under room temperature. A 100 °C hot plate temperature is giving, and the module temperature distribution is the same as Fig. 29(b). The switching waveforms and energy under the higher balanced temperatures are tested. The model-calculated and tested waveforms are compared in Fig. 32. They are matched well. The calculated and tested maximum unbalanced currents and switching energy are shown in Table V. The calculation errors are within 10%. Thus, the presented model enables accurate calculation of the unbalanced dynamic currents and switching energy under balanced, elevated die temperatures.

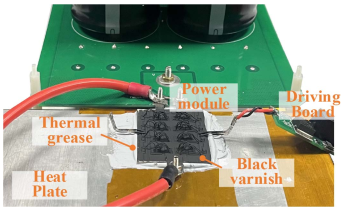


Fig. 31. Test setup under higher, balanced temperaturs.

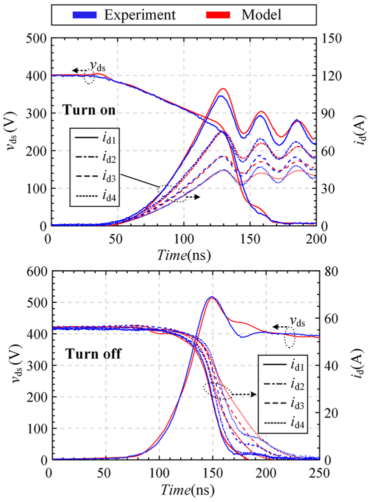
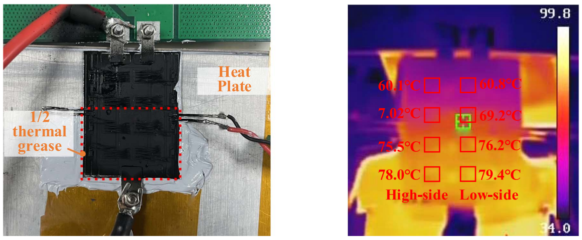


Fig. 32. Switching waveforms under balanced, higher die temperatures when $R_g = 4.1\ \Omega$ and $I_{load} = 230$ A.



(a) (b)

Fig. 33. Test setup under unbalanced die temperatures. (a) Module with thermal grease. (b) Temperature distribution.

To verify the accuracy of the presented model under unbalanced junction temperatures, the thermal grease is only added to the 1/2 area of the module, as shown in Fig. 33(a). Under 100 °C hot plate temperature, the temperature distribution is shown in Fig. 33(b). The temperatures on LQ1–LQ4 are 60.8 °C, 69.2 °C, 76.2 °C, and 79.4 °C, where the maximum difference is 40.1% of the average temperature rise. The model-calculated and tested waveforms are shown in Fig. 34. They are also matched well. The calculated and tested maximum unbalanced currents and switching energy are shown in Table VI. The calculation errors are within 10.4%. Thus, the presented model enables accurate

TABLE V

MAXIMUM UNBALANCED CURRENTS AND SWITCHING ENERGY UNDER BALANCED HIGHER TEMPERATURES ($I_{\mathrm{LOAD}} = 230$ A, $R_{\mathrm{G}} = 4.1\ \Omega$)

	MOSFET	Turn-ON			Turn-OFF		
		Experiment value	Model		Experiment value	Model	
			value	error		value	error
Maximum unbalanced currents	LQ1	33.9 A	37.9 A	6.90%	-9.40 A	-12.2 A	4.82%
	LQ2	5.85 A	3.92 A	3.32%	-4.60 A	-3.00 A	2.75%
	LQ3	-14.3 A	-15.6 A	2.36%	3.41 A	5.08 A	2.87%
	LQ4	-25.5 A	-26.2 A	1.22%	10.5 A	9.44 A	1.87%
Switching energy	LQ1	1.38 mJ	1.41 mJ	2.13%	0.827 mJ	0.760 mJ	8.15%
	LQ2	1.03 mJ	1.01 mJ	2.46%	0.910 mJ	0.979 mJ	7.55%
	LQ3	0.792 mJ	0.775 mJ	2.11%	1.08 mJ	1.17 mJ	7.95%
	LQ4	0.642 mJ	0.637 mJ	0.741%	1.23 mJ	1.21 mJ	1.63%

TABLE VI

MAXIMUM UNBALANCED CURRENTS AND SWITCHING ENERGY UNDER UNBALANCED TEMPERATURES ($I_{\mathrm{LOAD}} = 230$ A, $R_{\mathrm{G}} = 4.1\ \Omega$)

	MOSFET	Turn-ON			Turn-OFF		
		Experiment value	Model		Experiment value	Model	
			value	error		value	error
Maximum unbalanced currents	LQ1	32.2 A	29.9 A	4.72%	-11.2 A	-11.1 A	0.189%
	LQ2	5.66 A	3.68 A	2.50%	-3.59 A	-2.07 A	2.61%
	LQ3	-13.3 A	-11.8 A	3.40%	4.85 A	4.27 A	0.997%
	LQ4	-24.6 A	-21.8 A	3.81%	9.36 A	8.64 A	1.23%
Switching energy	LQ1	1.27 mJ	1.21 mJ	4.90%	0.774 mJ	0.785 mJ	1.48%
	LQ2	1.02 mJ	1.02 mJ	0.0400%	0.899 mJ	0.992 mJ	10.4%
	LQ3	0.811 mJ	0.872 mJ	7.49%	1.06 mJ	1.14 mJ	6.75%
	LQ4	0.692 mJ	0.754 mJ	8.90%	1.20 mJ	1.25 mJ	4.02%

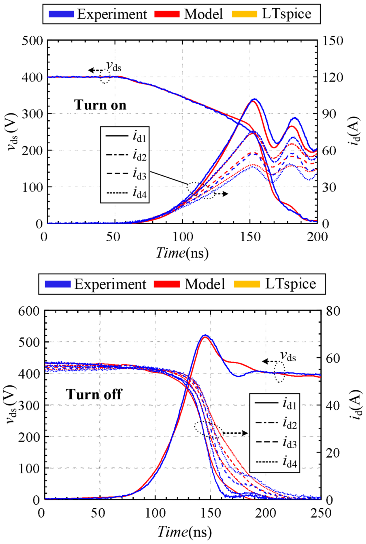


Fig. 34. Switching waveforms under unbalanced die temperatures when $R_{\mathrm{g}} = 4.1\ \Omega$ and $I_{\mathrm{load}} = 230$ A.

calculation of the unbalanced dynamic currents and switching energy under unbalanced die temperatures.

D. Calculation Error Analysis

The errors between the model-calculated and the experimental results may come from the following aspects.

1) The errors of the parasitic inductances used in the model calculation.
2) The errors of the die parameters used in the model calculation.
3) The errors introduced by the step calculation.
4) The errors induced by the assumption that the voltages on the freewheeling diodes are equal.
5) The chip screening is carried out at room temperature. Differences in the die parameters at high temperatures can introduce calculation errors.
6) Experimental measurement errors. However, the experimental verifications show that these errors are within the acceptable range.

In practical applications, to ensure and improve the accuracy of the model, the following points need to be noted.

1) Using Q3D simulation to extract parasitic inductances has been proven with high accuracy. On this basis, investigating the principles of high-precision extraction can further reduce the errors of the presented model.
2) Accurately measuring the ohmic-region output curves, transfer curves, and junction capacitances is the key to achieving high-precision calculation. The smaller the measurement errors, the more accurate the model will be.
3) Calculation time step selection: It can be concluded that when selecting 0.5% of the current rise or fall time, short calculation time, and high accuracy can be guaranteed simultaneously. When the time step exceeds 0.5% of the current rise or fall time, the calculation error will be large.
4) Screening the paralleled dies considering the temperature dependence can also help to reduce the errors.

V. CONCLUSION

This article presents a quantitative analytical model of paralleled MOSFETs for calculating the unbalanced dynamic currents and switching energy.

First, the equivalent circuit models of MOSFETs are established based on the different working regions. Then, the circuit with *n* paralleled MOSFETs is simplified, separating the power and driving circuits. Based on the simplified circuit model, decoupled modeling between the power and driving circuits and reduced orders are achieved. The order of the state equations is only $3n - 1$, which is lower than $5n$ of the unsimplified circuit. The parasitic self and mutual inductances, nonlinear die parameters, and their temperature dependence are considered to ensure calculation accuracy. The nonlinear parameters are integrated by interpolating in each time step without the high-precision curve fitting process. The model can be directly used in circuits with any parallel number and parameters. When used for different circuits, it only needs to update the parameter inputs without remodeling and reprogramming. Moreover, during each time step, the elements in the coefficient and excitation matrices of the state equations are constants, which is easy and fast to solve. The model is more user-friendly than Spice simulation.

The model is verified by a SiC power module with a conventional layout. Under different gate resistances, load currents, and die temperatures, the errors of the calculated maximum current differences are within 8%, and the errors of the switching energy are within 11%. The model is accurate for designing and evaluating the current sharing performances or calculating the maximum switching losses of paralleled MOSFETs. Moreover, the sources of the calculation errors are analyzed, and guidance is given to improve model accuracy. The precision of the model can be further improved by increasing the accuracy of the parasitic inductances and die characteristic curves, and by screening the dies considering the temperature dependence. Moreover, attention needs to be paid to the selection of the calculation time step.

APPENDIX

A. Definitions of Circuit Parameter Matrices

The parasitic inductance matrices and the matrix of the internal gate resistances $\boldsymbol{R}_{\text{gin}}$ are defined as (A1) shown at the bottom of this page

B. Analytical Model for Calculating Average Waveforms

Under the effect of the average current i_{dave}, the induced voltage $\boldsymbol{v}_{\text{d}}$' on $L_{\text{d}1}\sim L_{\text{d}n}$ and $L_{\text{s1-1}}\sim L_{\text{s}n-1}$ in Fig. 8(a) can be written as

$$\boldsymbol{v}_{\text{d}}{}' = (\boldsymbol{L}_{\text{d}} + \boldsymbol{M}_{\text{sd}} + \boldsymbol{L}_{\text{s}} + \boldsymbol{M}_{\text{ds}})\, \dot{i}_{\text{dave}} \boldsymbol{I}_1. \tag{A2}$$

$$\begin{cases}
\boldsymbol{L}_{\text{s}} = \begin{bmatrix} L_{\text{s}1} & M_{\text{s}12} & \cdots & M_{\text{s}1n} \\ M_{\text{s}12} & L_{\text{s}2} & \cdots & M_{\text{s}2n} \\ \vdots & \vdots & \ddots & \vdots \\ M_{\text{s}1n} & M_{\text{s}2n} & \cdots & L_{\text{s}n} \end{bmatrix}, \boldsymbol{L}_{\text{d}} = \begin{bmatrix} L_{\text{d}1} & M_{\text{d}12} & \cdots & M_{\text{d}1n} \\ M_{\text{d}12} & L_{\text{d}2} & \cdots & M_{\text{d}2n} \\ \vdots & \vdots & \ddots & \vdots \\ M_{\text{d}1n} & M_{\text{s}2n} & \cdots & L_{\text{d}n} \end{bmatrix} \\
\boldsymbol{L}_{\text{gin}} = \begin{bmatrix} L_{\text{gin}1} & M_{\text{gin}12} & \cdots & M_{\text{gin}1n} \\ M_{\text{gin}12} & L_{\text{gin}2} & \cdots & M_{\text{gin}2n} \\ \vdots & \vdots & \ddots & \vdots \\ M_{\text{gin}1n} & M_{\text{gin}2n} & \cdots & L_{\text{gin}n} \end{bmatrix}, \boldsymbol{L}_{\text{k}} = \begin{bmatrix} L_{\text{k}1} & M_{\text{k}12} & \cdots & M_{\text{k}1n} \\ M_{\text{k}12} & L_{\text{k}2} & \cdots & M_{\text{k}2n} \\ \vdots & \vdots & \ddots & \vdots \\ M_{\text{k}1n} & M_{\text{k}2n} & \cdots & L_{\text{k}n} \end{bmatrix} \\
\boldsymbol{R}_{\text{gin}} = R_{\text{gin}} \begin{bmatrix} 1 & 0 & \cdots & 0 \\ 0 & 1 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & 1 \end{bmatrix}, \boldsymbol{M}_{\text{ds}} = \begin{bmatrix} M_{\text{d1s1}} & M_{\text{d2s1}} & \cdots & M_{\text{d}n\text{s}1} \\ M_{\text{d1s2}} & M_{\text{d2s2}} & \cdots & M_{\text{d}n\text{s}2} \\ \vdots & \vdots & \ddots & \vdots \\ M_{\text{d1s}n} & M_{\text{d2s}n} & \cdots & M_{\text{d}n\text{s}n} \end{bmatrix} \\
\boldsymbol{M}_{\text{gs}} = \begin{bmatrix} M_{\text{g1s1}} & M_{\text{g2s1}} & \cdots & M_{\text{g}n\text{s}1} \\ M_{\text{g1s2}} & M_{\text{g2s2}} & \cdots & M_{\text{g}n\text{s}2} \\ \vdots & \vdots & \ddots & \vdots \\ M_{\text{g1s}n} & M_{\text{g2s}n} & \cdots & M_{\text{g}n\text{s}n} \end{bmatrix}, \boldsymbol{M}_{\text{ks}} = \begin{bmatrix} M_{\text{k1s1}} & M_{\text{k2s1}} & \cdots & M_{\text{k}n\text{s}1} \\ M_{\text{k1s2}} & M_{\text{k2s2}} & \cdots & M_{\text{k}n\text{s}2} \\ \vdots & \vdots & \ddots & \vdots \\ M_{\text{k1s}n} & M_{\text{k2s}n} & \cdots & M_{\text{k}n\text{s}n} \end{bmatrix} \\
\boldsymbol{M}_{\text{gk}} = \begin{bmatrix} M_{\text{g1k1}} & M_{\text{g2k1}} & \cdots & M_{\text{g}n\text{k}1} \\ M_{\text{g1k2}} & M_{\text{g2k2}} & \cdots & M_{\text{g}n\text{k}2} \\ \vdots & \vdots & \ddots & \vdots \\ M_{\text{g1k}n} & M_{\text{g2k}n} & \cdots & M_{\text{g}n\text{k}n} \end{bmatrix}, \boldsymbol{M}_{\text{dg}} = \begin{bmatrix} M_{\text{d1g1}} & M_{\text{d2g1}} & \cdots & M_{\text{d}n\text{g}1} \\ M_{\text{d1g2}} & M_{\text{d2g2}} & \cdots & M_{\text{d}n\text{g}2} \\ \vdots & \vdots & \ddots & \vdots \\ M_{\text{d1g}n} & M_{\text{d2g}n} & \cdots & M_{\text{d}n\text{g}n} \end{bmatrix} \\
\boldsymbol{M}_{\text{dk}} = \begin{bmatrix} M_{\text{d1k1}} & M_{\text{d2k1}} & \cdots & M_{\text{d}n\text{k}1} \\ M_{\text{d1k2}} & M_{\text{d2k2}} & \cdots & M_{\text{d}n\text{k}2} \\ \vdots & \vdots & \ddots & \vdots \\ M_{\text{d1k}n} & M_{\text{d2k}n} & \cdots & M_{\text{d}n\text{k}n} \end{bmatrix} \\
\boldsymbol{M}_{\text{sd}} = \boldsymbol{M}_{\text{ds}}{}^{T}, \boldsymbol{M}_{\text{kg}} = \boldsymbol{M}_{\text{gk}}{}^{T}, \boldsymbol{M}_{\text{sg}} = \boldsymbol{M}_{\text{gs}}{}^{T}, \boldsymbol{M}_{\text{sk}} = \boldsymbol{M}_{\text{ks}}{}^{T}.
\end{cases} \tag{A1}$$

Under the average currents $i_{\mathrm{gave}} = i_{\mathrm{kave}}$, the voltage $\boldsymbol{v}_{\mathrm{gk}}$' on $L_{\mathrm{gin}1}\sim L_{\mathrm{gin}\,n}$ and $L_{\mathrm{k}1}\sim L_{\mathrm{k}\,n}$ can be expressed as

$$\boldsymbol{v}_{\mathrm{gk}}{}' = (\boldsymbol{L}_{\mathrm{gin}} + \boldsymbol{L}_{\mathrm{k}} - \boldsymbol{M}_{\mathrm{kg}} - \boldsymbol{M}_{\mathrm{gk}})\,\dot{i}_{\mathrm{gave}}\,\boldsymbol{I}_1 + \boldsymbol{R}_{\mathrm{gin}} i_{\mathrm{gave}} \boldsymbol{I}_1. \tag{A3}$$

The induced voltages $\boldsymbol{v}_{\mathrm{pg}}$' and $\boldsymbol{v}_{\mathrm{pk}}$' in the driving circuit caused by i_{dave} can be written as

$$\begin{cases} \boldsymbol{v}_{\mathrm{pg}}{}' = \boldsymbol{M}_{\mathrm{pg}}\,\dot{i}_{\mathrm{dave}}\,\boldsymbol{I}_1 \\ \boldsymbol{v}_{\mathrm{pk}}{}' = \boldsymbol{M}_{\mathrm{pk}}\,\dot{i}_{\mathrm{dave}}\,\boldsymbol{I}_1 \end{cases}. \tag{A4}$$

i_{dave} and i_{gave} can be expressed by

$$i_{\mathrm{dave}} = \frac{i_{\mathrm{dtol}}}{n},\ i_{\mathrm{gave}} = \frac{i_{\mathrm{gtol}}}{n} \tag{A5}$$

where i_{dtol} and i_{gtol} are the total drain current and gate current. By (A2)–(A5), the average values of $\boldsymbol{v}_{\mathrm{d}}$', $\boldsymbol{v}_{\mathrm{gk}}$', $\boldsymbol{v}_{\mathrm{pg}}$', and $\boldsymbol{v}_{\mathrm{pk}}$' can be obtained as

$$\begin{cases} v_{\mathrm{dave}} = \frac{1}{n}\boldsymbol{I}_2\boldsymbol{v}_{\mathrm{d}}{}' = \frac{1}{n^2}\boldsymbol{I}_2(\boldsymbol{L}_{\mathrm{d}} + \boldsymbol{M}_{\mathrm{sd}} + \boldsymbol{L}_{\mathrm{s}} + \boldsymbol{M}_{\mathrm{ds}})\boldsymbol{I}_1\,\dot{i}_{\mathrm{dtol}} \\ v_{\mathrm{gkave}} = \frac{1}{n}\boldsymbol{I}_2\boldsymbol{v}_{\mathrm{gk}}{}' = \frac{1}{n^2}\boldsymbol{I}_2(\boldsymbol{L}_{\mathrm{gin}} + \boldsymbol{L}_{\mathrm{k}} - \boldsymbol{M}_{\mathrm{kg}} - \boldsymbol{M}_{\mathrm{gk}})\boldsymbol{I}_1\,\dot{i}_{\mathrm{gtol}} \\ \qquad + \frac{1}{n^2}\boldsymbol{I}_2\boldsymbol{R}_{\mathrm{gin}}\boldsymbol{I}_1 i_{\mathrm{gtol}} \\ v_{\mathrm{pgave}} = \frac{1}{n}\boldsymbol{I}_2\boldsymbol{v}_{\mathrm{pg}}{}' = \frac{1}{n^2}\boldsymbol{I}_2\boldsymbol{M}_{\mathrm{pg}}\boldsymbol{I}_1\,\dot{i}_{\mathrm{dtol}} \\ v_{\mathrm{pkave}} = \frac{1}{n}\boldsymbol{I}_2\boldsymbol{v}_{\mathrm{pk}}{}' = \frac{1}{n^2}\boldsymbol{I}_2\boldsymbol{M}_{\mathrm{pk}}\boldsymbol{I}_1\,\dot{i}_{\mathrm{dtol}}. \end{cases} \tag{A6}$$

Defining

$$\begin{cases} L_{\mathrm{deq}} = \frac{1}{n^2}\boldsymbol{I}_2\left(\boldsymbol{L}_{\mathrm{d}} + \boldsymbol{L}_{\mathrm{s}} + \boldsymbol{M}_{\mathrm{ds}} + \boldsymbol{M}_{\mathrm{sd}}\right)\boldsymbol{I}_1 \\ L_{\mathrm{gkeq}} = \frac{1}{n^2}\boldsymbol{I}_2(\boldsymbol{L}_{\mathrm{gin}} + \boldsymbol{L}_{\mathrm{k}} - \boldsymbol{M}_{\mathrm{kg}} - \boldsymbol{M}_{\mathrm{gk}})\boldsymbol{I}_1 \\ R_{\mathrm{gineq}} = \frac{1}{n}\boldsymbol{I}_2\boldsymbol{R}_{\mathrm{gin}}\boldsymbol{I}_1 \\ M_{\mathrm{pgeq}} = \frac{1}{n^2}\boldsymbol{I}_2\boldsymbol{M}_{\mathrm{pg}}\boldsymbol{I}_1 \\ M_{\mathrm{pkave}} = \frac{1}{n^2}\boldsymbol{I}_2\boldsymbol{M}_{\mathrm{pk}}\boldsymbol{I}_1. \end{cases} \tag{A7}$$

Equation (A6) can be written as

$$\begin{cases} v_{\mathrm{dave}} = L_{\mathrm{deq}}\,\dot{i}_{\mathrm{dtol}} \\ v_{\mathrm{gkave}} = L_{\mathrm{gkeq}}\,\dot{i}_{\mathrm{gtol}} + R_{\mathrm{gineq}} i_{\mathrm{gtol}} \\ v_{\mathrm{pgave}} = M_{\mathrm{pgeq}}\,\dot{i}_{\mathrm{dtol}} \\ v_{\mathrm{pkave}} = M_{\mathrm{pkeq}}\,\dot{i}_{\mathrm{dtol}}. \end{cases} \tag{A8}$$

Based on (A8), the average circuits are obtained, as shown in Fig. 35(a) and (b). The average model can be established based on the average circuits. The equations of the driving circuit are written as

$$\begin{cases} V_{\mathrm{dri}} = (R_{\mathrm{g}} + R_{\mathrm{gineq}})n i_{\mathrm{gave}} + (L_{\mathrm{g}} + L_{\mathrm{gkeq}})\,n\dot{i}_{\mathrm{gave}} \\ \qquad + v_{\mathrm{pgave}} - v_{\mathrm{pkave}} + v_{\mathrm{gsave}} \\ nC_{\mathrm{iss}}\,\dot{v}_{\mathrm{gsave}} = nC_{\mathrm{dg}}\,\dot{v}_{\mathrm{ds}} + n i_{\mathrm{gave}}. \end{cases} \tag{A9}$$

In many circuits, there are multiple paralleled ceramic decoupling capacitors. The decoupling branch's equivalent series inductance (ESL) is small, making the total equivalent ESL of C_{link} small, which can be neglected [35]. The equivalent series resistance (ESR) of the decoupling branch is also small. It only affects the loop oscillation after the switching transients and does not impact the transient current waveforms and switching energy. Therefore, the ESL and ESR of C_{link} are neglected. Moreover, the voltage change on C_{link} in Fig. 35(a) is neglected, and the equation of the power circuit can be written as

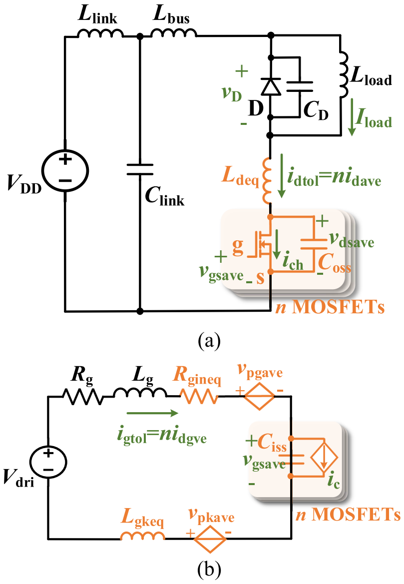


Fig. 35. Average circuits. (a) Average power circuit. (b) Average driving circuit.

$$V_{\mathrm{DD}} = (L_{\mathrm{bus}} + L_{\mathrm{deq}})\,\dot{i}_{\mathrm{dtol}} + v_{\mathrm{D}} + v_{\mathrm{ds}}. \tag{A10}$$

Based on the working region, Kirchhoff's current law (KCL) equations of the MOSFETs can be written.

1) When the MOSFETs work in the ohmic region

$$nC_{\mathrm{oss}}\,\dot{v}_{\mathrm{ds}} = n i_{\mathrm{dave}} - \frac{v_{\mathrm{ds}}}{R_{\mathrm{ds(on)ave}}/n} \tag{A11}$$

where $R_{\mathrm{ds(ON)ave}}$ is the average resistance of the MOSFETs, which is equal to $i_{\mathrm{chave}}/v_{\mathrm{ds}}$. i_{chave} is obtained by the average ohmic-region output characteristic using v_{ds} and v_{gsave}.

2) When the MOSFETs work in the controlled region

$$nC_{\mathrm{oss}}\,\dot{v}_{\mathrm{ds}} = n i_{\mathrm{dave}} - n i_{\mathrm{chave}} \tag{A12}$$

where i_{chave} is determined by v_{gsave} and the average transfer characteristic.

Based on the working region, the KCL of the diode can be written.

1) When $v_{\mathrm{D}} < -V_{\mathrm{D0}}$, the diode is conducting

$$C_{\mathrm{D}}\,\dot{v}_{\mathrm{D}} = n i_{\mathrm{dave}} + \frac{-v_{\mathrm{D}} - V_{\mathrm{D0}}}{R_{\mathrm{D}}} - I_{\mathrm{load}}. \tag{A13}$$

When the freewheeling diode is composed of n dies connected in parallel, V_{D0} takes the average value of the paralleled dies, and R_{D} takes the paralleled value.

2) When $v_{\mathrm{D}} > -V_{\mathrm{D0}}$, the diode is cut off

$$C_{\mathrm{D}}\,\dot{v}_{\mathrm{D}} = n i_{\mathrm{dave}} - I_{\mathrm{load}}. \tag{A14}$$

Choosing $v_{\mathrm{D}}, v_{\mathrm{ds}}, v_{\mathrm{gsave}}, i_{\mathrm{dave}}$, and i_{gave} as the state variables, the state equation can be written as

$$\dot{\boldsymbol{Z}} = \boldsymbol{G} \cdot \boldsymbol{Z} + \boldsymbol{H} \cdot \boldsymbol{K} \tag{A15}$$

where $\boldsymbol{Z}= [v_{\mathrm{D}}\ v_{\mathrm{ds}}\ v_{\mathrm{gsave}}\ i_{\mathrm{dave}}\ i_{\mathrm{gave}}]^{\mathrm{T}}$, and $\boldsymbol{K}= [V_{\mathrm{D0}}\ V_{\mathrm{DD}}\ V_{\mathrm{dri}}\ I_{\mathrm{load}}\ i_{\mathrm{chave}}]^{\mathrm{T}}$. $\boldsymbol{G}$ and $\boldsymbol{H}$ are different under different conditions of the MOSFETs and diode and are derived from (A9)–(A14).

1) When the MOSFETs work in the ohmic region and the diode is conducting, $\boldsymbol{G}$ and $\boldsymbol{H}$ are expressed as (A17), where

$$\begin{cases} \alpha = \frac{1}{C_{\mathrm{D}}}, \beta = \frac{1}{C_{\mathrm{oss}}}, \gamma = \frac{1}{C_{\mathrm{iss}}} \\ \delta = \frac{1}{n(L_{\mathrm{bus}}+L_{\mathrm{deq}})}, \varepsilon = \frac{1}{L_{\mathrm{g}}+L_{\mathrm{gkeq}}}, \varphi = M_{\mathrm{pgeq}} - M_{\mathrm{pkeq}}. \end{cases} \tag{A16}$$

2) When the MOSFETs work in the ohmic region and the diode is cut off, $\boldsymbol{G}$ and $\boldsymbol{H}$ are expressed as (A18).

3) When the MOSFETs work in the controlled region and the diode is conducting, $\boldsymbol{G}$ and $\boldsymbol{H}$ are expressed as (A19).

4) When the MOSFETs work in the controlled region and the diode is cut off. $\boldsymbol{G}$ and $\boldsymbol{H}$ are expressed as (A20)

$$\begin{cases} G = \begin{bmatrix} -\frac{\alpha}{R_{\mathrm{D}}} & 0 & 0 & n\alpha & 0 \\ 0 & -\frac{\beta}{R_{\mathrm{ds(on)}}} & 0 & \beta & 0 \\ 0 & -\frac{\beta\gamma C_{\mathrm{dg}}}{R_{\mathrm{ds(on)}}} & 0 & \beta\gamma C_{\mathrm{dg}} & \gamma \\ -\delta & -\delta & 0 & 0 & 0 \\ \varepsilon\delta\varphi & \varepsilon\delta\varphi & -\frac{\varepsilon}{n} & 0 & -\varepsilon(R_{\mathrm{g}} + R_{\mathrm{gineq}}) \end{bmatrix} \\ H = \begin{bmatrix} -\frac{\alpha}{R_{\mathrm{D}}} & 0 & 0 & -\alpha & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & \delta & 0 & 0 & 0 \\ 0 & -\varepsilon\delta\varphi & \frac{\varepsilon}{n} & 0 & 0 \end{bmatrix} \end{cases} \tag{A17}$$

$$\begin{cases} G = \begin{bmatrix} 0 & 0 & 0 & n\alpha & 0 \\ 0 & -\frac{\beta}{R_{\mathrm{ds(on)}}} & 0 & \beta & 0 \\ 0 & -\frac{\beta\gamma C_{\mathrm{dg}}}{R_{\mathrm{ds(on)}}} & 0 & \beta\gamma C_{\mathrm{dg}} & \gamma \\ -\delta & -\delta & 0 & 0 & 0 \\ \varepsilon\delta\varphi & \varepsilon\delta\varphi & -\frac{\varepsilon}{n} & 0 & -\varepsilon(R_{\mathrm{g}} + R_{\mathrm{gineq}}) \end{bmatrix} \\ H = \begin{bmatrix} 0 & 0 & 0 & -\alpha & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & \delta & 0 & 0 & 0 \\ 0 & -\varepsilon\delta\varphi & \frac{\varepsilon}{n} & 0 & 0 \end{bmatrix} \end{cases} \tag{A18}$$

$$\begin{cases} G = \begin{bmatrix} -\frac{\alpha}{R_{\mathrm{D}}} & 0 & 0 & n\alpha & 0 \\ 0 & 0 & 0 & \beta & 0 \\ 0 & 0 & 0 & \beta\gamma C_{\mathrm{dg}} & \gamma \\ -\delta & -\delta & 0 & 0 & 0 \\ \varepsilon\delta\varphi & \varepsilon\delta\varphi & -\frac{\varepsilon}{n} & 0 & -\varepsilon(R_{\mathrm{g}} + R_{\mathrm{gineq}}) \end{bmatrix} \\ H = \begin{bmatrix} -\frac{\alpha}{R_{\mathrm{D}}} & 0 & 0 & -\alpha & 0 \\ 0 & 0 & 0 & 0 & -\beta \\ 0 & 0 & 0 & 0 & -\beta\gamma C_{\mathrm{dg}} \\ 0 & \delta & 0 & 0 & 0 \\ 0 & -\varepsilon\delta\varphi & \frac{\varepsilon}{n} & 0 & 0 \end{bmatrix} \end{cases} \tag{A19}$$

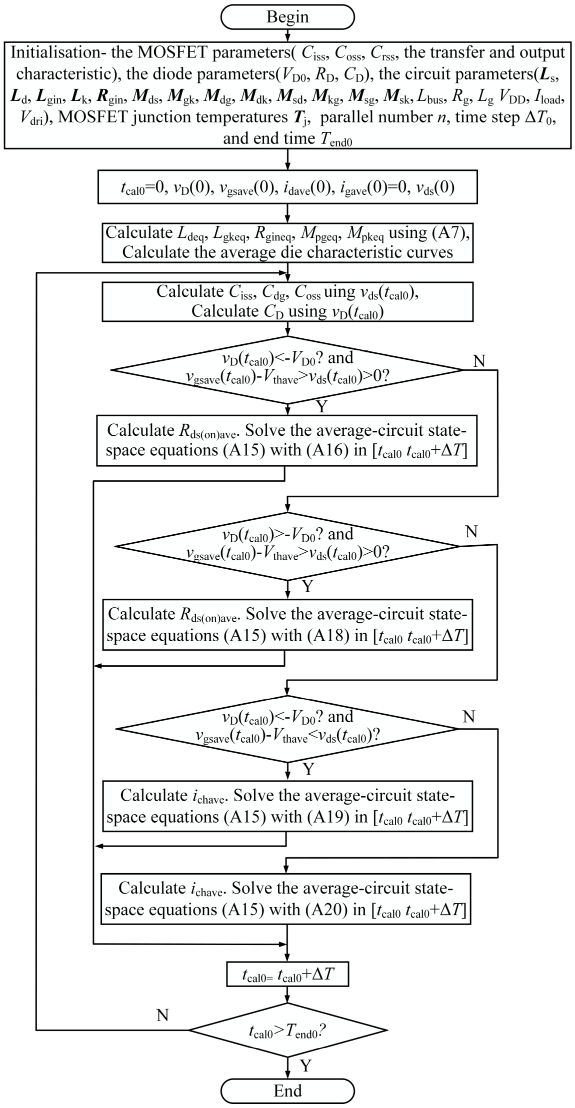


Fig. 36. Calculation flowchart of the average model.

$$\begin{cases} G = \begin{bmatrix} 0 & 0 & 0 & n\alpha & 0 \\ 0 & 0 & 0 & \beta & 0 \\ 0 & 0 & 0 & \beta\gamma C_{\mathrm{dg}} & \gamma \\ -\delta & -\delta & 0 & 0 & 0 \\ \varepsilon\delta\varphi & \varepsilon\delta\varphi & -\frac{\varepsilon}{n} & 0 & -\varepsilon(R_{\mathrm{g}} + R_{\mathrm{gineq}}) \end{bmatrix} \\ H = \begin{bmatrix} 0 & 0 & 0 & -\alpha & 0 \\ 0 & 0 & 0 & 0 & -\beta \\ 0 & 0 & 0 & 0 & -\beta\gamma C_{\mathrm{dg}} \\ 0 & \delta & 0 & 0 & 0 \\ 0 & -\varepsilon\delta\varphi & \frac{\varepsilon}{n} & 0 & 0 \end{bmatrix}. \end{cases} \tag{A20}$$

The calculation flowchart of the average model is shown in Fig. 36. First, the circuit parameters and the initial values are given. During the turn-ON period, the initial values can be written as

$$\begin{cases} v_{\mathrm{D}}(0) = -(R_{\mathrm{D}} I_{\mathrm{load}} + V_{\mathrm{D0}}) \\ v_{\mathrm{ds}}(0) = V_{\mathrm{DD}} - v_{\mathrm{D}}(0) \\ v_{\mathrm{gsave}}(0) = V_{\mathrm{dri(off)}} \\ i_{\mathrm{dave}}(0) = 0 \\ i_{\mathrm{gave}}(0) = 0. \end{cases} \tag{A21}$$

During the turn-OFF period, they can be written as

$$\begin{cases} v_{\mathrm{ds}}(0) = I_{\mathrm{load}} R_{\mathrm{ds(on)ave}}(0)/n \\ v_{\mathrm{D}}(0) = V_{\mathrm{DD}} - v_{\mathrm{ds}}(0) \\ v_{\mathrm{gsave}}(0) = V_{\mathrm{dri(on)}} \\ i_{\mathrm{dave}}(0) = I_{\mathrm{load}}/n \\ i_{\mathrm{gave}}(0) = 0. \end{cases} \tag{A22}$$

Then, the average circuit parameters are calculated by (A7). The transfer and output characteristic curves of the paralleled dies are obtained by interpolating using $\boldsymbol{T}_{\mathrm{j}}$ and then averaged to obtain the average characteristic curves. Then, the average model is solved by time stepping.

During each time step $[T_{\mathrm{cal0}}, T_{\mathrm{cal0}} + \Delta T]$: First, the curve data of $C_{\mathrm{iss}}(v_{\mathrm{ds}})$, $C_{\mathrm{dg}}(v_{\mathrm{ds}})$, and $C_{\mathrm{oss}}(v_{\mathrm{ds}})$ are linearly interpolated by the latest calculated $v_{\mathrm{ds}}(T_{\mathrm{cal0}})$, and the curve data of $C_{\mathrm{D}}(v_{\mathrm{D}})$ is linearly interpolated by $v_{\mathrm{D}}(T_{\mathrm{cal0}})$. The obtained C_{iss}, C_{dg}, C_{oss}, and C_{D} values are used for calculation in this time step. Then, the working conditions of the MOSFETs and diode are judged first, and the corresponding models are used for calculation.

1) When the MOSFETs work in the ohmic region, $i_{\mathrm{chave}}(T_{\mathrm{cal0}})$ is calculated by interpolating the average output curve data using $v_{\mathrm{gsave}}(T_{\mathrm{cal0}})$ and $v_{\mathrm{ds}}(T_{\mathrm{cal0}})$. Then, $R_{\mathrm{ds(on)ave}}(T_{\mathrm{cal0}})$ is calculated and used for calculation in this time step.
2) When the MOSFETs work in the controlled region, $i_{\mathrm{chave}}(T_{\mathrm{cal0}})$ is obtained by linearly interpolating the curve data of the average transfer characteristic using $v_{\mathrm{gsave}}(T_{\mathrm{cal0}})$. Then, $i_{\mathrm{chave}}(T_{\mathrm{cal0}})$ is used for calculation in this time step.

By reinterpolating the curve data of the average transfer characteristic, the average ohmic-region characteristic, and the capacitance curves within each time step, the nonlinearities of the characteristics are involved. Finally, the corresponding state equations are solved to obtain the average waveforms.

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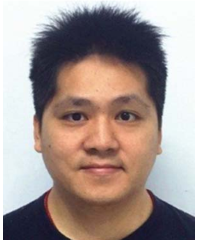
Jianwei Lv received the B.S. degree in electrical and electronic engineering in 2020 from Huazhong University of Science and Technology, Wuhan, China, where he is currently working toward the Ph.D. degree in electrical engineering with the School of Electrical and Electronic Engineering.

His current research interests include WBG devices modeling, packaging, and integration.



Cai Chen (Member, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from Huazhong University of Science and Technology, Wuhan, China, in 2008 and 2014, respectively.

From March to December 2013, he was an Intern in GE Global Research Center, Shanghai, China. From 2014 to 2016, he was with the Advanced Semiconductor, Packaging, and Integration Lab, Huazhong University of Science and Technology, Wuhan, Hubei, China as a Postdoctoral Researcher. From 2016 to 2017, he was a visiting scholar with the Center for High Performance Power Electronics, The Ohio State University, Columbus, OH, USA. From 2017 to 2018, he was a visiting scholar with the College of Engineering, University of Arkansas, Fayetteville, AR, USA. In 2019, he was with the Huazhong University of Science and Technology, Wuhan, China, as an Associate Research Fellow. In 2024, he was promoted to Professor. His research interests include WBG devices packaging, integration, packaging EMI issues, packaging reliability, and high-density applications.

Yiyang Yan received the B.S. degree in functional material and the M.S. degree in electrical engineering in 2018 and 2021, respectively, from Huazhong University of Science and Technology, Wuhan, China, where he is currently working toward the Ph.D. degree in electrical engineering with the School of Electrical and Electronic Engineering.

His research interests include wide bandgap devices double-sided-cooling packages, high power density inverters, and device thermal modeling.

Baihan Liu (Graduate Student Member, IEEE) received the B.S. degree in electrical and electronic engineering in 2021 from Huazhong University of Science and Technology, Wuhan, China, where he is currently working toward the Ph.D. degree in electrical engineering with the School of Electrical and Electronic Engineering.

His current research interests include wide bandgap devices packaging, integration, and high-temperature applications.

Zexiang Zheng received the B.S. degree in electrical and electronic engineering in 2023 from Huazhong University of Science and Technology, Wuhan, China, where he is currently working toward the Ph.D. degree in electrical engineering with the School of Electrical and Electronic Engineering.

His current research interests include wide-bandgap devices modeling, packaging, and high power density inverters.

Yong Kang (Fellow, IEEE) was born in Hubei Province, China, in 1965. He received the B.E., M.E, and Ph.D. degrees in electrical engineering from Huazhong University of Science and Technology, Wuhan China, in 1988, 1991, and 1994, respectively.

In 1994, he was with Huazhong University of Science and Technology as a Lecturer and was promoted to Associate Professor in 1996 and to Full Professor in 1998. He has authored more than 60 technical papers. His research interests include power electronic converter, ac drivers, electromagnetic compatibility, digital control techniques, WBG device packaging, and applications.