Letters

A Hybrid PWM Pattern of Three-Phase Buck PFC Converter With Low Common-Mode Voltage and Low Voltage Stress

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***Abstract*—A three-phase buck power factor correction (PFC) converter with high frequency and high power density faces the problems of high common-mode (CM) voltage and high voltage stress on switching devices. In this letter, the influence of different pulsewidth modulation (PWM) patterns on CM voltage and voltage stress is studied, and the high-frequency current paths in the three-phase buck PFC converter considering parasitic parameters is revealed. A hybrid PWM pattern is proposed to reduce the CM voltage and voltage stress on switching devices. An experimental prototype 200-kHz switching frequency is built to verify the analysis results in this letter.**

***Index Terms*—Common-mode (CM) voltage, pulsewidth modulation (PWM) pattern, three-phase buck PFC converter, voltage stress.**

I. Introduction

A THREE-PHASE power factor correction (PFC) converter is the key device to connect the three-phase ac power grid with the dc load. The three-phase buck PFC converter is also known as the current-source rectifier (CSR). It has the advantages of high reliability, small start-up current, and strong ability of current limiting, which can be widely used in small- and medium-power applications, such as multielectric aircraft and vehicle chargers [1]. In the aforementioned fields, the three-phase buck PFC converter with high switching frequency and high power density faces with issues of high common-mode (CM) noise and high voltage stress on switching devices. At present, these problems are mainly solved by improving topologies and their modulation strategies.

For the issue of CM noise suppression, the optimized modulation strategies are used to reduce the CM voltage peak of the high-power CSRs in [2] and [3]. In [4] and [5], the effect of parasitic capacitances on the input current of the three-phase buck PFC converter is revealed, and then, the CM filter is designed to provide a low-impedance path for high-frequency current. However, the existing solutions that can solve the problem of CM noise rarely focus on efficiency improvement, especially in high-frequency and high-power-density applications.

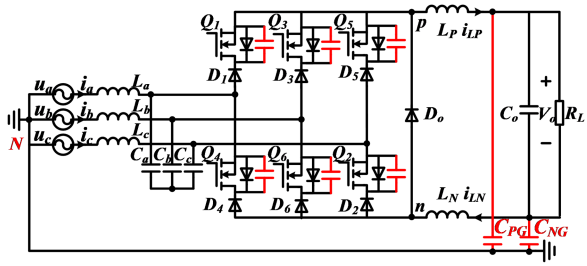

Fig. 1. Three-phase buck PFC converter topology considering parasitic parameters.

Reducing the voltage stress on the switching devices can significantly improve the efficiency of the three-phase buck PFC converter. The switching-loss-optimized (SLO) modulation strategy has lower input current harmonics and lower switching loss, which is widely used in three-phase buck PFC converters [6]. In [7], the influence of parasitic capacitances on the voltage stress of the three-phase buck PFC converter is studied, and an asymmetric modulation strategy to reduce the voltage stress on switching devices is proposed. An improved three-phase buck PFC converter is proposed in [8], where the switching devices only withstand the input phase voltage instead of the input line voltage. Furthermore, the topology proposed in [9] further reduces the voltage stress on switching devices, which enables a more cost-efficient and flexible selection of switching devices.

For the three-phase buck PFC converter with high frequency and high power density, it is difficult for the existing topologies or modulation strategies to take into account both CM voltage suppression and low voltage stress. In this letter, the influence of parasitic capacitances on three-phase buck PFC converters is studied, and the equivalent high-frequency paths of three-phase buck PFC converters are revealed. Moreover, a hybrid pulsewidth modulation (PWM) pattern is proposed, which can not only reduce the CM voltage but also provide a continuous

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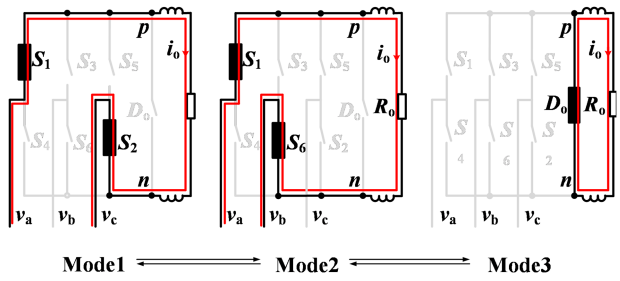

Fig. 2. Operating modes of the three-phase buck PFC converter in each switching period during sector 1.

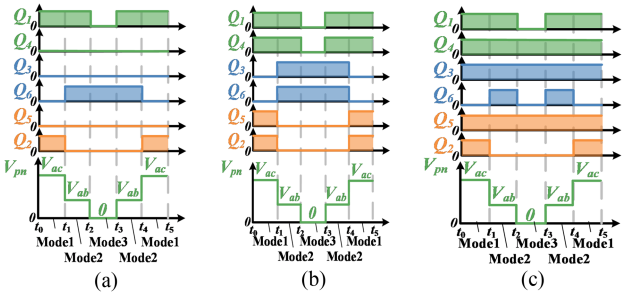

Fig. 3. Three different PWM patterns of the SLO modulation strategy during sector 1. (a) Independent PWM pattern. (b) Redundant PWM pattern. (c) Hybrid PWM pattern.

path for the CM current. The proposed PWM pattern is beneficial to the design of the three-phase buck PFC converter with high frequency and high power density.

II. Analysis of Three Different PWM Patterns of the SLO Modulation Strategy

The topology of the three-phase buck PFC converter is shown in Fig. 1. Each bridge leg of S_i ($i = 1$–6) in this converter consists of one switching device and one diode in series. Moreover, the junction capacitances of the switching devices and the equivalent parasitic capacitances $C_{\rm PG}$ and $C_{\rm NG}$ of the system are considered in this letter.

In the SLO modulation strategy, the input voltage period is equally divided into 12 sectors [5], [6], [7], [8]. For the convenience of analysis, this letter takes sector 1 ($v_a > 0 > v_b > v_c$) as an example for analysis. Fig. 2 shows the three operating modes of this converter within one switching period.

The bridge leg of the three-phase buck PFC converter can only be turned ON when the switching device has a driving signal, and the series diode is subjected to a forward voltage. Therefore, there are a variety of PWM patterns that can achieve the same operating modes shown in Fig. 2. Fig. 3 shows three different PWM patterns, which are named as the independent PWM pattern, the redundant PWM pattern, and the hybrid PWM pattern. The independent PWM pattern and the redundant PWM pattern are described in [5] and [6]; the hybrid PWM pattern is proposed in this letter.

In the independent PWM pattern shown in Fig. 3(a), the switches of bridge legs S_1, S_2, and S_6 have high-frequency driving signals, and the switches of other bridge legs remain OFF. In the redundant PWM pattern shown in Fig. 3(b), the switches of the upper and lower bridge legs of each phase share the same driving signal. In the hybrid PWM pattern shown in Fig. 3(c), the switches of bridge legs S_1, S_2, and S_6 have high-frequency driving signals, while the switches of other bridge legs remain ON. In addition, unlike the other two PWM patterns, when the hybrid PWM pattern is in mode 3, the switch of the bridge leg S_6 is turned OFF.

III. Analysis of the CM Voltage and the Voltage Stress Under Three Different PWM Patterns

Due to the existence of CM voltage and parasitic capacitances in the three-phase buck PFC converter, there are three current paths in the converter at any time: one low-frequency current path and two high-frequency current paths [5]. For the convenience of analysis, the main circuit parameters are as follows: input phase voltage v_i ($i = a, b, c$) is 115 $V_{\rm rms}$, input voltage frequency f_g is 50 Hz, switching frequency f_s is 200 kHz, output voltage $V_{\rm o}$ is 200 V, dc-link inductors L_P and L_N are 150 μH, parasitic capacitances $C_{\rm PG}$ and $C_{\rm NG}$ are set as 500 pF, and the parasitic capacitance $C_{\rm ds}$ of the switching devices is set as 30 pF.

Ignoring the effect of the input *LC* filter, the CM voltage $v_{\rm cm}$ of the converter is defined as

$$v_{\rm cm} = (v_p + v_n)/2 \tag{1}$$

where v_p is the potential difference between point p and neutral point N, and v_n is the potential difference between point n and neutral point N.

During modes 1 and 2, the high-frequency current paths of the three-phase buck PFC converter with three different PWM patterns are consistent, as shown in Fig. 4(a) and (b). Moreover, the switching device Q_1 is always ON during modes 1 and 2, so its voltage stress is 0.

During mode 1, the high-frequency current $i_{C\rm pg}$ flows between the input terminal and the parasitic capacitor $C_{\rm PG}$ through the upper bridge leg S_1. The high-frequency current $i_{C\rm ng}$ flows between the input terminal and the parasitic capacitor $C_{\rm NG}$ through the lower bridge leg S_2. At this time, the CM voltage $v_{\rm cm}$ of the converter under three different PWM patterns is equal, and is -$v_{\rm b}$/2.

When mode 1 transits to mode 2, the path of current $i_{C\rm pg}$ remains unchanged, while the path of the current $i_{C\rm ng}$ is switched from the bridge leg S_2 to the bridge leg S_6. During mode 2, the $v_{\rm cm}$ of the converter with the three different PWM patterns is equal and is $-v_c/2$.

Different PWM patterns mainly affect the operating characteristics of the converter during mode 3, so the CM voltage and the voltage stress on the switching devices under different PWM patterns are analyzed in detail.

A. Independent PWM Pattern

During mode 3, the high-frequency current path of the three-phase buck PFC converter under the independent PWM pattern is shown in Fig. 4(c). When the converter transits from mode 2 to mode 3, the upper bridge leg S_1 is turned OFF, and the high-frequency current $i_{C\rm pg}$ can only flow through the junction

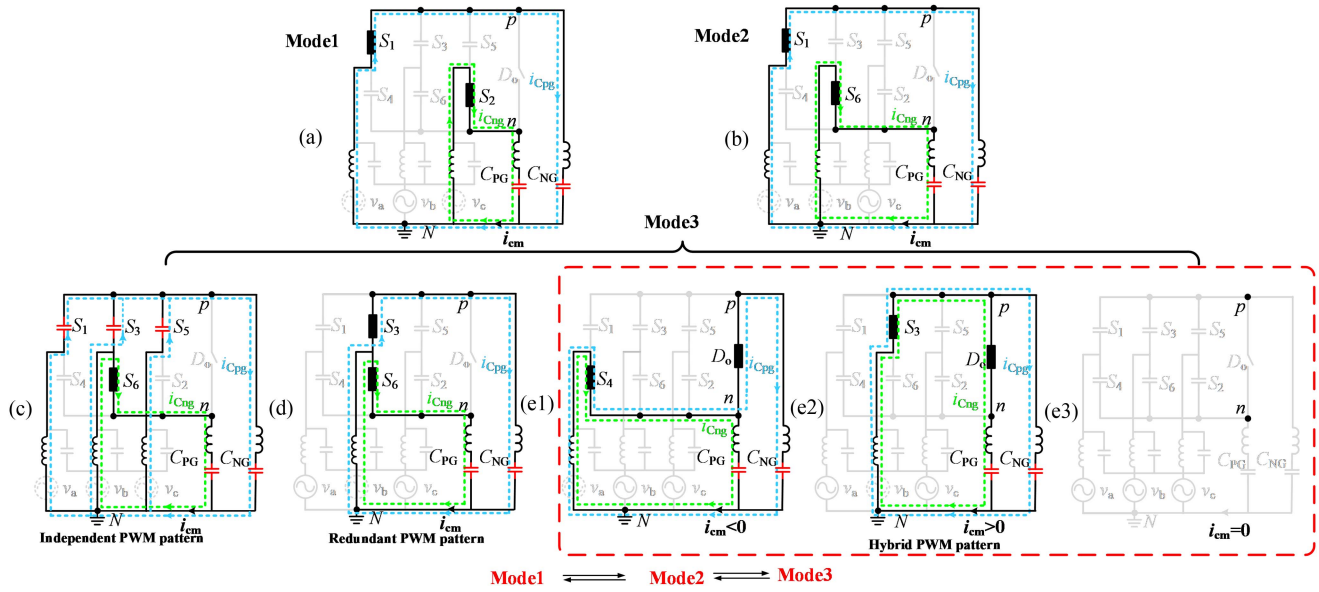

Fig. 4. High-frequency current paths of the three-phase buck PFC converter under different PWM patterns. (a) Mode 1 under different PWM patterns. (b) Mode 2 under different PWM patterns. (c) Mode 3 under the independent PWM pattern. (d) Mode 3 under the redundant PWM pattern. (e1) State 1 of mode 3 under the hybrid PWM pattern. (e2) State 2 of mode 3 under the hybrid PWM pattern. (e3) State 3 of mode 3 under the hybrid PWM pattern.

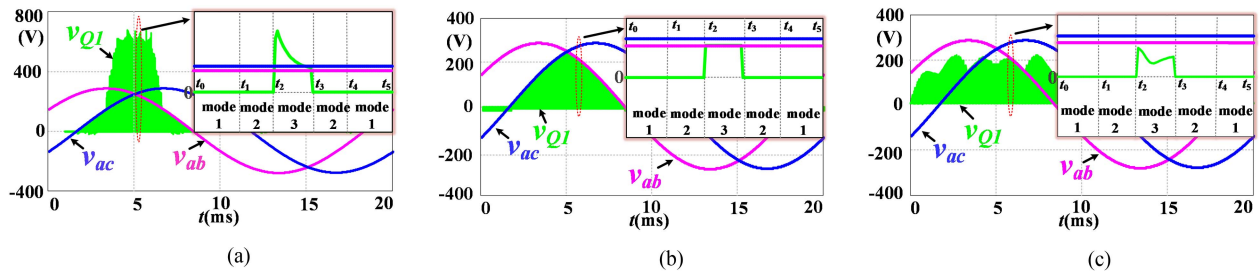

Fig. 5. Voltage across Q_1 of the three-phase buck PFC converter under three different PWM patterns. (a) Independent PWM pattern. (b) Redundant PWM pattern. (c) Hybrid PWM pattern.

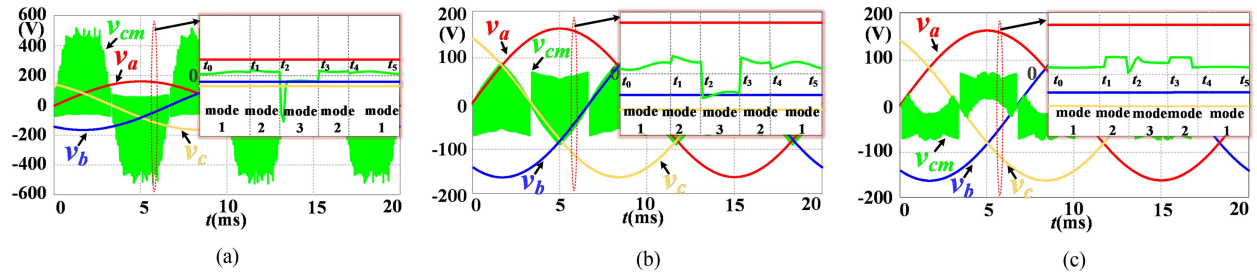

Fig. 6. CM voltage of the three-phase buck PFC converter under three different PWM patterns. (a) Independent PWM pattern. (b) Redundant PWM pattern. (c) Hybrid PWM pattern.

capacitances of switching devices in the upper bridge legs. However, the flow path of the current $i_{C\mathrm{ng}}$ remains unchanged. The unsmooth transition of the current $i_{C\mathrm{pg}}$ leads to the large voltage spike of v_p and v_n during mode 3. In the meantime, the voltage across Q_1 is

$$v_{Q1} = v_a - v_b + \int_{t_2}^{t-t_2} i_{C_{\mathrm{PG}}}(t)/\left(3 \times C_{ds}\right) dt \gg v_{ab}. \quad (2)$$

According to (2), there is a large voltage spike on the switching device of the bridge leg under the independent PWM pattern, which is closely related to the parasitic parameters of the converter. It can be seen from Fig. 5(a) that the voltage stress on Q_1 is higher than the peak value of input line-to-line voltage. Fig. 6(a) shows that the large voltage spike also exists in the CM voltage during the transition from mode 2 to mode 3.

B. Redundant PWM Pattern

During mode 3, the high-frequency current paths of the three-phase buck PFC converter under the redundant PWM pattern are

shown in Fig. 4(d). When mode 2 transitions to mode 3, the path of the current $i_{C\mathrm{pg}}$ is switched from bridge leg S_1 to bridge leg S_3. The path of the current $i_{C\mathrm{ng}}$ remains unchanged. During mode 3, the CM voltage is v_b, and the voltage across Q_1 is expressed as

$$v_{Q1} = v_a - v_b = v_{ab}. \tag{3}$$

Therefore, the peak-to-peak value of the CM voltage during each switching period in sector 1 is

$$v_{\mathrm{cm\_}p} = -\frac{v_c}{2} - v_b = \frac{v_{ab}}{2}. \tag{4}$$

Figs. 5(b) and 6(b) show the voltage across Q_1 and the CM voltage of the converter under the redundant PWM pattern, respectively. Since mode 2 can smoothly transition to mode 3, Q_1 always withstands the input line-to-line voltage. It can be seen from Fig. 6(b) that the maximum peak-to-peak value of the CM voltage is 122 V within one input voltage period, and it occurs when the odd sectors switch to the even sectors.

C. Hybrid PWM Pattern

The three-phase buck PFC converter under the hybrid PWM pattern may have three operating states during mode 3. The high-frequency current paths of these three operating states are shown in Fig. 4(e1)–(e3), respectively. Which state will happen depends on the CM current.

If i_{CM} is less than 0, operating state 1 is shown in Fig. 4(e1). When mode 2 transitions to mode 3, the path of the current $i_{C\mathrm{pg}}$ is switched from bridge leg S_1 to bridge leg S_4 and the freewheeling diode D_{o}. The path of the high-frequency current $i_{C\mathrm{ng}}$ is switched from bridge leg S_6 to bridge leg S_4. At this time, v_p and v_n are the same, both are v_a, and the CM voltage during this state is v_a. During state 1, due to $v_{pn} = 0$ and the conduction of bridge leg S_4, the voltage across Q_1 is 0.

If i_{CM} is greater than 0, operating state 2 is shown in Fig. 4(e2). When mode 2 transitions to mode 3, the path of the current $i_{C\mathrm{pg}}$ is switched from bridge leg S_1 to bridge leg S_3. The path of the high-frequency current $i_{C\mathrm{ng}}$ is switched from bridge leg S_6 to bridge leg S_3 and the freewheeling diode D_{o}. At this time, v_p and v_n are the same, both are v_b, and the CM voltage of this state is v_b. The voltage across Q_1 is v_{ab}.

If i_{CM} is equal to 0, operating state 3 is shown in Fig. 4(e3). The high-frequency currents $i_{C\mathrm{pg}}$ and $i_{C\mathrm{ng}}$ are equal to 0. The high-frequency current paths are not existed in the converter. The CM voltage of this state is

$$v_{\mathrm{cm}} = 0.5\,(v_p + v_n) \approx -\frac{v_b v_c}{v_b + v_c}. \tag{5}$$

According to (5), the CM voltage satisfies as

$$-\frac{v_b}{2} \le v_{\mathrm{cm}} \le -\frac{v_c}{2}. \tag{6}$$

During state 3, the voltage across Q_1 is expressed as

$$v_{Q1} = v_a - v_{\mathrm{cm}} \le v_{ab}. \tag{7}$$

Based on the aforementioned analysis, it can be concluded that the voltage stress on Q_1 is less than the peak value of the line voltage.

It also should be noted that considering the small CM current in hybrid PWM pattern, states 1 and 2 are usually maintained for a relatively short time. The CM voltage of these two states usually does not affect the magnitude of the CM current. Therefore, when considering the CM voltage during mode 3, these two states can be ignored. In summary, the peak-to-peak value of the CM voltage during each switching period in sector 1 is

$$v_{\mathrm{cm\_}p} = -\frac{v_c}{2} - \left(-\frac{v_b}{2}\right) = \frac{v_{bc}}{2}. \tag{8}$$

Based on the aforementioned analysis, the peak-to-peak values of the CM voltage within one input voltage period under redundant PWM pattern and hybrid PWM pattern are shown in Fig. 7. It can be seen that the peak-to-peak value of the CM voltage of the three-phase buck PFC converter under the hybrid PWM pattern is less than that under the redundant PWM pattern within each input voltage period.

Figs. 5(c) and 6(c) show the voltage across Q_1 and CM voltage of the three-phase buck PFC converter under the hybrid PWM pattern, respectively. It can be observed that the voltage stress on Q_1 is lower than the peak value of the input line-to-line voltage. From Fig. 6, the converter under the hybrid PWM pattern has the lowest CM voltage, compared to the independent and redundant PWM patterns.

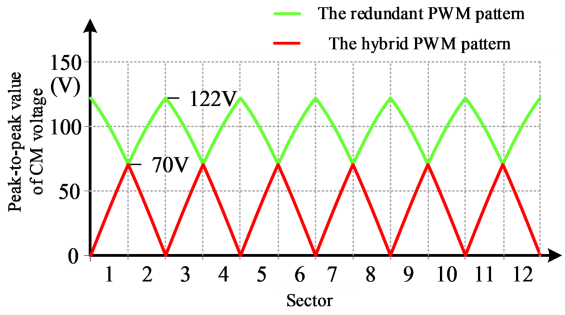

Fig. 7. Calculated peak-to-peak value of the CM voltage under the redundant PWM pattern and the hybrid PWM pattern.

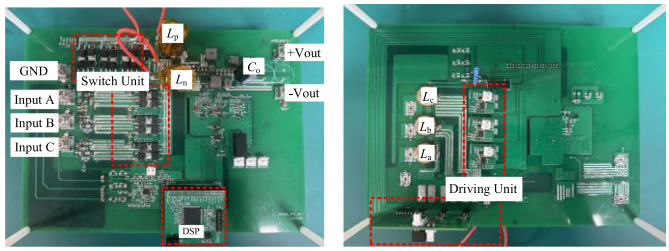

Fig. 8. Snapshots of the experimental prototype. (a) Top view. (b) Bottom view.

IV. Experimental Verification

To verify the feasibility of the proposed hybrid PWM pattern, a 500-W experimental prototype is developed, as shown in Fig. 8. Because of the large voltage spike in independent PWM pattern, the redundant PWM and the hybrid PWM patterns are adopted in the experimental prototype. The main circuit parameters are consistent with the simulation parameters.

Figs. 9 shows experimental results of the three-phase input voltage and input current of phase A. As can be seen from

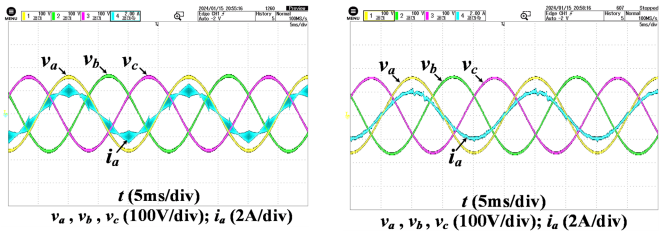

Fig. 9. Experimental results of the three-phase input voltage and input current of phase A. (a) Under the redundant PWM pattern. (b) Under the hybrid PWM pattern.

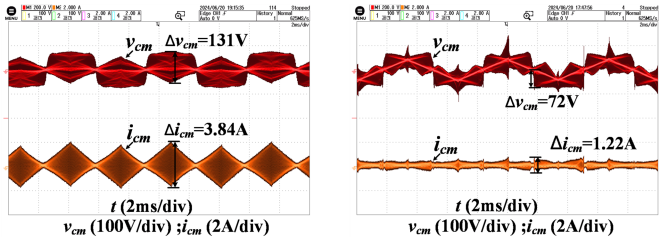

Fig. 10. Experimental results of CM voltage and CM current. (a) Under the redundant PWM pattern. (b) Under the hybrid PWM pattern.

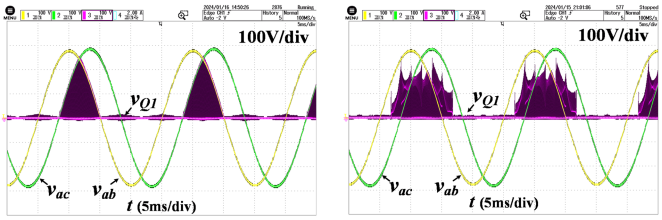

Fig. 11. Experimental results of voltage across Q1. (a) Under the redundant PWM pattern. (b) Under the hybrid PWM pattern.

Fig. 9, the hybrid PWM pattern can effectively suppress the high-frequency noise of the input current compared with the redundant PWM pattern.

Fig. 10 shows the CM voltage and the CM current waveforms by the following measurements. The CM voltage waveforms are obtained by averaging v_p and v_n, and the CM current can be obtained by subtracting the inductor currents i_{LP} and i_{LN}. Ignoring the slight oscillation, the peak-to-peak value of the CM voltage of the converter under the hybrid pattern is much smaller than that under the redundant pattern within an input voltage period. Furthermore, the CM current under the redundant PWM pattern is as high as 3.84 A. However, the CM current under the hybrid PWM pattern is only 1.22 A. This comparison shows that the hybrid PWM pattern can effectively reduce the CM current.

Fig. 11 shows the voltage waveform across Q_1. No matter whether the redundant PWM pattern or the hybrid PWM pattern is used in this converter, the voltage across Q_1 is always lower than the peak value of the input line-to-line voltage.

Fig. 12 shows the efficiency curves of the three-phase buck PFC converter using the redundant PWM pattern and the hybrid PWM pattern under different loads. The proposed hybrid PWM pattern effectively reduces the CM current circulation in the system, thereby decreasing the conduction loss. Therefore, compared with the redundant PWM pattern, the hybrid PWM pattern achieves higher system efficiency under different loads.

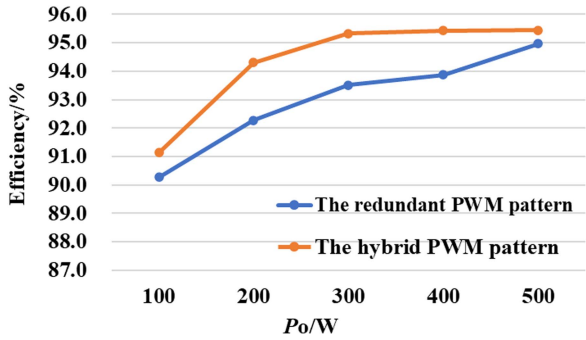

Fig. 12. Efficiency curves of the three-phase buck PFC converter using the redundant PWM pattern and the hybrid PWM pattern under different loads.

V. Conclusion

For the three-phase buck PFC converter with high switching frequency, the traditional PWM pattern may lead to larger CM current and higher voltage stress on switching devices. In this letter, the influence of three PWM patterns on the high-frequency current paths of the three-phase buck PFC converter is studied. A hybrid PWM pattern with low voltage stress and low CM voltage is proposed, which is of great significance for the design three-phase buck PFC converters with high frequency and high efficiency.

References

[1] A. Stupar, T. Friedli, J. Minibock, and J. W. Kolar, "Towards a 99% efficient three-phase buck-type PFC rectifier for 400-V DC distribution systems," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1732–1744, Apr. 2012.

[2] N. Zhu, D. Xu, B. Wu, N. R. Zargari, M. Kazerani, and F. Liu, "Common-mode voltage reduction methods for current-source converters in medium-voltage drives," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 995–1006, Feb. 2013.

[3] J. Shang and Y. W. Li, "A space-vector modulation method for common-mode voltage reduction in current-source converters," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 374–385, Jan. 2014.

[4] M. L. Heldwein, T. Nussbaumer, and J. W. Kolar, "Common mode modelling and filter design for a three-phase buck-type pulse width modulated rectifier system," *IET Power Electron*, vol. 3, no. 2, pp. 209–218, 2010.

[5] Q. Chen, J. Xu, L. Wang, R. Huang, and H. Ma, "Analysis and improvement of the effect of distributed parasitic capacitance on high-frequency high-density three-phase buck rectifier," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 6415–6428, Jun. 2021.

[6] F. Xu, B. Guo, L. M. Tolbert, F. Wang, and B. J. Blalock, "An all-SiC three-phase buck rectifier for high-efficiency data center power supplies," *IEEE Trans. Ind. Appl.*, vol. 49, no. 6, pp. 2662–2673, Nov./Dec. 2013.

[7] H. Cao, P. Yang, X. Guo, R. Huang, and J. Xu, "An improved asymmetric modulation of current-source rectifier with cm filter for low voltage stress on switching devices," *IEEE Trans. Power Electron.*, vol. 38, no. 7, pp. 7964–7970, Jul. 2023.

[8] J. Lei, S. Feng, J. Zhao, W. Chen, P. Wheeler, and M. Shi, "An improved three-phase buck rectifier topology with reduced voltage stress on transistors," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2458–2466, Mar. 2020.

[9] Q. Chen, J. Xu, Z. Fei, R. Huang, and L. Wang, "An improved three-phase buck rectifier with low voltage stress on switching devices," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 6168–6174, Jun. 2021.