A Gate Open-Circuit Failure Detection Method of SiC MOSFETs Based on Internal Gate State Extraction

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***Abstract*—Gate open-circuit failure caused by cracking and liftoff of gate bond wires has been demonstrated to be a new failure mode of silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs), which can cause serious consequences such as shoot-through fault and gate-oxide breakdown. To enhance the reliability and robustness of SiC MOSFETs, a fast and accurate detection scheme for such failure is required. This article proposes a gate open-circuit failure detection method based on the extraction of the internal gate state. Although this state is unavailable externally, it can be extracted from gate current pulses. The gate open-circuit failures are then detected by checking the inconsistency between the drive signal and the internal gate state. Experimental results validate that the proposed method can accurately detect all types of gate open-circuit failures within 55 ns.**

***Index Terms*—Failure detection, gate open-circuit failure, internal gate state, SiC MOSFETs.**

I. Introduction

SILICON carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) have been widely used in power converters due to their higher breakdown voltage, higher operating temperature, and faster switching speed than their silicon (Si) counterparts [1]. However, due to the lack of related research and practical application data, SiC MOSFETs still face many reliability issues, one of which is the bond wire failure that has received much attention [2]. In the past, research of bond wire failures in SiC MOSFETs almost exclusively focused only on power source bond wires and not on gate bond wires. However, according to the results of power cycling tests in [3], the gate and Kelvin source bond wires (referred to as gate bond wires hereafter) are also a weak part of the package structure in SiC MOSFETs and can even fail before the power source bond wires. From the perspective of thermo-mechanical stress, the mechanism of gate bond wire failures can be explained as follows.

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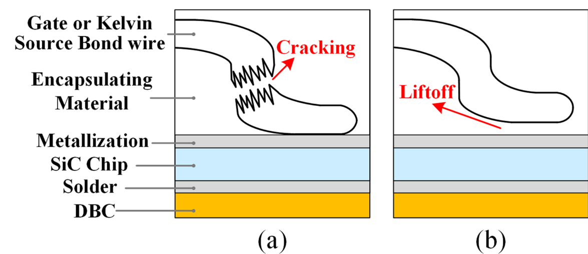

Fig. 1. Schematic package cross section of gate open-circuit failures. (a) Gate bond wire cracking. (b) Gate bond wire liftoff.

1) *Cracking:* Due to the coefficient of thermal expansion (CTE) mismatch between different materials, thermo-mechanical stress can be formed at the gate bond wires when the device temperature swings [4]. Such long-term thermo-mechanical stress can eventually cause gate bond wires to crack, as shown in Fig. 1(a).
2) *Liftoff:* The thermo-mechanical stress can also change the aluminum metallization structure of the chip, reduce the interface bonding strength, and eventually force gate bond wires to liftoff [5], as shown in Fig. 1(b).

Since gate bond wire failure results in an open circuit in the gate loop, this type of failure is defined as gate open-circuit failure. After a gate open-circuit failure, the gate driver loses control of the gate, leaving the device in an always-ON or always-OFF state. If this failure is not detected in time and addressed properly, it may evolve into a shoot-through fault, and even extend the failure to the healthy complementary device. It, therefore, requires a fast and reliable detection scheme.

However, the detection of gate open-circuit failures is challenging in the following aspects.

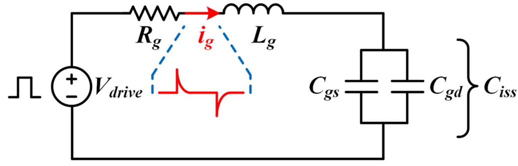

Fig. 2. Gate loop equivalent circuit.

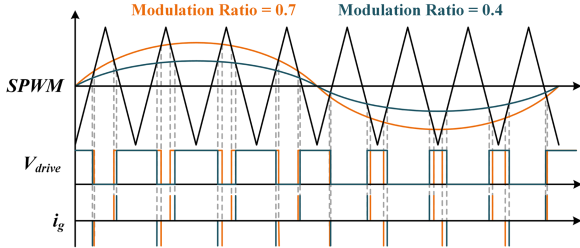

Fig. 3. Drive signal and gate current of sinusoidal pulse width modulation inverter under different modulation ratios.

1) The gate open-circuit failures always occur inside the device package. The externally measured gate-source voltage after failure is not significantly different from that before failure (both equal to the driver output voltage), and the actual internal gate-source voltage cannot be measured.
2) Gate open-circuit failures can evolve into short-circuit faults or cause the device to fail to turn ON. Thus, the characteristics of gate open-circuit failures are complex and variable. This means that it is difficult to distinguish gate open-circuit failures from other types of failures, such as short-circuit caused by gate-oxide degradation [6] and source open-circuit caused by source bond wires cracking [7].
3) The gate loop only flows high-frequency pulse current during switching transient, whereas no current flows during steady state, except for a small to negligible gate leakage current [8], as shown in Fig. 2. This means that gate open-circuit failures cannot be detected by the typical open-circuit failure detection method of detecting current in real-time [9], but only by detecting gate current pulses during switching transient. However, the gate current pulses have a high degree of freedom. In the converter based on pulse frequency modulation, the frequency of the gate current pulses is variable. In the converter based on pulsewidth modulation (PWM), the pulse position of the gate current pulses is variable. For example, the gate current pulses under different modulation ratios in sinusoidal PWM are shown as orange and blue waveforms in Fig. 3. Therefore, the detection should be performed synchronously with the drive signal.

The detection method proposed in [3] first measures external gate-source and drain-source voltage to obtain the gate driver state and device state, respectively. After a failure, the gate driver loses control of the device, leaving the gate driver state inconsistent with the device state. The method then checks the inconsistency between the gate driver state and the device state using logic circuits. However, the detection circuit of this method is too complex, and the detection speed is slow.

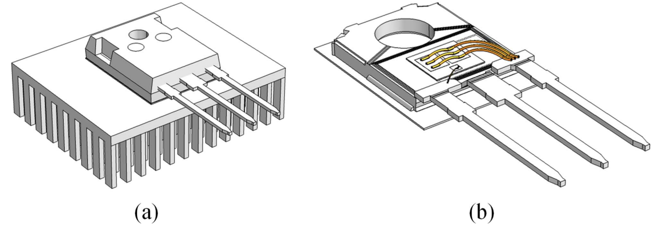

Fig. 4. Thermo-mechanical coupled finite element analysis (FEA) model of a TO-247 package discrete SiC MOSFET. (a) Entire model. (b) Hide case and heat sink.

Other than that, the gate open-circuit failures have not been well investigated. Therefore, the detection schemes for such failures are urgent.

This article proposes a gate open-circuit failure detection method based on internal gate state extraction. The rest of this article is organized as follows. Section II analyzes the mechanisms and characteristics of gate open-circuit failures. The principle of the proposed method and its advantages over universal short-circuit protection schemes are described in Section III. The circuit design methodology and application considerations of the proposed method are discussed in Section IV. In Section V, the proposed method is experimentally validated in both a pulse test circuit and a single-phase full-bridge inverter prototype. Finally, Section VI concludes this article.

II. Analysis of Gate Open-Circuit Failures

A. Mechanisms of Gate Open-Circuit Failures

According to the results of power cycling tests and comprehensive failure analysis in [3], four of the eight devices under test (50%) experienced cracking or liftoff of gate bond wires before the power source bond wires failed. However, in the past, the power source bond wires were usually considered to be the weakest part of the package structure due to the flow of current. In order to reveal the mechanisms of the phenomenon that the gate bond wires can fail before the power source bond wires, a thermo-mechanical coupled finite element analysis (FEA) model of a TO-247 package discrete SiC MOSFET device was established in COMSOL Multiphysics, as shown in Fig. 4.

The dimensions, materials, die power loss (heat source), and heat sink of the model are set according to manufacturer datasheets and typical values. It is worth noting that the roots of the three pins of the device are set as fixed mechanical constraints, while the rest of the model is set mechanically free, which represents a typical application of soldering the device pins to a PCB [10]. The steady-state temperature distribution is shown in Fig. 5 with a junction temperature (T_j) of 115 °C. The steady-state von Mises stress distribution is shown in Fig. 6. As can be seen, the stresses on the gate bond wires and power source bond wires are concentrated at the root and the interface with

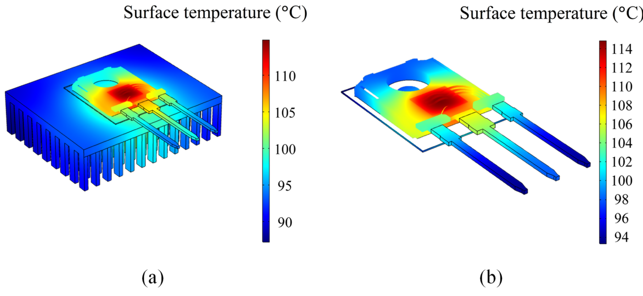

Fig. 5. Steady state surface temperature distribution. (a) Hide case. (b) Hide case and heat sink.

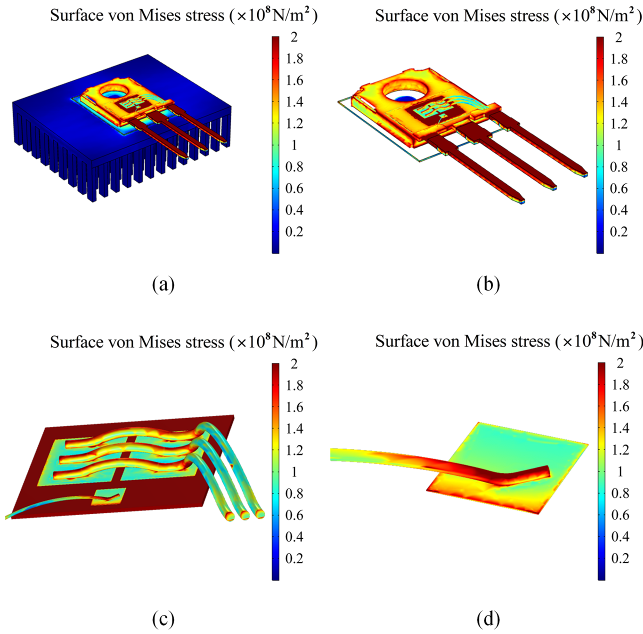

Fig. 6. Steady state surface von Mises stress distribution. (a) Hide case. (b) Hide case and heat sink. (c) Only chip and bond wires are visible. (d) Only gate pad and gate bond wire are visible.

the die surface, which is consistent with the failure mechanism analyzed above [11].

To obtain further conclusions, the maximum stresses on gate bond wires (F_{MG}) and source bond wires (F_{MS}) under different conditions are calculated by FEA as follows.

1) CTE of Encapsulating Materials: The CTE of encapsulating material (CTE_{EM}) varies significantly with the synthesis formulation and production process [12], which affects the CTE match and the bond wire thermo-mechanical stress. The F_{MG} and F_{MS}, when CTE_{EM} has different values (5 ppm/K–60 ppm/K) and T_j is fixed at 115 °C, are shown in Fig. 7(a).

As the CTE_{EM} increases, both F_{MG} and F_{MS} first decrease and then increase. The stress is minimum when the CTE_{EM} is about 20 ppm/K. This is because, at this point, the CTE_{EM} is equal to the CTE of the Al bond wires ($\text{CTE}_{\text{Al}} = 23$ ppm/K), and the CTE match is achieved [12]. The important conclusion is that F_{MG} and F_{MS} do not differ much regardless of the value of CTE_{EM}, and even when CTE_{EM} is matched with CTE_{Al}

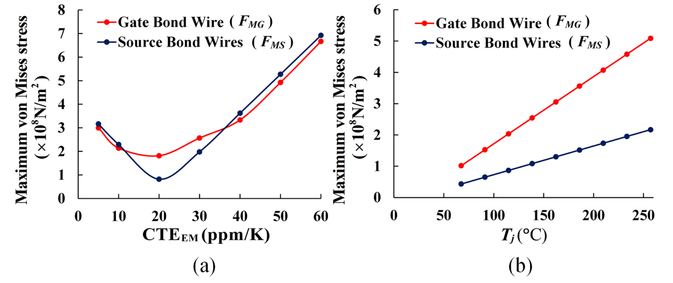

Fig. 7. Maximum von Mises stress on gate bond wires and source bond wires under different conditions. (a) CTE_{EM} ranges from 5 ppm/K–60 ppm/K. (b) Die temperature ranges from 67 °C–257 °C.

($\text{CTE}_{\text{EM}} = \text{CTE}_{\text{Al}} = 23$ ppm/K), F_{MG} is greater than F_{MS}. Since there is always only one gate bond wire and one Kelvin source bond wire, and they are typically much thinner than source bond wires, they have much lower mechanical strength. When subjected to similar stress, gate bond wires are more likely to fail than power source bond wires.

2) Temperature: The thermo-mechanical stress is also highly dependent on the temperature. The F_{MG} and F_{MS} at different junction temperatures are calculated by changing the die power losses, as shown in Fig. 7(b). It is worth noting that CTE_{EM} is currently set at 23 ppm/K, which is perfect for achieving a CTE match between the encapsulating material and the bond wires.

As T_j increases, both F_{MG} and F_{MS} increase, which is consistent with the general conclusion. However, F_{MG} increases faster than F_{MS}, which can be explained by the fact that the gate bond wires are thinner, have lower mechanical strength, and are subject to more severe strains at high temperatures. This means that in high-temperature applications where SiC MOSFETs are expected to be widely used, such as aerospace and oil drilling, gate bond wires may be less reliable than power source bond wires.

The above analysis indicates that, in addition to the power source bond wires, gate bond wires are also critical to the overall reliability and lifetime of SiC MOSFETs and need more attention.

B. Characteristics of Gate Open-Circuit Failures

Gate open-circuit failures occurring at different operating states of the device (such as ON and OFF) show distinguished failure characteristics. They can lead to various consequences, making failure identification difficult. Hence, it is necessary to analyze the various failure types.

After a failure, the driver loses control of the gate, leaving the gate of the failure device electrically isolated and floating [13], as shown in Fig. 8. The gate-drain capacitance (C_{gd}) and gate-source capacitance (C_{gs}) are actually connected in series, as shown in Fig. 8. Therefore, the gate-source voltage after the failure ($V_{gs\text{-}af}$) is not necessarily equal to the driver output voltage (V_{driver}). Instead, it is determined by (1), in which $V_{gs\text{-}bf}$ is the gate-source voltage before the failure, and ΔQ_{gs} is the change of C_{gs} charge. Since C_{gs} and C_{gd} are connected in series, ΔQ_{gs} can be written as (2), in which ΔQ_{gd} is the change of C_{gd} charge. Combining (1) and (2), $V_{gs\text{-}af}$ can be expressed as (3),

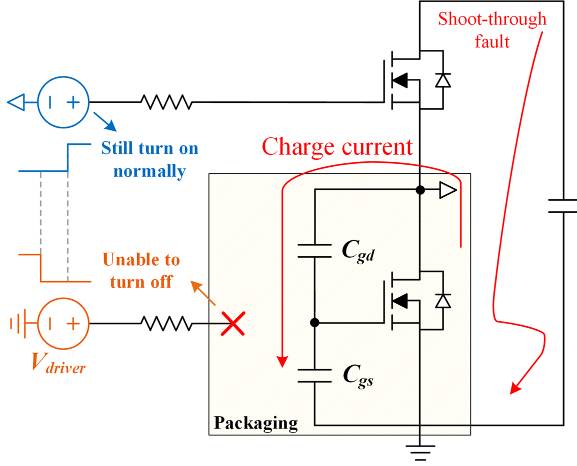

Fig. 8. Electrical behavior after a gate open-circuit failure evolving into a shoot-through fault.

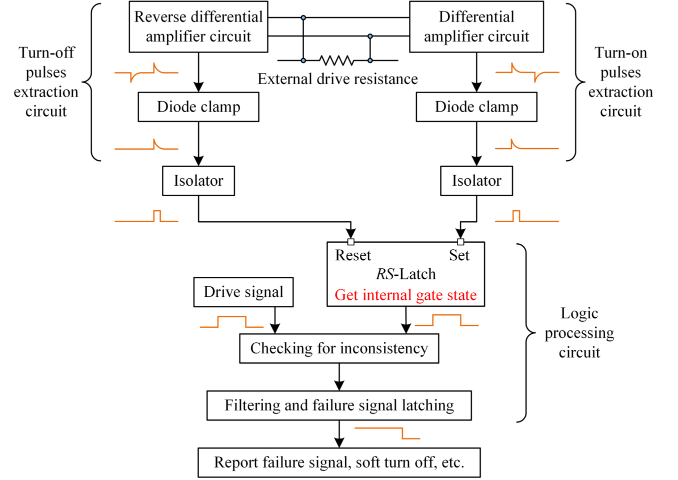

Fig. 9. Overview of the operation mechanism of the proposed method.

TABLE I
FAILURE TYPES

Failure type	$V_{gs\text{-}bf}$	$V_{gs\text{-}af}$	$V_{ds\text{-}bf}$	$V_{ds\text{-}af}$	ΔV_{ds}
Type-1	15V	>15V	$V_{ds\text{-}on}$	$V_{ds\text{-}st}$	$V_{ds\text{-}st}$ - $V_{ds\text{-}on}$
Type-2	15V	>15V	$V_{sd\text{-}on}$	$V_{ds\text{-}st}$	$V_{ds\text{-}st}$ - $V_{sd\text{-}on}$
Type-3	-5V	<-5V	V_{dc}	V_{sd}	V_{sd} - V_{dc}
Type-4	-5V	-5V	V_{dc}	V_{dc}	V_{dc} - V_{dc}
Type-5	-5V	>-5V	V_{sd}	V_{dc}	V_{dc} - V_{sd}

meaning that $V_{gs\text{-}af}$ is determined by $V_{gs\text{-}bf}$ and the change of drain-source voltage (ΔV_{ds}) after the failure

$$V_{gs-af} = V_{gs-bf} + \frac{\Delta Q_{gs}}{C_{gs}} \quad (1)$$

$$\Delta Q_{gs} = \Delta Q_{gd} = \frac{C_{gd}C_{gs}}{C_{gd} + C_{gs}} \Delta V_{ds} \quad (2)$$

$$V_{gs-af} = V_{gs-bf} + \left(\frac{C_{gd}}{C_{gd} + C_{gs}}\right) \Delta V_{ds}. \quad (3)$$

Based on the possible values of $V_{gs\text{-}bf}$ and ΔV_{ds}, gate open-circuit failures are classified into five types, as shown in Table I. $V_{ds\text{-}bf}$ and $V_{ds\text{-}af}$ are the drain-source voltage before and after failure, respectively. $V_{ds\text{-ON}}$, $V_{sd\text{-ON}}$, $V_{ds\text{-}st}$, V_{dc}, and V_{sd} are the drain-source voltage during ON-state, synchronous ON-state, shoot-through fault, OFF-state, and body-diode conduction, respectively. It is worth mentioning that the changes in gate-source voltage (V_{gs}) and drain-source voltage (V_{ds}) may occur within an interval instead of immediately after failure.

For example, the evolution of a type-1 failure in Table I is analyzed as follows. If a gate open-circuit failure occurs when the device is ON, it cannot turn OFF at the next turn-OFF moment. After the complementary device turns ON after the dead time, a shoot-through fault happens. The drain current (I_d) will increase dramatically, causing the V_{ds} of the failure device to increase from $V_{ds\text{-ON}}$ to $V_{ds\text{-}st}$. C_{gd} and C_{gs} will be charged, as shown in Fig. 8. $V_{gs\text{-}af}$ will increase according to (3).

As obtained from the LTspice simulation, $V_{gs\text{-}af}$ will increase from 15 V to 24 V. Due to the high transconductance of SiC MOSFETs [14], the increase of V_{gs} causes a significant reduction in $R_{ds\text{-ON}}$ and an increase in short-circuit current. The above analysis means that such shoot-through fault evolving from a gate open-circuit failure is even more severe than conventional shoot-through faults.

In addition, due to the higher V_{gs} and lower $R_{ds\text{-ON}}$ of the failure device, most of the short-circuit energy (nearly 85% according to LTspice simulation) is dissipated in the healthy complementary device, which may cause the failure to extend to the complementary device. Similar results can happen for type-2 failure. These two types of failures with serious consequences are the focus of attention for the detection circuits proposed in this article.

The analysis for other types of failure is similar and is omitted here due to limited space. The evolution of all types of failures is listed in Table I. It should be noted that failure types listed in Table I are derived assuming that the direction of the load current is constant within a short term.

III. Proposed Gate Open-Circuit Failure Detection Method

A. *Principle of the Proposed Gate Open-Circuit Failure Detection Circuit*

The operation mechanism of the method proposed in this article is shown in Fig. 9. The method firstly extracts turn-ON and turn-OFF pulses from the gate current. Then internal gate state is extracted using the turn-ON and turn-OFF pulses. Finally, the gate open-circuit failure is detected by checking the inconsistency between the extracted internal gate state and the drive signal. The schematic diagram of the proposed method is shown in Fig. 10. The example detection sequence diagram for the low-side device is illustrated in Fig. 11 and described step-by-step as follows.

Step 1: Extract the turn-ON and turn-OFF pulses. The voltage across the low-side external gate resistance (V_{RgL}) is first

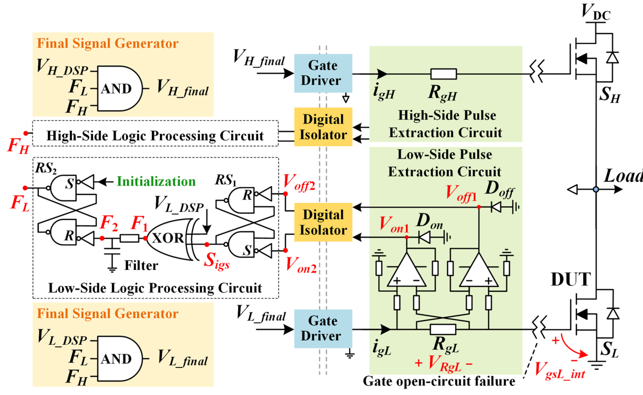

Fig. 10. Schematic diagram of the proposed method.

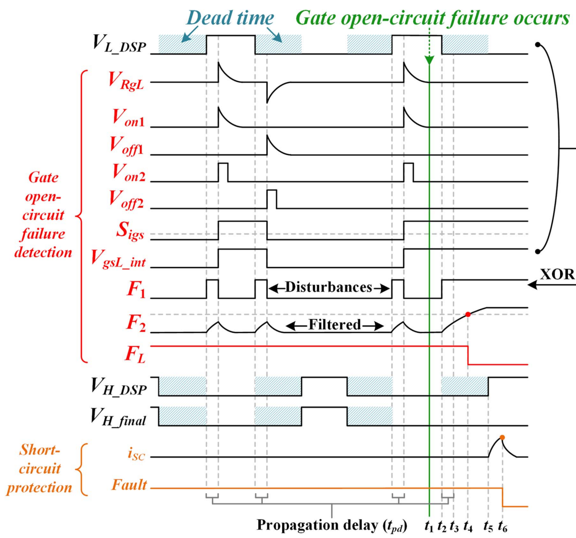

Fig. 11. Sequence diagram of the proposed method.

measured using a differential amplifier circuit. The negative half of V_{RgL} is clamped to zero by a Schottky diode D_{ON} to obtain the turn-ON pulse V_{ON1}, as shown in Figs. 10 and 11. Similarly, the turn-OFF pulse V_{OFF1} is obtained using a reverse differential amplifier circuit and D_{OFF}. Finally, V_{ON1} and V_{OFF1} are sent to the signal side by digital isolators to obtain V_{ON2} and V_{OFF2}.

Step 2: Extract the internal gate state. V_{ON2} and V_{OFF2} are sent to the active high set input (*S*) and the active high reset input (*R*), respectively, of an *R-S* latch (RS_1). In normal operation, the output of RS_1 (S_{igs}) is set when the device turns ON and reset when it turns OFF. After the failure (see t_1 in Fig. 11), the gate current path is cut OFF. Despite the next turn-OFF signal (t_2), no gate discharge current is formed, and the internal gate voltage (V_{gsL_int}) remains high. Without an active V_{OFF2} pulse, S_{igs} cannot be reset and also remains high, as shown in Fig. 11. Therefore, S_{igs} can be utilized as an indicator for the internal gate state that cannot be measured externally.

Step 3: Check for the inconsistency between the drive signal and the internal gate state. Perform the XOR logic operation on the drive signal from DSP (V_{L_DSP}) and S_{igs} to obtain F_1. Before the failure, S_{igs} follows V_{L_DSP}. Therefore, F_1 is low if disturbance pulses caused by propagation delay (t_{pd}) are not considered. At the next switching moment after failure, S_{igs} and V_{L_DSP} will not match anymore, and F_1 will stay high, as shown in Fig. 11.

Step 4: Filter disturbances in F_1. Due to the propagation delay (t_{pd}) between V_{L_DSP} and S_{igs}, F_1 will be high for a short time during the switching transient, even when there is no failure, as shown in Fig. 11. Therefore, an *RC* low-pass filter is employed to filter disturbances in F_1 and obtain F_2 to prevent misjudgment.

Step 5: Latch failure signal. An *R-S* latch (RS_2) is then used to latch F_2 and obtain the low-side failure signal (F_L). At the next switching moment after the failure, F_2 is activated by F_1 (t_4), thus making F_L low.

Step 6: Generate final drive signals. The same failure detection procedure is performed simultaneously on the high-side device to create the high-side failure signal (F_H). Performing the AND logic operation on V_{L_DSP}, F_H, and F_L will then give the final low-side drive signal (V_{L_final}), as illustrated in Fig. 10. The final high-side drive signal (V_{H_final}) is generated in a similar way.

In this way, regardless of whether a gate open-circuit failure occurs in the high-side or low-side device, the detection circuit can detect the failure after the next switching moment of the failure device within a delay time (see $t_d = t_2$–t_4 in Fig. 11) and latch all drive signals. After type-1 and type-2 failures that can evolve into shoot-through faults, as long as this delay time can be less than the dead time, the final drive signal of the complementary device (such as V_{H_final} in Fig. 11) will not go high at all after the dead time (see t_5 in Fig. 11), and the failure will not evolve into shoot-through fault.

In addition, in operating conditions where the dead time is very short, it may be difficult to achieve a delay time less than the dead time, and a slight shoot-through fault may still occur. Therefore, it is necessary to perform a soft turn-OFF procedure on both devices of the bridge after a failure is detected to protect the devices. The soft turn-OFF circuit is triggered by the failure signal (F_L and F_H) and can be easily integrated with the detection circuit. The design methodology of the soft turn-OFF circuit can be referred to [15], [16], and [17] and will not be duplicated.

B. Advantages of the Proposed Method Compared to Universal Short-Circuit Protection Schemes

Since the method proposed in this article focuses on type-1 and type-2 gate open-circuit failures that can evolve into shoot-through faults, and typically configured universal short-circuit protection can also protect against such shoot-through faults by blocking the drive signals [18], it is necessary to discuss the advantages of the method proposed in this article over universal short-circuit protection.

1) Faster Detection Speed: According to the detection principle, as long as the detection delay time is less than the dead time, the method proposed in this article can completely avoid the occurrence of shoot-through faults. In contrast, universal short-circuit protection schemes rely on the short-circuit event

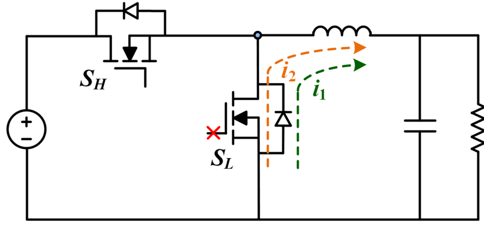

Fig. 12. Synchronous switch suffers a cryptic failure in a synchronous buck converter.

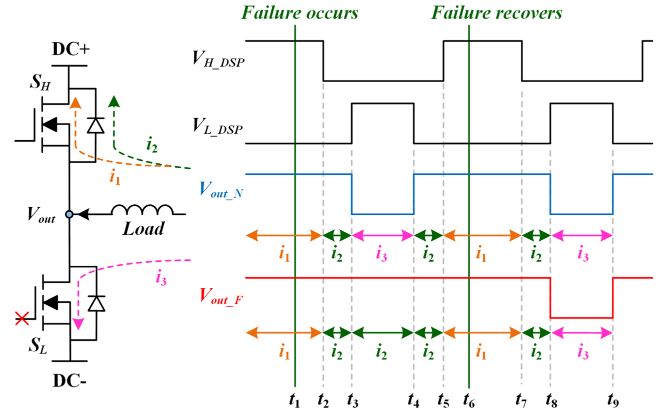

Fig. 13. Circuit diagram and waveforms of an intermittent failure.

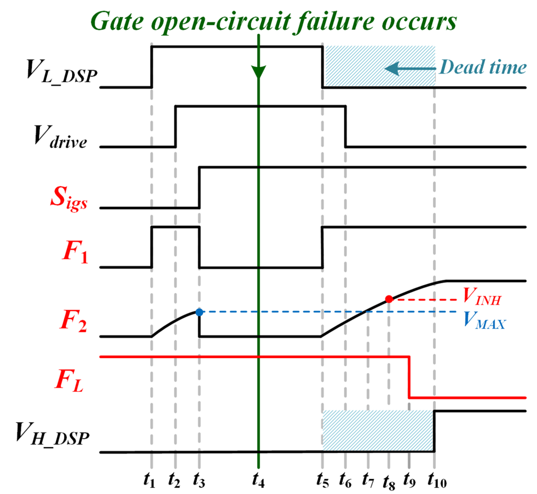

Fig. 14. Time delay analysis of the proposed method.

itself to achieve the protection [19], e.g., desaturation protection takes advantage of the feature that $V_{ds\text{-ON}}$ increases dramatically after a short-circuit fault [20]. In other words, they must act only after the complementary device drive signal (see V_{H_DSP} in Fig. 11) becomes high (see t_5 in Fig. 11), and then a shoot-through fault occurs (see t_6 in Fig. 11). However, according to the analysis in Section II, in this shoot-through fault caused by the type-1 or type-2 gate open-circuit failure, most of the short-circuit energy is dissipated in the healthy complementary device, which may cause the failure to expand due to the weaker short-circuit capability of SiC MOSFETs compared to their Si counterparts [21].

2) Ability to Identify Cryptic Failures in Certain Topologies or Operating Conditions: For example, the synchronous buck converter shown in Fig. 12 is analyzed as follows. If the synchronous switch (S_L) suffers a gate open-circuit failure during an off state, the S_L will not be able to turn ON afterward. However, current can still flow through the body diode or antiparallel diode of S_L. The converter can still operate normally with control loop compensation except for the increased losses [22]. Universal short-circuit protection is not capable of detecting this type of failure. This means that the converter may operate for a long time with the failure, which is a potential danger to the entire system. In contrast, the method proposed in this article can detect such cryptic failure and thus support converter maintenance.

3) Ability to Identify Intermittent Failures: It is well known that the gate bond wires are wrapped in encapsulated components [23]. The encapsulated components can maintain physical contact between the gate bond wires and the pad even if the cracking or liftoff has occurred. As the temperature rises, the relative displacement of encapsulated components due to thermal expansion can cause a break in contact. Therefore, the gate open-circuit failures usually occur intermittently [3]. For example, in the case shown in Fig. 13, the S_L suffers a gate open-circuit failure at t_1, followed by a failure recovery at t_6. The S_L is always OFF during t_1– t_6. Therefore, during t_3–t_4, the S_L cannot turn ON as expected. Since the load current flows into the half-bridge at this time and can be considered to be constant for a period of time, the load current that should flow to the channel of S_L (i_3) during t_3–t_4 can flow to the diode of S_H (i_2). The half-bridge output voltage during t_3–t_4 that should be dc- without failure becomes dc+ after failure, as shown by V_{out_N} and V_{out_F} in Fig. 13. However, since the converter is usually connected to an inductive load, the output voltage distortion of only one switching cycle (t_3–t_4) has almost no effect on the converter. This failure cannot be detected by universal short-circuit protection schemes. In contrast, the method proposed in this article still has the same detection capability for such intermittent failures.

IV. Considerations of Circuit Design and Application

A. Design Methodology for the Proposed Detection Circuit

According to the previous analysis, to avoid the type-1 and type-2 gate open-circuit failures evolving into shoot-through faults, the detection has to be completed before the end of dead time. Therefore, the goal of the detection circuit design is to shorten the delay time (t_d) as much as possible, as shown in Fig. 14. The t_d (see t_5–t_9 in Fig. 14) can be divided into the following two parts:

$$t_d = t_{d-RC} + t_{RS2} \tag{4}$$

where $t_{d\text{-}RC} = t_5$–t_8 is the delay time for the output voltage (F_2) of the *RC* low-pass filter to rise from 0 V to the high input threshold of RS_2 (see V_{INH} in Fig. 14), and $t_{RS2} = t_8$–t_9 is the propagation delay of the *RS*-latch RS_2. t_{RS2} is fixed and can be

obtained from the datasheet of RS_2. The key is to design the filter properly to reduce $t_{d\text{-}RC}$ as much as possible.

Since the filter is intended to avoid false detection due to the propagation delay between V_{L_DSP} and S_{igs} without failure (see $t_{pd} = t_1$–$t_3 = t_5$–t_7 in Fig. 14), it is sufficient to ensure that the maximum value of F_2 within t_{pd} (see V_{MAX} in Fig. 14) is less than V_{INH}. The V_{MAX} can be expressed as

$$V_{\mathrm{MAX}} = V_{INH} - V_{MAR} \tag{5}$$

where V_{MAR} is the voltage margin to avoid false detection, and V_{INH} can be obtained from the datasheet of RS_2.

The t_{pd} can be divided into the following two parts:

$$t_{pd} = t_{dr} + t_{igs} \tag{6}$$

where $t_{dr} = t_1$–t_2 is the propagation delay of the driver chip, and $t_{igs} = t_2$–t_3 is the total propagation delay of the internal gate state extraction circuit.

The t_{igs} can be divided into the following three parts:

$$t_{igs} = t_{op-amp} + t_{iso} + t_{RS1} \tag{7}$$

where $t_{op\text{-}amp}$, t_{iso}, and t_{RS1} are the propagation delay of the pulse extraction circuit (differential amplifier circuit), the digital isolator, and the *RS*-latch (RS_1), respectively. t_{iso} and t_{RS1} can be obtained from the datasheet, and the $t_{op\text{-}amp}$ can be estimated as follows:

$$t_{op-amp} = \frac{V_{OH}}{SR} \tag{8}$$

where V_{OH} is the high-level output voltage of the operational amplifier (op-amp), and *SR* is the slew rate of op-amp.

In this way, V_{MAX} and t_{pd} can be obtained according to (5) and (6). The filter can be designed to have a zero-state response where the output voltage rises to V_{MAX} at t_{pd}. Once the filter is designed, $t_{d\text{-}RC}$ can be calculated as the time that the zero-state response output voltage rises to V_{INH}, and t_d can be calculated according to (4). The relationship between t_d, t_{dr}, $t_{op\text{-}amp}$, t_{iso}, t_{RS1}, t_{MAR}, t_{RS2}, t_{igs}, t_{pd}, and $t_{d\text{-}RC}$ can be written as follows, where t_{MAR} is the time margin corresponding to V_{MAR}

$$t_d = \underbrace{\underbrace{t_{dr} + \underbrace{t_{op-amp} + t_{iso} + t_{RS1}}_{t_{igs}}}_{t_{pd}} + t_{MAR}}_{t_{d-RC}} + t_{RS2}. \tag{9}$$

In summary, to improve detection speed, driver chips with low propagation delay, high slew rate op-amps, and high-speed logic devices should be selected. In addition, to reduce $t_{op\text{-}amp}$, the differential amplifier circuit needs to be operated close to saturation to take advantage of the high-speed performance of the op-amp.

B. Possible False Detection Analysis and Avoidance Methods

It is well known that the switching of complementary device can also form gate current in the device under test (DUT), i.e., the crosstalk phenomenon [24], [25]. Since the method proposed in this article uses the gate current to extract the internal gate state, the crosstalk current may lead to false detection. The false detection can only occur during the hard turn-OFF transients of the complementary device, as shown in Fig. 15. This is because, in this case, the crosstalk current (i_{cro}) is in the same direction as the turn-ON gate current (i_{g_ON}) of the DUT, and the i_{cro} appears before the i_{g_ON}. The S_{igs} that should normally be set by i_{g_ON} at t_2 (S_{igs_N}) may be incorrectly set early by i_{cro} at t_1 (S_{igs_F}), resulting in incorrect extraction of the internal gate state and triggering false detection.

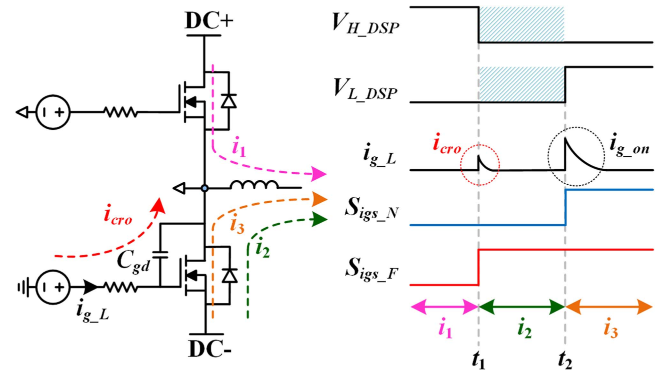

Fig. 15. Circuit diagram and waveforms for false detection analysis.

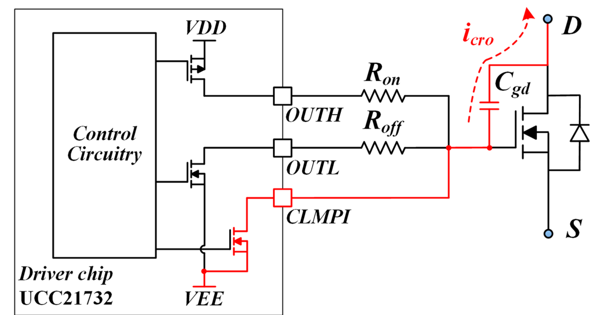

Fig. 16. Active miller clamp circuit diagram of the driver chip used in this paper.

Fortunately, the amplitude of the crosstalk current is usually less than normal switching gate current. The false detection can be avoided by properly reducing the gain of the differential amplifier circuit. Therefore, the practical design method for this gain can be briefly described as follows: 1) Obtain the gate current amplitude and crosstalk current amplitude by simulation or experiment; 2) The gain of the differential amplifier circuit should be selected as large as possible under the premise that the crosstalk current will not form an effective pulse.

In addition, even if the crosstalk current amplitude is close to or even exceeds the normal switch gate current amplitude, false detection can be avoided with the aid of an active miller clamp. The active miller clamp provides a low impedance path for the crosstalk current when the device is OFF [26], [27], [28], as shown by the red line in Fig. 16. This way, the crosstalk current hardly flows through the external drive resistance and no false detection will occur. Therefore, in practice, as long as the active miller clamp is configured, the effect of crosstalk can

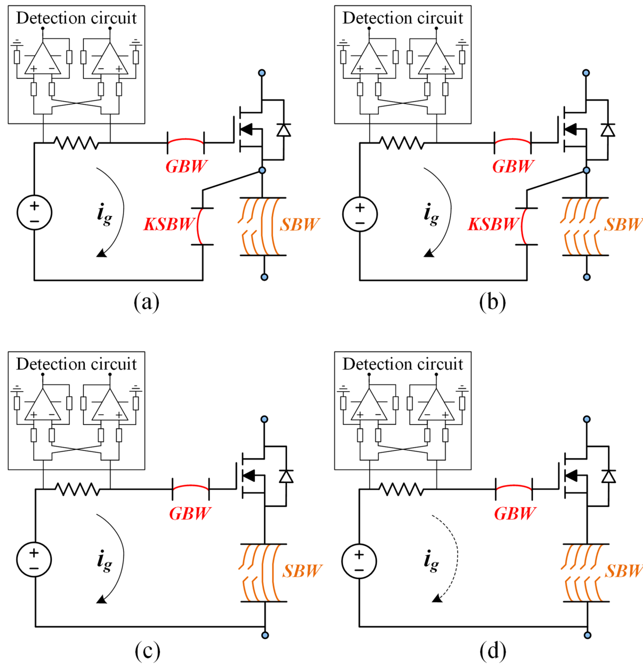

Fig. 17. Effect of power source bond wire failure on gate open-circuit failure detection circuit in devices with different source structures. (a) Partial failure in Kelvin source packaged devices. (b) Complete failure in Kelvin source packaged devices. (c) Partial failure in non-Kelvin source packaged devices. (d) Complete failure in non-Kelvin source packaged devices.

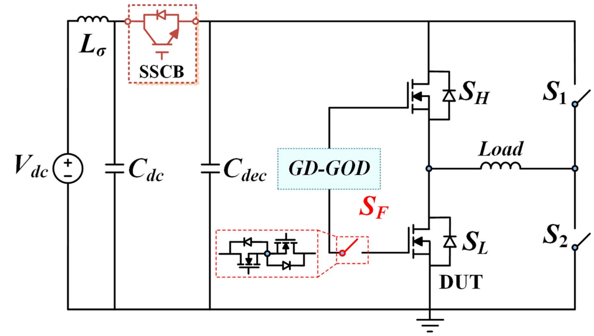

Fig. 18. Pulse test circuit diagram.

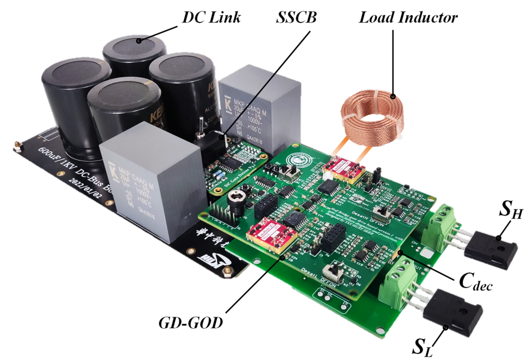

Fig. 19. Pulse test platform.

be disregarded, and a larger gain of the differential amplifier circuit can be simply selected.

C. Effect of Power Source Bond Wire Failure on Gate Open-Circuit Failure Detection Circuit

In practice, power source bond wires can also age or even fail. The effect of power source bond wire failure on the gate open-circuit failure detection circuit proposed in this paper is illustrated in Fig. 17, where *GBW*, *KSBW*, and *SBW* represent the gate bond wire, Kelvin source bond wire, and power source bond wires, respectively.

For Kelvin source packaged devices, the gate loop and power loop are decoupled [29], as shown in Fig. 17(a). Therefore, whether the power source bond wires fail partially [see Fig. 17(a)] or completely [see Fig. 17(b)], the gate loop will not be affected, and the detection circuit is still able to determine whether an open-circuit failure has occurred in the gate loop (*GBW* and *KSBW*). There are other dedicated detection circuits for power loop open-circuit failures caused by power source bond wires (*SBW*) failure. This area has been extensively researched [30], [31], [32], [33], [34] and is not the focus of this article.

For non-Kelvin source packaged devices, the method proposed in this article is unable to distinguish between gate bond wire failure and source bond wire failure. However, there are usually multiple source bond wires, and they do not fail together [7]. When only part of the source bond wires fails, as shown in Fig. 17(c), the gate loop is almost unaffected, except that the equivalent resistance becomes slightly larger. Assuming empirically that the resistance of one bond wire is 10 mΩ [11], the total equivalent resistance increases only from 2.5 mΩ to 10 mΩ even if three of the four bond wires are broken. The small change in resistance has almost no effect on the gate current according to circuit simulation in LTspice. In addition, even when the total equivalent resistance increases to 1 Ω (100 times) to simulate the situation where the last bond wire is also close to failure, the peak gate current only decreases from 640 mA to 620 mA according to circuit simulation in LTspice. Since the differential amplifier circuits in the method operate in a high gain state (close to saturation) to enhance the detection speed, this small reduction in the peak gate current will not affect the normal operation of the circuit according to LTspice simulation. Furthermore, if the device is configured with source bond wire aging detection as proposed in [30], [31], [32], [33], and [34], the partial failure of source bond wires can be detected to guide maintenance. The situation shown in Fig. 17(d), where all source bond wires are failed, can be effectively avoided.

V. Experimental Verification

A. Verification in Pulse Test

The proposed method is first verified in a half-bridge pulse test circuit with an inductor load, as shown in Fig. 18. The high-side and low-side devices are driven by a half-bridge gate driver with gate open-circuit failure detection (GD-GOD). All devices are C3M0075120D, and the low-side device is selected as the DUT.

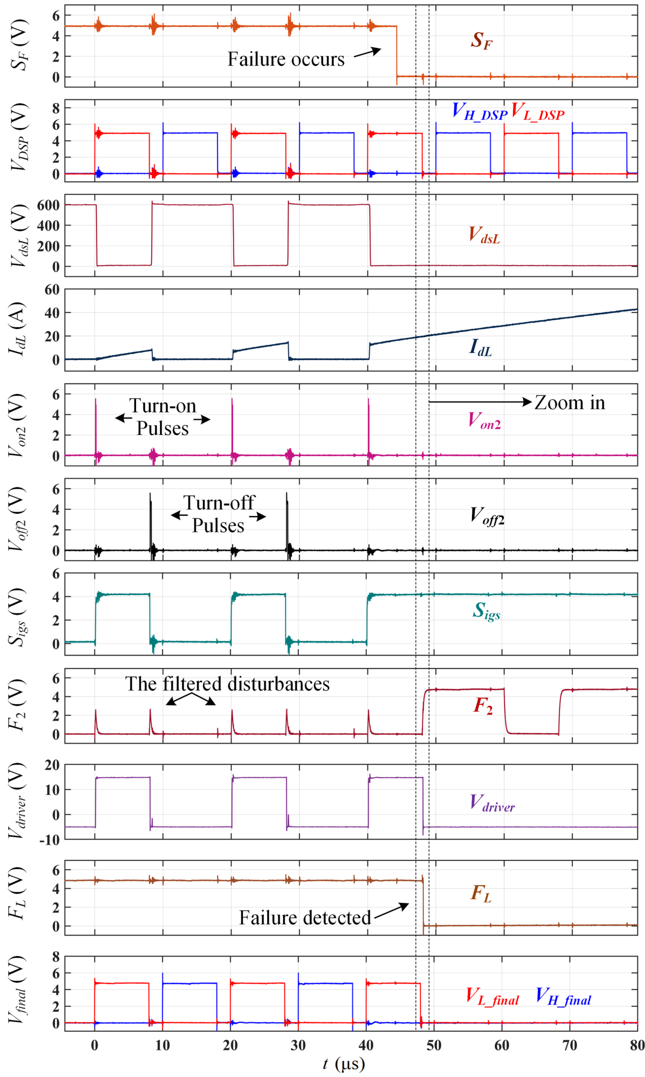

Fig. 20. Experimental waveforms of pulse test including S_F, V_{H_DSP}, V_{L_DSP}, V_{dsL}, I_{dL}, V_{ON2}, V_{OFF2}, S_{igs}, F_2, V_{driver}, F_L, V_{L_final}, and V_{H_final}.

The gate open-circuit failure is emulated by opening the switch S_F, which consists of two N-MOSFETs connected in reverse series and is capable of bidirectional current cutoff. The dc voltage is 600 V, and the load current during failure is 20 A.

By manipulating S_1 and S_2, both the hard and soft switching can be created for DUT to comprehensively verify the applicability of the proposed method under failures listed in Table I. The DUT operates in a hard switching when S_1 is closed and S_2 is open, while in a soft switching when S_1 is open and S_2 is closed. A solid-state circuit breaker (SSCB) is utilized to protect possible short-circuit faults [35]. The overall experimental setup is shown in Fig. 19.

Take the type-1 as an example, where DUT operates in the hard switching. The DSP generates five complementary pulses, including V_{L_DSP} and V_{H_DSP}, as shown in Fig. 20. S_F opens at the third pulse of V_{L_DSP} when the DUT is conducting. Before the failure, S_{igs} are set when DUT turns ON and reset when DUT turns OFF. S_{igs} follows V_{L_DSP}, as shown in Fig. 20. The

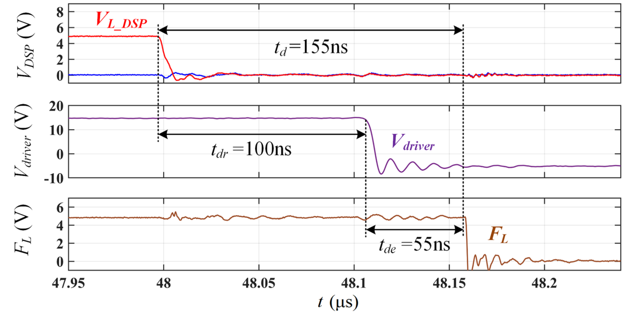

Fig. 21. Zoomed experimental waveforms of V_{L_DSP}, V_{driver}, and F_L to quantify detection time.

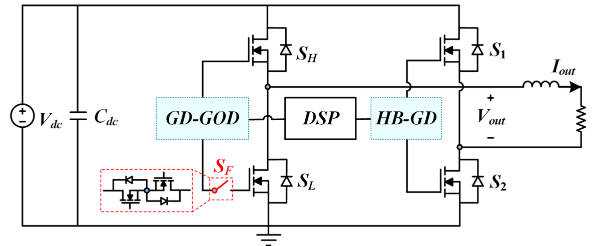

Fig. 22. Single-phase full-bridge inverter circuit diagram.

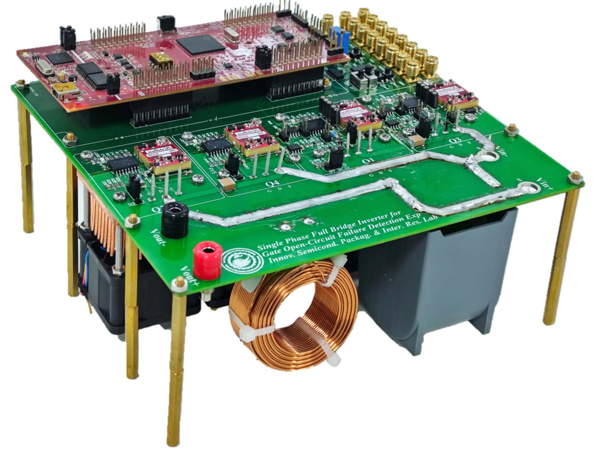

Fig. 23. Single-phase full-bridge inverter prototype.

disturbances are effectively filtered, and F_L stays high. V_{H_final} follows V_{H_DSP}, and V_{L_final} follows V_{L_DSP} as expected, as shown in Fig. 20. After the failure, there is no pulse in V_{OFF2} at the next turn-OFF moment. S_{igs} remains high, and F_2 becomes active. F_L then becomes low, thus deactivating V_{H_final} and V_{L_final}.

It is worth noting that, in this case, the failure device cannot turn OFF even if the failure is detected. The dc bus will continue to charge the load inductor after the failure until the SSCB actions. This phenomenon only occurs for special type of failure (type-1) and topology and can be avoided by switching OFF the power supply (e.g., using the SSCB) after detecting failures. In circuits with more than one bridge, the other bridge will lock after the failure is detected and it will not be an issue anymore.

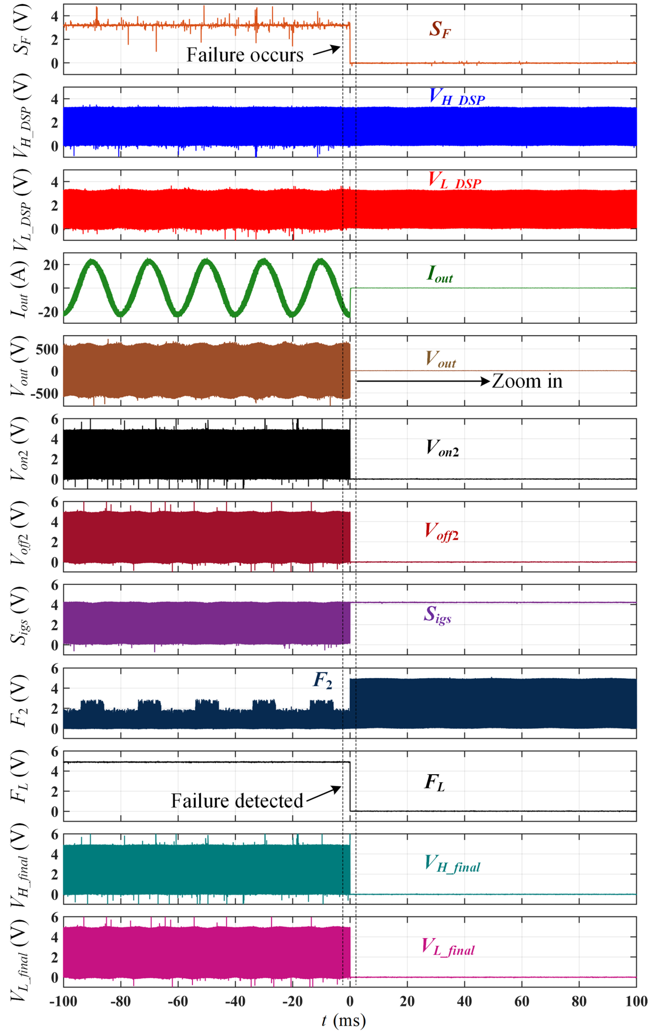

Fig. 24. Experimental waveforms of single-phase full-bridge inverter including S_F, V_{H_DSP}, V_{L_DSP}, I_{out}, V_{out}, V_{ON2}, V_{OFF2}, S_{igs}, F_2, F_L, V_{H_final}, and V_{L_final}.

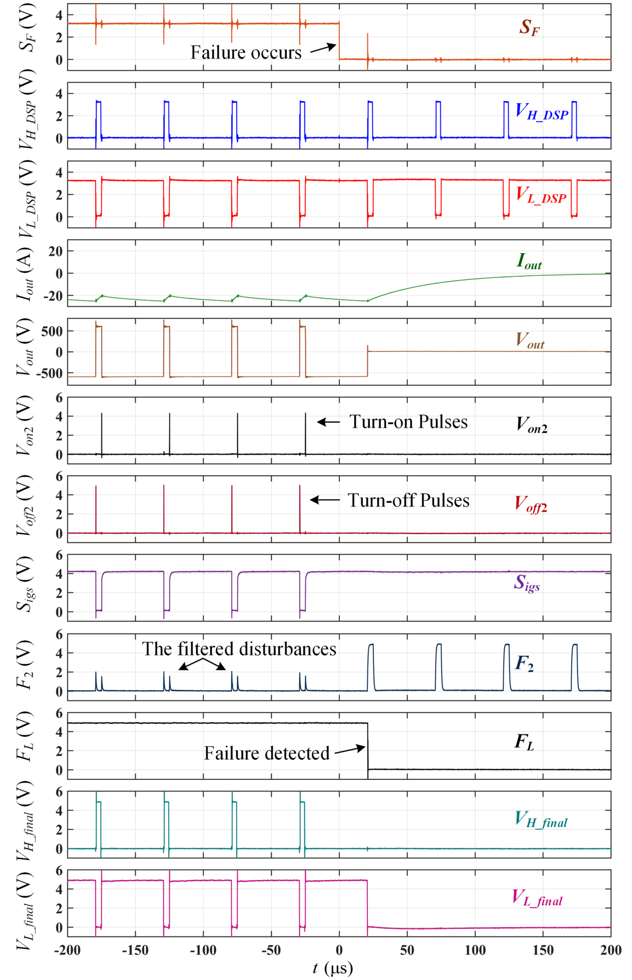

Fig. 25. Zoomed experimental waveforms of single-phase full-bridge inverter including S_F, V_{H_DSP}, V_{L_DSP}, I_{out}, V_{out}, V_{ON2}, V_{OFF2}, S_{igs}, F_2, F_L, V_{H_final}, and V_{L_final}.

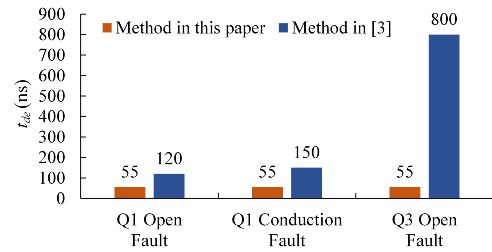

Fig. 26. Comparison of detection time between the method proposed in this article and state-of-the-art technology.

The t_d of the detection circuit designed in this article is 155 ns, as shown in Fig. 21. The shortest effective input pulse width of the driver chip (UCC21732) used in this article is experimentally tested to be 36 ns. Therefore, the detection circuit can effectively avoid shoot-through faults when the dead time is longer than 119 ns (155 ns–36 ns). In addition, it can be seen that most of the t_d comes from the propagation delay of the driver chip ($t_{dr} = 100$ ns). The t_{dr} is irrelevant to the detection circuit designed in this article because, before the driver output V_{driver} is flipped, the characteristics of the whole gate loop are the same regardless of whether the device has failed or not. Therefore, the detection time (t_{de}) of the detection circuit is defined as the time between the driver output voltage V_{driver} flipping and F_L going low [3]. As shown in Fig. 21, t_{de} of the detection circuit designed in this article is approximately 55 ns, mainly including the inherent propagation delay of the differential amplifier circuit (9 ns), digital isolator (8 ns), RS_1 (15 ns), and RS_2 (15 ns). Additionally, a filter time margin (8 ns) is also included in the t_{de} to avoid misjudgment.

Other types of failures in Table I are also experimentally verified, and they can all be detected within 55 ns by the proposed detection circuit. The test results are not duplicated here due to their similarity to Figs. 20 and 21.

B. Verification in Inverter

The proposed method is also verified in a 2-kW single-phase full-bridge inverter, as shown in Fig. 22. The left half-bridge is driven by the same GD-GOD as in the pulse test, and the low-side

device is also selected as the DUT. The right half-bridge is driven by a typical half-bridge GD. The prototype is shown in Fig. 23. Still taking the most dangerous type-1 failure as an example, the experimental results are shown in Figs. 24 and 25.

The detailed experimental waveforms are similar to those of the pulse test and will not be repeated. Since the detection circuit parameters are the same as in the pulse test, t_d is also 155 ns, and t_{de} is also 55 ns.

It is worth noting that in circuits with more than one bridge, such as the single-phase full-bridge circuit in this article, one bridge can transmit the failure signal to the other bridges through the DSP or a separate circuit. For example, after the failure is detected in the left bridge, both the left and right bridges in Fig. 22 lock. The output current quickly drops to zero, as shown in Figs. 24 and 25. The phenomenon of the dc bus continuing to charge the load in the pulse test does not occur, which is consistent with the previous analysis.

C. Comparison of Proposed Method to Other Detection Method

The advantages of the method proposed in this article over the state-of-the-art technique [3] are concluded as follows.

1) The biggest advantage is the fast detection speed, as shown in Fig. 26. It can be seen that the detection times of the method in [3] for three different types of failures are 120 ns, 150 ns, and 800 ns, respectively. With the same definition of detection time, the detection time of the method proposed in this article is 55 ns for all types of failures.
2) The method proposed in this article requires fewer components and a simpler design process compared to the method in [3].
3) The method proposed in this article only needs to measure the gate, while the method in [3] needs to measure both the gate and the drain. This means that the detection circuit proposed in this article is easier to integrate and has less impact on the system.

VI. Conclusion

In this article, a gate open-circuit failure detection method based on internal gate state extraction is proposed. The failure mechanisms and characteristics are first discussed in detail. Then, the detection circuit principle, circuit design methodology, and application considerations are described. Finally, experimental results verify that the proposed method can accurately detect all types of gate open-circuit failures within 55 ns, which can prevent serious faults and provide failure information for maintenance. The proposed detection circuit can be easily integrated into the gate driver and effectively improve the reliability of SiC converters.

References

[1] Z. Wang et al., "Temperature-dependent short-circuit capability of silicon carbide power MOSFETs," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1555–1566, Feb. 2016.

[2] S. Pu, F. Yang, B. T. Vankayalapati, and B. Akin, "Aging mechanisms and accelerated lifetime tests for SiC MOSFETs: An overview," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 1, pp. 1232–1254, Feb. 2022.

[3] B. T. Vankayalapati, S. Pu, F. Yang, M. Farhadi, V. Gurusamy, and B. Akin, "Investigation and on-board detection of gate-open failure in SiC MOSFETs," *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 4658–4671, Apr. 2022.

[4] A. Hanif, Y. Yu, D. DeVoto, and F. Khan, "A comprehensive review toward the state-of-the-art in failure and lifetime predictions of power electronic devices," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4729–4746, May 2019.

[5] Z. Ni, X. Lyu, O. P. Yadav, B. N. Singh, S. Zheng, and D. Cao, "Overview of real-time lifetime prediction and extension for SiC power converters," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 7765–7794, Aug. 2020.

[6] S. Yu, Z. Wang, D. Zhou, Y. Zhou, Y. Li, and X. Shi, "Online gate-oxide degradation monitoring of SiC MOSFETs based on parasitic capacitance aging characteristics," in *Proc. IEEE Energy Convers. Congr. Expo.*, Nashville, TN, USA, Oct. 2023, pp. 5959–5963.

[7] C. Chen, V. Pickert, M. Al-Greer, C. Jia, and C. Ng, "Localization and detection of bond wire faults in multichip IGBT power modules," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 7804–7815, Aug. 2020.

[8] N. Baker, S. Munk-Nielsen, F. Iannuzzo, and M. Liserre, "IGBT junction temperature measurement via peak gate current," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3784–3793, May 2016.

[9] N. B. Y. Gorla, S. Kolluri, M. Chai, and S. K. Panda, "A novel open-circuit fault detection and localization scheme for cascaded H-bridge stage of a three-stage solid-state transformer," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 8713–8729, Aug. 2021,.

[10] A. Surendar, L. G. Akhmetov, L. K. Ilyashenko, A. Maseleno, and V. Samavatian, "Effect of thermal cycle loadings on mechanical properties and thermal conductivity of a porous lead-free solder joint," *IEEE Trans. Compon., Packag. Manuf. Technol.*, vol. 8, no. 10, pp. 1769–1776, Oct. 2018.

[11] H. Luo, F. Iannuzzo, N. Baker, F. Blaabjerg, W. Li, and X. He, "Study of current density influence on bond wire degradation rate in SiC MOSFET modules," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 2, pp. 1622–1632, Jun. 2020.

[12] F. Boshkovski, C. Nicholas, Z. Zhang, P. Paret, K. D. T. Ngo, and G. Q. Lu, "Effects of encapsulant properties on the thermo-mechanical reliability of double-side cooled power modules for traction inverters," in *Proc. IEEE Energy Convers. Congr. Expo.*, Nashville, TN, USA, Oct. 2023, pp. 5934–5938.

[13] C. Delepaut, S. Siconolfi, O. Mourra, and F. Tonicello, "MOSFET gate open failure analysis in power electronics," in *Proc. 28th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2013, pp. 189–196.

[14] C. Zhao, L. Wang, X. Yang, F. Zhang, and Y. Gan, "Comparative investigation on paralleling suitability for SiC MOSFETs and SiC/Si cascode devices," *IEEE Trans. Ind. Electron.*, vol. 69, no. 4, pp. 3503–3515, Apr. 2022.

[15] Texas Instruments, UCC21732-Isolated single channel gate driver for SiC/IGBT with active protection, isolated analog sensing and high-CMTI datasheet, 2020. [Online]. Available: https://www.ti.com.cn/

[16] S. Zhao et al., "Soft turn-off DC solid-state circuit breakers with flexible dual tripping schemes," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 12, no. 1, pp. 997–1010, Feb. 2024.

[17] S. K. Roy and K. Basu, "Analytical model to study turn-off soft switching dynamics of SiC MOSFET in a half-bridge configuration," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 13039–13056, Nov. 2021.

[18] W. Ouyang, P. Sun, M. Xie, Q. Luo, and X. Du, "A fast short-circuit protection method for SiC MOSFET based on indirect power dissipation level," *IEEE Trans. Power Electron.*, vol. 37, no. 8, pp. 8825–8829, Aug. 2022.

[19] D.-P. Sadik et al., "Short-circuit protection circuits for silicon-carbide power transistors," *IEEE Trans. Ind. Electron.*, vol. 63, no. 4, pp. 1995–2004, Apr. 2016.

[20] S.-S. Min and R.-Y. Kim, "Improved gate-voltage-driven desaturation short-circuit protection circuit with robust switching noise immunity for WBG power semiconductors," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 3, pp. 2535–2544, Jun. 2023.

[21] T. Shoji, M. Kuwahara, and M. Usui, "Dependence of short-circuit withstand capability of SiC MOSFETs on short-circuit failure time," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 11739–11747, Oct. 2021.

[22] Y. Zhou, Z. Wang, G. Xin, J. Yuan, and X. Shi, "Dead time optimization for synchronous switching of SiC MOSFETs considering nonlinear gate capacitance," *IEEE Trans. Power Electron.*, vol. 38, no. 5, pp. 5665–5669, May 2023.
[23] R. Khazaka, L. Mendizabal, D. Henry, and R. Hanna, "Survey of high-temperature reliability of power electronics packaging components," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2456–2464, May 2015.
[24] Z. Zhang, J. Dix, F. F. Wang, B. J. Blalock, D. Costinett, and L. M. Tolbert, "Intelligent gate drive for fast switching and crosstalk suppression of SiC devices," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9319–9332, Dec. 2017.
[25] C. Qian, Z. Wang, G. Xin, and X. Shi, "Partial-bootstrap gate driver for switching loss reduction and crosstalk mitigation," *IEEE Trans. Power Electron.*, vol. 37, no. 10, pp. 11523–11527, Oct. 2022.
[26] E. Aeloiza, A. Kadavelugu, and R. Rodrigues, "Novel bipolar active miller clamp for parallel SiC MOSFET power modules," in *Proc. IEEE Energy Convers. Congr. Expo.*, Portland, OR, USA, 2018, pp. 401–407.
[27] L. Dulau, S. Pontarollo, A. Boimond, J.-F. Garnier, N. Giraudo, and O. Terrasse, "A new gate driver integrated circuit for IGBT devices with advanced protections," *IEEE Trans. Power Electron.*, vol. 21, no. 1, pp. 38–44, Jan. 2006.
[28] C. Li et al., "High off-state impedance gate driver of SiC MOSFETs for crosstalk voltage elimination considering common-source inductance," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2999–3011, Mar. 2020.
[29] S. Pu, F. Yang, N. Zhang, B. T. Vankayalapati, and B. Akin, "A comparative study on reliability and ruggedness of Kelvin and non-kelvin packaged SiC MOSFETs," *IEEE Trans. Ind. Appl.*, vol. 58, no. 3, pp. 3863–3874, May/Jun. 2022.
[30] E. Ugur, C. Xu, F. Yang, S. Pu, and B. Akin, "A new complete condition monitoring method for SiC power MOSFETs," *IEEE Trans. Ind. Electron.*, vol. 68, no. 2, pp. 1654–1664, Feb. 2021.
[31] K. Wang, L. Zhou, P. Sun, and X. Du, "Monitoring bond wires fatigue of multichip IGBT module using time duration of the gate charge," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 888–897, Jan. 2021.
[32] R. Mandeya, C. Chen, V. Pickert, R. T. Naayagi, and B. Ji, "Gate–emitter pre-threshold voltage as a health-sensitive parameter for IGBT chip failure monitoring in high-voltage multichip IGBT power modules," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 9158–9169, Sep. 2019.
[33] Y. Yang and P. Zhang, "A novel bond wire fault detection method for IGBT modules based on turn-on gate voltage overshoot," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 7501–7512, Jul. 2021.
[34] F. Gonzalez-Hernando, J. San-Sebastian, A. Garcia-Bediaga, M. Arias, F. Iannuzzo, and F. Blaabjerg, "Wear-out condition monitoring of IGBT and MOSFET power modules in inverter operation," *IEEE Trans. Ind. Appl.*, vol. 55, no. 6, pp. 6184–6192, Nov./Dec. 2019.
[35] R. Rodrigues, Y. Du, A. Antoniazzi, and P. Cairoli, "A review of solid-state circuit breakers," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 364–377, Jan. 2021.

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