Soft-Switched Interleaved Ultra-High Step-Down Converter With Low-Voltage Stress

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***Abstract*—This article introduces a novel interleaved ultra-high step-down dc–dc converter with soft-switching. Among its outstanding features are the minimal voltage stress on power switches and diodes, extended duty cycle, soft-switching conditions for both the switches and diodes, continuous output current with minimal ripple, and the small size of the magnetic inductors and their low conduction losses. Lowering switches' voltage and current stress is achieved by input series capacitors and interleaved topologies, respectively. This approach can lead to a significant reduction in conduction loss experienced by switches. Moreover, by using blocking capacitors and winding-cross-coupled inductors techniques, it is possible to reduce both the voltage gain and the ripple in the output current. In addition, by utilizing soft switching for semiconductor devices, significant reductions in switching losses, including turn-ON, turn-OFF, capacitive turn-ON, and reverse recovery losses, can be achieved. Thus, the converter's overall efficiency is significantly improved. The experimental results obtained from a 200-W prototype, operating with a 300-V input voltage and 25-V output voltage, confirm the validity of the theoretical analysis.**

***Index Terms*—Coupled inductors (CI), high step-down converter, interleaved, low voltage stress, soft switching.**

I. Introduction

RECENTLY, step-down dc–dc converters have gained popularity in a broad range of applications, including battery chargers, electric vehicles, fuel cell systems, voltage regulator modules (VRMs), and LED drivers [1], [2], [3], [4]. Due to fewer components and lower complexity, nonisolated converters are preferred over isolated converters for applications where electrical isolation is unnecessary [5]. Despite that, the conventional buck converter offers advantages such as low ripple in the output current, uncomplicated control, and simple non-isolated topology; in applications that require a high step-down ratio and have a high input voltage, it is subjected to high voltage stress and an extremely low duty cycle [6], [7]. Thus, the converter's efficiency is significantly reduced. In order to eliminate the issues faced by the conventional buck converter in high-step-down applications, a converter with an improved voltage conversion ratio (VCR) to prevent a low-duty cycle and minimize voltage stress on high-current semiconductor devices is necessary. To facilitate the development and introduction of a converter with desired characteristics, several studies have been conducted [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28].

Using tapped inductors (TIs) or coupled inductors (CIs) based structures is a simple method of extending duty cycles while adjusting the conversion ratio according to the CIs' turn ratio. However, these converters suffer from pulsating output currents due to the leakage inductance of CIs which reduces the lifespan of the output capacitor [8], [9], [10]. Furthermore, power switches in TI and CI topologies are subjected to a high voltage spike caused by leakage inductance. Also, elevating the turn ratio of CI to reduce voltage gain leads to a rise in the value of leakage inductance, increasing converter losses. However, the implementation of the winding-cross-coupled-inductors (WCCI) method achieves the cancellation of the current ripple [11], [12]. Switched capacitor converters, which consist of switches and capacitors, are a viable strategy for increasing the duty cycle and reducing the voltage stress on switches. However, getting high step-down voltage gain requires many capacitors and switches that commutate under hard switching conditions, which reduces efficiency [13], [14]. Increasing the switching frequency can reduce the size of passive elements, but it also leads to higher switching losses. Thus, soft-switching techniques, such as zero-current switching (ZCS) and zero-voltage switching (ZVS), reduce switching losses and improve efficiency. However, compared to the conventional buck converter, obtaining soft-switching conditions in high step-down converters presents a considerable challenge due to their multiple switches. As a result, conventional soft-switching circuits are typically ineffective for all switches in these converters [15], [16], [17].

Typically, an LLC structure is employed to achieve high efficiency. However, this configuration is not capable of delivering optimal efficiency for a wide range of input voltage variations and load changes. Furthermore, in isolated converters aiming for enhanced efficiency, where rectifying diodes consistently play a role in the power-transfer path, the circuit needs to employ the synchronous rectifier (SR) technique, which, in turn, increases the intricacy of the circuit design [18]. Another way to achieve a significant reduction in voltage gain is by using cascade connections. These converters reduce VCRs by multiplying the voltage gain of several stages rather than requiring transformers or CIs [19]. However, these converters experience significant

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conduction and switching losses owing to the high number of components involved, which causes their overall efficiency to be decreased.

In high-step-down applications with low voltage and high current output, semiconductor elements suffer from high current ripple and high current stress. In order to resolve this problem, interleaved buck converters (IBCs) are presented. In addition to power distribution among interleaved modules, phase shift reduces input current ripple to a significant extent. However, IBC topologies use many components, which leads to higher expenses and greater weight [20]. Moreover, these converters are ineffective for applications with high step-down voltages because the voltage gain is not effectively improved. In [21], an interleaved two-phase converter is presented, which reduces the output current ripple. However, the VCR and voltage stress on the main switches have not undergone significant improvement, despite other efforts being made. In addition, it is possible to achieve high step-down converters by combining these methods [22], [23], [24], [25], [26], [27], [28]. In [25], an interleaved two-phase converter with CIs is presented, which provides power to the other module through a capacitor in one module's power path. However, this converter consists of six switches and has many components. In [28], an asymmetric interleaved configuration is presented by connecting a buck converter and a Cuk converter. In addition, using CIs, series capacitors, and WCCI techniques can effectively decrease both the voltage gain and output current ripple. However, its magnetized inductors have a large volume and weight. Moreover, in [28], one of the switches experiences a voltage spike that decreases efficiency.

This article describes a nonisolated interleaved ultra-high step-down converter that can significantly reduce the voltage stress on its semiconductor components and achieve ripple cancellation in the output current. The proposed converter employs IBC topologies, CIs, input series capacitors, blocking capacitors, and WCCI techniques to effectively reduce the voltage and current stress on the semiconductor components. In addition, soft-switching conditions can be achieved for all switches and diodes at ZVS and ZCS, respectively, without the need for any additional auxiliary circuits. As a result, the converter's efficiency is improved, and the occurrence of reverse recovery problems is prevented.

The article is organized into six sections. In Section II, the proposed converter's operating principle is described. In Section III of the article, a detailed explanation of the steady-state analysis and theoretical waveforms of the converter is presented. Then, the proposed converter comparisons with other converters are provided in Section IV. The experimental results of an implemented prototype converter are presented in Section V, along with a detailed analysis of its losses and efficiency. Eventually, this article is concluded in Section VI.

II. Converter Description and Operational Principle

Fig. 1(a) shows the suggested high step-down converter derived from merging two conventional buck converters, and Fig. 1(b) shows the equivalent circuit for the proposed converter. The topology mentioned above demonstrates a decrease in VCR

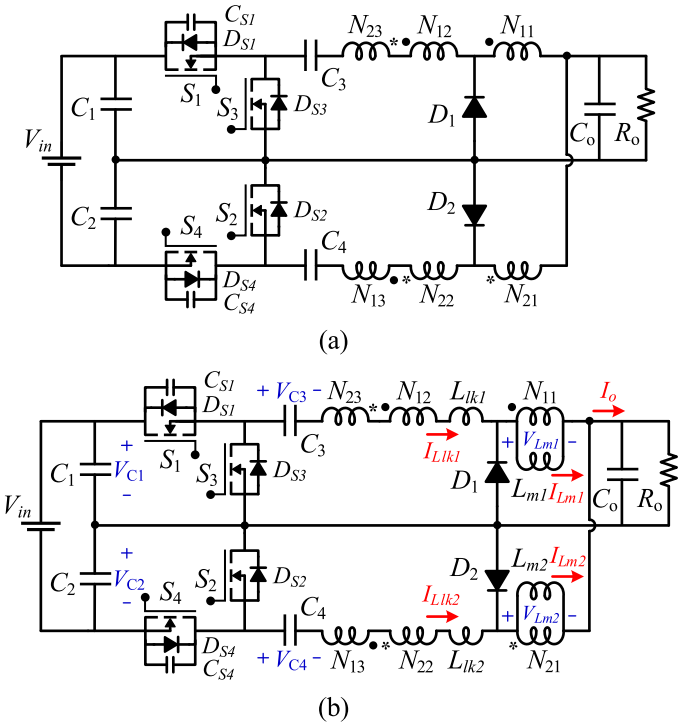

Fig. 1. (a) Topology of the proposed converter. (b) Equivalent circuit.

and reduces the voltage stress on semiconductor components compared to [28]. In addition, all switches meet the conditions for soft switching, and employing an interleaved structure reduces the ripple in output current. In addition, implementing the WCCI technique yields improvements in voltage gain and output current ripple. The converter contains four switches S_1, S_2, S_3, and S_4, two diodes D_1 and D_2, two input capacitors C_1 and C_2, along with two blocking capacitors C_3 and C_4, one output capacitor C_o, two snubber capacitors C_{S_1} and C_{S_4}, one CI composed of three windings N_{11}, N_{12}, and N_{13}, one leakage inductor L_{lk_1} and one magnetizing inductor L_{m_1}, and the other CI consisting of three windings N_{21}, N_{22}, and N_{23}, one leakage inductor L_{lk_2} and one magnetizing inductor L_{m_2}.

By placing snubber capacitors in parallel with switches S_1 and S_4, the ZVS turn-OFF condition is achieved for switches by limiting the rate of voltage change. CIs have the same turns ratio, which is as follows:

$$N_{12} = N_{13} = nN_{11}, \quad N_{22} = N_{23} = nN_{21}. \tag{1}$$

As shown in Fig. 2, the converter operates in six distinct modes throughout a single switching cycle. Also, Fig. 3 demonstrates the crucial theoretical waveforms for the operation of the suggested converter.

In order to streamline the analysis of the proposed converter, the following assumptions have been taken into consideration:

1) All converter components are ideal, and the converter operates at a steady state.
2) It is assumed that all capacitors have enough capacitance to maintain a constant voltage across them, and the

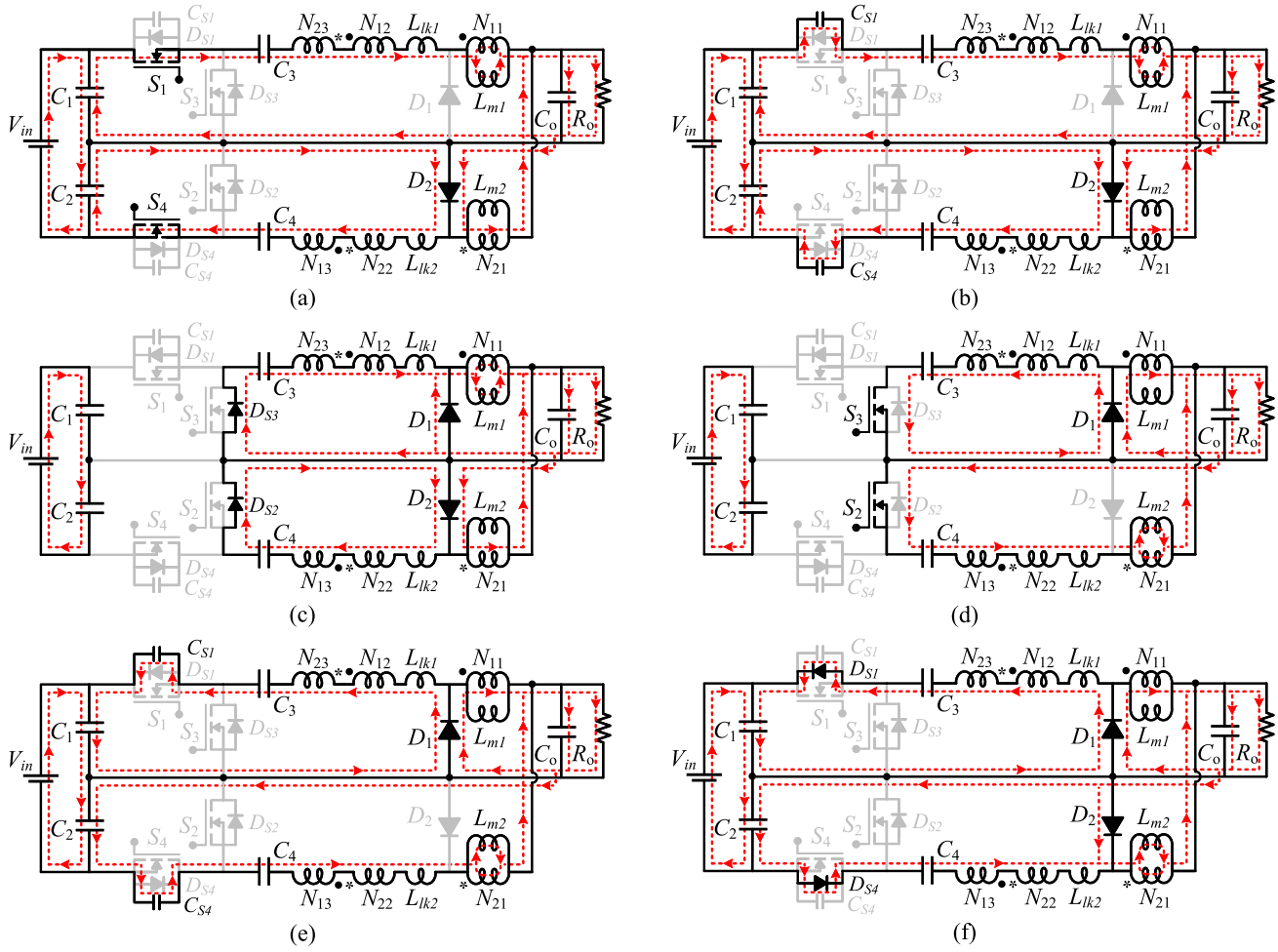

Fig. 2. Equivalent circuit of each operating mode. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6.

magnetizing inductances have enough inductance to maintain a constant current.

Before the first operating mode, all the switches are OFF while S_1 and S_4 body diodes are conducting. In addition, D_1 and D_2 are ON.

A. Mode 1 ($t_0 - t_1$) [see Fig. 2(a)]

At the start of this operational stage, under ZVS conditions, the switches S_1 and S_4 are activated, while all other switches are deactivated. In addition, D_1 is turned OFF under ZCS conditions. As a result, the current passing through S_1 and S_4 grows linearly, and the magnetizing inductance L_{m_1} is charged by C_1. The equations for V_{lk_1} and L_{lk_1} are as follows:

$$V_{lk_1} = V_{C_1} - (V_{C_2} + V_{C_4}) \left(\frac{n+1}{n}\right) - V_{C_3} \tag{2}$$

$$I_{lk_1}(t) = I_{S_1}(t) = I_{lk_1}(t_0) + \frac{1}{L_{lk_1}} \times \left(V_{C_1} - (V_{C_2} + V_{C_4}) \left(\frac{n+1}{n}\right) - V_{C_3}\right)(t - t_0). \tag{3}$$

B. Mode 2 ($t_1 - t_2$) [see Fig. 2(b)]:

At t_1, to end the power transfer mode, S_1 and S_4 are turned OFF under ZVS conditions by the snubber capacitors. Then, at the end of this mode C_{S_1} and C_{S_2} are charged up to V_{C_1} and V_{C_2}, respectively.

C. Mode 3 ($t_2 - t_3$) [see Fig. 2(c)]

At t_2, D_{S_2} and D_{S_3} are turned ON to provide ZVS turn-ON conditions for switches S_2 and S_3, and D_1 also turns ON. As described by the following relationships, the current passing through L_{lk_1} (I_{lk_1}) and the current flowing through D_2 (I_{D_2}) undergoes linear reduction while I_{D_1} linearly increases:

$$I_{lk_1}(t) = I_{lk_1}(t_2) - \frac{V_{C_3}}{L_{lk_1}}(t - t_2) \tag{4}$$

$$I_{D_1}(t) = I_{lm_1} - \left(I_{lk_1}(t_2) - \frac{V_{C_3}}{L_{lk_1}}(t - t_2)\right)(n+1) \tag{5}$$

$$I_{D_2}(t) = I_{lm_2} + \left(I_{lk_1}(t_2) - \frac{V_{C_3}}{L_{lk_1}}(t - t_2)\right)(n+1). \tag{6}$$

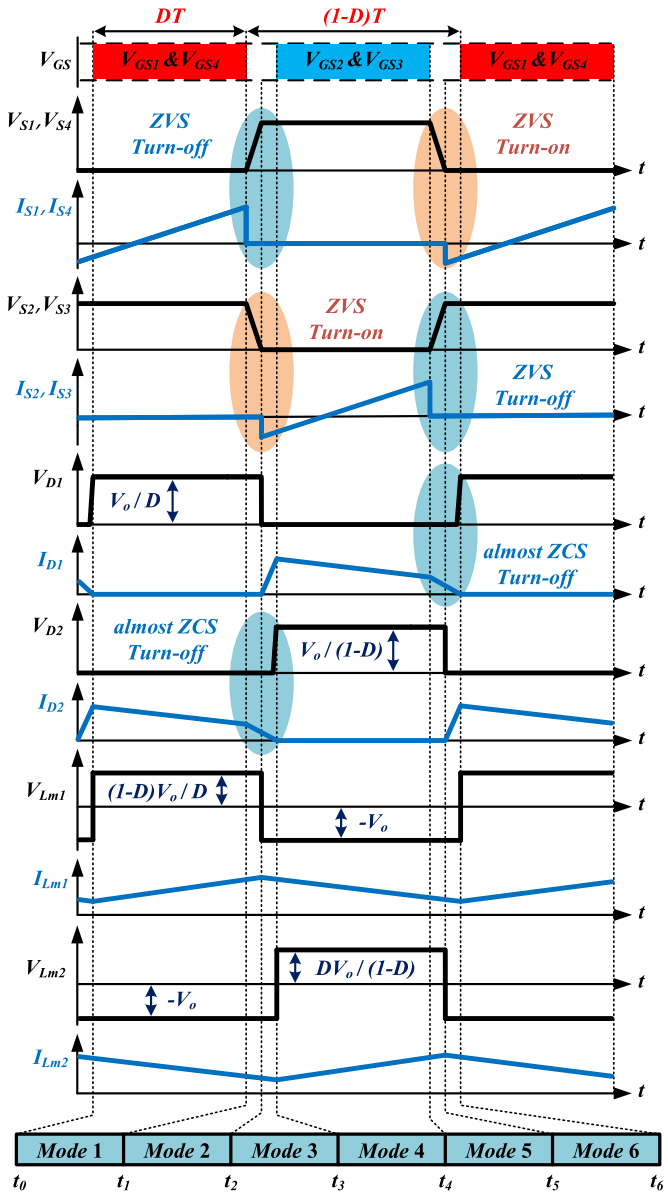

Fig. 3. Converter crucial theoretical waveforms.

D. Mode 4 ($t_3 - t_4$) [see Fig. 2(d)]

At t_3, S_2 and S_3 are turned ON under the ZVS condition, and D_2 turns OFF under the ZCS condition. In this mode, the current of S_2 and S_3 increases linearly, while the current of magnetizing inductance L_{m_1} decreases, and the current of L_{m_2} increases. The equations for V_{lk_2} and I_{S_2} are as follows:

$$V_{lk_2}(t) = -V_{C_4} - (V_{C_3} + V_{lk_1})\left(\frac{n+1}{n}\right) \tag{7}$$

$$I_{S_2}(t) = I_{lk_2}(t) = I_{lk_2}(t_2) - \frac{1}{L_{lk_2}} \times \left[V_{C_4} + (V_{C_3} + V_{lk_1})\left(\frac{n+1}{n}\right)\right](t - t_3). \tag{8}$$

E. Mode 5 ($t_4 - t_5$) [see Fig. 2(e)]

During this mode, C_{S_1} and C_{S_2} are discharged to zero voltage. In addition, since the capacitor loop includes snubber capacitors and input capacitors connected in parallel with the switches, S_2 and S_3 are turned OFF in the ZVS condition.

F. Mode 6 ($t_5 - t_6$) [see Fig. 2(f)]

In this mode, due to I_{lk_1} and I_{lk_2}, S_1 and S_4 body diodes are turned ON to provide ZVS conditions for S_1 and S_4 turn ON. Also, D_2 turns ON while I_{D_1} decreases linearly. Moreover, the current of L_{lk_1} decreases linearly, as described by the following relations:

$$I_{lk_1}(t) = I_{lk_1}(t_5) + \frac{V_{C_1} - V_{C_3}}{L_{lk_1}}(t - t_5) \tag{9}$$

$$I_{D_1}(t) = I_{lm_1} + \left(I_{lk_1}(t_5) + \frac{V_{C_1} - V_{C_3}}{L_{lk_1}}(t - t_5)\right)(n+1). \tag{10}$$

III. Steady-State Analysis and Design Considerations

A. Converter VCR

Since modes 2, 3, 5, and 6 have such short durations, they are not considered in the description of the converter operating at a steady state to simplify the explanation.

By utilizing the volt-second balance principle during the first and fourth modes for L_{m_1} and L_{m_2}, the following equations can be derived:

$$\left[\frac{(V_{C_1} - V_{C_3})}{n+1} - V_o\right] DT = V_o(1-D)T \tag{11}$$

$$[-V_o]\, DT = \left[\frac{V_{C_4}}{n+1} + V_o\right](1-D)T \tag{12}$$

where D is the duty cycle of switches S_1 and S_4, and T is the switching period. Also, by employing the KVL principle during the first and fourth modes and utilizing (11) and (12), capacitor voltages can be derived from the following relations:

$$V_{C_1} = \left[\frac{n - D + 1}{D(1-D)}\right] V_o \tag{13}$$

$$V_{C_2} = \left[\frac{n + D}{D(1-D)}\right] V_o \tag{14}$$

$$V_{C_3} = \frac{nV_o}{1-D} \tag{15}$$

$$V_{C_4} = \frac{-(n+1)V_o}{1-D}. \tag{16}$$

As observed, capacitor voltages are determined based on the output voltage of the converter, converging to a constant value.

By using the input voltage equation in (17) and substituting (13) and (14) into (17), the conversion ratio for the suggested converter is attained through (18):

$$V_{\text{in}} = V_{C_1} + V_{C_2} \tag{17}$$

$$\frac{V_{\text{o}}}{V_{\text{in}}} = \frac{D(1-D)}{2n+1}. \tag{18}$$

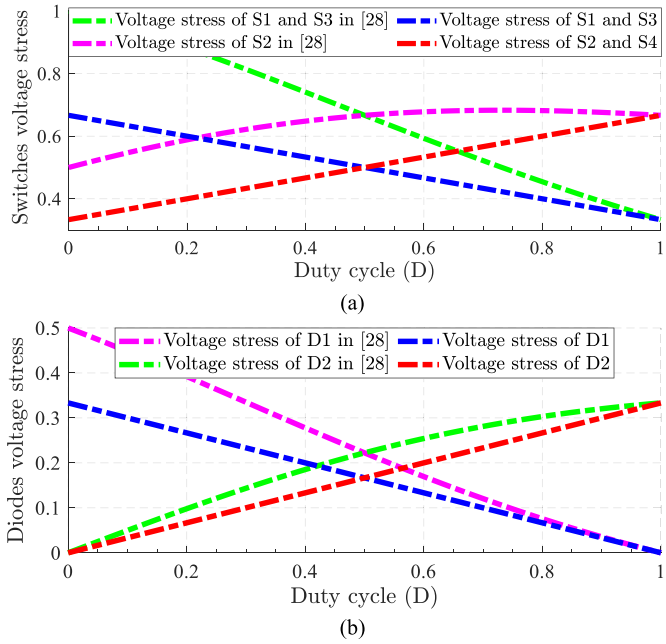

Fig. 4. Comparison of the voltage stress on switches and diodes between the proposed converter and with [28] for different duty cycles. (a) Voltage stress on switches. (b) Voltage stress on diodes.

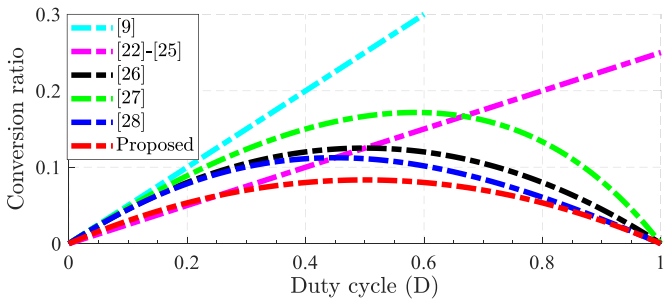

Fig. 5. Comparison of the VCR for various duty cycle.

According to (18), the voltage gain of the recommended converter is a notable decrease while disregarding the duty cycle that has disappeared.

To calculate the lost duty cycle (D_l), the KCL principle can be utilized during modes 1 and 4 to derive the following equations:

$$I_{\mathrm{a}} + nI_{\mathrm{a}} = I_{L_{m_1}} \rightarrow I_{\mathrm{a}} = \frac{I_{L_{m_1}}}{n+1} \tag{19}$$

$$I_{L_{m_1}} + I_{L_{m_2}} + nI_{\mathrm{d}} = nI_{\mathrm{a}} + I_{\mathrm{o}}$$
$$\rightarrow I_{\mathrm{d}} = \frac{1}{n}\left[I_{\mathrm{o}} - \frac{I_{L_{m_1}}}{n+1} - I_{L_{m_2}}\right] \tag{20}$$

$$I_{\mathrm{b}} + nI_{\mathrm{b}} = I_{L_{m_2}} \rightarrow I_{\mathrm{b}} = \frac{I_{L_{m_2}}}{n+1} \tag{21}$$

$$I_{L_{m_1}} + I_{L_{m_2}} + nI_{\mathrm{c}} = nI_{\mathrm{b}} + I_{\mathrm{o}}$$
$$\rightarrow I_{\mathrm{c}} = \frac{1}{n}\left[I_{\mathrm{o}} - I_{L_{m_1}} - \frac{I_{L_{m_2}}}{n+1}\right] \tag{22}$$

where I_{a} and I_{b} represent the charging currents of C_3 and C_4, respectively, while I_{c} and I_{d} indicate the discharging currents of C_3 and C_4, respectively, in the given context.

The expressions obtained by utilizing the ampere-second balance approach for C_3 and C_4 are stated below:

$$I_{\mathrm{a}}(DT) = I_{\mathrm{c}}(1-D)T, \quad I_{\mathrm{d}}(DT) = I_{\mathrm{b}}(1-D)T. \tag{23}$$

The substitution of (19)–(22) into (23), results in

$$I_{L_{m_1}} = (1-D)I_{\mathrm{o}}, \quad I_{L_{m_2}} = DI_{\mathrm{o}}. \tag{24}$$

In order to prevent short circuits in input capacitors, when the gate signal of S_1 and S_4 are removed, it is impossible to instantaneously apply the gate signals for S_2 and S_3 once they have been removed. Therefore, the gate signals must be separated by a short dead time. Also, in modes 3 and 6, the switches' body diodes become conductive by L_{lk_1} and L_{lk_2}, which provide ZVS turn-ON conditions. Consequently, a part of the duty cycle is forfeited, and the calculation of the operational duty cycle (D_{o}) can be determined using the following formula:

$$D_{\mathrm{o}} = D - D_l \tag{25}$$

where D_l represents the lost duty cycle. By transferring L_{lk_2} to the first phase, the following results are obtained:

$$L_{\mathrm{lk}_t} = L_{\mathrm{lk}_1} + \left(\frac{N_{23}}{N_{22}}\right)^2 L_{\mathrm{lk}_2}. \tag{26}$$

Considering L_{lk_1}=L_{lk_2}=L_{lk} and N_{23}=N_{22}, L_{lk_t} is as follows:

$$L_{\mathrm{lk}_t} = 2L_{\mathrm{lk}} \tag{27}$$

which

$$V_{L_{\mathrm{lk}_1}} D_l T = L_{\mathrm{lk}_t} \Delta I_1, \quad \Delta I_1 = I_{\mathrm{a}} - I_{\mathrm{c}}. \tag{28}$$

Thus, D_l is obtained as

$$D_l = \left(\frac{(D-1)(1-2D)I_o}{n(n+1)V_oT}\right)(2L_{\mathrm{lk}}). \tag{29}$$

B. Voltage and Current Stress of the Switches and Diodes

Using the KVL principle at the circuit input during modes 1 and 4 yields that the voltage stress on switches S_1 and S_3 is equal to V_{C_1}, while the voltage stress on switches S_2 and S_4 is equal to V_{C_2}. Therefore

$$V_{S_1} = V_{S_3} = \left[\frac{(n+1-D)}{2n+1}\right] V_{\mathrm{in}} \tag{30}$$

$$V_{S_2} = V_{S_4} = \left[\frac{(n+D)}{2n+1}\right] V_{\mathrm{in}}. \tag{31}$$

According to modes 1 and 4, the highest level of voltage stress experienced by D_1 and D_2 can be achieved in the following manner:

$$V_{D_1} = \left[\frac{(1-D)}{2n+1}\right] V_{\mathrm{in}} \tag{32}$$

$$V_{D_2} = \left[\frac{D}{2n+1}\right] V_{\mathrm{in}}. \tag{33}$$

Fig. 4 compares the voltage stress experienced by switches and diodes in the suggested converter and the topology introduced in [28] for different duty cycles when n=1. As illustrated in Fig. 4(a), when the duty cycle exceeds 0.5, the voltage stress in S_1 and S_3 decreases linearly below half of the input voltage. Also, the voltage stress in S_2 and S_4 at its maximum value is less than two-thirds of the input voltage. In addition, as shown in Fig. 4(b), in the middle of the duty cycle range, the voltage stress encountered by D_1 and D_2 is lower than one-fifth of the input voltage. Compared to [28], the suggested converter experiences significantly lower voltage stresses on its switches and diodes. This means that high-quality diodes and low-voltage switches can be used for the suggested converter.

The RMS current of power switches and the mean current of the diodes are computed by applying the KCL principle in modes 1 and 4, as demonstrated below:

$$I_{\text{rms\_}S_1} = I_{\text{rms\_}S_4} = \frac{\sqrt{D} I_{L_{m_1}}}{n+1}$$

$$I_{\text{rms\_}S_2} = I_{\text{rms\_}S_3} = \frac{\sqrt{1-D} I_{L_{m_2}}}{n+1} \tag{34}$$

$$I_{\text{avg}-D_1} = I_{L_{m_1}}, \quad I_{\text{avg}-D_2} = I_{L_{m_2}}. \tag{35}$$

C. Passive Components' Design

Based on (19), the mean current flowing through capacitor C_3 during DT is determined. According to (24) and (19), the design of capacitor C_3 can be accomplished in the following manner:

$$C_3 = \frac{\left[\frac{(1-D)I_o}{n+1}\right] DT}{\Delta V_{C_3}} = \frac{D(1-D)I_o}{0.2(n+1)V_{C_3} f_s} \tag{36}$$

where ΔV_{C_3} is the peak-to-peak voltage ripple of V_{C_3} during DT. Also, the mean current flowing through capacitor C_3 throughout the DT period can be computed using (21). By substituting (24) into (21), C_4 can be designed as follows:

$$C_4 = \frac{\left[\frac{DI_o}{n+1}\right] (1-D)T}{\Delta V_{C_4}} = \frac{D(1-D)I_o}{0.2(n+1)V_{C_4} f_s} \tag{37}$$

where ΔV_{C_4} is the peak-to-peak voltage ripple of V_{C_4} during DT.

In modes 1 and 4, the voltage V_{o} is applied to the magnetizing inductances L_{m_2} during DT and L_{m_1} during (1-D)T. By utilizing (24), the boundary conditions for L_{m_1} and L_{m_2} to operate in CCM can be obtained as follows:

$$V_{L_{m_1}} = L_{m_1} \frac{dI_{L_{m_1}}}{dt} \rightarrow L_{m_1} \geq \frac{V_o(1-D)T}{2(1-D)I_o} = \frac{V_o}{2I_o f_s} \tag{38}$$

$$V_{L_{m_2}} = L_{m_2} \frac{dI_{L_{m_2}}}{dt} \rightarrow L_{m_2} \geq \frac{V_o DT}{2DI_o} = \frac{V_o}{2I_o f_s}. \tag{39}$$

D. ZVS Conditions for Power Switches

To satisfy soft-switching conditions for S_3 and S_2, the leakage inductances (L_{lk_1} and L_{lk_2}) along with L_{m_1} should be sufficient to charge the snubber and output capacitors of S_1 and S_4, as well as to discharge the output capacitor of S_3 and S_2. Conversely, the opposite is true for S_4 and S_1 with the help of L_{lk_1}, L_{lk_2}, and L_{m_2}. Thus, the snubber capacitors limit the rate of voltage change for the switches, and the ZVS condition is achieved when $\frac{1}{2}L_{\text{lk}} i_{\text{lk}}^2 \geq \frac{1}{2}C_S V_S^2$. Therefore

$$\begin{cases} S_3, S_2 : L_{m_1}[(n+1)I_a + nI_d]^2 + L_{lk_1} I_a^2 + L_{lk_2} I_d^2 \geq \\ (2C_{\text{oss}} + C_{S_1})(V_{C_1})^2 + (2C_{\text{oss}} + C_{S_4})(V_{C_2})^2 \\ S_4, S_1 : L_{m_2}[(n+1)I_b + nI_c]^2 + L_{lk_1} I_c^2 + L_{lk_2} I_b^2 \geq \\ (2C_{\text{oss}} + C_{S_1})(V_{C_1})^2 + (2C_{\text{oss}} + C_{S_4})(V_{C_2})^2. \end{cases} \tag{40}$$

By substituting the capacitor currents using (24) and (19)–(22) in terms of I_o, and substituting the designed values for L_{m_1} and L_{m_2}, along with other voltages and parameters obtained using relevant equations or datasheets in (40), the minimum boundary power required to satisfy the ZVS condition for all switches is approximately one-third of the full load power.

IV. Performance Analysis and Comparison

In this passage, the operational characteristics of the suggested converter with other high-step-down converters are compared, and these instances are summarized in Table I. In [9], a high step-down converter is introduced, which is nonisolated and capable of recycling leakage energy while achieving soft switching conditions. However, the VCR has not improved sufficiently, and the two switches experience the same voltage stress equal to the input voltage. Regarding the converters mentioned in [22], [25], [26], and [27], SRs are used in order to reduce conduction losses and increase efficiency. By using the interleaved structure described in [22], [23], [24], [25], [26], [27], and [28] along with the suggested converter, the VCR can be improved.

Another method to decrease the VCR is employing CIs and modifying the winding turns ratio. However, this was not achieved in [24], and the voltage gain is constrained. Also, the CIs in [25] have a large volume and weight. It is important to note that the output current in [22] is pulsing. In [26] and [27], a reduction in voltage gain can be achieved by combining series capacitors and CIs. However, the voltage stress on the power switches is equal to the input voltage. Higher switching frequencies are required to enhance power density and improve dynamic response. However, hard switching in [24] reduces efficiency and limits the switching frequency. In the proposed converter and [28], uncommon ground between input and output may impose limitations in certain applications. However, these converters are designed for use in battery chargers, LED drivers, and similar applications, where common ground is unnecessary. In [28], the voltage reduction ratio of the presented converter is substantial, and its semiconductor elements are subjected to low voltage stress. However, full soft switching conditions are not achieved in [28]. Moreover, the suggested converter decreases the size of magnetized inductors to less than 15% in comparison to the converter described in [28], leading to a decrease in both cost and

TABLE I
COMPARISON OF THE PROPOSED CONVERTER WITH OTHER CONVERTERS

Characteristics	[9]	[22]	[23]	[24]	[25]	[26]	[27]	[28]	Proposed
Voltage gain	$\frac{D}{n+1}$	$\frac{D}{2(n+1)}$	$\frac{D}{2(n+1)}$	$\frac{D}{4}$	$\frac{D}{2(n+1)}$	$\frac{nD(1-D)}{n+1}$	$\frac{D(1-D)}{n+1-D}$	$\frac{D(1-D)}{n(D+1)+D(D-1)+1}$	$\frac{D(1-D)}{2n+1}$
Switch count	4	6	4	4	6	4	4	3	4
Diode count	0	0	2	4	0	0	0	2	2
Capacitors	4	4	4	4	4	2	2	5	5
Inductors/CIs	1/1	0/2	4/1	4/0	0/2	0/2	0/2	1/2	0/2
Switching condition	ZVS	ZVS	ZVS	Hard	ZVS	ZVS	ZVS	2×ZVS, 1×ZCS-ON	ZVS
Implemented Prototype	33W 48V/3.3V	66W 48V/3.3V	450W 400V/12V	500W 400V/24V	100W 400V/24V	20W 12V/1V	30W 48V/1V	200W 310V/24V	200W 300V/25V
Switching frequency	50 kHz	400 kHz	100 kHz	40 kHz	100 kHz	100 kHz	50 kHz	100 kHz	100 kHz
Reported full load efficiency	93.6%	95.6%	94.9%	91.8%	92.7%	92%	93.1%	93.6%	97%
Common ground	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	No
Output current	Continuous	Pulse	Continuous	Continuous	Continuous	Continuous	Continuous	Continuous	Continuous
Switches voltage stress	V_{in} $\frac{V_{in}}{n+1}$	V_{in} $\frac{1}{2}V_{in}$	$\frac{1}{2}V_{in}$	$\frac{1}{4}V_{in}$ $\frac{1}{2}V_{in}$	$\frac{1}{2}V_{in}$	V_{in}	V_{in}	$\frac{n-D+1}{n(D+1)+D(D-1)+1}V_{in}$ $\frac{n+D}{n(D+1)+D(D-1)+1}V_{in}$	See equations (30) and (31)
Diodes voltage stress (or synch. rectifiers)	-	$\frac{V_{in}}{n+1}$	$\frac{1}{4}V_{in}$	$\frac{1}{4}V_{in}$	$\frac{1}{4}V_{in}$	$\left[\frac{1-D}{1+n}\right]V_{in}$	$\frac{DV_{in}}{n+1-D}$	$\frac{1-D}{n(D+1)+D(D-1)+1}V_{in}$ $\frac{D}{n(D+1)+D(D-1)+1}V_{in}$	See equations (32) and (33)

TABLE II
IMPLEMENTED CONVERTER PROTOTYPE SPECIFICATIONS

Parameter	Symbol	Specifications
Input voltage	V_{in}	300 V
Output power	P_o	200 W
Switching frequency	f_s	100 kHz
Input capacitors	C_1, C_2	100 μF
Blocking capacitors	C_3, C_4	4.7 μF
Output capacitor	C_o	100 μF
Snubber capacitors	C_{S_1}, C_{S_2}	470 pF
Magnetizing inductances	L_{m_1}, L_{m_2}	21 μH
Turn ratio	n	1
Main switches	S_1, S_2 S_3, S_4	IRFP4668
Main diodes	D_1, D_2	MBR20100CT

volume. Furthermore, one of the switches in [28] experiences a spike in voltage, resulting in a decrease in efficiency.

Fig. 5 compares the VCR for the introduced topology to its recent counterparts when n=1. As can be seen, the topology introduced here has a lower conversion ratio.

V. EXPERIMENTAL RESULTS AND EFFICIENCY

A. Design Procedure

This section describes a prototype of the proposed converter, implemented at 300-V input voltage, 25-V output voltage, 200-W output power, and 100-kHz operating frequency. Table II illustrates the specifications of the designed converter. The proposed converter design is implemented under the conditions of minimum input voltage and maximum output load, with D approximately equal to 0.5. Therefore, it can regulate the output voltage to lower values and operate with various duty cycles. By utilizing the input and output voltages in (18), the duty cycles of S_1, S_2, S_3, and S_4 can be computed as 0.48. Furthermore, the control of the converter follows a simple structure. By using the SG3525 IC, simultaneous gate pulses can be applied to switches S_1 and S_4, while switches S_2 and S_3 receive pulses via a NOT gate. It is worth noting that, to prevent short-circuiting of input capacitors, a delay has been introduced at the rising edge of the pulses. Based on (30) and (31), the approximate voltage stress on switches is 150 V; thus, IRFP4668 (V_{DS}= 200 V, $R_{\text{DS(ON)}}$= 8 mΩ) is used for the switches. Based on (40), the snubber capacitors are calculated as C_{S_1}= C_{S_4}= 470 pF. According to (32) and (33), the voltage stress on the diodes is 49 V and 51 V; therefore, MBR20100 (V_F = 0.64 V) is used for the diodes. By choosing $n = 1$ and utilizing (38) and (39) for CCM, and applying (40) to satisfy the ZVS condition for all switches under one-third of the nominal load, the magnetizing inductances are calculated as 21 μH. In addition, the number of turns (N) for each winding of the inductors is determined to be 19 turns using the relation $LI_{\text{peak}} = NBA_e$ in the linear region. Thus, EE25/19 ferrite core ($V_e = 1950$ mm^3, $A_e = 40$ mm^2) is picked for L_{m_1} and L_{m_2}. Moreover, based on (36) and (37), blocking capacitors are calculated as 4.7 μF.

B. Experimental Waveforms

Fig. 6(a) and (d) illustrates the waveforms of the voltage and current for the power switches. As observed, ZVS conditions are attained for all switches. In addition, the voltage stress experienced by the switches is notably below the input voltage. Also, in Fig. 6(b) and (e), the voltage and current waveforms of the diodes are shown. As can be seen, the ZCS conditions are almost met for all diodes during turn OFF, thereby resolving the problem of reverse recovery. The voltages of C_1 and C_2 are illustrated in Fig. 6(c). The output currents for each phase and their summation are shown in Fig. 6(f) to effectively demonstrate the impact of ripple cancellation on the current I_o. Also, I_{C_3} is shown in Fig. 6(g). Furthermore, to demonstrate the wide input voltage range capability of the proposed converter, considering the converter is designed for an input voltage of 300 V with a maximum output voltage of 25 V, and due to the inability to achieve a conversion from 150 to 25 V, the converter was tested with 300 to 12 V and 150 to 12 V using the same prototype. The results of these experiments are shown in Fig. 6(h) to (k). In addition, a laboratory prototype is presented in Fig. 7.

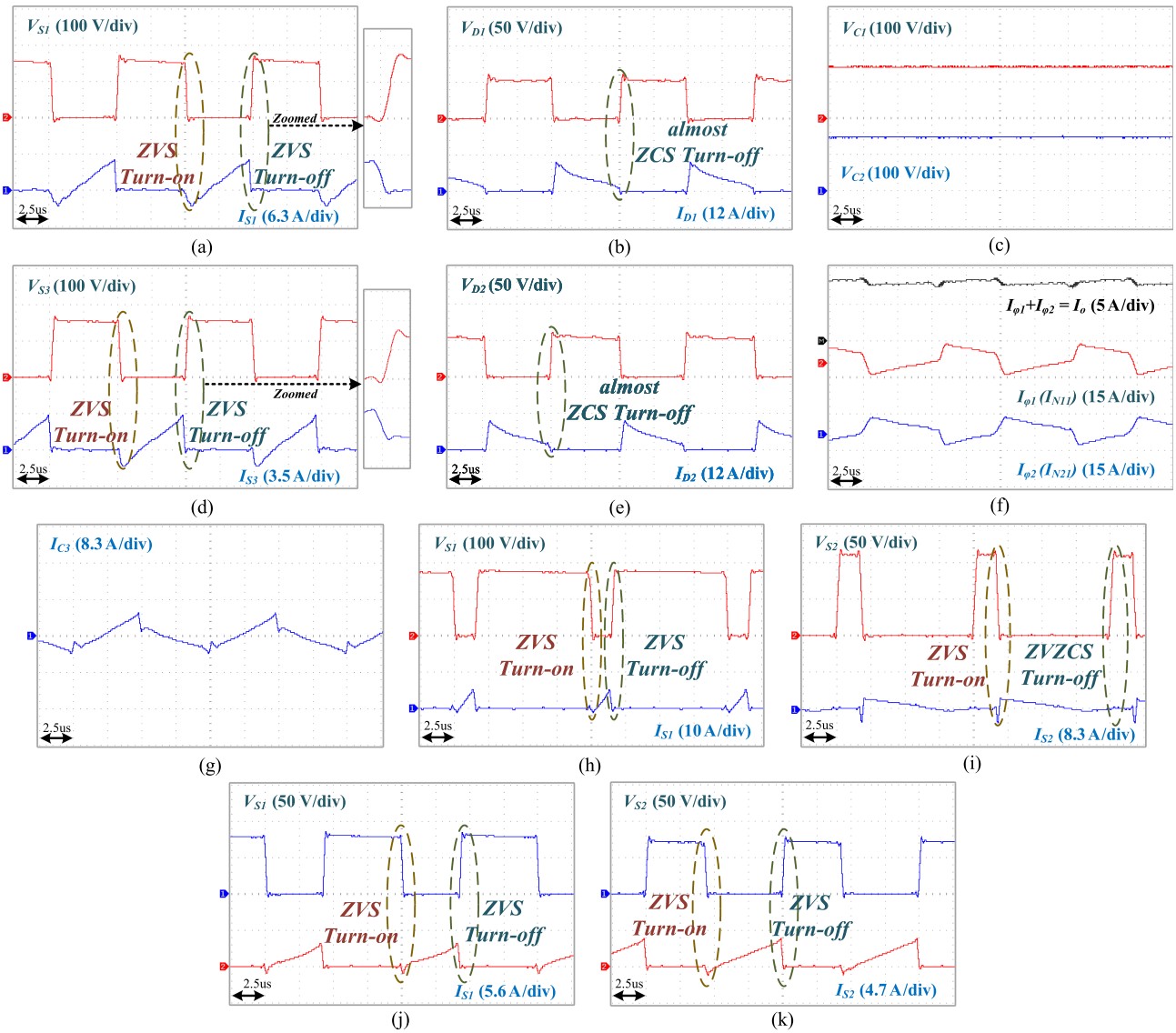

Fig. 6. Experimental waveforms (300 to 25 V at 200 W). (a) Voltage and current of S_1. (b) Voltage and current of D_1. (c) C_1 and C_2 voltages. (d) Voltage and current of S_3. (e) Voltage and current of D_2. (f) Output currents for each phase and their summations, and (g) current of C_3 (the waveforms of switches S_4 and S_2, respectively, are similar to those of switches S_1 and S_3, and I_{C_4} is also similar to that of $-I_{C_3}$). Experimental waveforms (300 to 12 V at 100 W). (h) Voltage and current of S_1. (i) Voltage and current of S_2. Experimental waveforms (150 to 12 V at 100 W). (j) Voltage and current of S_1. (k) Voltage and current of S_2.

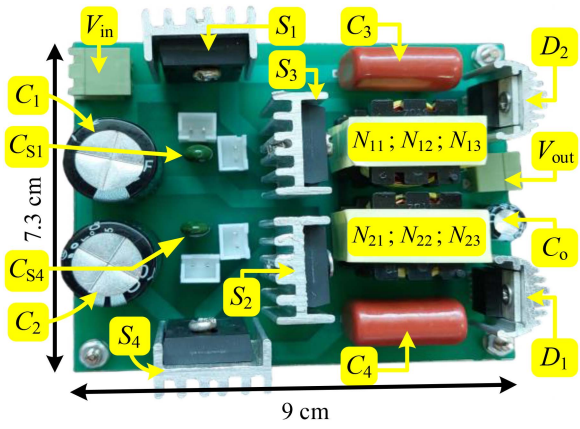

Fig. 7. Converter implemented prototype.

C. Loss Analysis and Converter Efficiency

The loss distribution of the proposed high step-down converter and converter in [28] is shown in Fig. 8(a). Except for one of the switches in [28], which experienced a voltage spike and IRFP4768PbF is selected for it, to ensure a fair comparison, the type of all other components considered is identical to that of the suggested converter. According to Fig. 8(a), the switching losses in the proposed converter are eliminated by establishing ZVS turn-ON and turn-OFF conditions for all switches. As observed, the major portion of converter losses is attributed to conduction losses in its diodes. The converter can achieve an efficiency of 97% at full load, while this value is 93.6% for the converter [28]. The efficiency is improved to 98% by substituting diodes with SR. Finally, the proposed converter efficiency diagram at different output powers is illustrated in Fig. 8(b). It should be noted

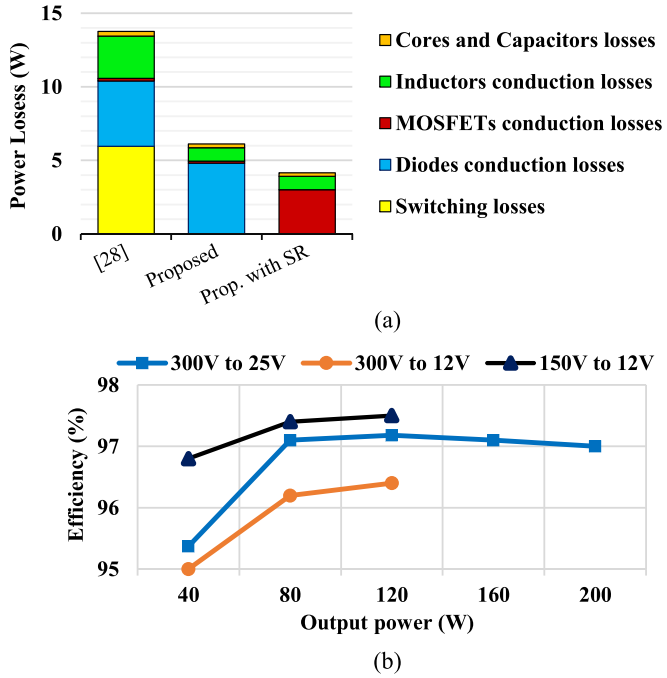

Fig. 8. (a) Loss distribution comparison between the suggested converter and converter introduced in [28] (300 to 25 V at $P_o = 200\,W$). (b) Suggested converter efficiency at different output powers.

that, due to the design of the converter for 300 V input voltage and 25 V output voltage, with a reduction in the output voltage to 12 V, the power in the other two states is limited to a maximum of 120 W.

VI. Conclusion

In this article, a soft-switched ultra-high step-down converter is introduced with low voltage stress on semiconductor components. The converter achieves high efficiency by eliminating switching losses, reverse recovery losses of diodes, and low conduction losses. Moreover, utilizing the WCCI technique results in an improvement in voltage gain and a reduction in the voltage stress experienced by the diodes. To confirm the theoretical analysis and demonstrate the advantages of the converter, a laboratory prototype with a power output of 200 W and 300-to-25 V was developed. Also, the results obtained from the prototype verified the analysis and performance of the converter.

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