Modeling and Analysis of IGBT Based on Two-Dimensional Charge Distribution

Qi Li, Xianwen Cui, Yonghe Chen, Jian Ye, Shi Cheng, and Li Guan

***Abstract*—This article presents an enhanced physical SPICE model for insulated gate bipolar transistor (IGBT) modules, grounded in a two-dimensional charge distribution. The model accurately delineates the lateral charge distribution under both static conduction and transient conditions, providing a precise representation of the PNP and PIN components of the IGBT. The improved model more effectively describes current distribution and clarifies parasitic effects, such as latch-up phenomenon. Furthermore, a negative carrier lifetime near the gate is introduced in accordance with the carrier movement direction, resulting in a catenary charge distribution in the PIN segment of the IGBT. This aligns closely with the technology computer-aided design (TCAD) results. Notably, the carrier concentration in the N^-base region significantly escalates under high-level injection conditions. The model incorporates an N^+N^- junction and a P^+N^- junction within the channel to portray the carrier concentration variation during the transient state, also factoring in the effect of temperature on the IGBT characteristics. Implemented in PSPICE, the model's findings are compared with TCAD outcomes and experimental data. These comparisons illustrate that the proposed model precisely delivers the charge distribution, as well as dynamic/static characteristics and unbalanced current in parallel devices of the IGBT.**

***Index Terms*—Insulated-gate bipolar transistors (IGBT), negative carrier lifetime, SPICE model, two-dimensional (2-D) charge distribution.**

I. Introduction

INSULATED-GATE bipolar transistors (IGBTs) have become pivotal as switching devices, widely adopted in power electronic applications due to their optimal blend of bipolar and metal-oxide-semiconductor field-effect transistor (MOSFET) structures [1]. The physics model that accurately delineates the operating characteristics and parasitic effects of IGBTs is of significant interest to both device manufacturers and power electronics systems designers [2]. A variety of IGBT models have been proposed in recent years, primarily bifurcating into two categories: 1) behavioral and 2) physical models. However, the former tends to lack precision across a broad range of operating conditions [3], [4], [5].

The physical model combines the carrier transport process with physical parameters to enhance the prediction accuracy of IGBT performance and has been integrated into simulators such as PSPICE as a device model [6], [7]. This model can be further dissected into a shape function model, a space transformation model, and a lumped-charge model. These not only ensure superior simulation accuracy but also offer insights into the internal behavior of the IGBT. By consolidating and equating the device's charge, the physical-based lumped-charge model, provides approximations of internal physical characteristics that bring device characteristics closer [8]. High simulation efficiency and straightforward model parameter extraction are the key advantages of the lumped-charge model, which was initially applied to the IGBT model [9]. In subsequent research [10], [11], an IGBT lumped-charge model with enhanced simulation accuracy was proposed, along with an equivalent circuit simulation model for multidevice parallel combinations. In [12], the carrier transport equation is written as a differential equation to accurately solve the diffusion equation of the *LC* model, providing a more accurate current expression. In [13], the transmission line theory is introduced into the *LC* model of a diode to achieve dynamic partitioning, which facilitates the allocation of computational resources and improves the convergence of the model. However, these models do not account for the significant two-dimensional (2-D) distribution effect of carriers in the base region during the IGBT's turn-ON and turn-OFF phases, so there is a poor performance in the prediction of latch-up effect and trailing current of the device. A dynamic charge control equation is proposed in [14] to solve for the derivative of the set total charge over time, which is used to better account for the carrier distribution effect at the boundary. However, this method discretizes the base region and the number of charge points complicates the calculation of the model. As a result, they take less account of the description of physical phenomena such as latch-up [15], [16], [17]. While existing device simulation software can employ a finite element model to accurately calculate the 2-D carrier distribution [18], [19], [20], this method involves high computational demands and is heavily reliant on structural parameters, such as the internal gate of the chip, which presents significant limitations [21], [22], [23].

Manuscript received 23 July 2023; revised 3 December 2023, 18 March 2024, and 16 June 2024; accepted 28 July 2024. Date of publication 8 August 2024; date of current version 11 September 2024. This work was supported by the Chinese National Natural Science Foundation under Grant 62064003. Recommended for publication by Associate Editor J. Popovic-Gerber. *(Corresponding author: Xianwen Cui.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3439612.

Digital Object Identifier 10.1109/TPEL.2024.3439612

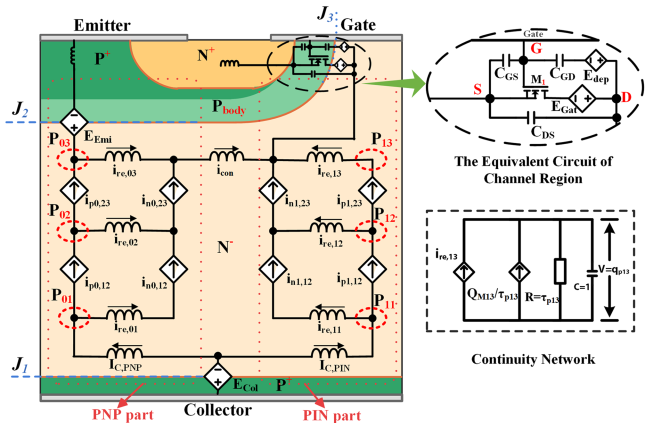

Fig. 1. Proposed physical model of IGBT.

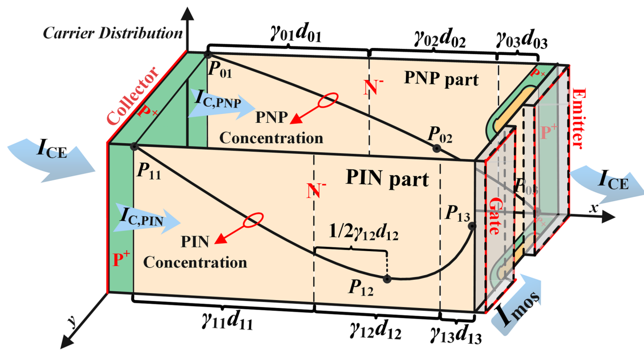

Fig. 2. Position of lumped charge of IGBT.

Addressing these shortcomings, this study developed a physical SPICE model of an IGBT based on a 2-D charge distribution, considering the direction of carrier movement. The device was partitioned into PNP and PIN segments and compared with the Sentaurus technology computer-aided design (TCAD) results. The proposed model accurately described the 2-D carrier distribution and predicted device parasitic latch-up effects. For depicting the carrier variation near the gate during the transient process, N+N- and P+N- junctions were introduced. For experimental validation, the Infineon FF1000R17IE4 (1700 V/1000 A) module and the IKW40N65ET7 (650 V/40 A) device were utilized. A comparison between the simulated and experimental results confirmed the precision of the proposed IGBT model.

II. Lumped-Charge IGBT Model

As illustrated in Fig. 1, a nonpunch-through IGBT was utilized as the foundation for our model, simplifying the IGBT into three primary components: 1) the MOSFET, 2) PNP, and 3) PIN.

A. Model Overview

In Fig. 1, our proposed model bifurcates the N- region of the IGBT into PNP and PIN. The base region is segmented into six parts, with each region's charge being aggregated into a lumped charge, resulting in six lumped charges (P_{01}, P_{02}, P_{03}, P_{11}, P_{12}, P_{13}). The lump charges are allocated to three points each in the PIN and PNP sections, which can better save computational resources under the premise of completely describing the catenary distribution of the carriers [9], [10]. The P^+N^- junction (J_1) at the collector and the $P_{body}N^-$ junction (J_2) under the emitter are depicted by the voltage generators E_{Col} and E_{Emi}, respectively. Moreover, the voltage generator, E_{Gat} portrays a variable junction (J_3) near the gate. Their corresponding voltages are denoted as V_{Col}, V_{Emi}, and V_{Gat}, respectively.

The region under the gate, the N- base region, and the P^+ collector collectively form a p-i-n diode, while the P_{body}, N- base region, and P^+ collector construct a PNP transistor. Unlike the exponential distribution of the carriers in the PNP, the carriers in the PIN exhibit a catenary distribution.

The MOSFET component (M_1) of the IGBT model provides the electron current to the bipolar component. To represent the dynamic behavior of the MOSFET, a series voltage-controlled generator (E_{dep}) is introduced on the capacitance C_{GD} to depict the nonlinear behavior of the capacitance under reverse-biased conditions. Capacitance C_{GD}, C_{GS}, and C_{DS} are considered constant, and their corresponding voltages are denoted as V_{GD}, V_{GS}, and V_{DS}. Fig. 1 also showcases the continuity network at point P_{13}, used to ascertain the charge at this point.

B. Main Part of Model

Fig. 2 depicts the location of the lumped charge and the composition of the current. The values of these lumped charges, normalized to the volume of their corresponding regions, can be calculated using

$$q_{pij} = qd_{ij}A_i p_{ij}, (i = 0, 1; j = 1, 2, 3) \quad (1)$$

$$A_{\text{total}} = A_0 + A_1 \quad (2)$$

where q is the electron charge, $d_{ij} = \gamma_{ij} d_i$, d_i represents the width of the PNP and PIN parts, and d_{ij} is the width of the P_{ij} lumped charge region in the part of the IGBT. γ_{ij} is the partition coefficient that satisfies the condition $\gamma_{11}+\gamma_{12}+\gamma_{13} = 1$; the same applies to $\gamma_{01}\sim\gamma_{03}$ Furthermore, A_0, A_1, and A_{total} represent the areas of the PNP part, the PIN part, and the chip, respectively, and p_{ij} represents the concentration of minority carriers at P_{ij}.

The current I_{CE} between the collector and emitter can be expressed as follows:

$$I_{CE} = I_{C,PNP} + I_{C,PIN} = I_{E,PNP} + I_{E,MOS} \quad (3)$$

where $I_{C,PNP}$ and $I_{C,PIN}$ represent the currents of the PNP and PIN parts at the collector, and $I_{E,PNP}$, $I_{E,MOS}$ denote the currents of the PNP part and the MOSFET part, respectively.

1) Physical Model Near Collector Region: Each current generator in Fig. 1 implements the current density equation between two adjacent nodes as follows:

$$\begin{cases} i_{p1,12} = \frac{2\mu_p\mu_n}{\mu_n-\mu_p}\frac{q_{p11}V_{Col}}{(d_{11}+d_{12}/2)^2} - \frac{\mu_p}{\mu_n-\mu_p}I_{C,PIN} \\ i_{n1,12} = \frac{2\mu_p\mu_n}{\mu_n-\mu_p}\frac{q_{p11}V_{Col}}{(d_{11}+d_{12}/2)^2} + \frac{\mu_p}{\mu_n-\mu_p}I_{C,PIN} \end{cases} \quad (4)$$

where μ_{n} and μ_{p} denote electron mobility and hole mobility, respectively, as follows:

$$I_{\mathrm{C,PIN}} = A_1 \times \frac{q n_i d_1}{\tau_{\mathrm{p11}}} \left[\exp\left(\frac{V_{\mathrm{Col}}}{V_{\mathrm{T}}} \right) - 1 \right] \tag{5}$$

where n_i represents the intrinsic carrier concentration and d_1 represents the width of the PIN part. Furthermore, τ_{p11} is the minority carrier lifetime and $V_{\mathrm{T}} = kT/q$ is the equivalent thermal voltage, with k being Boltzmann's constant and T the thermodynamic temperature.

This same methodology can also be employed to calculate the hole current ($i_{\mathrm{p0,12}}$) and electron current ($i_{\mathrm{n0,12}}$) at the P_{01} charge point

$$I_{\mathrm{C,PNP}} = A_0 \times \frac{q n_i d_1}{\tau_{\mathrm{p01}}} \left[\exp\left(\frac{V_{\mathrm{Col}}}{V_{\mathrm{T}}} \right) - 1 \right]. \tag{6}$$

The $\mathrm{P}^{+}\mathrm{N}^{-}$ junction model at the IGBT collector describes the recombination current $i_{\mathrm{re,11}}$ in the PIN region

$$i_{\mathrm{re,11}} = I_{\mathrm{C,PIN}} + C_{\mathrm{Col}} \frac{\mathrm{d}V_{\mathrm{Col}}}{\mathrm{d}t} \tag{7}$$

where C_{Col} is the junction capacitance for J_1. The same principle applies to $i_{\mathrm{re,01}}$.

2) Physical Model Located in the Middle of N^- Region: The hole current density between P_{12} and P_{13} can be formulated as

$$i_{\mathrm{p1,23}} = \frac{q_{\mathrm{p12}} - q_{\mathrm{p13}}}{(d_{13} + d_{12}/2)^2} V_{\mathrm{T}} \mu_{\mathrm{p}} + \frac{q_{\mathrm{p13}} V_{1,23}}{(d_{13} + d_{12}/2)^2} \mu_{\mathrm{p}} \tag{8}$$

where $V_{1,23}$ is represented the voltage from P_{12} to P_{13}. In accordance with the electricity-neutral equation, the electron charge can be depicted as follows:

$$q_{\mathrm{n}ij} = q_{\mathrm{p}ij} + Q_{\mathrm{M},ij} \tag{9}$$

where $Q_{\mathrm{M},ij}$ is the normalized majority concentration at point P_{ij} under thermal equilibrium conditions, and $Q_{\mathrm{M},ij} = qAd_iN_{N-}$, with N_{N^-} being the thermal equilibrium electron concentration in the N^- region. The electron current $i_{\mathrm{n1,12}}$ can be depicted as

$$i_{\mathrm{n1,23}} = \frac{q_{\mathrm{p13}} - q_{\mathrm{p12}}}{(d_{13} + d_{12}/2)^2} V_{\mathrm{T}} \mu_{\mathrm{n}} + \frac{(Q_{\mathrm{M13}} + q_{\mathrm{p13}}) V_{1,23}}{(d_{13} + d_{12}/2)^2} \mu_{\mathrm{n}}. \tag{10}$$

The hole and electron currents from P_{02} and P_{03} can be derived in a similar manner.

By integrating the current continuity equation in the direction of the current, the recombination current $i_{\mathrm{re,12}}$ can be deduced as followed:

$$i_{\mathrm{re,12}} = (\gamma_{12} + \gamma_{13}) \frac{q_{\mathrm{p12}} - Q_{\mathrm{m,12}}}{\tau_{\mathrm{p12}}} + \frac{\mathrm{d}(\gamma_{12} + \gamma_{13}) q_{\mathrm{p12}}}{\mathrm{d}t} \tag{11}$$

where $Q_{\mathrm{m},ij}$ is the normalized minority concentration at P_{ij} under thermal equilibrium conditions, and $Q_{\mathrm{m},ij} = qA_in_i^2/N_{\mathrm{N}^-}$. The same principle applies to $i_{\mathrm{re,02}}$ and $i_{\mathrm{re,03}}$.

The current between the PIN and PNP parts can be expressed as

$$i_{\mathrm{con}} = i_{\mathrm{re,03}} + i_{\mathrm{n0,23}}. \tag{12}$$

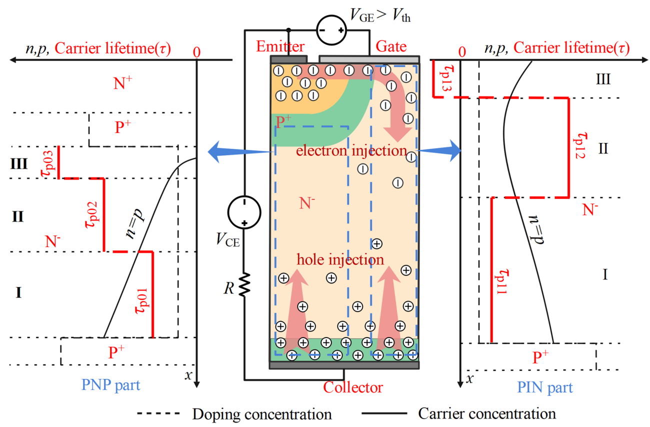

Fig. 3. Charge injection induced changes in minority carrier lifetime.

3) Physical Model Near Emitter and Channel Regions: When the device is activated, a large influx of holes is injected into the base region from the collector, concurrent with the injection of electrons into the base region through channel conduction. Under the principle of electrical neutrality, the carrier lifetime of holes in the N^- region near the collector is low, resulting in substantial hole recombination. Conversely, there is a significant accumulation of holes in the base region near the channel.

As depicted in Fig. 3 for the PIN part of the device, when the device is switched on, the injection of electrons from the emitter and holes from the collector into the N^- region transpires, producing high-level injection as V_{CE} increases. The electron and hole concentrations within the N^- region follow a catenary distribution. In regions I and II of the PIN part, holes move upwards and recombine, with the lifetime of the hole (τ_{p11}, τ_{p12}) being positive. However, in region III, electrons move downwards from the M_1 channel, and to maintain electrical neutrality, $n(x) = p(x)$. Consequently, the hole lifetime in P_{13} can be equated to an effective negative number, written as τ_{p13}, implying that hole generation occurs in the upward direction near the gate.

In contrast, for the PNP part of the device, holes move upwards from the collector, recombine in the N^- base, and are extracted by the negatively biased $\mathrm{P}_{\mathrm{body}}\mathrm{N}^-$ junction, exhibiting an approximately exponential decline in carrier concentration.

The hole's lifetime ($\tau_{\mathrm{p}ij}$) in the physical model is defined as

$$\begin{cases} \tau_{\mathrm{p13}} \geq 0, V_{\mathrm{GS}} \leq V_{\mathrm{th}} \\ \tau_{\mathrm{p13}} < 0, V_{\mathrm{GS}} > V_{\mathrm{th}} \end{cases}. \tag{13}$$

Depending on the presence or absence of a channel, the charge point P_{13} can be expressed as follows:

$$i_{\mathrm{re,13}} = \gamma_{13} \frac{q_{\mathrm{p13}} - Q_{\mathrm{m13}}}{\tau_{\mathrm{p13}}} + \frac{\mathrm{d}\gamma_{13} \cdot q_{\mathrm{p12}}}{\mathrm{d}t} \tag{14}$$

where $\mathrm{V_{th}}$ is the threshold voltage. From Fig. 1, the charge P_{13} can be derived through the continuous network of current as follows:

$$q_{\mathrm{p13}} = C \cdot V = C \times i_{\mathrm{re,13}} \times R \tag{15}$$

where $C = 1$, $R = |\tau_{\text{p13}}|$. Equation (15) can then be simplified to

$$q_{\text{p13}} = i_{\text{re,13}} \times |\tau_{\text{p13}}| . \quad (16)$$

The remaining charge points can be similarly calculated. Subsequently, the lumped-charge concentration was validated using the TCAD results.

C. Physical Model of Junction

In this model, both E_{Col} and E_{Emi} represent P^+N junctions. However, the channel/ N^- (E_{Gat}) functions as an N^+N junction when the device is ON, and it turns into a P^+N^- junction when M_1 is OFF.

In the case of the P^+N^- junction, when it is forward-biased or reverse-biased, it can be conceptualized as the charging and discharging of a parallel plate capacitor. Therefore, a segmented model can be used to describe the characteristics of P^+N^- junctions. As the junction becomes reverse-biased, the width of the depletion region gradually increases, equivalent to an increase in capacitance value. The formula to calculate the depletion region capacitance is as follows:

$$C_j = \frac{\varepsilon_{si}}{W} = A\sqrt{q\varepsilon_{si}N_{N^-}/(2(V_b - V_j))} \quad (17)$$

where V_b represents the built-in potential of the depletion region, and V_j is the reverse voltage applied to the junction. $V_j = V_{\text{Col}}/2$, $V_{\text{Emi}}/2$ and $V_{\text{Gat}}/2$, respectively. The junction capacitances (C_{Col}, C_{Emi}, and C_{Gat}) of the depletion junction (E_{Col}, E_{Emi}, and E_{Gat}) can be obtained from (17). The depletion width W_{Col} of junction E_{Col} can be determined as follows:

$$W_{Col} = \sqrt{\frac{2\varepsilon_{si}}{qN_{N^-}}(V_d - V_{Col})}. \quad (18)$$

The junction voltage V_{Col} can be calculated using the following equation:

$$V_{Col} = \begin{cases} \frac{kT}{q}\ln\left[\frac{q_{p11}N_{N^-}}{n_i^2}\right], V_{GS} \geq V_{th} \\ V_{Col}^* - \left[\frac{q_{p11}-Q_{Col}}{C_{Col}}\right]^2, V_{GS} < V_{th} \end{cases} \quad (19)$$

where $V_{Col}{}^*$ and Q_{Col} are the threshold voltage and charge of the P^+N^- junction when transitioning from forward conduction to reverse blocking, respectively. The same method can be applied to calculate the junction voltages V_{Emi}. The voltage of E_{dep} can be expressed as follows:

$$V_{dep} = \begin{cases} V_{GD} + V_n\left(1 - \sqrt{1 + 1.6V_{GD}/V_n}\right), V_{GD} \geq 0 \\ 0, V_{GD} < 0 \end{cases} \quad (20)$$

where V_n is a normalization factor mainly dependent on the gate-drain overlap area and the doping concentration of the base region.

As depicted in Fig. 4, the channel/N^- junction exists in three states: when V_{GS}-$V_{th} \geq V_{DS}$, the channel is fully conducting and forms an N^+N^- junction; when V_{GS}-$V_{th} < V_{DS}$, the channel starts to pinch OFF, transitioning to a P^+N^- junction; when $V_{GS} < V_{th}$, the channel is completely cut off, resulting in a P^+N^- junction.

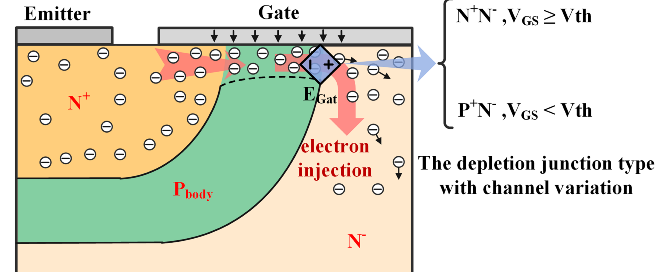

Fig. 4. Channel/N- junction state near the gate.

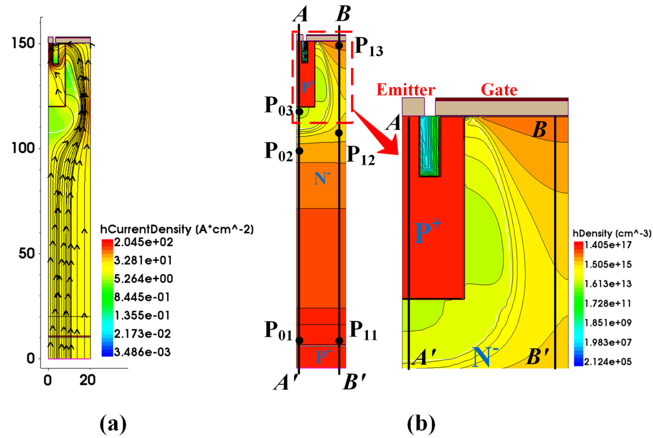

Fig. 5. (a) Current density distribution of the device. (b) Carrier concentration distribution from TCAD simulation.

The voltage of the channel/N^- junction can be expressed as follows:

$$V_{Gat} = \begin{cases} \frac{kT}{q}\ln\left[\frac{q_{p12}N_{N^-}}{n_i^2}\right], (V_{GS} - V_{th} \geq V_{DS}) \\ V_{Gat}^* - \left[\frac{q_{p13}-Q_{Gat}}{C_{Gat}}\right], (V_{GS} - V_{th} < V_{DS}) \\ V_{Emi}^* - \left[\frac{q_{p13}-Q_{Emi}}{C_{Emi}}\right], (V_{GS} < V_{th}) \end{cases} \quad (21)$$

where $V_{Gat}{}^*$ and Q_{Gat} are the threshold voltage and charge in reverse blocking, respectively. The junction model can more accurately describe the trend of a rapid decrease in carrier concentration near the gate when the device is transiently turned OFF.

III. Model Implementation and Validation

The proposed IGBT model was implemented in PSPICE and validated through experimental testing, and its accuracy was compared with Sentaurus TCAD simulations.

A. Simulations and Experiments of Static Characteristics

As shown in Fig. 5, we chose a voltage range of $V_{\text{GE}} = 14$ V and $V_{\text{CE}} = 10$ V to obtain a more significant carrier change curve. Fig. 5(a) illustrates the internal hole current density distribution during the device conduction process. From the graph, it is evident that owing to the presence of the depletion region, the current flows laterally to the channel, resulting in a distinct

TABLE I
PHYSICAL PARAMETERS FOR THE IGBT MODEL

Model parameters description	Value
The area of the chip A (mm^2)	184.96
The area of active region A_{act} (mm^2)	104.04
The width of chip W_C (mm)	13.6
The length of chip W_L (mm)	13.6
The thickness N-base W_B (μm)	142
The radius of a cell W_{cell} (μm)	20
The thickness of Gate oxide T_{ox} (μm)	0.1
the triode region factor K_f	0.95
P-base surface concentration N_C (cm^{-3})	2×10^{17}
Doping of base region N_B (cm^{-3})	9.91×10^{13}
The active area of IGBT N^+ (cm^{-3})	2×10^{19}
P-Emitter concentration N_A (cm^{-3})	1×10^{17}

2-D distribution of current. Fig. 5(b) shows the distribution of the hole concentration in the TCAD simulation. In this scenario, carriers accumulated in the N$^-$ base region and high-level injection occurred. The AA' and BB' lines were positioned in the middle of the PNP part and the PIN part. The Infineon FF1000R17IE4 IGBT-module (1700 V/1000 A) was selected in this study, and contains twelve IGBT chips. The chip's current was determined through the ratio of the chip and cell areas. Using TCAD simulations, we determined the conduction current of a single cell.

Currently, if there are few design parameters or insufficient information for reverse engineering from the device manufacturer, the device model parameters are estimated within a wide margin. The parameter extraction method is typically divided into two steps to extract the parameters of the IGBT. The first step involves evaluating parameters through technical manuals or physical measurements, such as semiconductor device structural parameters and circuit parasitic parameters such as A, W_c. The second step involves optimizing parameter extraction through software and equation [9], [24]. The parameters of the IGBT module are summarized in Table I, and the detailed equations for the calculation of some of the parameters are presented in Table II.

In Table II, V_{BR} is the breakdown voltage value from the manufacturer's datasheet plus about 200 V margin, the E_C is the critical electric field for breakdown corresponding, W_N is the N-base width. K_f the triode region factor, $V_{bi\text{-}pin}$ is the voltage of the equivalent pin. E_g is the bandgap width of the silicon. The source data can be obtained from the manufacturer's datasheet, simple static and dynamic characteristic measurement.

The circuit simulation of the model was implemented in PSPICE with less consideration for hardware conditions, using the same circuit and test conditions. The run time for static characteristics ($V_{GE} = 10$ V, V_{GE} from 0 to 20 V) for the proposed model was 6.01 s, compared to 10.11 s for the traditional model. For dynamic characteristics ($V_{GE} = 900$ V, $I_{GE} = 300$ A, time of 20 μs), the proposed model's run time was 8.43 s, compared to 14.11 s for the traditional model.

Fig. 6(a) and (d) depicts the hole distribution of the PNP part of the IGBT from the proposed model. In these figures, the hole concentration decreases exponentially from the collector (P_{01} point) to the emitter (P_{03} point), and it increases as the temperature increases. Fig. 6(b) and (e) illustrates the hole distribution in the PIN part of the IGBT from the proposed model, showing holes accumulating on both sides of the PIN part. In the middle of the N$^-$ base region, the hole concentration is very low, eventually forming a catenary hole distribution. The proposed model accurately captures the 2-D charge distribution characteristics in the IGBT base region, and aligns well with the TCAD results. Fig. 6(c) and (f) shows the traditional IGBT lumped-charge model [25], which uses four charges (P_{T1}–P_{T4}) to represent the base region carriers. However, compared with the TCAD simulation, some discrepancies exist, especially in the channel region (P_{T4} point).

In Fig. 7, which compared the static I-V curves of the proposed model with the experimental data, traditional *LC* model, and Macro model from Onsemi, the traditional models mentioned later specifically refer to the traditional *LC* model. Fig. 7(a) shows that I_{CE} increases exponentially with the increase of V_{GE}, I_{CE} with I_{CE} at 25 °C exceeding that at 150 °C. The experimental conditions ($V_{CE} = 20$ V) were set based on the data manual provided by the company. The proposed model demonstrates greater accuracy compared to the traditional model at higher gate voltages, with this advantage becoming more pronounced at a temperature of 150 °C. In Fig. 7(b), under different gate voltages, the proposed model exhibits better agreement with the experimental data. This result indicates that the 2-D carrier distribution in the proposed model is more in line with the actual IGBT operation than the 1-D carrier descriptions provided by the traditional model.

When the device experiences latch-up, a current snap-back phenomenon occurs. The static latch-up characteristics of the IGBT is simulated by TCAD, and the current snap-back phenomenon is achieved through current sweeping method.

Fig. 8 shows the comparison between the proposed model, TCAD simulation results, and the traditional model. The proposed 2-D model exhibits a larger PNP and a current snap-back, and the static latch-up characteristic can be observed. The proposed 2-D model effectively represents the device's static latch-up characteristics, compared to the traditional 1-D model.

B. Simulations and Experiments of Dynamic Characteristics

The IGBT module's performance, which includes antiparallel diodes, is significantly influenced by these diodes, especially their reverse recovery current during the turn-OFF process. Fig. 9 depicts the TCAD simulation setup designed to capture the transient response of an IGBT. The simulation circuit takes into account the presence of parasitic components. During the

TABLE II
PARAMETER EXTRACTION PROCESS FOR THE IGBT MODEL

Using Equation	Source Data	Extracting Para
$V_{BR}=E_C W_N+qN_B W_N^2/(2\varepsilon_{si}),E_C=4010N_B^{0.125}$	V_{BR}	W_N
$V_T=2\emptyset_F+K_S/K_o\cdot t_{OX}(4qN_A\emptyset_F/K_S\varepsilon_o)^{1/2}$, $\emptyset_F=kT/q\cdot\ln(N_A/n_i)$	V_T	N_A for P well
$V_{DS}-V_{bi-pin}=(V_{GS}-V_T)/K_f$	$I_C(V_{GE},V_{CE})$	K_f
$N_B=[60\cdot(E_g/1.1)^{3/2}/V_{BR}]^{4/3}\cdot 10^{16}$	E_g	N_B
Surveying/Manufacturer's datasheet	On/off Test	A, W_C and T_{ox}, V_{BR} et al

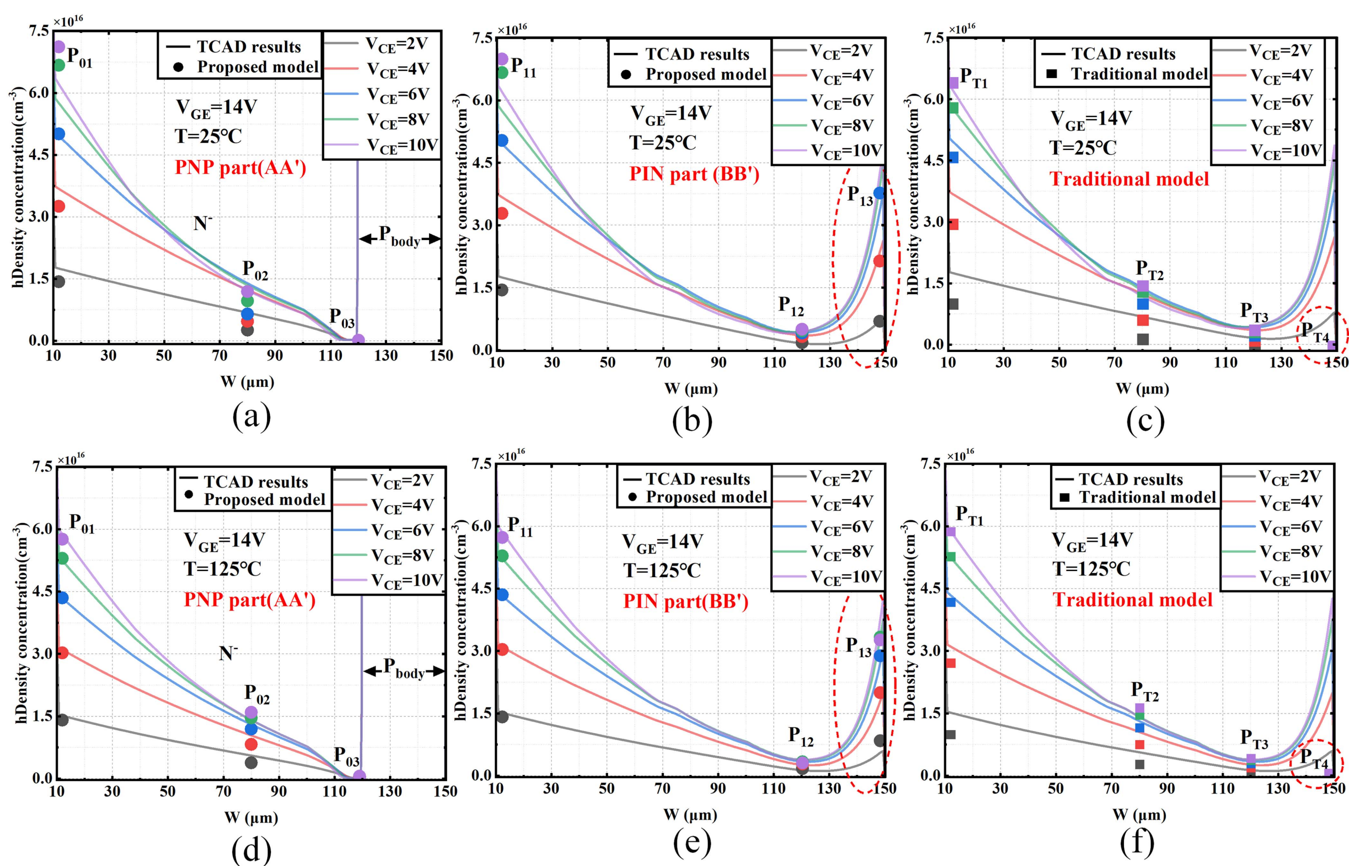

Fig. 6. Static hole distribution in base region: (a) in PNP part of IGBT at 25 °C from proposed model, (b) in PIN part of IGBT at 25 °C from proposed model, (c) in IGBT at 25 °C from traditional model, (d) in PNP part of IGBT at 125 °C from proposed model, (e) in PIN part of IGBT at 125 °C from proposed model, and (f) in IGBT at 125 °C from traditional model.

turn-ON phase, the current flowing through the IGBT is referred to as I_{CE}.

Taking into account the influence of parasitic resistances and capacitances in the actual test circuit, an appropriate gate drive circuit was selected. The gate drive method was estimated by [26] to avoid the short circuit. When the gate turns OFF, the gate capacitance discharges, leading to the extraction of the hole injection from the base region toward the P_{body} region and emitter. This results in the reestablishment of a reverse-biased P^+N^- junction at the interface between the channel and N^- region. The carriers near the channel rapidly recombine, forming a space-charge layer that progressively extends toward the collector electrode. As this space-charge layer moves toward the collector, carriers are removed from the base region, resulting in the formation of a trailing current. Fig. 10 illustrates the variation in carrier concentration in the IGBT's N^- region when the device is turned OFF at 14.50 μs. Fig. 10(a) and (d) displays the hole distribution in the PNP part of the IGBT under different V_{CE} conditions, while Fig. 10(b) and (c) depict the hole distribution in the PIN part where the proposed model is applied. The proposed model accurately represents the dynamic response of the 2-D carrier distribution. Upon device turn-OFF, the hole concentration declines rapidly, and the channel disappears.

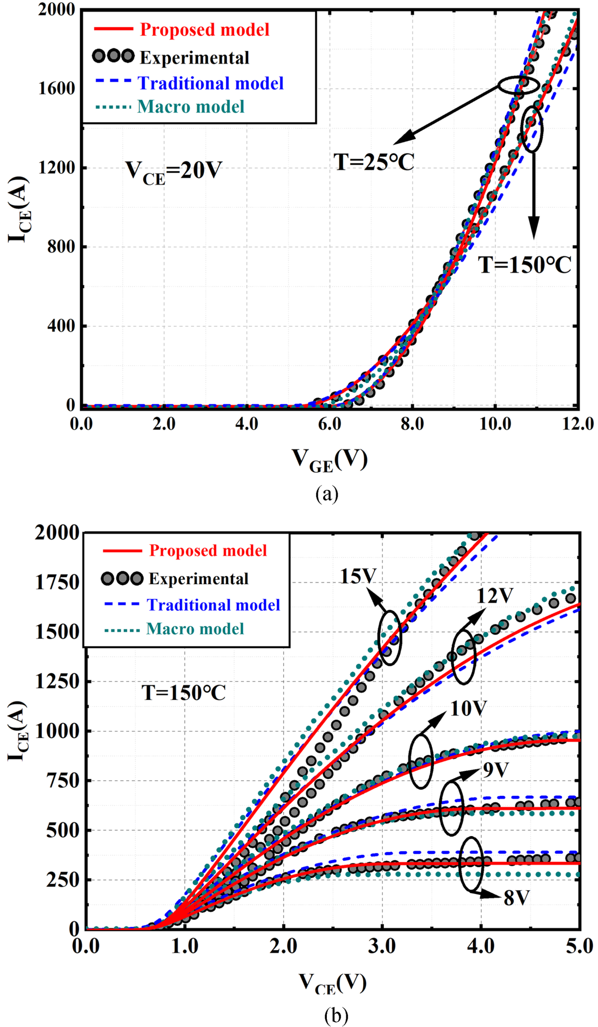

Fig. 7. Direct current characteristics: (a) transfer curve and (b) output curve.

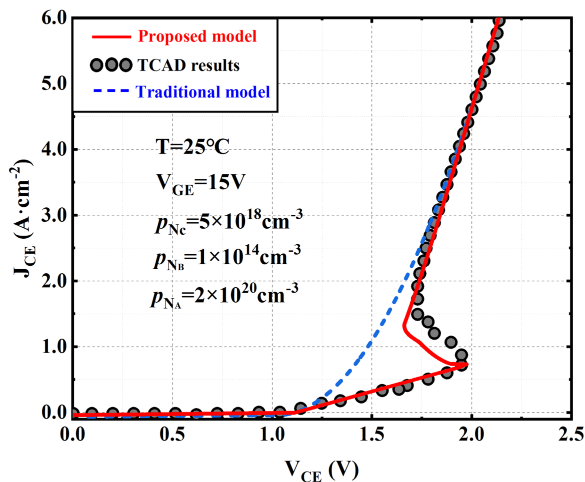

Fig. 8. IGBT static latch-up characteristic.

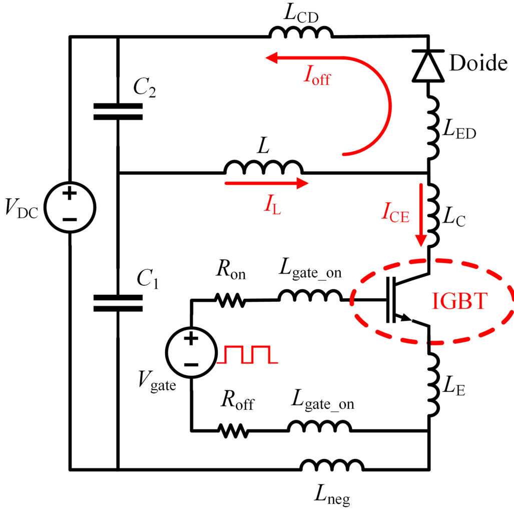

Fig. 9. Chopper cell circuit with clamped inductive load for TCAD simulations and experiment; snubber: $C_1 = C_2 = 3.7$ mF; primary stray inductance: $L_C = 12$ nH; diode inductance: $L_{ED} = L_{CD} = 5$ nH; emitter kelvin inductance: $L_E = 2.87$ nH, $L_{neg} = 8$ nH; gate resistance and inductance: $R_{OFF} = 1.64$, $R_{ON} = 0.9$, $L_{gate_ON} = L_{gate_OFF} = 30$ nH; the gate voltage: $V_{gate} = +14$ V/-5 V.

In contrast, the traditional model [as seen in Fig. 10(c) and (f)] exhibit only an exponential decline in hole concentration distribution, with a markedly higher concentration drop rate that does not align well with the TCAD simulation results. The proposed model incorporates the effects of the carrier lifetime on J_3 to enhance the model's accuracy during switching operations.

Fig. 11(a)–(c) depicts the turn-OFF characteristics of an IGBT module for varying I_{CE} at 25 °C with a V_{CE} of 900 V. Meanwhile, Fig. 10(d)–(f) represents the IGBT at 125 °C with a V_{CE} of 1200 V for different I_{CE}. When the device is turned OFF, I_{CE} decreases rapidly, and V_{CE} exhibits overshoot before stabilizing. The peak of the overshoot increases with an increment in the I_{CE}. The proposed model, accounting for the variation in the N^-/P_{body} junction, precisely represents the spatial charge distribution in the N^- base region during device conduction. This, in turn, enhances the model's accuracy during turn-OFF transients under various temperatures, V_{CE}, and I_{CE}, a feature more pronounced in the turn-OFF current compared to the traditional model.

Fig. 12(a)–(c) illustrates the turn-ON process of the IGBT for different I_{CE} with V_{CE} of 900 V, and V_{CE} in Fig. 11(d)–(f) is 1200 V. During the turn-ON transient, the collector voltage V_{CE} declines rapidly. The collector current I_{CE} overshoots, and its value increases with an increase in V_{CE} for the same I_{CE}. The proposed model demonstrates excellent accuracy for the slopes of the voltage and current variations, which are mainly associated with the carrier distribution in the device.

Fig. 13 illustrates a comparison of power dissipation waveforms. The proposed model exhibits a more accurate representation of tail current, closely matching the experimental curve during the turn-OFF process. The power consumption during device switching transients and errors is presented in Table III.

In Table III, I_{CE} represents the conduction current, I_{oc} is the peak current during the turn-ON transient, and T_{OFF} and T_{ON} are the turn-OFF and turn-ON times of the IGBT module, respectively. When applying the model, it is important to accurately predict the power wastage, peak current, and rates during turn-ON and turn-OFF.

Fig. 10. Transient hole concentration distribution during turn-OFF process: (a), (b), (d), and (e) PNP and PIN part of IGBT with 200 V and 500 V of V_{CE} from the proposed model, (c) and (f) in IGBT with 200 V and 500 V of V_{CE} from the traditional model.

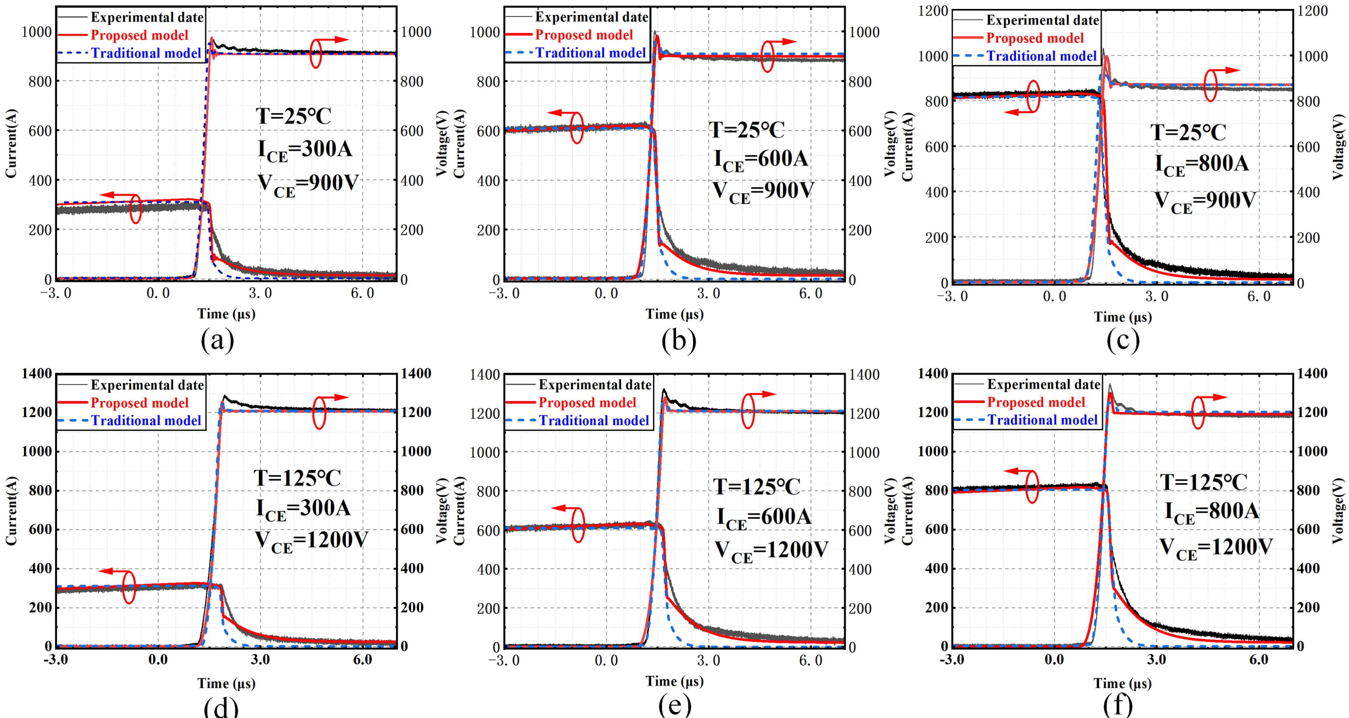

Fig. 11. Turn-OFF transient waveforms of IGBT with (a) $V_{CE} = 900$ V, $I_{CE} = 300$ A, T = 25 °C. (b) $V_{CE} = 900$ V, $I_{CE} = 600$ A, T = 25 °C. (c) $V_{CE} = 900$ V, $I_{CE} = 800$ A, T = 25 °C. (d) $V_{CE} = 1200$ V, $I_{CE} = 300$ A, T = 125 °C. (e) $V_{CE} = 1200$ V, $I_{CE} = 600$ A, T = 125 °C. (f) $V_{CE} = 1200$ V, $I_{CE} = 800$ A, T = 125 °C.

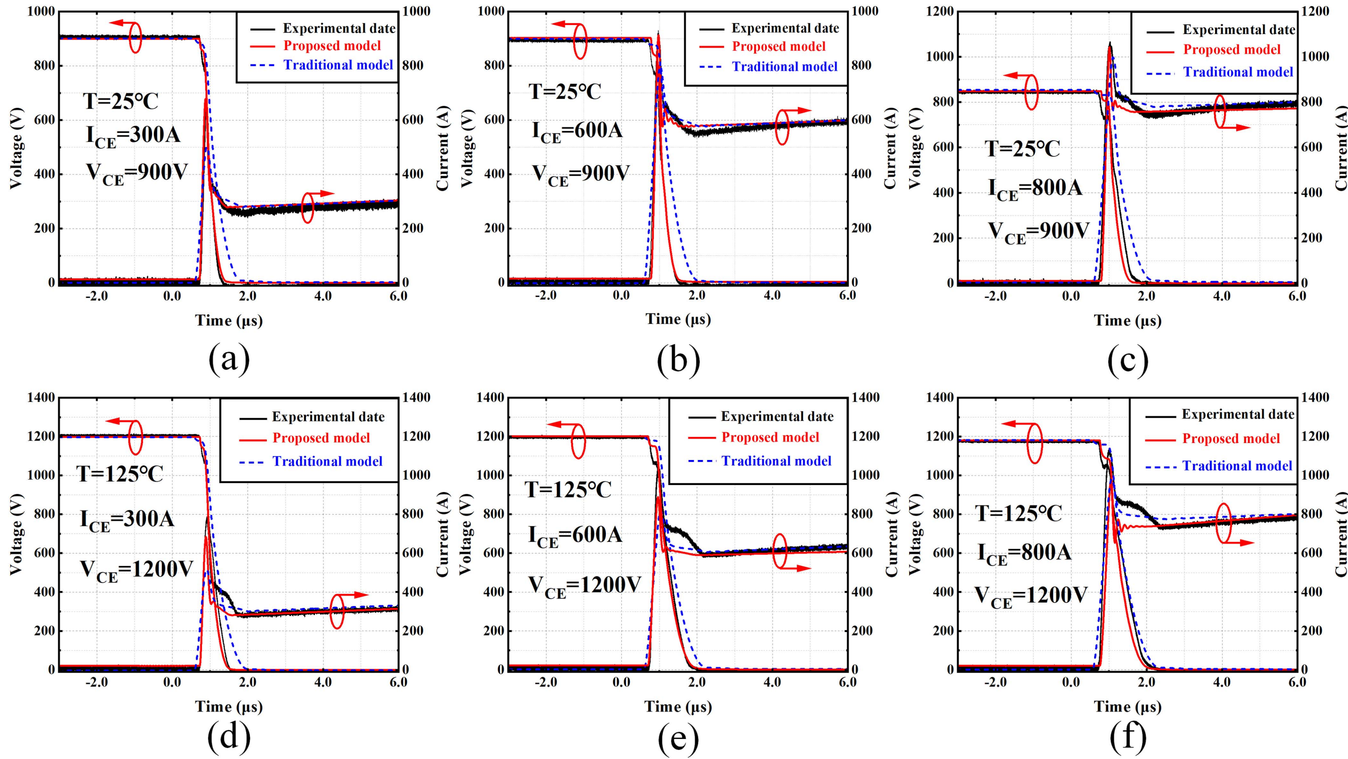

Fig. 12. Turn-ON transient waveforms with (a) $V_{CE} = 900$ V, $I_{CE} = 300$ A, T = 25 °C. (b) $V_{CE} = 900$ V, $I_{CE} = 600$ A, T = 25 °C. (c) $V_{CE} = 900$ V, $I_{CE} = 800$ A, T = 25 °C. (d) $V_{CE} = 1200$ V, $I_{CE} = 300$ A, T = 125 °C; (e) $V_{CE} = 1200$ V, $I_{CE} = 600$ A, T = 125 °C. (f) $V_{CE} = 1200$ V, $I_{CE} = 800$ A, T = 125 °C.

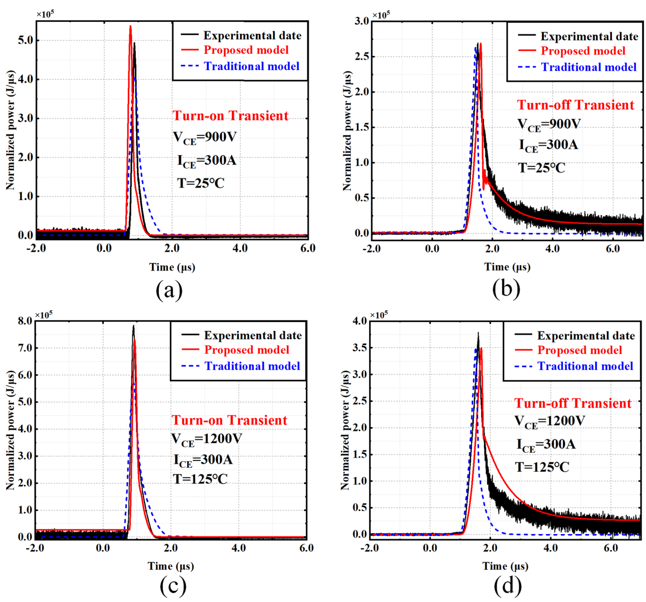

Fig. 13. (a) and (c) are instantaneous power dissipation at turn-ON. (b) and (d) are instantaneous power dissipation at turn-OFF.

TABLE III
COMPARISON BETWEEN THE MEASURED AND SIMULATED TRANSIENT CHARACTERISTICS OF IGBT

Model/Experiment		Experiment	Proposed model	Error1	Traditional model	Error2
Turn-off transient						
25 °C V_{CE}=900 V I=300 A	I_{CE}	293.779 A	317.919 A	8.21%	308.866 A	5.13%
	E_{off}	0.15495 J	0.13226 J	14.64%	0.0814 J	47.47%
	T_{off}	2.867 μs	2.832 μs	1.22%	1.811 μs	36.81%
125 °C V_{CE}=1200 V I=300 A	I_{CE}	283.79 A	297.779 A	4.92%	308.918 A	8.85%
	E_{off}	0.27052 J	0.29656 J	9.62%	0.1225 J	54.72%
	T_{off}	4.6 μs	4.37 μs	5.00%	4.1 μs	10.86%
Turn-on transient						
25 °C V_{CE}=900 V I=300 A	I_{oc}	676.530 A	661.723 A	2.18%	500.266 A	26.05%
	E_{on}	0.08893 J	0.10316 J	16.00%	0.13322 J	49.80%
	T_{on}	1.372 μs	1.469 μs	7.07%	1.902 μs	27.86%
125 °C V_{CE}=1200 V I=300 A	I_{oc}	779.778 A	686.464 A	11.96%	511.432 A	34.41%
	E_{on}	0.19598 J	0.15809 J	19.33%	0.24019 J	22.56%
	T_{on}	1.464 μs	1.4186 μs	3.10%	1.958 μs	33.74%

From these comparative results, the traditional models were insufficient to accurately describe the changes in turn-OFF tail current and conduction voltage, primarily because they neglect the internal carrier distribution. Under turn-OFF transient conditions, the traditional model is constrained by limitations in the calculation of tail current, where the maximum error is manifested in the turn-OFF tail current with an error value of 54.72%. In contrast, the proposed model maintains errors within 15% or less. To predict switching rates, the traditional model consistently exhibits errors of over 10%, whereas the maximum error of the new model in the prediction of switching rates is capped at 7%. From these comparisons, it can be concluded that the proposed model has a more excellent performance in terms of power wastage, but there still remain some discrepancies, the reason for the error was more in the measurement and extraction

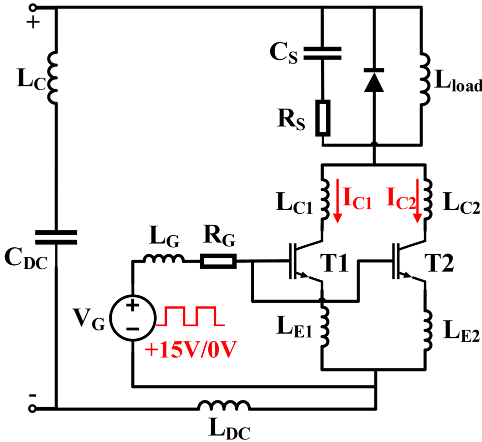

Fig. 14. Schematic diagram of unbalanced stay parameters with paralleled IGBTs: the load inductance L_{load} = 50 μH, C_S = 200 pF, R_S = 100 Ω, $L_{C1} = L_{C2}$ = 2 nH, L_{E1} = 18 nH, L_{E2} = 28 nH, busbar stray inductors L_{dc} = 82.3 nH, DC capacitor stray inductor L_C = 126.2 nH, R_G = 10 Ω, L_G = 6 nH.

error for the parameters such as the gate length and width inside the device, as well as the gap between the model and the actual device doping method and other process parameters.

C. Parallel Current Modeling of Discrete Devices

In this model, a parallel test platform was constructed for IGBTs, and the Infineon IKW40N65ET7 650 V/40 A was chosen to be tested for unbalanced currents. As a discrete device, the IKW40N65ET7 is capable of passing transient currents up to 120 A and has a 12.25 mm^2 IGBT chip area and 9.92 mm^2 active area.

As shown in Fig. 14, a 10 nH inductor at the emitter of device T2 to increase the emitter-stage inductance difference, which results in unbalanced current flow when the devices are connected in parallel [27], [28]. Both L_{dc} and L_C can be extracted using the equations in the Appendix. The result obtained from the experiment is shown in Fig. 15, where the behavior model is the model provided by Infineon.

In Fig. 15(a) depicts the current variation with different parallel inductances, while Fig. 15(b) illustrates the current variation with different resistances. By analyzing the current curves in Fig. 15(a), for dynamic currents, the side with the smaller emitter inductance has a larger current overshoot at turn-ON. At turn-OFF, the other side will carry more current and turn OFF slower. When the device is ON, I_{C1} and I_{C2} have an unbalanced current, and it then gradually tends to balance. Compared with experimental data, the largest difference is in the current I_{C2}, where the greatest error of the behavior model current is 12.02%, and the greatest error of the proposed model is 6.27%. For the time of the device T2 turn-OFF, the error is 73.83% for the behavior model and 17.32% for the proposed model. From this, owing to an error in the extraction of the circuit stray inductance, the proposed model still has a specific error with the experimental data, but from a general perspective, the proposed model can more completely describes the current change of the device parallel connection.

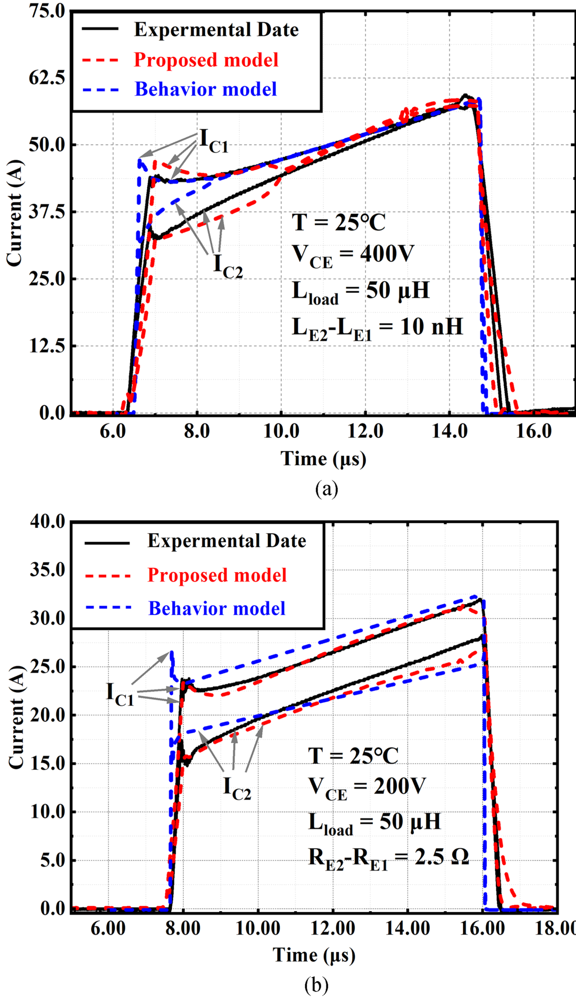

Fig. 15. Comparison of parallel current (a) different inductances (b) different resistances.

IV. Conclusion

This study introduced a physical model for IGBT that considers the 2-D charge distribution in the base region, splitting the IGBT into two primary components: PNP and PIN parts. By introducing the concept of negative carrier lifetime, this model effectively illustrated the accumulation of holes near the gate, based on the principle of electric neutralization, and the parasitic effects of the device were efficiently predicted by the 2-D charge distribution. Additionally, the model acknowledged the existence of N^+N^- junctions between the channel and the base region and took into consideration the impact of temperature on the characteristics of the device. These features were integrated to present a more accurate depiction of the IGBT's dynamic behavior and temperature dependence. The model's accuracy was corroborated through comparisons with TCAD simulation results. Consequently, this model can more precisely describe the static and switching transient behaviors of the device under different temperature conditions, as confirmed by tests conducted on the 1700 V/1000 A IGBT module and the discrete device IKW40N650ET7.

APPENDIX

Intrinsic carrier concentration

$$n_i^2(T) = N_c N_v \left(\frac{T}{300}\right)^3 e^{-\frac{E_g}{kT}}$$

where N_c represents the effective density of states in the conduction band, N_v represents the effective density of states in the valence band, and E_g represents the bandgap of silicon

$$E_g = 1.17 - 4.73e^{-4}T$$

$$n_i = n_{i0} \times \left(\frac{T}{300}\right)^{1.5} e^{\frac{1}{2\times(9.0663+0.269T^2)}}$$

where n_{i0} represents the intrinsic carrier concentration of Si at T = 300 K.

Transconductance parameter

$$K_{pm} = K_p(T_{emp})(T/T_{emp})^{-0.8}$$

where K_p denotes the transconductance at normal atmospheric temperature, T_{emp} is the room temperature.

Threshold voltage of IGBT

$$V_{th}(T) = -0.0064 \times (T - T_{emp}) + V_{th}(T_{emp}).$$

The busbar stray inductors

$$L_{\text{dc}} = \frac{\int_{t_1}^{t_2} (v_{\text{dc}} - v_{\text{diode}} - v_{CE})dt}{i_C(t_2) - i_C(t_1)}$$

where v_{dc} is the dc capacitor voltage, v_{diode} is the diode voltage, v_{CE} is the device under test voltage, t_1 and t_2 are to be measured for the IGBT conduction start time and the diode into reverse recovery of the voltage at its ends to the lowest point of time.

The dc capacitor stray inductor

$$LS = \frac{\int_{t_1}^{t_2} (v_{\text{in}} - v_{\text{diode}} - v_{CE})dt}{i_C(t_2) - i_C(t_1)}$$

where v_{in} is the standard input voltage.

The internal stray inductance of device

$$L_M = \frac{\int_{t_1}^{t_2} v_{\text{diode}}dt}{i_C(t_2) - i_C(t_1)}.$$

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