Inertia Emulation in Droop-Based DC Microgrids With Equivalent Converter Impedance Reshaping

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***Abstract*—With the high penetration of renewable energy sources, the inertia of microgrids has declined. In dc microgrids, the lack of inertia leads to bus voltage fluctuations, which may threaten system stability. To mitigate this issue, virtual inertia can be provided by energy storage units via emulating the inertial properties akin to virtual dc motors. Although the fast voltage change can be restrained, the principle of virtual inertia remains elusive and there is no suitable implementation for V-I droop. With these considerations, in this article, the voltage regulation issue is analysed from an impedance perspective, and it is revealed as transient current sharing between the dc-link capacitor and equivalent converter impedance. On this basis, an inertia emulation strategy is proposed based on capacitor current regulation and droop gain modification. With the proposed strategy, the equivalent converter impedance is reshaped in the medium-frequency range to absorb the transient current, and the capacitor current is suppressed. Consequently, the virtual inertia is provided to improve voltage regulation. Remarkably, in the proposed strategy, no additional control loops or measurement is required, and it seamlessly integrates with existing V-I droop control methods. Then, the proposed inertia emulation is validated with hardware-in-loop and experimental test results.**

***Index Terms*—DC microgrids, droop control, dynamic voltage response, impedance reshaping, inertia emulation.**

I. Introduction

MICROGRIDS have drawn more and more attention to integrating various renewable energy sources (RESs), e.g., photovoltaic (PV) arrays and wind turbines (WTs), coping with global energy crisis [1]. On the other hand, RESs are interfaced into microgrids via inertia-less power electronic converters. Compared with conventional power systems, the inertia of microgrids is therefore almost eliminated [2]. Consequently, the frequency in ac microgrids and voltage in dc microgrids and their rate of change may exceed the nominal ranges, causing damage to equipment and threatening the operation safety of power systems [3]. To address the abovementioned issue, inertia emulation is introduced for the control of microgrids.

Note that, inertia can be in the mathematical and physical sense. The concept of inertia here refers to the latter. Generally speaking, inertia is a transient characteristic that relies on energy storage units (ESUs), such as motor rotors, batteries, and supercapacitors, to release/absorb energy when there is an imbalance between source and load power. Fortunately, due to the intermittent power generation from RESs, ESUs are consistently available in microgrids for peak shaving. In dc microgrids, bus voltage fluctuations are caused by sudden changes in load or source powers. Virtual inertia is deployed to suppress its oscillations and rate of change of voltage (RoCoV), thereby enhancing dynamic response. In existing strategies, inertia emulation in dc microgrids is mainly implemented based on virtual synchronous generators (VSGs), virtual impedance and dc electric springs.

Similar to ac microgrids, VSG loops are exploited for inertia emulation in dc microgrids. For ESUs in voltage mode, VSG loops can be inserted both in the inner voltage loop [4], [5], [6], [7], [8], [9], and as an outer loop of voltage regulation loops [10], [11], [12]. In [4], [5], and [6], a VSG path, which mimics the completed swing equation of synchronous generators, is inserted between the outer voltage loop and inner current loop in the controller of dc–dc converters. A single voltage loop is designed in [7], which is followed by an inner VSG path. In strategies in [4], [5], [6], and [7], numerous additional virtual variables, e.g., frequency, torque, and power, are introduced, complicating design and implementation. To simplify the controller structure, the virtual dc machine control in [8] eliminates the requirement of calculating torques. However, extra droop loops are still required for parallel DGUs. To solve this problem, the virtual dc machine armature resistance in [9] is adaptively regulated to adjust the state of charge (SoC) balancing rate for multiple battery modules. In [10], [11], and [12], the VSG path is moved outside of the voltage loop. In [10], it is integrated with I-V droop, and a supercapacitor is deployed for high-frequency inertia emulation, which, however, requires extra hardware devices. The outer VSG loop [11] is introduced in the grid-tied converter controller, and is modified as a fractional-order transfer function in [12]. Although virtual inertia is provided with grid-tied converters, the transient active power transmitted to the ac side will also disturb grid frequency in ac microgrids. Besides, the VSG is introduced in current-source converters in [13], it requires that

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at least one other distributed generation unit (DGU) operates in voltage mode.

Another solution to inertia emulation in dc microgrids is based on virtual impedance, which is equivalent to reshaping the output impedance of DGUs, and is mainly implemented in three ways. The first one is virtual capacitors [14], [15], [16], [17]. The virtual capacitor loop in [14] is followed by voltage loops, and its current reference is generated with an outer I-V droop loop. The dynamic response of this method is improved in [15] with two output current feedforwards, but the gains rely on converter parameters and operating points. A virtual capacitor control is proposed in [16] to mitigate dc voltage fluctuations in modular multilevel converters-based dc systems, but the dynamic power required is from the ac side. In [17], a virtual capacitor is parallel with virtual resistance in the droop loop to compensate for surge current, it alternately operates with the SoC regulation loop, but the mode switch degrades system reliability. The second implementation is droop gains modification [18], [19], [20], [21], [22]. The V-I droop gain is modified as a transfer function in [18] to eliminate voltage overshoot during load change transient, and it is further studied to simplify as a low-pass filter (LPF) in [19]. However, the voltage change is still rapid, revealing insufficient inertia. A similar solution is proposed in [20], but its steady-state and dynamic performances are coupled with each other and the design of LPF is unclear. It is proved in [21] that the dynamic response of the I-V droop is faster than that of the V-I droop, and the droop gain in this article is modified as resistive–capacitive impedance, but the detailed implementation is not mentioned. The droop coefficient in [22] is adaptively regulated based on RoCoV, which is equivalent to an adaptive parallel virtual resistance and capacitance, but the calculation of capacitor voltage derivative is sensitive to sampling noises. Besides, inertia emulation can be realized with the reconfiguration of inner loops [23], [24]. The proportional gain in the current regulator in [23] is adaptively adjusted based on the current error. In [24], a capacitor current controller, following the inductor current regulator, is inserted, which is equivalent to simultaneously changing the proportional and integral gains in the inductor current regulator. However, in [23] and [24], inertia emulation is coupled with current regulators, which may lead to the tradeoff between system stability and bus voltage dynamic response.

DC electric springs are also effective for bus voltage stabilization and power balance in dc microgrids [25]. They are serially connected with noncritical loads as smart loads on the demand side to realize/absorb transient power [26], [27]. However, dedicated power converters and control algorithms are required, which complicates system structure.

Although existing strategies can provide virtual inertia, the principle of how virtual inertia impacts voltage regulation performance is still unclear, which makes systematic mechanism analysis on voltage oscillation an urgent need for control algorithm design and parameter selection. Besides, in existing methods, virtual inertia is mainly implemented based on I-V droop, how to achieve inertia emulation compatible with V-I droop is still challenging. In this article, the voltage regulation issue is analysed from an impedance perspective. The converter impedance is divided into two parts: the dc-link capacitor and the rest, which is called equivalent converter impedance in this article. Then, the inertia issue is transferred as the transient current sharing between the dc-link capacitor and equivalent converter impedance, and it is concluded that the inertia emulation can be realized by suppressing the dc-link capacitor, with equivalent converter impedance reshaping. On this basis, the capacitor current regulation and droop coefficient modification are implemented to provide virtual inertia in dc microgrids. In the proposed strategy, no extra control loop is introduced, it is easily compatible with the V-I droop control method. Besides, compared with existing solutions, this strategy further improves dynamic voltage response.

The rest of this article is organized as follows. In Section II, the concept of equivalent converter impedance is introduced, and the voltage regulation performance is analyzed in terms of transient current sharing between equivalent converter impedance and dc-link capacitor. In Section III, the proposed equivalent converter impedance reshaping strategy is illustrated for inertia emulation. Then, the hardware-in-loop (HIL) and experimental test results are presented in Sections IV and V to validate the effectiveness of the proposed strategy. Finally, Section VI concludes this article.

II. Equivalent Converter Impedance and Inertia Emulation in DC Microgrids

In dc microgrids, multiple DGUs are parallelly connected to form bus voltage and supply loads. Among them, RESs (e.g., PV and WT) always operate as power sources to track the maximum power points, they are nondispatchable. Meanwhile, ESUs, e.g., batteries, are always connected to dc microgrids via bidirectional power converters for peak shaving and voltage regulation [28]. ESUs' powers are determined by the source-load power balance in microgrids, therefore they can be exploited to provide virtual inertia, preventing bus voltage from sudden change. For parallel ESUs, droop control is always utilized for power sharing between them.

A. Equivalent Converter Impedance

First, a single ESU is studied, and it is interfaced with a power electronic converter. With reasonable voltage controller design, its output characteristic can be equivalent with the series of a controlled voltage source v_e and an $Z_o(s)$ in the voltage loop bandwidth, as shown in Fig. 1(a). Besides, a dc-link capacitor is always placed on the output side, and its energy generation/absorption reveals the change in dc voltage. Therefore, to highlight the impact of output current on capacitor voltage, as depicted in Fig. 1(b), $Z_o(s)$ is divided into two parallel parts: dc-link capacitor impedance $Z_C(s) = 1/sC_f$ and the rest part $Z_{ec}(s)$, which is defined as equivalent converter impedance in this article. Therefore

$$\frac{1}{Z_o(s)} = \frac{1}{Z_C(s)} + \frac{1}{Z_{ec}(s)}. \tag{1}$$

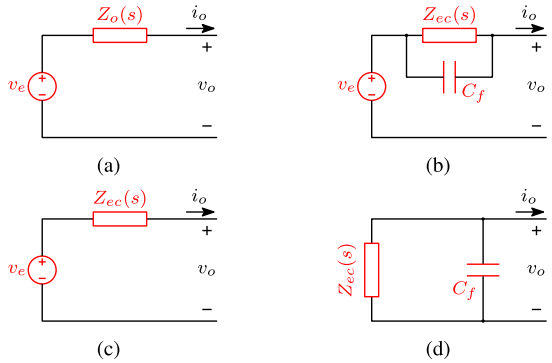

Fig. 1. Output Characteristic of ESUs. (a) Equivalent output characteristic, and (b) dividing $Z_o(s)$ into parallel connection of Z_{ec} and Z_C, (c) equivalent model for DC component ($s \to 0$), and (d) equivalent model for AC components.

Based on (1), $Z_{ec}(s)$ can be calculated as

$$Z_{ec}(s) = \frac{Z_o(s)Z_C(s)}{Z_C(s) - Z_o(s)}. \tag{2}$$

In steady state, $s \to 0$, except switching-frequency ripples, only dc components are involved in output voltage and current, and the dc-link capacitor is open-circuit ($Z_C(j0) \to \infty$). Therefore, the output impedance is dominated by $Z_{ec}(s)$, as presented in Fig. 1(c). During transient, disturbance current from the load side can be modelled as a current source, and ac components in a wide frequency range exist in the output current of ESUs. At those frequencies, the voltage reference is zero, the equivalent model for ac components, as depicted in Fig. 1(d), is the parallel connection of $Z_{ec}(s)$ and $Z_C(s)$. With this model, dynamic voltage response can be revealed.

B. Transient Current Sharing Between $Z_{ec}(s)$ and $Z_C(s)$

As analyzed previously, disturbance current during transients flows to $Z_{ec}(s)$ and $Z_C(s)$. The equivalent converter current i_{ec} and capacitor current i_C is determined with the relative relationship between Z_{ec} and Z_C as

$$\begin{cases} i_{ec} - i_C = i_o \\ i_{ec}Z_{ec}(s) + i_C Z_C(s) = 0. \end{cases} \tag{3}$$

Therefore, the capacitor current can be expressed as

$$i_C = -\frac{1}{1 + \dfrac{Z_C(s)}{Z_{ec}(s)}} \cdot i_o. \tag{4}$$

Furthermore, based on the inherent physical characteristic, dc-link capacitor current is

$$i_C = -C_f \frac{dv_o}{dt}. \tag{5}$$

It is revealed in (5) that, the magnitude of i_C is proportional to dc-link capacitor RoCoV. During transients, the larger i_C is, the faster v_o changes. Thus, i_C can be exploited as an indicator to reflect voltage regulation performance. Besides, to impede capacitor RoCoV, the current flow through the capacitor should

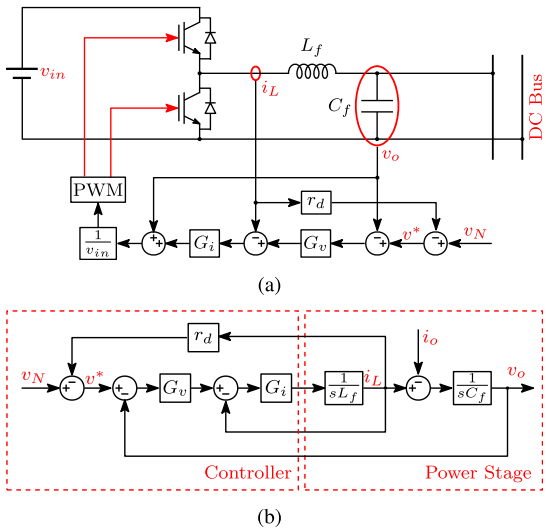

Fig. 2. ESU interfaced with buck converter. (a) V-I droop-controlled buck converter and (b) linearized block diagram of (a).

be hindered. Inspired by current distribution in hybrid energy storage systems, the equivalent converter impedance and dc-link capacitor can be regarded as two units. To retard voltage change can be regarded as minimizing the impact of disturbance current on i_C by generating/absorbing transient power with converter equivalent impedance. That is, the voltage regulation is actually transient current sharing between them: the converter can be exploited as a buffer to shave transient current flow through the dc-link capacitor. Based on (3), enlarging the ratio between $Z_C(s)$ to $Z_{ec}(s)$ can realize this target, providing virtual inertia to improve voltage regulation performance. Generally, the filter parameters, L_f and C_f, are selected in the power converter hardware design stage, it is almost constant in operation. Therefore, the only degree of freedom is the equivalent converter impedance. Based on this principle, an inertia emulation strategy based on equivalent impedance reshaping is proposed in this article.

III. Inertia Emulation Based on Equivalent Impedance Reshaping

As analyzed in the last section, the key to inertia emulation is suppressing dc-link capacitor current with reshaping equivalent converter impedance at medium frequency. In this section, the implementation of equivalent impedance reshaping is illustrated in detail.

Without loss of generality, an ESU interfaced with bidirectional buck converter in Fig. 2(a) is studied, inductor current i_L and capacitor voltage v_o are regulated with a proportional gain $G_i(s) = k_{p,i}$ proportional– controller $G_v(s) = k_{p,v} + k_{i,v}/s$, respectively, and an inductor-current-based V-I droop loop (gain is r_d) is followed by inner loops. The bandwidths of the current loop and voltage loop are $f_{c,i} = 3\,\text{kHz}$ and $f_{c,v} = 1\,\text{kHz}$, respectively.

Based on Fig. 2(b), the closed-loop current and voltage gains $G_{i,\mathrm{cl}}(s)$ and $G_{v,\mathrm{cl}}(s)$ are expressed as

$$\begin{cases} G_{i,\mathrm{cl}}(s) = \dfrac{T_i(s)}{1+T_i(s)} \\ G_{v,\mathrm{cl}}(s) = \dfrac{T_v(s)}{1+T_d(s)+T_v(s)} \end{cases} \tag{6}$$

where $T_i(s)$ and $T_v(s)$ are the current-loop and voltage-loop gains, respectively, and $T_d(s)$ is loop gain introduced by r_d, they are

$$\begin{cases} T_i(s) = G_i(s)\dfrac{1}{sL_f} \\ T_d(s) = r_d G_v(s) G_{i,\mathrm{cl}}(s) \\ T_v(s) = G_v(s) G_{i,\mathrm{cl}}(s)\dfrac{1}{sC_f} \end{cases}$$

where L_f and C_f are filter inductor and capacitor, respectively.

Furthermore, the output impedance with V-I droop loop is

$$Z_{o,d}(s) = \frac{\dfrac{1}{sC_f}(1+T_d(s))}{1+T_d(s)+T_v(s)}. \tag{7}$$

Based on (6), (7) can be rewritten as

$$Z_{o,d}(s) = \frac{1}{sC_f + \dfrac{G_v(s)G_{i,\mathrm{cl}}(s)}{1+Z_d(s)G_v(s)G_{i,\mathrm{cl}}(s)}}. \tag{8}$$

Consequently, the output characteristic of ESUs is

$$v_o = v_N \cdot G_{v,cl}(s) - i_o \cdot Z_{o,d}(s) \tag{9}$$

where v_N is nominal dc-bus voltage, i_o is output current.

Substituting (8) into (2), the equivalent converter impedance with droop loop is obtained as

$$Z_{ec,d}(s) = Z_{ec,0}(s) + Z_d(s) \tag{10}$$

where $Z_{ec,0} = 1/G_v(s)G_{i,\mathrm{cl}}(s)$ is the equivalent converter impedance without droop loop, and $Z_d(s) = r_d$.

It is revealed in (10) that, there are two parts involved in $Z_{ec,d}(s)$, both $Z_{ec,0}(s)$ and $Z_d(s)$ can be reshaping for inertia emulation. In this article, two measures are exploited for them, respectively: 1) changing the feedback of current loop from inductor current to capacitor current to eliminate the impact of $Z_{ec,0}(s)$ at medium frequency, and 2) modifying the droop gain $Z_d(s)$ from virtual resistance r_d to parallel connection of virtual resistance and capacitor, decoupling steady-state and transient performance, and reducing total equivalent converter impedance at medium frequency. The principle and impact of the abovementioned two measures are illustrated as follows.

A. Original Equivalent Converter Impedance Reshaping With Capacitor Current Regulation

For voltage–current dual loop, $G_{i,cl}(j\omega) \approx 1\angle 0$ in the voltage loop bandwidth. Therefore, it can be simplified as $Z_{ec,0}(j\omega) = 1/G_v(j\omega)$. A direct solution can be modifying voltage regulator parameters for equivalent converter impedance

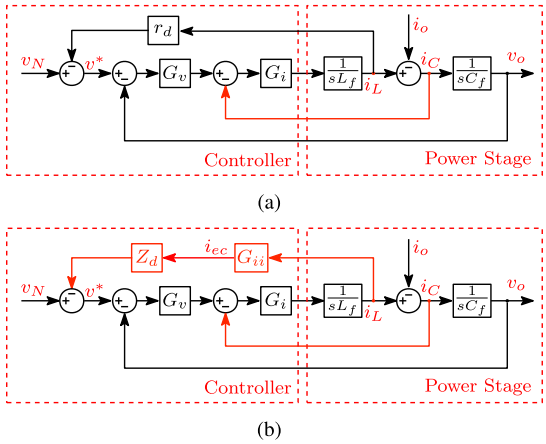

Fig. 3. Control block diagram (a) with capacitor current regulation and (b) with both capacitor current regulation and droop gain modification.

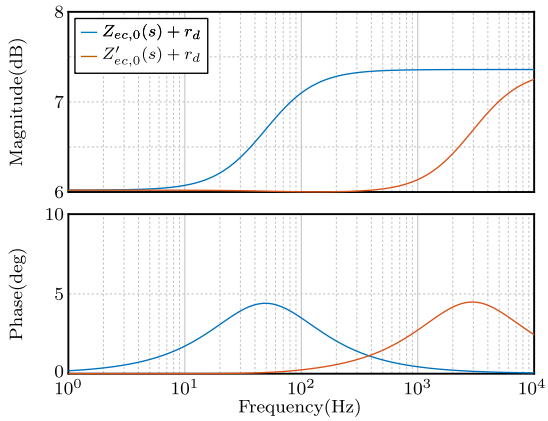

Fig. 4. Bode diagrams of equivalent converter impedance with (a) inductor current regulation and (b) capacitor current regulation ($r_d = 2\,\Omega$).

reshaping, e.g., decreasing $k_{p,v}$ and $k_{i,v}$. But it meanwhile reduces the bandwidth of the voltage loop, which may degrade the effect of the controller in the medium-frequency range, and system stability is also reduced. To avoid this problem, in this article, $G_v(s)$ is designed based on the desired phase margin and bandwidth, and the original equivalent converter impedance reshaping is implemented by replacing the feedback of the current loop as capacitor current. The modified control block diagram is presented in Fig. 3(a). Compared with Fig. 2(b), the closed-loop voltage gain are not changed, thus the voltage regulation is not impacted. Meanwhile, the equivalent converter impedance without a droop loop is modified as

$$Z'_{ec,0}(s) = Z_{ec,0}(s) \cdot \frac{1}{1+T_i(s)}. \tag{11}$$

From the comparison between (11) and (10), it is revealed that an extra gain $1/(1+T_i(s))$ is introduced with capacitor current regulation. For $f < f_{c,i}$, the magnitude of $T_i(j2\pi f)$ is much larger than 1, thus $Z'_{ec,0}(s)$ is much smaller than $Z_{ec,0}(s)$. As a result, the original equivalent converter impedance is drastically suppressed and the equivalent converter impedance is then reduced in the medium frequency range, as depicted in Fig. 4.

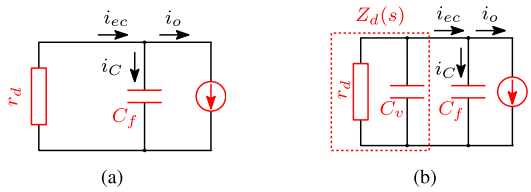

Fig. 5. Simplified Output Characteristic of ESUs (a) with r_d as droop gain and (b) with $Z_d(s)$ as droop gain.

B. Droop Gain Modification With Resistive-Capacitive Virtual Impedances

With capacitor current regulation, the equivalent converter impedance is therefore dominated by r_d in low and medium frequency. Consequently, the equivalent model in Fig. 1(d) can be simplified as that in Fig. 5(a). In steady states, r_d achieves current sharing between ESUs. However, since r_d keeps the same value in all frequency ranges, the equivalent converter impedance in medium frequency is also enlarged, which hinders transient current flow through the equivalent converter impedance. Thus, the medium-frequency characteristic of $Z_d(s)$ is modified, which is realized by parallelly connecting a virtual capacitor C_v with r_d for inertia emulation. Therefore, the equivalent model of ESUs can be further changed as Fig. 5(b). Then, the droop gain is corrected as

$$Z_d(s) = \frac{1}{\frac{1}{r_d} + sC_v} = \frac{r_d}{sC_v r_d + 1}. \tag{12}$$

The bode diagram of $Z_d(s)$ in (12) is plotted in Fig. 6. As depicted in Fig. 6(a), its low-frequency characteristic is mainly determined by r_d as resistive. With growing r_d, the low-frequency impedance is also increased, but the impedance at medium and high frequency is hardly influenced. Also, as seen in Fig. 6(b), C_v dominates medium and high-frequency range characteristics to be capacitive, which sharply reduces impedance magnitude at this frequency range. Furthermore, the larger C_v, the lower the impedance at medium and high frequency. Meanwhile, the low-frequency characteristic of $Z_d(s)$ is not changed. Therefore, with $Z_d(s)$ in (12), the steady-state and dynamic performances are decoupled with each other.

Please note that, $Z_d(s)$ in (12) is merely effective in buck converter. To improve the feasibility of the proposed strategy, as depicted in Fig. 3(b), a transfer function $G_{ii}(s)$ is inserted in the droop path to indicate the relationship from inductor current i_L to equivalent converter current i_{ec}, and it is determined with converter structure. In buck converter $G_{ii}(s) = 1$, and in boost converter $G_{ii}(s) = 1 - D$. Consequently, the droop gain is modified as $G_{ii}(s) \cdot Z_d(s)$. Without loss of generality, $G_{ii}(s) = 1$ is considered in the following analysis.

C. Impact of Capacitor Current Regulation and Droop Gain Modification on Equivalent Converter Impedance

To highlight the impact of the introduced two measures, the equivalent converter impedances in different cases are compared, and their bode diagrams are depicted in Fig. 7. Apparently, with droop gain r_d, the equivalent converter impedance is

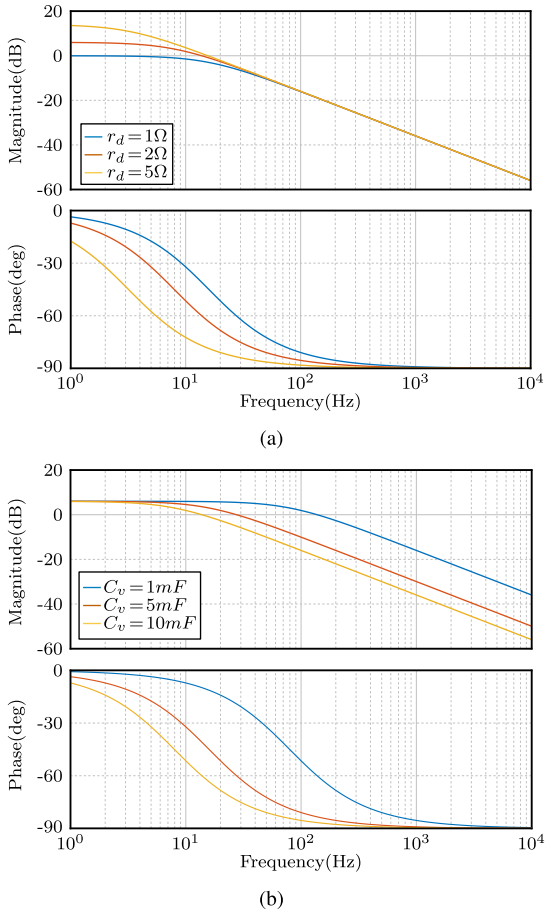

Fig. 6. Bode diagrams of $Z_d(s)$ (a) with different r_d ($C_v = 10mF$) and (b) with different C_v ($r_d = 2\,\Omega$).

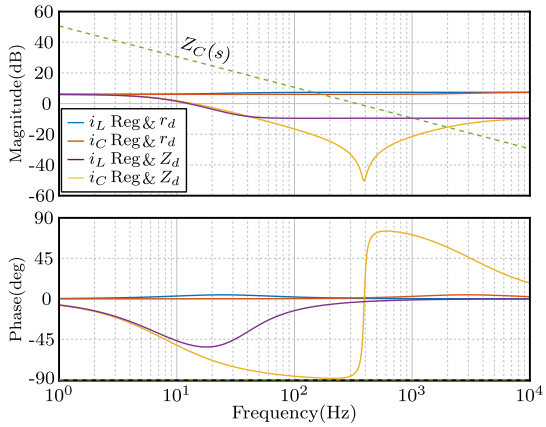

Fig. 7. Bode diagrams comparison of equivalent converter impedances.

smaller than $Z_c(s)$ in the low-frequency range, but is larger than $Z_c(s)$ in the medium-frequency range, the transient current will flow into dc-link capacitor and lead to sharp voltage fluctuation. When $Z_d(s)$ in (12) is introduced, the equivalent converter impedance as low-frequency range is not influenced but the magnitude at medium-frequency range is suppressed. Besides, with capacitor current regulation, equivalent converter impedance at medium-frequency range is further reduced. Compared with $Z_c(s)$, $Z_{ec}(s)$ with both i_C regulation and $Z_d(s)$ droop is much

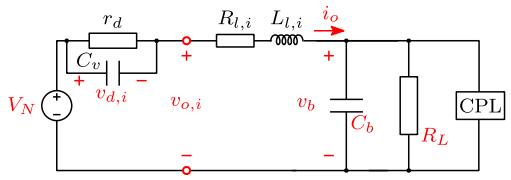

Fig. 8. Equivalent model of the DC microgrid for large-signal stability.

smaller. Consequently, i_C will be drastically restrained, and sufficient virtual inertia is provided by ESUs. Meanwhile, at all frequencies, the impedance angle of the equivalent converter impedance is always during $(-90°, 90°)$ in ESUs, based on the passivity theory, the stability of the power system can be ensured [29].

D. Large-Signal Stability Analysis

For comprehensive stability analysis, as depicted in Fig. 8, dc capacitors C_b connected to the common bus, line impedance ($R_{l,i}$ and $L_{l,i}$), resistive loads R_L and constant-power loads (CPLs, power is P_{cpl}) are involved in the system model.

On this basis, the transient control model of ith ESU is expressed as

$$\begin{cases} \dfrac{dv_{d,i}}{dt} = \dfrac{i_{o,i}}{C_v} - \dfrac{v_{d,i}}{r_d C_v} \\ \dfrac{di_{o,i}}{dt} = \dfrac{V_N - v_{d,i} - v_b}{L_{l,i}} - \dfrac{R_{l,i}}{L_{l,i}} \cdot i_{o,i} \\ \dfrac{dv_b}{dt} = \dfrac{i_{o,i}}{C_b} - \dfrac{v_b}{R_L C_b} - \dfrac{P_{\text{cpl}}}{v_b C_b}. \end{cases} \tag{13}$$

Based on (13), selecting $\mathbf{x} = [v_{d,i}, i_{o,i}, v_b]^T$ as state variables. Then, Jacobian matrix of system at the equilibrium point $\mathbf{x}_e = [V_{d,i}, I_{o,i}, V_b]^T$ is fetched as

$$\mathbf{J} = \begin{bmatrix} -\dfrac{1}{r_d C_v} & \dfrac{1}{C_v} & 0 \\ -\dfrac{1}{L_{l,i}} & -\dfrac{R_{l,i}}{L_{l,i}} & -\dfrac{1}{L_{l,i}} \\ 0 & \dfrac{1}{C_b} & \dfrac{P_{cpl}}{V_b^2 C_b} - \dfrac{1}{R_L C_b} \end{bmatrix}. \tag{14}$$

To guarantee the system large-signal stability, all the eigenvalues of matrix $\mathbf{J}$ must have negative real parts [30], [31], which can be ensured with the following condition:

$$tr(\mathbf{J}) < 0 \tag{15}$$

which is equivalent to

$$P_{\text{cpl}} < V_b^2 C_b \frac{L_{l,i} + R_{l,i} r_d C_v}{r_d C_v L_{l,i}} + \frac{V_b^2}{R_L} = P_{\text{cpl,max}} \tag{16}$$

where $P_{\text{cpl,max}}$ is the maximum allowable CPL power.

In dc microgrids, the line impedances are always dominated by $R_{l,i}$. Besides, to realize the desired current sharing performance, r_d is always much larger than $R_{l,i}$. Meanwhile, a large C_v is selected to improve dynamic voltage response. That is, $L_{l,i} \ll R_{l,i} r_d C_v$, and (16) can be rewritten as

$$P_{\text{cpl}} < \frac{V_b^2 C_b R_{l,i}}{L_{l,i}} + \frac{V_b^2}{R_L} \approx P_{\text{cpl,max}}. \tag{17}$$

It is inferred from (17) that, the parameters r_d and C_v introduced in droop gain hardly impact the large-signal stability of the power system. When the condition in (17) is satisfied, the system stability can be ensured, which relies on the original power system structure, the detailed parameter selection process can be found in [30] and [31].

E. Selection of r_d and C_v

The selection of r_d should consider two requirements. First, to ensure current sharing performance between ESUs, r_d should be much larger than the line impedances of ESUs. Meanwhile, too large r_d will generate an undesired voltage excursion. Based on these two concerns, r_d is selected based on the maximum allowable dc voltage deviation $\Delta v_{\max}$ caused by the magnitude of the maximum output current $i_{o,\max}$ as [32]

$$r_d = \frac{\Delta v_{\max}}{i_{o,\max}}. \tag{18}$$

Then, with the proposed strategy, the output impedance of each ESU is modified as

$$Z_{o,d}(s) = Z_d(s) // Z_C(s) = \frac{r_d}{s\left(C_v + C_f\right) r_d + 1}. \tag{19}$$

In (19), the time constant of DGU can fetched as $T = (C_v + C_f) r_d$. Based on classical control theory, the settling time T_{es} is an transient performance index, and the system reaches 99.3% of the final step-change value in $T_{es} = 5T$. On this basis, the virtual capacitor can be determined as

$$C_v = \frac{T_{es}}{5 r_d} - C_f. \tag{20}$$

In general cases, to provide sufficient virtual inertia, C_v is much larger than C_f. C_v in (20) can be therefore selected as

$$C_v \approx \frac{T_{es}}{5 r_d}. \tag{21}$$

Note that, with the selected r_d and C_v, the difference between output voltages of ESUs and bus voltage would be small. Although only the output voltage of each ESU is regulated, the steady-state and dynamic response of bus voltage can also be ensured.

IV. HIL Test Results

In this section, the effectiveness of the proposed strategy is validated with HIL test results. As depicted in Fig. 9, circuit models are established in PLECS and then operated in RT Box 1, and controllers are implemented with DSP TMS320F28379D LaunchPad. System parameters are listed in Table I. First, the test on a single buck converter is conducted to study the impact of r_d and C_v, and prove the effect of the proposed method with common dc-bus capacitors. Then, the tests on a dc microgrid are

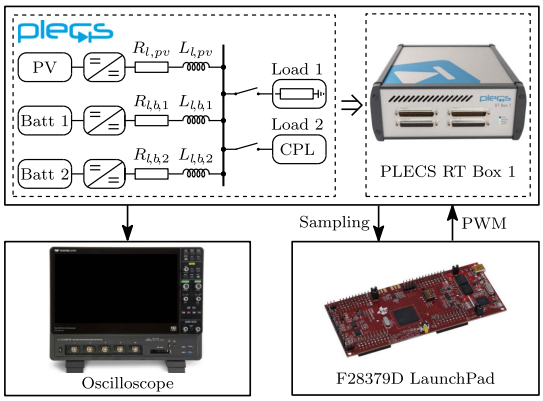

Fig. 9. HIL test platform of a PV-battery-based microgrid.

TABLE I
SYSTEM PARAMETERS IN PV-BATTERY-BASED MICROGRID

Parameters	Symbols	Values
Battery voltage	V_{bat}	380 V
PV open-circuit voltage	V_{pv}	400 V
Rated bus voltage	$V_{N,b}$	200 V
Switching frequency	f_{sw}	20 kHz
Filter inductance	L_f	0.5 mH
Filter capacitance	C_f	470 μF
Line impedances	$R_{l,\text{pv}}$ / $L_{l,\text{pv}}$	0.12 Ω / 120 μH
	$R_{l,b,1}$ / $L_{l,b,1}$	0.1 Ω / 100 μH
	$R_{l,b,2}$ / $L_{l,b,2}$	0.2 Ω / 200 μH

TABLE II
SIMULATION RESULTS WITH DIFFERENT r_d AND C_v

	Same r_d			Same C_v			Same T_{es}		
r_d (Ω)	1.0			0.4	0.8	1.6	0.5	1.0	2.0
C_v (F)	0.05	0.1	0.25		0.1		0.2	0.1	0.05
T^*_{es} (s)	0.25	0.50	1.25	0.20	0.40	0.80		0.50	
T_{es} (s)	0.25	0.48	1.22	0.20	0.39	0.78	0.49	0.48	0.48
V_o (V) #	195.1	195.1	195.1	198.0	196.1	192.2	197.5	195.1	190.5

The steady-state output voltage before the first transient.

implemented to further present the feasibility of the proposed solution.

A. Tests of Impacts of r_d and C_v

In this test, three buck converters operate independently at the same time. For each converter, a 40 Ω resistive load is supplied in the beginning, and another 40 Ω resistive load is connected, and then disconnected. r_d and C_v are set as different values to reveal their impacts, the results are depicted in Table II and Figs. 10 to 12, where T^*_{es} and T_{es} are theoretical and practical settling times, respectively.

1) Same r_d and Different C_v: As revealed in Fig. 10, with the same r_d, the steady-state operating point in each test is the same. Meanwhile, with increasing C_v, seen from both load increase and decrease transients, the settling time of the voltage regulation dynamic is proportionally increased.

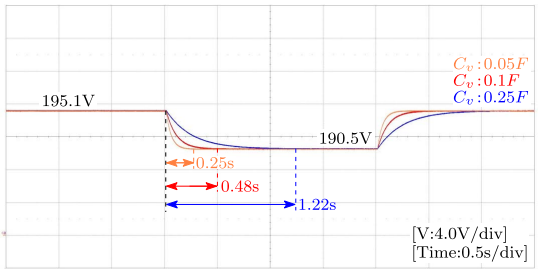

Fig. 10. HIL test results on a buck converter for the same r_d (1.0 Ω) and different C_v.

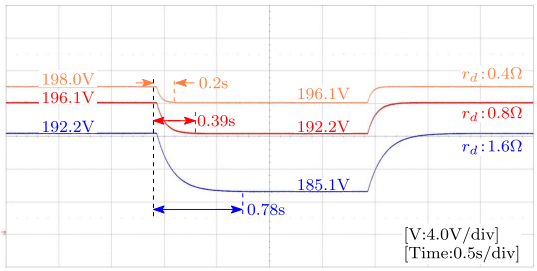

Fig. 11. HIL test results on a buck converter for the same C_v (0.1 F) and different r_d.

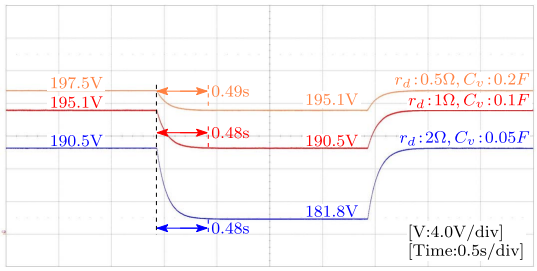

Fig. 12. HIL test results on a buck converter for the same settling time (0.50 s).

2) Same C_v and Different r_d: When C_v is constant and r_d is varied, as presented in Fig. 11, first, the steady–steady operating point of each converter is also changed, the voltage drop is proportional to r_d. Furthermore, during transients, T_{es} is proportionally changed as well.

3) Same T^*_{es}: If the desired settling time is given, as shown in Fig. 12, r_d and C_v are inversely proportional to each other. Meanwhile, since r_d is different in each scenario, its increase generates a proportionally growing steady-state voltage drop.

In summary, with the proposed strategy, the steady-state operating point of ESUs is determined by r_d, and the dynamic voltage response relies on both r_d and C_v. Notably, the simulation results and settling times in all three cases are consistent with the theoretical analysis in Section III.

B. Tests on a Single Buck Converter With Bus Capacitors

In this case, a single buck converter is involved, and a large capacitor $C_b = 3$ mF is connected to the common dc bus. It is set as $r_d = 1\ \Omega$ and $C_v = 0.25$ F, and test results are depicted in Fig. 13. It is inferred from the comparison that, the steady-state bus voltages in each operating point are the same. Furthermore, the bus voltage settling times without and with C_v are 1.22

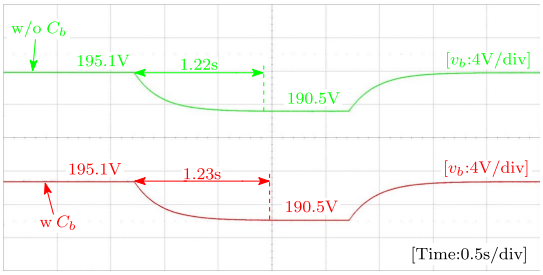

Fig. 13. HIL test results on a buck converter with bus capacitors.

and 1.23 s, respectively, they are also almost the same. In this condition, the proposed strategy is still effective.

C. Tests in a PV-Battery-Based DC Microgrid

In this test, the studied dc microgrid prototype is as presented in Fig. 9, where a PV module and two battery modules are parallelly connected via dc–dc converters. In the following tests, the PV module operates in maximum power point track mode to maximize its output power, and two battery modules are in voltage mode to form bus voltage. Besides, the modified droop gains are introduced in battery modules for power sharing. In the following conditions, $r_d = 2\ \Omega$ and $C_v = 0.05\ F$, that is, the desired settling time is 0.5 s. The proposed strategy is tested in the conditions where resistive and CPLs are supplied, respectively.

1) Resistive-Load Condition: At first, a 40 Ω resistive load is supplied, and then another the same load is connected and disconnected. During the whole process, the desired PV power is kept constant. In this condition, the proposed strategy is compared with V-I droop and the method in [15], and the test results are depicted in Figs. 14 and 15. In the steady state, the operating points of ESUs with three methods are almost the same. However, the dynamic voltage responses are different. With V-I droop control, the transient voltage fluctuates suddenly during load change transients and an overshoot is also observed, exposing poor system inertia. Consequently, as revealed in Fig. 15, a drastic PV power fluctuation exists during load change transients. On the contrary, both the strategies in [15] and in this article are effective to provide virtual inertia, retarding bus voltage fluctuation and suppressing PV power spikes. Meanwhile, it is also seen from Fig. 15 that, with the method in [15] it takes about 19 ms to track the desired voltage trajectory, the dynamic voltage response is still sluggish. With the proposed strategy, this duration is reduced to less than 1 ms, the dynamic voltage response is further improved with the proposed strategy, and PV power fluctuations are consequently restrained by about 51% and 45% during load increase and decrease transients, respectively. Remarkably, the test results during load increase and decrease transient are similar to each other, the settling times match the expected value.

2) CPL Condition: In this condition, the proposed method is tested with load demand change and PV power change transients, the test results are shown in Fig. 16.

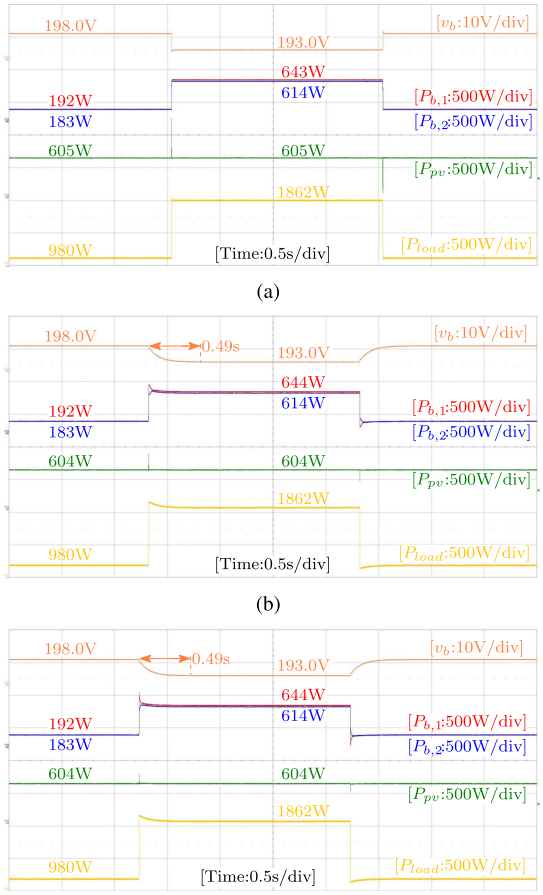

Fig. 14. HIL test results in a DC microgrid in resistive-load conditions. Bus voltage, and PV, ESUs and load powers (a) with V-I droop, (b) with method in [15], and (c) with the proposed method.

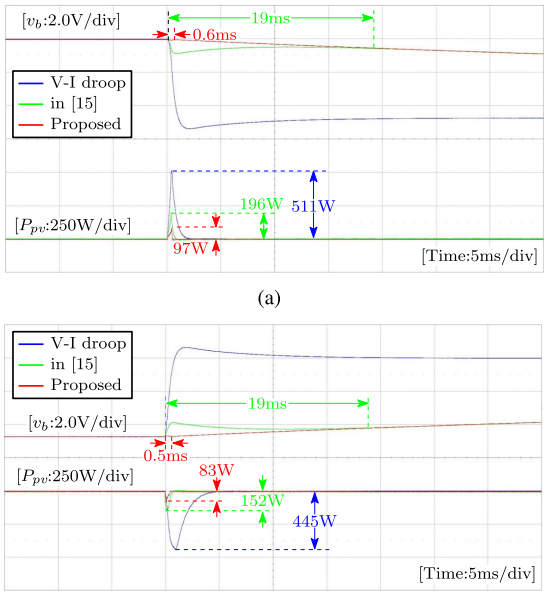

Fig. 15. Comparative HIL test results in a DC microgrid in resistive-load conditions. Bus voltage and PV power during (a) load increase transient and (b) load decrease transient.

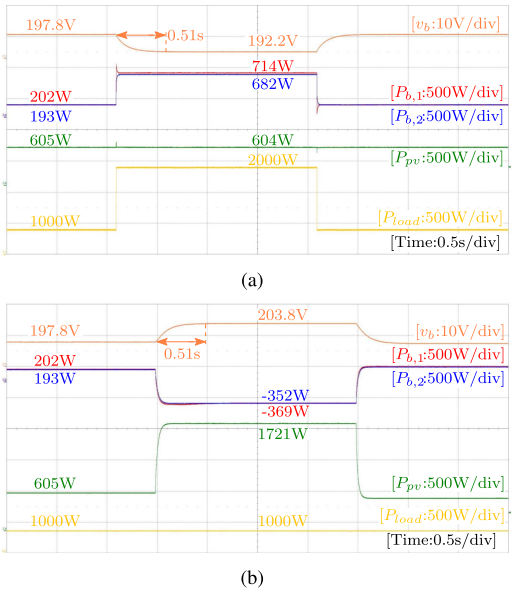

Fig. 16. HIL test results in DC microgrid in CPL conditions. (a) Load demand change and (b) PV power change transients.

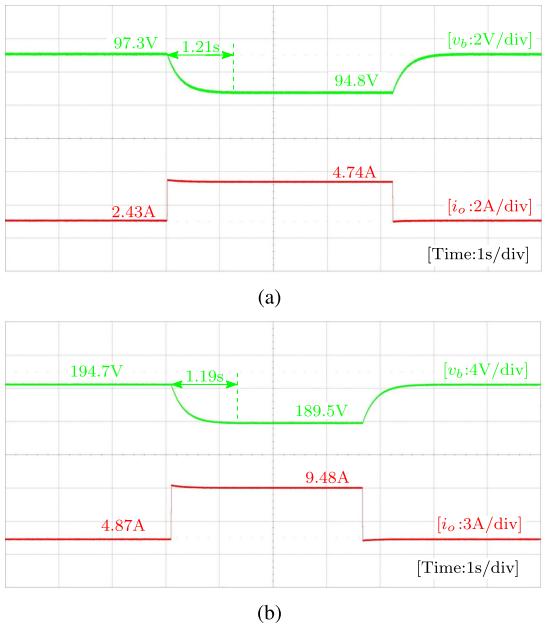

Fig. 17. Experimental test results on converters. (a) Buck converter and (b) boost converter.

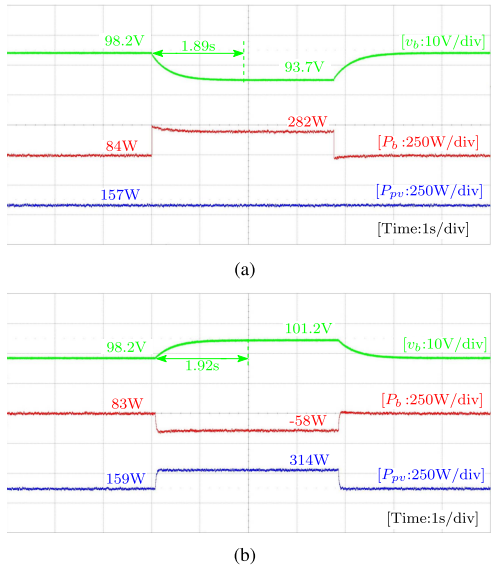

Fig. 18. Experimental test results in a PV-battery-based dc microgrid. (a) Load demand change and (b) PV power change transients.

First, the test with load change transients is conducted. A 1 kW CPL is supplied in the beginning, and the same load is parallelly connected and then disconnected. PV power reference remains all the time. As seen in Fig. 16(a), during both transients, bus voltage changes slowly, the settling times are 0.51 s, they are in accordance with the desired value. Besides, PV power fluctuations during these two transients are also suppressed to 81 W and 80 W, respectively.

Then, the load demand keeps as 1 kW, PV power reference is varied. As shown In Fig. 16(b), PV power is insufficient to serve the load, both ESUs are discharging in the beginning. Then, PV power is surplus after the increase at t_3, ESUs are therefore charging. After t_4, PV power is smaller than load power again, discharging ESUs to fill the gap. During both transients, bus voltage gradually changes, and the settling times are both 0.51 s, they agree with the desired value.

It is also revealed in all tests that, from the perspective of ESUs, the effects of the PV module power change and load change transients on parallel ESUs are similar, they both can be regarded as power demand changes.

V. Experimental Test Results

To further prove the feasibility of the proposed strategy, experimental tests on a hardware platform are conducted.

A. Experimental Test on a Single Converter

In this condition, the proposed strategy is tested on a single buck and boost converter, respectively, and both load demand increase and decrease transients are considered. In each test, $r_d = 1\ \Omega$ and $C_v = 0.25$ F, thus $T_{es}^* = 1.25$ s.

1) Test on a Single Buck Converter: In this test, the input and output voltages of the buck converter are set as 200 and 100 V, respectively. From Fig. 17(a), it can be seen that bus voltage during both transients changes smoothly, and the settling time is consistent with the desired value.

2) Test on a Single Boost Converter: The input and output voltages of the boost converter are set as 100 and 200 V, respectively, in this test. It can be seen from Fig. 17(b) that, during both load increase and decrease transients, bus voltage changes smoothly, and the settling time is consistent with the desired value as well.

B. Experimental Test on a PV-Battery-Based DC Microgrid

In this test, a dc microgrid prototype is built, where a PV module and battery module are involved and they both are

interfaced with buck converters, and resistive loads are supplied. Both the battery input voltage and open-circuit voltage of the PV module are 200 V. The nominal dc-bus voltage is 100 V. $r_d = 2\ \Omega$ and $C_v = 0.2$ F, then the desired bus voltage settling time is 2.0 s.

1) Load Demand Change: In this case, both the load demand increase and decrease events occur, and the test results are presented in Fig. 18(a). It is revealed that during both transients, bus voltage changes smoothly, and the settling time is about 1.89 s, which agrees with its desired value. Besides, there are no apparent PV power fluctuations.

2) PV Power Change: In this case, solar irradiance is changed to increase and decrease PV output power, respectively, the test results are shown in Fig. 18(b). It can be seen that, bus voltage changes smoothly during both transients, and the settling times are consistent with the desired values.

VI. Conclusion

In this article, the voltage regulation issue in dc microgrids is illustrated from an impedance perspective, as transient current sharing between dc-link capacitor and equivalent converter impedance. It is revealed that virtual inertia can be provided by suppressing dc-link capacitor current with reshaping equivalent converter impedance in the medium-frequency range. On this basis, the inertia emulation is realized based on both capacitor current regulation and droop gain modification. The proposed strategy requires neither extra control loops nor measurement, and is simple to be compatible with V-I droop control. Its effectiveness is validated with HIL and experimental test results.

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