Improved Packaging of Power Module With Low-Permittivity Material for Low Common-Mode Noise and High Reliability

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***Abstract*—This article proposes a novel power module configuration which replaces a part of the bottom copper layer of a direct-bonded copper by low-permittivity (low-ε) epoxy. The proposed power module reduced common-mode (CM) capacitance by 52.5% compared to that of the conventional counterpart. The CM noise measured from line impedance stabilization network was reduced by 4–5 dBμV in steady-state operation. The proposed power module does not sacrifice thermal performance which is proved by simulation and thermal resistance measurement. Thermal cycling tests confirmed high mechanical reliability with no cracks in the solder near the epoxy region. Less mechanical deformation of 5.80 μm was observed compared to the 9.48 μm of the power module that adopts air instead of low-ε epoxy.**

***Index Terms*—Common-mode (CM) noise, high reliability, low-permittivity material, parasitic capacitance, power module design.**

I. Introduction

SILICON carbide (SiC) devices provide higher switching frequency compared with their silicon counterpart [1], [2] and improve power density and efficiency of power conversion systems. However, high *dv/dt* and *di/dt* of SiC devices generate considerable electromagnetic interference, such as conducted common-mode (CM) noise, which requires careful designs to minimize parasitic inductance and capacitance.

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Several power module designs have been introduced to attenuate the CM noise. One of the effective methods is the integration of CM filters within the power module [3], [4], [5], [6]. The capacitors between the positive dc terminal (referred to as dc+) or the negative dc terminal (referred to as dc−) node and ground function as *Y* capacitors [3], [4]. Another solution integrates a CM filter into the power module, which improves the CM noise suppression within the frequency range of 10–100 MHz [5], [6]. These capacitors, however, are exposed to high ambient temperature and may degrade the reliability of the module.

Other techniques stack substrates, such as direct-bonded coppers (DBCs), direct-bonded aluminums (DBAs), and printed circuit boards (PCBs) [7], [8], [9], [10], [11], [12], [13], [14], [15]. The secondary DBC with vias in its ceramic layer diverts the CM current and modifies the effective CM capacitance [7]. In [8], the CM noise propagation path was further improved by the middle copper layer of the stacked DBC substrate. The authors in [9], [10], and [11] proposed a multistack DBA for screening CM current in 10-kV power module packaging. Ma et al. [12] introduced a new structure which places the voltage-pulsating node, i.e., the ac node, between the dc+ and dc− nodes, with no close contact to the frame ground. While these configurations effectively reduce CM noise, the additional substrates can degrade thermal performance, complicate manufacturing processes, and decrease cost effectiveness. In another approach, a PCB mounted on the DBC reduces the area of the ac node at the top copper layer [13], [14], [15]. However, combining PCB and DBC may not guarantee simple manufacturing and high reliability.

Other approaches have been reported focusing on the design of substrates [16], [17], [18], [19], [20] or heatsinks [21], [22] to attenuate CM noise. In [16], the layout of the top copper layer was designed to reduce the area of which voltage pulsates. Though the method effectively decreased the CM capacitance, its performance is limited by the minimum area of the copper layer. Another approach connected the bottom copper of a direct-plated-copper substrate [17] to the dc− node through vias [18]. The bottom copper layer works as a shield between the midpoint of a half-bridge circuit and a baseplate, allowing the CM current to bypass the ground. This configuration can be implemented under specific conditions, such as using a thermal interface material between the bottom copper layer and the

heatsink and forming vias in a ceramic layer. The authors in [19] and [20] decreased the CM capacitance by etching a part of the bottom copper layer and replacing it with air. Though the design scheme does not sacrifice its thermal performance compared to the conventional power module, its mechanical reliability remains uncertain. Separate heatsinks with CM snubbers have been utilized to attenuate CM noise [21], and the use of a nonmetallic heatsink has been explored to achieve small CM capacitance [22]. However, these techniques face challenges when the design freedom of the heatsinks is limited.

Mathematical models of the CM noise propagation have been investigated [24], [25], [26], [27]. The equivalent circuits for the CM noise were configured based on the distribution of the parasitic capacitances [24], [27]. In the model, the capacitances were added between each terminal of the power module and the baseplate to cancel the CM current [23]. In [24], the model was used to design the inner layout of the power module to compensate for large capacitive coupling of an organic DBC substrate. Balance techniques for paralleled power modules were also introduced [25]. An equivalent circuit model for paralleled SiC bare dies was analyzed and a decoupling capacitor was added between every paralleled pair of bare dies to reduce CM noise [26]. These approaches require the redesign of the layout, additional circuit components, and the increased size of the power module. Various methods to attenuate CM noise in power module design are summarized in [8] and [31].

This article proposes a novel power module to reduce the CM noise without decreasing its mechanical stability as an extension of the research conducted in [28] and [29]: the proposed module replaces a specific area of bottom copper with a low-permittivity (low-ε) epoxy material to reduce the capacitance between the midpoint of a half-bridge circuit and a grounded baseplate. Heat flow between the dies and the baseplate was considered to design the bottom copper, ensuring that the thermal performance is not degraded. The insertion of the low-ε material does not compromise the size and the isolation voltage of the power module. The proposed design is not limited to power modules with numerous devices or double-sided cooling modules.

A steady-state thermal analysis and a static structural analysis were performed by Ansys Workbench and Mechanical to examine the mechanical deformation. The proposed module presented virtually the same level of deformation as the conventional module and smaller deformation than the previous article [20]. Mechanical reliability of the proposed module was also examined by thermal cycling test (TCT). The output characteristics of the power modules, i.e., drain currents with respect to the drain-source voltages, were measured to verify that the proposed module does not compromise the electrical performance.

The manufacturing process of the proposed module is explained in detail to validate its feasibility for production. The injection, thorough filling, and curing methods are proved by inspecting its cross-section.

The rest of this article is organized as follows. Section II provides a comprehensive overview of the design methodology employed for the proposed power module. The primary objective of this methodology is to reduce CM capacitance while also considering the heat flux region at the bottom copper layer.

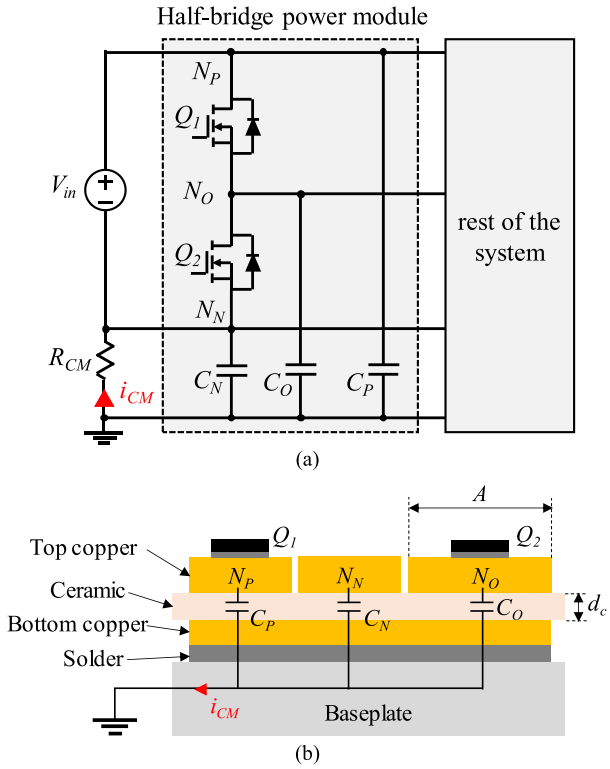

Fig. 1. (a) Half-bridge power module and its parasitic capacitances. (b) Cross-section view of the conventional power module.

Section III elaborates the estimation of capacitance, assessment of mechanical reliability, evaluation of thermal performance, and the manufacturing process of the proposed module. In Section IV, the CM noise reduction of the proposed module is verified by the steady-state converter operation. Results of TCTs and thermal resistance measurements are also introduced. Finally, Section V concludes this article.

II. Proposed Power Module Design to Reduce CM Capacitance

Fig. 1(a) shows a half-bridge power module and the distribution of its parasitic CM capacitances C_N, C_O, and C_P. The literals N_P, N_O, and N_N represent the dc+, ac, and dc− nodes in the power module and R_{CM} denotes CM impedance. Among the three parasitic capacitances, C_O has the most significant impact on the CM current i_{CM} because of the pulsating voltage at N_O. The voltage source V_{in} is the dc input voltage.

Fig. 1(b) describes a cross-sectional view of the power module which consists of a high-side bare die Q_1, a low-side bare die Q_2, a DBC substrate (simply DBC hereafter), and a baseplate. Parasitic capacitances caused by the gate and source pads were not considered because their effect on CM noise was negligible due to the small area of the gate and source pads. In case these pads are comparable or larger than drain pads, their effect should be considered as well to estimate capacitance and thus quantify CM noise accurately as shown in [32]. The DBC consists of a top copper layer which includes N_P, N_N, and N_O nodes, a ceramic layer, and a bottom copper layer. The device Q_1 is placed on

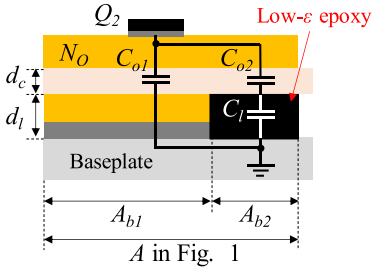

Fig. 2. Proposed configuration where a low-ε epoxy material (black area) replaces a part of bottom copper of DBC substrate.

N_P and Q_2 is on N_O because the drain pad of an SiC bare die is located at its bottom side. The baseplate is attached beneath the bottom copper layer by solder. The capacitor C_O, which exists between N_O and the grounded baseplate, is determined as

$$C_O = \varepsilon_0 \varepsilon_c \frac{A}{d_c}. \tag{1}$$

In (1), ε_o, A, ε_c, and d_c are the permittivity of free space (8.85 $\times 10^{-12}$ F·m^{-1}), area of N_O, relative permittivity of the ceramic material, and thickness of the ceramic layer, respectively. To mitigate C_O and CM noise, a specific portion of the bottom copper beneath N_O is etched out and replaced by low-ε epoxy as shown in Fig. 2. The newly designed $C_{O.\text{new}}$ becomes smaller than the original capacitance C_O by combining the capacitances of C_{O1}, C_{O2}, and C_l, as follows:

$$C_{O.\text{new}} = C_{O1} + \frac{C_{O2} C_l}{C_{O2} + C_l} \tag{2}$$

$$C_{O1} = \varepsilon_0 \varepsilon_c \frac{A_{b1}}{d_c} \tag{3}$$

$$C_{O2} = \varepsilon_0 \varepsilon_c \frac{A_{b2}}{d_c} \tag{4}$$

$$C_l = \varepsilon_0 \varepsilon_l \frac{A_{b2}}{d_l} \tag{5}$$

where A_{b1} represents the remaining area of the bottom copper layer under N_O, A_{b2} denotes the area of the etched space, ε_l represents the relative permittivity of the low-ε epoxy, and d_l is the thickness of the low-ε layer.

III. Prototype Power Module

Power modules were prototyped to verify the effectiveness of the proposed CM noise attenuation scheme. Fig. 3 presents photographs of 25 $\times$ 19.2 mm^2 DBC which is used in this article. The DBC consists of copper-Al_2O_3-copper layers with thickness of 0.3, 0.38, and 0.3 mm, respectively. Fig. 3(a) shows layout of the top copper layer with the location of four SiC dies of which specifications are shown in Table I. Two dies in parallel configure Q_1 or Q_2. The areas outlined by red dashed lines are the nodes N_P, N_O, and N_N. Fig. 3(b) describes the bottom copper layer of the proposed module. The region indicated by black dotted lines represents the space beneath the node N_O, where the copper is replaced by a low-ε epoxy. The size of this area is defined as A_{b2}. The orange region provides enough cross-sectional area

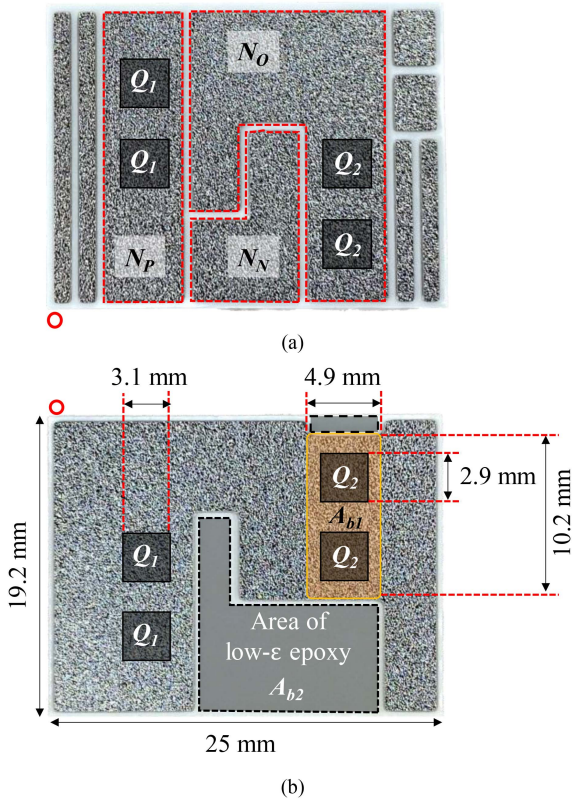

Fig. 3. Photograph of the 19.2 $\times$ 25-mm^2 DBC used in the prototype power modules. (a) Top copper layer with highlights of Q_1, Q_2, N_P, N_O, and N_N. (b) Bottom copper layer of the air and proposed modules with A_{b1} (orange area) and A_{b2}. The area A_{b2} is filled with air in the air module, or with epoxy in the proposed module.

TABLE I
Specifications of Proposed Power Module

Components		Description
SiC die		S4503/750 V/56 A/26 mΩ by Rohm
DBC		19.2 mm × 25 mm
	Top Cu	0.3-mm thickness
	Ceramic	Al_2O_3/0.38-mm thickness
	Bottom Cu	0.3-mm thickness
Baseplate		C1020/2-mm thickness
Solder		(between dies and top copper layer) Pb95Sn5, 48.1 W/m·K (between bottom copper layer and baseplate) SAC305, 58 W/m·K
Low permittivity material		ε_l = 3.5, coefficient of temperature expansion = 32 ppm/K, viscosity = 40 Pa·s, T_g = 137 °C (after injection, 150 °C, 1-h curing)
Aluminum wire		(source connections) 400-μm diameter (gate connections) 125-μm diameter
Thermistor		HM104J1A by Littelfuse
Silicone gel		For power module encapsulation (80 °C, 1-h curing)

of heat flow between Q_1 dies and the baseplate not to degrade thermal performance regarding Fig. 5 of [28] and [30]. Based on the thickness of the DBC layers and their heat spreading angles, at least 0.92-mm distance from each edge of the dies should be secured in the bottom copper not to sacrifice the thermal performance. The area A_{b1} in Fig. 3(b) is enough since

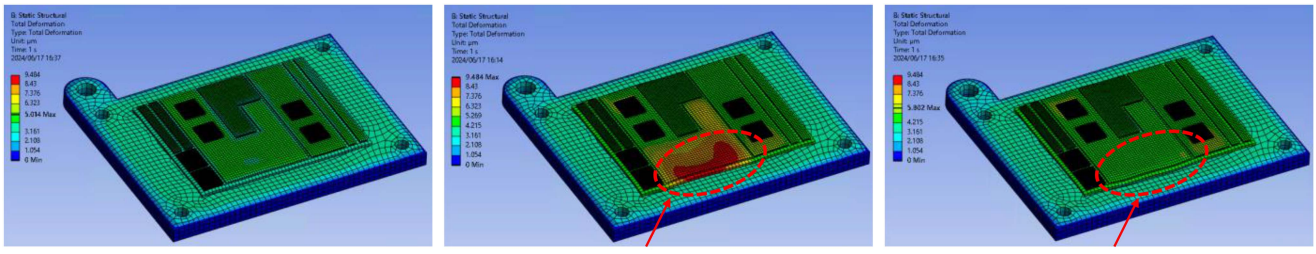

Fig. 4. Mechanical deformation simulated by Ansys Workbench and Mechanical. (a) Full-copper module. (b) Air module with severe deformation at N_O. (c) Proposed module with minor deformation at N_O.

TABLE II
CALCULATED AND SIMULATED CM CAPACITANCES OF THREE MODULES

	Full-copper module	Air module	Proposed module
Calculation	35.71 pF	13.34 pF	17.01 pF
Simulation	40.75 pF	20.18 pF	23.97 pF

it includes orange-colored area which provides 1-mm distance from all edges Q_2 dies. Table I summarizes the components used in the power module. Two conventional power modules, the one with the full bottom copper layer (full-copper module hereafter) and the one that uses air as the low-ε material in [20] (air module hereafter), were also fabricated with the same layout and components for fair comparison.

A. Estimation of C_O

In Fig. 2, $d_c = 0.38$ mm, $\varepsilon_c = 9.8$, and $A_{b1} = 49.98$ mm^2. Substituting these into (3) yields 11.39 pF C_{O1}. Assuming that the solder layer thickness between the DBC and baseplate is 0.15 mm, A_{b2} and d_l are calculated as 106.4 mm^2 and 0.45 mm, respectively. The low-ε material used in this article is an epoxy with a relative permittivity ε_l of 3.5 at 1 MHz. Details of the manufacturing process are provided in Section III-D. From (4)–(5), C_{O2} and C_l are derived as 24.26 and 7.32 pF, respectively. The CM capacitance of the proposed module $C_{O.\text{new}}$ becomes 17.01 pF by (2). For comparison, C_O of the full-copper module and air module are calculated as 35.71 and 13.34 pF, respectively. The proposed power module reduced CM capacitance by 52.5% compared to that of the conventional counterpart. It is noted that the calculated capacitance using (1)–(5) could be lower than actual values, since fringing fields of the capacitors are not considered [33]. The CM capacitances of the full-copper, air, and the proposed modules were also simulated by Ansys 2023 R2 Q3D Extractor as 40.75, 20.18, and 23.97 pF, respectively. The calculated and simulated capacitances are in Table II. Though the capacitance of the proposed module is larger than that of the air module, its impact on the CM noise is negligible as illustrated in Section IV-A.

B. Simulated Mechanical Deformation

A steady-state thermal analysis was performed by Ansys 2023 R2 Workbench Mechanical, and the results were imported as the loads for the static structural analysis. A thermal load of 10 W was applied to the top surface of each die which is the maximum loss budget when the converter outputs the maximum power or 1 kW. Film coefficient of 4 kW/m^2·K was assigned to the baseplate of the power module with 65 °C ambient temperature. A static structural analysis was carried out assuming 9.8 m/s^2 gravity. The side and bottom surfaces of the baseplate and screw holes of the busbars were fixed in position. The material properties used in the simulation are listed in Table III.

TABLE III
MATERIAL PROPERTIES USED IN THE MECHANICAL SIMULATION

Material	CTE (ppm/K)	Young's modulus (GPa)	Poisson's ratio	Tensile yield strength (MPa)
Copper	16	130	0.34	333
Al_2O_3	8.1	315	0.22	100
SiC	4	410	0.14	550
Pb95Sn5	25	18	0.44	28
SAC305	21.9	16.6	0.4	49.6
Low-ε epoxy	32	8	0.35	130

Fig. 4(a)–(c) shows the simulation results of the full-copper, air, and the proposed module, respectively. The busbars were set to be invisible for clear view. The air module shown in Fig. 4(b) experienced significant mechanical deformation at N_O which is above the air region as indicated by the dashed circle. The proposed module exhibited minor deformation at the same location as in Fig. 4(c), which is negligible compared to that of the air module. The maximum deformations at N_O for full-copper, air, and proposed modules were observed as 5.01, 9.48, and 5.80 μm, respectively. This demonstrates the greater mechanical reliability of the proposed module compared to the air module. Section IV-B further provides evidence of the improved mechanical robustness.

C. Thermal Performance

A steady-state thermal simulation of the three modules was performed by Ansys 2023 R2 Icepak. The coolant temperature and flow rate were 65 °C and 8 liter per minute, respectively, which are typical in automotive power module cooling. A thermal load of 10 W was again assigned to the top surface of each die. The thermal conductivity of the low-ε

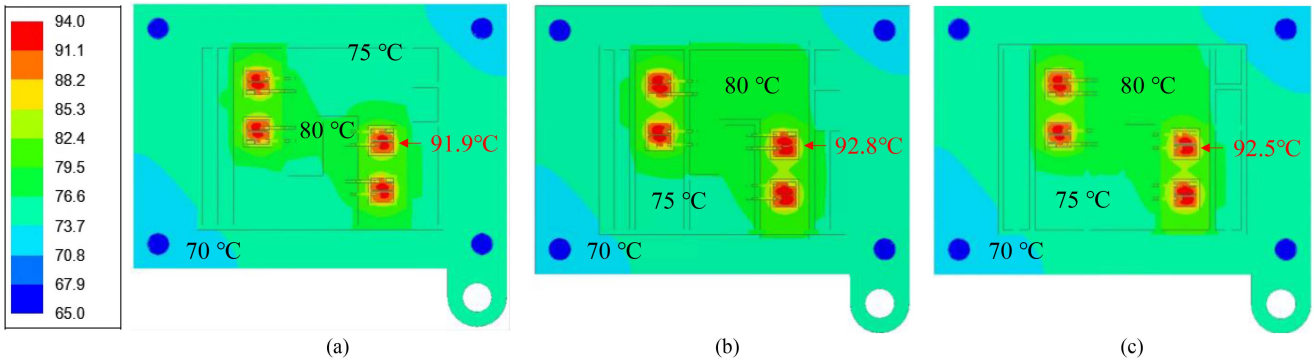

Fig. 5. Thermal simulation results by Ansys Icepak of (a) full copper, (b) air, and (c) proposed modules.

epoxy was set 0.2 W/m·K. Fig. 5(a)–(c) shows the simulation results of the full-copper, air, and the proposed module, respectively. The maximum temperatures at Q_2 are as follows: 91.9 °C in the full-copper module; 92.8 °C in the air module; 92.5 °C in the proposed module. The proposed module showed only 0.6 °C difference compared to the full-copper module. Thermal resistances were also experimentally measured and the same thermal performance was also observed in Section IV-C.

D. Manufacturing Process of the Proposed Power Module

This section introduces the manufacturing process to validate manufacturability of the proposed power module [28].

The formic acid vacuum reflow soldering was conducted after placing all components in a jig. The assembly is afterward fixed in a vertical position. The epoxy is injected into the gap between the Al_2O_3 layer and the baseplate shown in Fig. 3(b). The injection process was carried out on an 80 °C hotplate to lower the viscosity of the epoxy, since viscosity <1 Pa·s is preferred to remove potential voids in the epoxy. Injecting the epoxy in a vacuum is also recommended, though the prototypes in this article were manufactured under typical atmospheric pressure. The epoxy employed in this article possesses thermosetting properties, hence it is subsequently cured in a temperature chamber at 150 °C for 1 h. Curing conditions may vary depending on the material being used. This article used the epoxy with a glass transition temperature T_g of 137 °C to secure at least 10 °C margin from the maximum storage temperature of 125 °C.

Integration of the case and wire bonding were conducted after the injection and curing of the epoxy. Silicone gel is finally encapsulated. The gel is subjected to curing at a temperature of 80 °C for 1 h in a temperature chamber.

Fig. 6(a) shows the prototype power module where silicone gel is not shown for clear view. A terminal at the baseplate was made to facilitate the ground connection. The filling conditions were determined based on the constant-depth mode scanning acoustic microscope (C-SAM) images. To verify the complete filling of epoxy, a cross-section was observed by cutting the module along the red dashed line indicated in Fig. 6(a) as shown in Fig. 6(b).

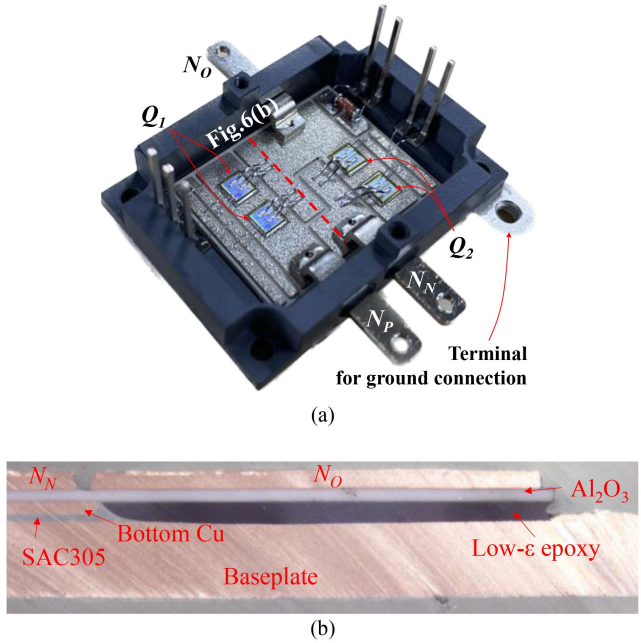

Fig. 6. (a) Photograph of the prototype power module. (b) Cross-section view of the power module to verify the complete filling. The prototype was cut-off along the red dashed line shown in (a).

IV. Experimental Verification

A. CM Noise Measurement

Fig. 7(a) shows the experimental setup to measure the CM noise of the power modules. The specifications for the converter are listed in Table IV. Two line impedance stabilization networks (LISNs) NNBM8124 are connected to the dc power supply HX01000-12G2. The full-copper and air modules were also manufactured and implemented in the same test setup as shown in Fig. 7(b). In addition, the same gate driver boards shown in Fig. 7(c) were used for fair comparison. A gate driver with 2EDS8265HXUMA2 by Infineon and bottom-entry connectors 18021-series by IRISO Electronics were used. Currents i_{CM} and i_L flow through the LISN and the inductor L, respectively. The gate-source and drain-source voltage of Q_1 are denoted as v_{gs} and v_{ds}, respectively. Gate and source nodes of Q_2 were shorted to prevent its false turn-ON.

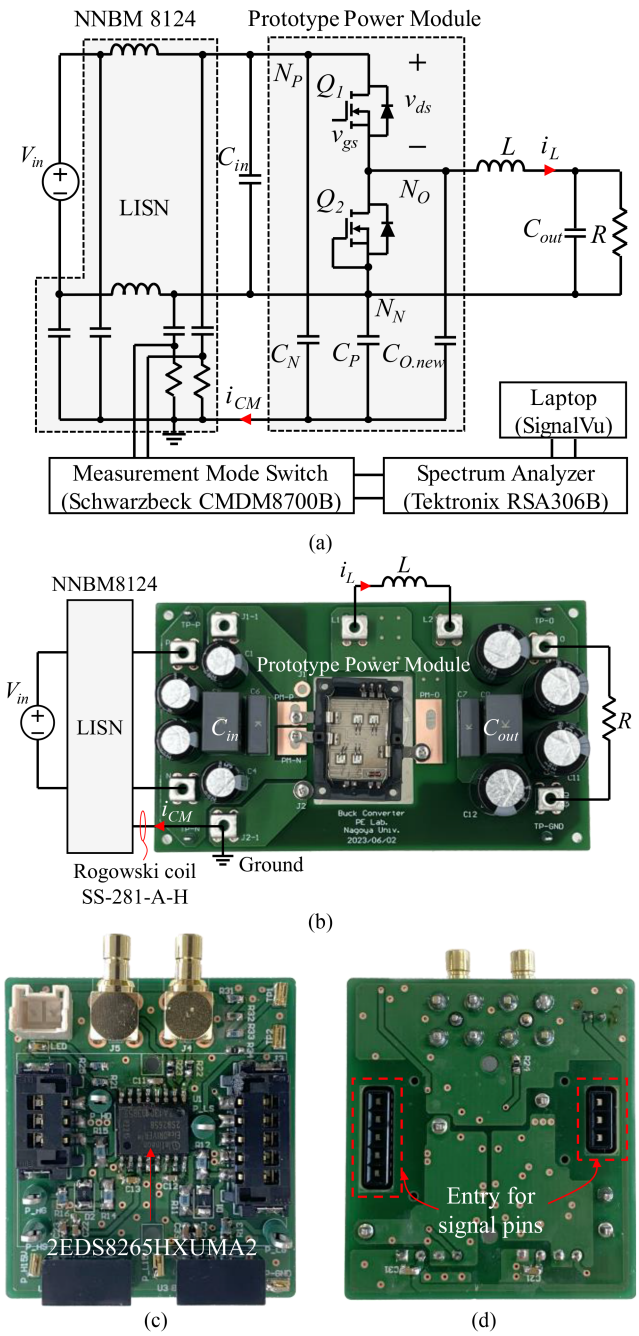

Fig. 7. (a) Experimental setup to measure CM noise. (b) Photograph of test setup. (c) Top view and (d) bottom view of gate drive board.

TABLE IV
SPECIFICATIONS OF THE CIRCUIT TO MEASURE CM NOISE

Input voltage	400 V
Output voltage	200 V
Switching frequency	50 kHz
L	7 mH
P_o	1 kW
C_{in}	132.8 μF
C_{out}	401.8 μF
R	40 Ω
LISN	NNBM8124
DC power supply	HX01000-12G2
Spectrum analyzer	RSA306B

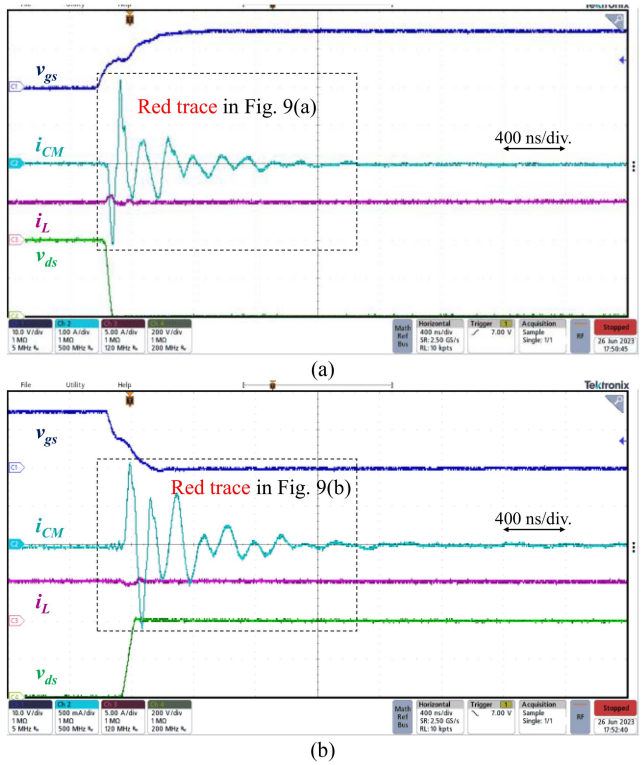

Fig. 8. Experimental waveforms of the proposed power module during the steady-state operation. (v_{gs}: 10 V/div., i_L: 5 A/div., v_{ds}: 200 V/div., time scale: 400 ns/div.). (a) Turn-ON instant (i_{CM}: 1 A/div.) (b) Turn-OFF instant (i_{CM}: 500 mA/div.).

Fig. 8 shows the experimental waveforms of turn-ON [Fig. 8(a)] and turn-OFF [Fig. 8(b)] instant of Q_1 for the proposed modules with 400-ns/division time scale. The oscilloscope used to capture the waveform is Tektronix MDO34 with 1-GHz frequency bandwidth and 5-GS/s sampling rate. A current probe, IWATSU SS-281-A-H with a sensitivity of 200 mV/A and a frequency bandwidth up to 30 MHz measured i_{CM}. The Tektronix THDP0200 differential voltage probe measured v_{ds} with a frequency bandwidth of 200 MHz. The same gate driver boards were used for all three modules so that the switching speeds are identical to guarantee fair comparison.

The i_{CM} of the three modules during 1.6 μs after turn-ON and -OFF of Q_1 are compared in Fig. 9. At the turn-ON instant in Fig. 9(a), peak magnitudes of i_{CM} were 2.72, 2.20, and 2.12 A for the full-copper (black trace), air (blue), and proposed modules (red), respectively. The proposed module achieved a 22% reduction in i_{CM} compared to the full-copper module. Similarly, i_{CM} was decreased in the proposed module by 20% at the turn-OFF instant shown in Fig. 9(b).

Fig. 10 compares the measured CM noise spectra of full-copper (black), air (blue), and proposed (orange) modules in the frequency domain. The spectrum analyzer RSA306B was used in conjunction with the software SignalVu by Tektronix. The

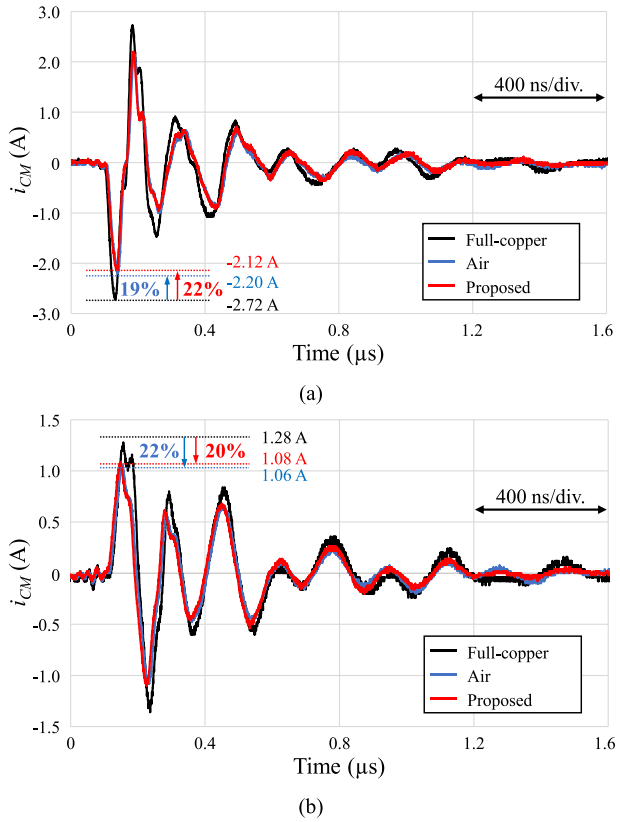

Fig. 9. Comparison of i_{CM}. Black, blue, and red traces are for the full-copper, air, and proposed modules, respectively. (a) At turn-ON instants (time scale: 400 ns/div.). (b) At turn-OFF instants (time scale: 400 ns/div.).

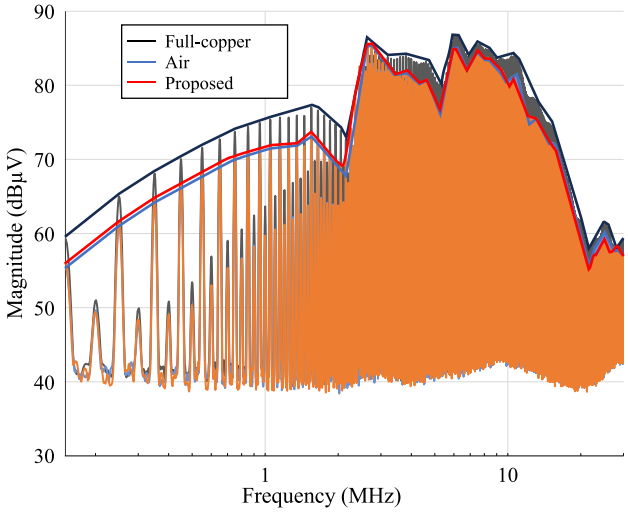

Fig. 10. Measured CM noise of full-copper (black), air (blue), and proposed (red) modules.

CM noise was captured by peak detector with 9-kHz resolution bandwidth. The proposed module exhibited lower amplitude than the full-copper module by 4–5 dBμV in the frequency range below 2 MHz. At higher frequency, improvement by 1–5 dBμV was observed. The proposed module presents almost the same level of improvement compared to the air module, though it shows slightly lower amplitude of CM noise than expected in Section III-A.

B. Thermal Cycling Test

TCTs were conducted to validate the mechanical reliability of the modules. The lowest and highest storage temperatures were set at −40 °C and 125 °C, and each temperature was maintained for 30 min. To assess thermal fatigue in the solder layers, C-SAM captured horizontally inverted images of power modules after 1000 cycles as shown in Fig. 11.

Fig. 11(a) shows the C-SAM image of the full-copper module. The solder layer on the baseplate experienced delamination from the boundary. This makes the images black near the surroundings. Fig. 11(b) and (c) presents C-SAM images of the air and proposed modules, respectively. The regions filled with air and low-ε epoxy are indicated by white dashed areas. Cross-sections along the red and yellow lines in Fig. 11(b) and (c) were observed in Fig. 12 by scanning electron microscope. Solder cracks were found in Fig. 12(a) and (b) which may degrade the thermal performance and mechanical stability of the air module. The crack in the ceramic layer as shown by the red dashed circle in Fig. 11(b) occurred due to the larger stress in the air module. Fig. 12(c) shows no crack and delamination in the solder layer which proves the improved mechanical stability of the proposed module.

Output characteristics of the full-copper and proposed power modules were assessed by Keysight B1506A to validate their electrical performance. Fig. 13 shows the output characteristics of Q_2. Fig. 13(a) and (b) presents those of the full-copper module before and after TCT, respectively, while Fig. 13(c) and (d) describes the characteristics of proposed module before and after TCT, respectively. It is observed that the electrical characteristics of the proposed module remain nearly identical to those of the full-copper module even after TCT. This verifies that the proposed module maintains its electrical performance without deterioration compared to the conventional module.

C. Thermal Resistance

Thermal resistances $R_{\rm th}$ were measured with Power Tester 1500 A by Mentor Graphics (now Siemens EDA) to verify that the proposed module does not sacrifice the thermal performance. Fig. 14(a) shows the setup for measuring the thermal resistance from the Q_2 to the baseplate $R_{{\rm th}.Q2}$. The power modules were positioned on the cold plate by the two fixtures from the top frame with 0.5-N·m torque. After the body diode of Q_2 carried 13 A for 30 s, $R_{{\rm th}.Q2}$ of each module was measured while $v_{\rm gs}$ of Q_2 was –3 V. This measurement was conducted twice, i.e., with enough (Case 1) and small (Case 2) amount of thermal grease, to separate $R_{{\rm th}.Q2}$ and the thermal resistance of thermal grease $R_{{\rm th}.{\rm Gr}}$.

Fig. 14(b)–(d) shows the structure functions of the three modules where $C_{\rm th}$ denotes their thermal capacitance. Red and black traces represent Case1 and Case2, respectively. The point where the two traces meet represents $R_{{\rm th}.Q2}$. All three modules provide

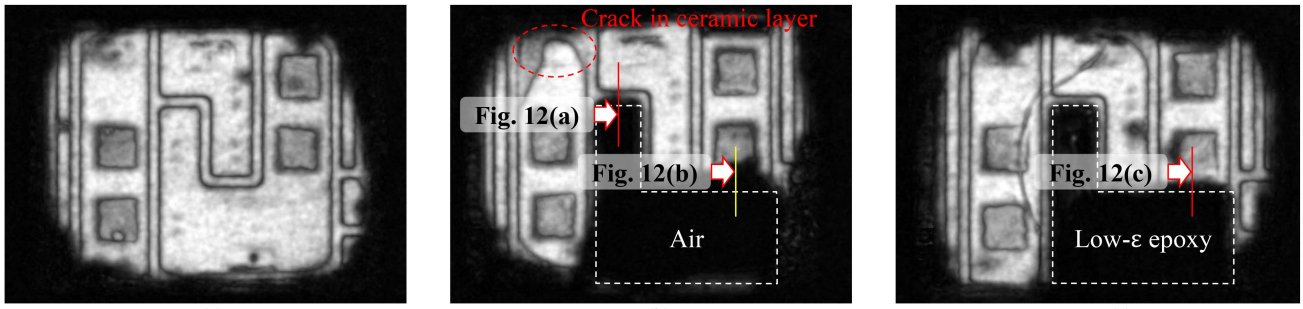

Fig. 11. C-SAM images after undergoing 1000 cycles of TCTs. (a) Full-copper module. (b) Air module. (c) Proposed module.

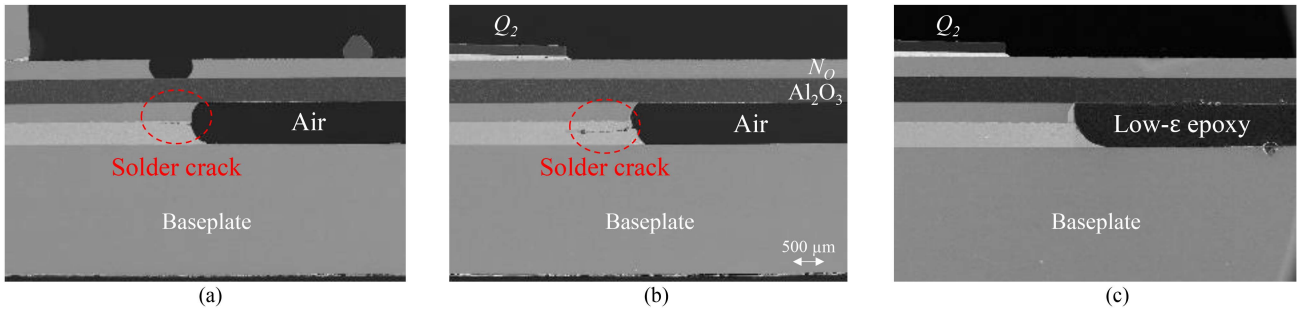

Fig. 12. SEM images of the cross-sections after undergoing 1000 cycles of TCTs. (a) Along the red line in Fig. 11(b). (b) Along the yellow line in Fig. 11(b). (c) Along the red line in Fig. 11(c).

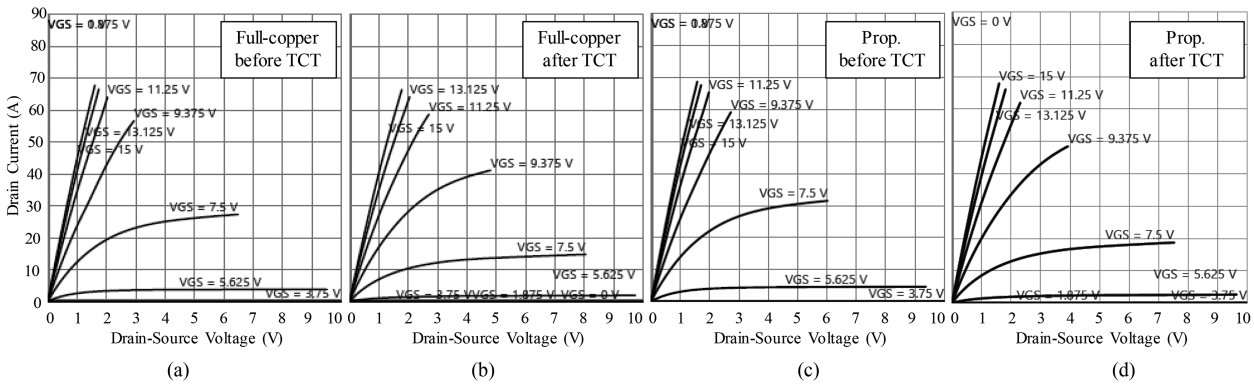

Fig. 13. Measured output characteristics of Q_2. Full-copper module (a) before TCT and (b) after TCT. Proposed module (c) before TCT and (d) after TCT.

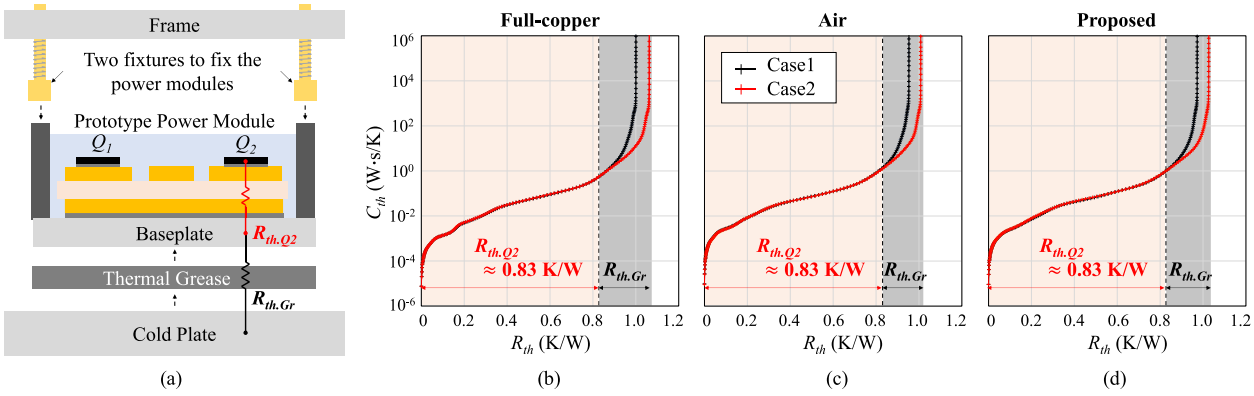

Fig. 14. (a) Setup for measuring R_{th} and measured structure functions of (b) full-copper, (c) air, and (d) proposed modules with enough (Case 1) and small (Case 2) amount of thermal grease to separate $R_{\mathrm{th}.Q2}$ and the thermal resistance of thermal grease $R_{\mathrm{th}.\mathrm{Gr}}$.

almost the same $R_{\mathrm{th}.Q2}$, 0.83 K/W, which proves compatible thermal performance of the proposed module.

V. Conclusion

This article proposes a novel SiC power module to effectively mitigate CM noise. The approach replaces a portion of the bottom copper layer in a DBC by a low-ε epoxy, resulting in 52% reduction in CM capacitance. Experimental results verified 4–5 dBμV CM noise reduction during steady-state operation.

The proposed module exhibits only a 0.6 °C increase in simulations, confirming no compromise in thermal performance. In addition, thermal resistances of the full-copper, air, and the proposed module were measured, and no degradation was confirmed. Reliability of the proposed power module was also examined by simulations, presenting the same level of deformation compared to the full-copper module. TCTs also demonstrated the proposed power module has higher reliability than the air module. Output characteristics were also measured before and after the tests and comparable electrical performance was observed.

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