Hybrid Data-Driven and Mechanistic Modeling Approach for Power Module Rapid Thermal Analysis

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***Abstract*—The safe operation and lifetime of the power module are heavily dependent on the temperature distribution, making it imperative to optimize the thermal performance of the layout at the design stage. During the module design phase, a significant number of layouts are assessed. It is important to constrain computational complexity while achieving high accuracy. Mechanistic modeling and data-driven modeling have limitations in terms of complexity and generalizability respectively. Therefore, this article proposes a hybrid data-driven and mechanistic modeling approach. This approach incorporates the theoretical analysis of mechanistic modeling and the high efficiency of data-driven modeling to accurately and efficiently compute the temperature distribution of a given layout. This approach initially acquires the dataset from simple structures and conducts a dimensionality reduction to obtain the isothermal point set (IPS). Later, IPS of complex structures is developed based on mechanistic modeling. Finally, the IPS is converted to a field to obtain a temperature distribution of the given layout. The accuracy of the approach is verified by a steady-state thermal experiment. With the proposed approach, an accurate assessment of surface thermal distribution of different layouts can be quickly finished. The thermal characteristics evaluation efficiency can be improved roughly 300 times, which provides the necessary technical basis for layout optimization.**

***Index Terms*—Data-driven approach, layout optimization, packaging, power module, thermal modeling.**

I. Introduction

WITH the increasing application of wide bandgap semiconductor devices in fields such as electric vehicles and renewable energy generation [1], the demand for large capacity power modules has grown. Due to the current capacity limitations of wide band gap semiconductor devices, parallel connection of chips has become a solution for large capacity power modules. However, the paralleled chips tend to cause an unbalanced temperature distribution due to their distinctive thermal paths and thermal coupling effects. According to the research, thermal imbalance will derate the power module and cause reliability issues [2], [3], [4], [5].

The layout within the power module determines the thermal path and the thermal coupling, so optimizing the layout is crucial. Layout optimization, whether currently or in the future, requires the evaluation of dimensional parameters and geometric topology [5], resulting in a vast solution space. Besides this, the thermal distribution model for each layout should be iteratively solved to achieve accurate calculations of both electrical and thermal stress [7]. Typically, this process takes a few weeks when simulation software is utilized. Therefore, to reduce the optimization process from weeks to a single day, an efficient and accurate thermal modeling method is necessary. Many thermal analysis approaches have been proposed. The existing approach includes numerical approaches, analytical approaches, and data driven approaches, where analytical approaches and numerical approaches both belong to mechanistic modeling.

Numerical approaches pertain to obtaining numerical solutions to intricate problems. Numerical approaches used for thermal analysis mainly cover finite element method (FEM), finite volume method (FVM), finite difference method (FDM), and boundary element method (BEM). FEM and FVM are widely used in commercial software like COMSOL and ANSYS. These methods have solid mathematical foundations and high accuracy. However, their computation process is slow. Many researchers propose a numerical methodology similar to FDM, known as the three-dimensional (3-D) nodal resistor network method [5], [9], [10], [11], [12]. Both methods address the issue of heat transfer by dividing solid domains into discrete elements. Depending on the size of the discrete elements, the method allows for highly accurate or efficient computations. However, they are not typically employed for irregular geometries. Simplification of the original geometry is often required [13], which will cause some errors. BEM is applicable to problems where Green's functions can be calculated. However, the Green's function for power modules with complex structures is difficult to obtain, which impedes the application of BEM.

Analytical approaches use methods of symbolic manipulation to obtain results. One analytical approach is the heat spreading angle approach [14], [15]. It calculates a heat-spreading angle Φ within each layer. After determining Φ, the 1-D thermal impedance network is established based on the heat transfer path.

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It is characterized by its simple expression and fast calculation speed. However, 1-D thermal networks are difficult to account for chip thermal coupling effects and provide a thermal field, leading to underestimation of junction temperature and unclear thermal distribution. Besides this, researchers have utilized the analytical solution of the heat diffusion equation as the basis for their thermal modeling. Choudhury and Rogers [16] obtained the steady-state thermal field using an N-layer Fourier series expansion, Zhan and Sapatnekar [17] proposed a Green's function based high-efficiency thermal modeling method. The analytical expressions of the Fourier series and Green's function are both derived based on a multilayer rectangular structure with the same size. If the power module is similar to that structure, accurate, and fast solutions can be obtained. However, the calculation results for structures exceeding these limitations will introduce some errors.

Data-driven approaches are innovative techniques for modeling issues. It establishes the relationship between inputs and outputs by learning the dataset through an intelligent system. Since the intelligent system maps the inputs directly to the outputs, the data-driven approach has an extremely fast computational speed compared to numerical methods. Many researchers proposed the machine-learning based thermal modeling method by learning from numerical analysis results [18], [19]. The method exhibits high computational accuracy when the heat source varies in different locations. But the trained process of the network focuses on a fixed module structure, its application to layout optimization with changing layout will omit some key features, whether it is a supervised method or an unsupervised method [19]. Besides this, machine-learning based method lacks interpretability and needs large amounts of data for training in some cases. All these factors constrain the wide use of the machine learning based data-driven approach in the design phase.

Combining the physical mechanisms with a data-driven approach can enhance the adaptivity of the model. A data-driven method combined with thermal spreading resistance theorem is proposed in [20]. This method outputs the thermal resistance network based on the simulation results of specified layouts. Heat transfer formulas are employed to handle temperature evaluation beyond the dataset. For the first time, the effect of layout on the thermal characteristics of the power module is modeled. It also has a high computation speed. However, this work sacrifices some accuracy and cannot output the thermal distribution.

Aiming to provide an efficient and accurate thermal field calculation approach, this article established a steady-state thermal modeling approach that combines mechanistic knowledge and data-driven concepts. It introduces a dimensionality reduction variable for managing intricate thermal field data. By researching the impact of alterations in layout size parameters on heat distribution, we can achieve excellent accuracy and computational speed. This approach will further improve the quality and efficiency of the optimized design of the power module.

The rest of this article is organized as follows. Section II gives an overview of the proposed approach. Section III introduces the dataset acquisition and dimensionality reduction process. Then, in Section IV, the thermal field reconstruction algorithm is proposed. In Section V, the experiment and comparative analysis

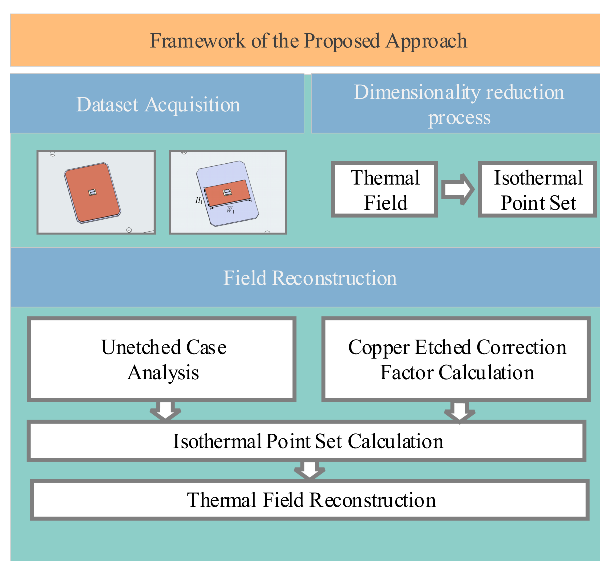


Fig. 1. Framework of the proposed approach.

with different approach is conducted to verify the speed and accuracy. Finally, Section VI concludes this article.

II. Overview of the Proposed Approach

This approach was developed for thermal modeling in layout optimization. Optimization focuses on the horizontal layout of the module. Thus, the horizontal parameters are set as variables, i.e., the size and location parameters of the copper traces and chips. The proposed approach can estimate the surface temperature of the power module in which chips and passive components are placed horizontally on one plane, like the traditional package and double-sided cooling package. The procedure of the proposed approach is shown in Fig. 1, which can be divided into two steps as follows.

Step 1: Data acquisition and dimensionality reduction process. The data acquisition step gathers simulation data from diverse layouts. The dimensionality reduction process introduces the isothermal point set (IPS) to establish a relationship between essential thermal features and the changing layouts.

Step 2: The reconstruction of the thermal field. This step combines the heat transfer theory and the obtained dataset to calculate the IPS of the layout, then the thermal field is reconstructed based on the IPS of the layout.

In this article, the research object is a single-sided cooling power module with a pin-fin cooler, as shown in Fig. 2. This kind of power module does not have a baseplate, thus, its thermal resistance is significantly reduced. This structure is widely used in hybrid and electric vehicle traction applications. The power module materials are summarized in Table I.

III. Data Acquisition and Dimensionality Reduction Process

This section serves two purposes: on the one hand, acquiring sufficient dataset of the thermal field, on the other hand, establishing the dimensionality reduction representation of the thermal field to facilitate the subsequent analysis. Finite element

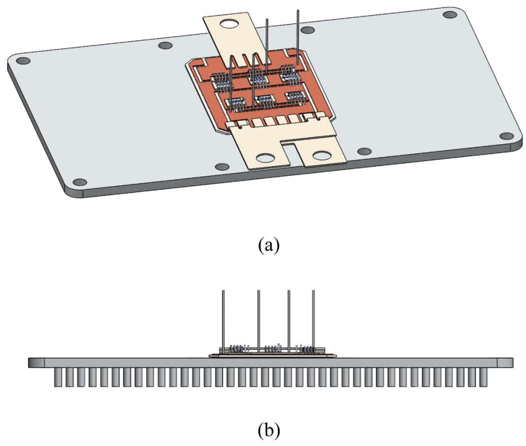


Fig. 2. Module structure. (a) View 1. (b) View 2.

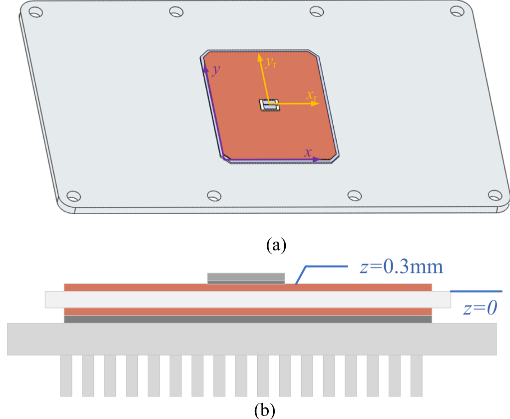


Fig. 3. Simulation model of the first simulation stage and the coordinate systems. (a) View 1. (b) View 2.

TABLE I
MATERIALS FOR THE POWER MODULE

Part	Material	Specifications
Die	SiC MOSFET bare die	CETC WM1A025120B 1200 V/25 mΩ Die size: 6.2×4.6×0.37 mm^3 Top side metallization:Al Bottom Drain metallization: Ni/Ag
Die-attach material	SAC305	Thickness: 0.15 mm Thermal conductivity:58 W/(m·K)
Substrate	Al_2O_3 DBC	Cu layer size: 38×48×0.3 mm^3 Al_2O_3 layer size: 40×50×0.63 mm^3
Cooler solder	Sn63/Pb37	Thickness: 0.15 mm Thermal conductivity :50 W/(m·K)
Cooler	Copper	Pin-Fin structure

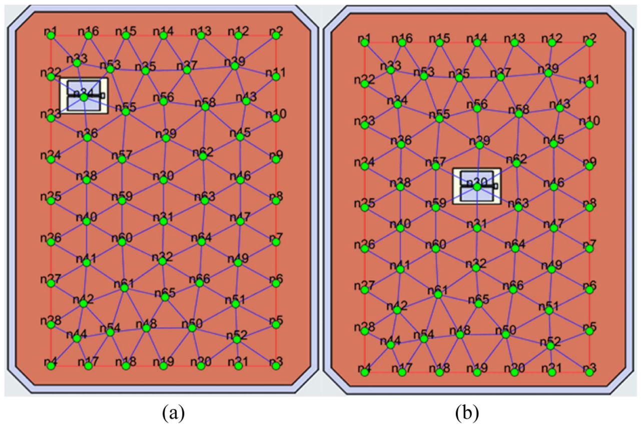


Fig. 4. Mesh generation result mapped to simulation model. (a) Model structure when node n24 is selected as the chip center. (b) Model structure when node n30 is selected as the chip center.

analysis software like COMSOL is used for the data acquisition, and MATLAB scripts are used to automate the dataset acquisition process. Two types of simulation models are implemented to consider the influence of different chip positions and different copper traces. Then, a dimensionality reduction variable called IPS is defined to represent the essential feature of the thermal field.

A. Simulation Stage With Changing Chip Positions

Chip position significantly influences the thermal distribution inside the module. The influence of different chip positions is considered in the model of the first simulation stage.

In the model, the model with direct bonded copper (DBC) in nonetched(complete) state is established. Chip position is set as a variable parameter. Because the bond wire has little effect on the thermal characteristics [12], the bond wire is omitted in the simulation model, as shown in Fig. 3. In addition, two coordinate systems are used in this article. They are the absolute coordinate system, denoted as xyz system, and the relative coordinate system of chips, denoted as $x_r y_r z$ system. The direction of the axis in horizontal plane is shown in Fig. 3(a). The z-axis origin is defined in Fig. 3(b), the two coordinate systems share the same z-axis.

The active area of the chip is set as the heat source, and an even heat rate of 50 W is given as the excitation. The equivalent heat transfer coefficient (htc) of the pin-fin cooling surface is set as $h = 8500$ W/(m2·K), which can be obtained from numerical analysis or experiments. The coolant temperature is set as 20 °C. The steady state thermal simulation is conducted.

The chip position varies among different simulation models. In order to get an accurate thermal profile across the whole plane no matter where the chip is, the selected positions of the chip center should be spread throughout the plane. The triangular mesh generation method is used to split the plane and determine the position of the die. The maximum mesh edge length is defined to regulate sparsity and control dataset size, it is set as 5 mm in this article. Each node of the triangular mesh is selected as the central position of the chip once in the first simulation stage, Fig. 4 demonstrates two cases of the simulation model. As shown in Fig. 4, there are 66 nodes, so this process needs 66 simulations. It should be noted that the chip needs to keep some distance from the edge of the copper trace, in this article, the distance is set as 1.5 mm.

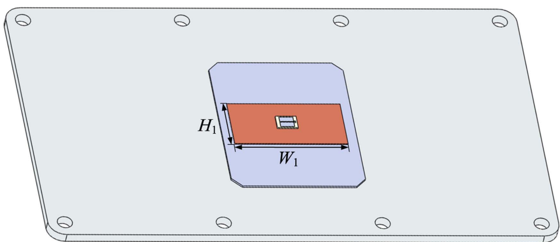


Fig. 5. Simulation model of the second simulation stage.

After the simulation, the surface temperature of the z = 0.3 (i.e., the upper surface of the copper trace) is recorded as dataset. The sampling interval in both the *x*- and *y*-directions is 0.5 mm. Besides this, the average temperature rise at the top surface of the ceramic isolator (i.e., surface z = 0) is recorded as dataset.

B. Simulation Stage With Changing Copper Size

The maximum temperature and temperature distribution of the chip changes as the trace shrinks. In order to cover power modules with different copper trace sizes, the simulation model of the second simulation stage set the copper trace size as variable parameters.

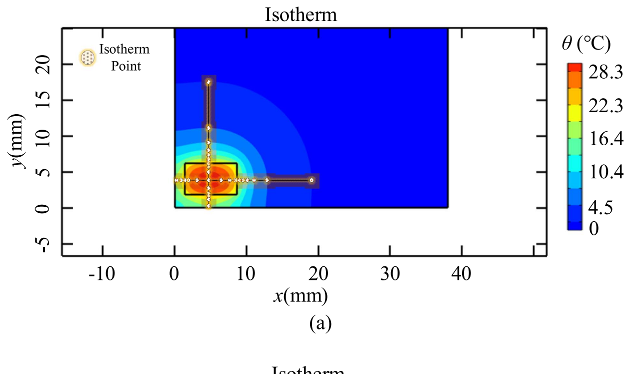
In the second simulation stage, the chip is placed in the center of the module and given an even heat rate of 50 W. To control the sample size, the copper trace is centrally symmetrical, the equivalent htc of the pin fin cooling surface is set as $h = 8500$ W/(m^2·K), coolant temperature is set as 20 °C. The size parameters of the upper copper trace are defined as H_1 and W_1, as shown in Fig. 5.

In this simulation stage, both H_1 and W_1 have 10 sampling values. The value is logarithmically spaced because the temperature changes sharply when the size of the copper trace is small. The simulation is performed for all variations of H_1 and W_1. Thus, this process has 100 simulations. After the simulation, the surface temperature of the z = 0.3 is recorded as dataset. If there is no trace, the temperature value recorded is NaN. Besides this, the average temperature rises of the chip and the trace are recorded as dataset.

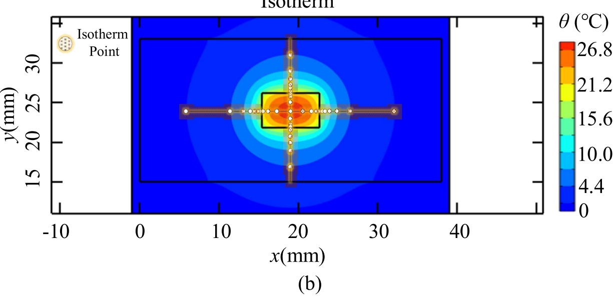
C. Dimensionality Reduction Process

After the dataset acquisition process, the recorded data is cumbersome. Field distribution information is difficult to process. A dimensionality reduction representation of the surface thermal field is proposed.

First, the field point is interpolated to produce a continuous surface. Linear interpolation is used in this article. After that, the IPS is defined to represent the vital information, i.e., dimensionality reduction representation of the thermal field. M denotes the temperature rise of the point beneath the chip center at surface z = 0.3 mm. In general, the position with the highest temperature point is near center of the chip. Then, record the position in the *x*-axis and *y*-axis in both directions when the temperature rise θ decreases to different isothermal levels (0.9M, 0.8M, 0.7M, 0.6M, 0.5M, 0.4M, 0.3M, 0.2M, 0.1M, 0.05M). If the position is not found, NaN is assigned. The



(a)



(b)

Fig. 6. Example of the isothermal point. (a) One sample in the first simulation stage. (b) One sample in the second simulation stage.

position information is converted into the distance from the chip center and subsequently becomes a component of IPS, defined as the isothermal point matrix. The distance information and temperature rise values form the IPS, M is also included. The isothermal point is demonstrated in Fig. 6. All IPS are recorded in dataset.

Fig. 6(a) shows the isothermal point of one sample in the first simulation stage, and Fig. 6(b) shows the isothermal point of one sample in the second simulation stage. The isothermal point matrix is denoted as $\boldsymbol{A}$. Denote the matrixes in each direction of the axis as $\boldsymbol{A}^{\mathrm{W}}$, $\boldsymbol{A}^{\mathrm{S}}$, $\boldsymbol{A}^{\mathrm{E}}$, $\boldsymbol{A}^{\mathrm{N}}$, respectively, $\boldsymbol{A}^{\mathrm{W}}$ means an array of isothermal point distance along the negative *x*-axis, $\boldsymbol{A}^{\mathrm{E}}$ means an array along the positive *x*-axis, $\boldsymbol{A}^{\mathrm{S}}$ means an array along the negative-*y*-axis, $\boldsymbol{A}^{\mathrm{N}}$ means an array along the positive *y*-axis. $\boldsymbol{A}$ is a 4×10 matrix, and $\boldsymbol{A}^{\mathrm{W}}$, $\boldsymbol{A}^{\mathrm{S}}$, $\boldsymbol{A}^{\mathrm{E}}$, $\boldsymbol{A}^{\mathrm{N}}$ are all 1×10 arrays

$$\boldsymbol{A} = \begin{bmatrix} \boldsymbol{A}^{\mathrm{W}} \\ \boldsymbol{A}^{\mathrm{E}} \\ \boldsymbol{A}^{\mathrm{S}} \\ \boldsymbol{A}^{\mathrm{N}} \end{bmatrix}. \tag{1}$$

After all the isothermal point matrixes are generated, the NaN data needs to be processed. Supposing the isothermal point matrix of the case with unetched copper and centered chip is $\boldsymbol{A}_{\text{u-c.}}$ In this article, there is no NaN in $\boldsymbol{A}_{\text{u-c}}$. if an isothermal point matrix $\boldsymbol{A}_{\text{nan}}$ has NaN in it, supposing NaN starts at the ith element in $\boldsymbol{A}^{\mathrm{W}}{}_{\text{nan}}$. Then, $\boldsymbol{A}^{\mathrm{W}}{}_{\text{nan}}$ is modified to $\boldsymbol{A}^{\mathrm{W}}{}_{\text{nan_m}}$, as shown in

$$\boldsymbol{A}^{\mathrm{W}}_{\text{nan_m}}(s) = \frac{\sum_{u=1}^{i-1} \boldsymbol{A}^{\mathrm{W}}_{\text{nan}}(u)}{\sum_{u=1}^{i-1} \boldsymbol{A}^{\mathrm{W}}_{\text{u-c}}(u)} \boldsymbol{A}^{\mathrm{W}}_{\text{nan}}(s)(s = i \text{ to } 10). \tag{2}$$

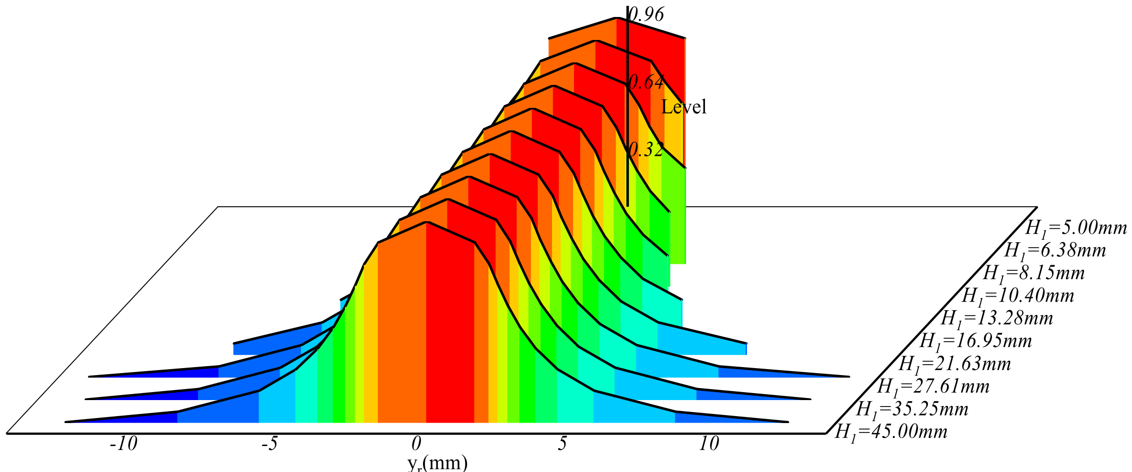


Fig. 7. Distribution of normalized profile temperature for different H_1.

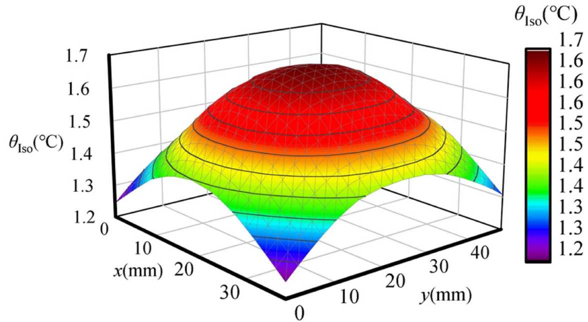


Fig. 8. Function $\theta_{\text{iso}}(x,y)$.

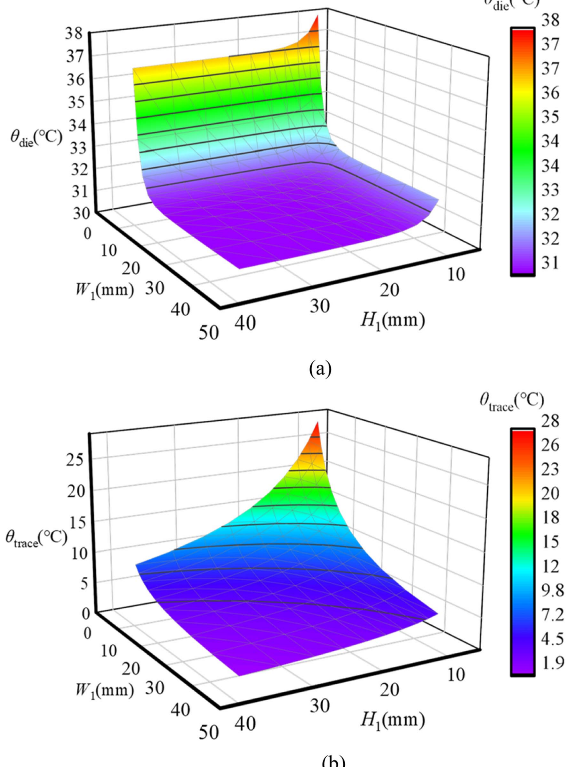


Fig. 9. Relationship of the average temperature rise of the chip and trace to H_1 and W_1. (a) Relationship of the average temperature rise of the chip to H_1 and W_1. (b) Relationship of the average temperature rise of the trace to H_1 and W_1.

For the matrix in other directions, the same treatments are applied. Using this method, the matrices in the dataset can have a reasonable value

Fig. 7 shows the distribution of normalized profile temperature along y-axis when H_1 changes, which is obtained from dataset of the second simulation stage. The distance between the highest temperature point and the 90% highest temperature point (namely $\boldsymbol{A}^{\mathrm{N}}(1)$ and $\boldsymbol{A}^{\mathrm{S}}(1)$) decreases from 2.31 mm to 1.65 mm when H_1 changes from 5 mm to 45 mm. The distribution of the isothermal point shrinks as the expansion of the copper layer. This is because increased copper layer area reduces the restrictions on thermal diffusion.

The relationship between the chip position and the average temperature rise of the top surface of the ceramic isolator is interpolated to get a function $\theta_{\text{iso}}(x,y)$, where x and y are the chip center position, θ means temperature rise (temperature minus coolant temperature). Absolute coordinate system is used. The function $\theta_{\text{iso}}(x,y)$ is shown in Fig. 8.

From Fig. 8, it can be found that the θ_{iso} decreases when the chip position deviates from the center of the direct bonded copper. This is because the thermal spread between the DBC and the heatsink is enhanced when the chip is near the edge of the DBC, and more heat is spread through the heatsink.

The relationship of the average temperature rise of the chip and copper trace to H_1 and W_1 are interpolated to get the function $\theta_{\text{die}}(H_1,W_1)$ and $\theta_{\text{trace}}(H_1,W_1)$. The 3-D graphs of $\theta_{\text{die}}(H_1,W_1)$ and $\theta_{\text{trace}}(H_1,W_1)$ are shown in Fig. 9(a) and (b).

It can be seen from Fig. 9 that $\theta_{\text{die}}(h_1,v_1)$ and $\theta_{\text{trace}}(h_1,v_1)$ change sharply when v_1 and h_1 are small, so the sample points need to be logarithmically spaced. It also proves that the impact of copper layer size on temperature distribution should be considered.

IV. Thermal Field Reconstruction

This section illustrates the method to reconstruct the temperature distribution by utilizing the dataset gathered in Section III and theoretical analysis. First, the effect of chip position and copper layer size on IPS is considered progressively for one heat source case. When the copper is etched, both the temperature distribution on the copper trace and the ceramic isolator top surface is analyzed. Then, the complete reconstruction process considering all heat sources is conducted by using superposition theorem [16].

A. Field Reconstruction With Unetched Copper Layer

Although the upper copper layer of DBC is always etched, it is still meaningful to study the heat distribution of the unetched state, as this study can clarify the influence of the chip position on the thermal distribution.

Supposing the chip center is (x_{ued},y_{ued}). The first step is to find out which triangle the center of the chip position belongs to in the triangular mesh shown in Fig. 4. Afterward the isothermal point matrix and maximum surface temperature rise are fitted with the isothermal point matrixes and maximum surface temperature rise from the dataset. Supposing the isothermal point matrixes when the chip center is at the triangle's vertices and at (x_{ued},y_{ued}) are $\boldsymbol{A}_{\mathrm{v1}}, \boldsymbol{A}_{\mathrm{v2}}, \boldsymbol{A}_{\mathrm{v3}}, \boldsymbol{A}_{\mathrm{ued}}$, respectively. The maximum surface temperature rise at the triangle's vertices and at position to be analyzed are M_{v1}, M_{v2}, M_{v3}, M_{ued}, respectively. The vertex coordinates of the triangle are (x_1,y_1), (x_2,y_2), (x_3,y_3), respectively. Then, $\boldsymbol{A}_{\mathrm{ued}}$ and M_{ued} can be obtained by linear fitting

$$\begin{aligned} \boldsymbol{A}_{\mathrm{ued}} &= \boldsymbol{A}_{\mathrm{v1}} + a(x_{\mathrm{d}} - x_1) + b(y_{\mathrm{d}} - y_1) \\ M_{\mathrm{ued}} &= M_{\mathrm{v1}} + c(x_{\mathrm{d}} - x_1) + d(y_{\mathrm{d}} - y_1) \end{aligned} \tag{3}$$

where

$$\begin{aligned} a &= [(\boldsymbol{A}_{\mathrm{v2}} - \boldsymbol{A}_{\mathrm{v1}})(y_3 - y_1) - (\boldsymbol{A}_{\mathrm{v3}} - \boldsymbol{A}_{\mathrm{v1}})(y_2 - y_1)]/e \\ b &= [(\boldsymbol{A}_{\mathrm{v2}} - \boldsymbol{A}_{\mathrm{v1}})(x_3 - x_1) - (\boldsymbol{A}_{\mathrm{v3}} - \boldsymbol{A}_{\mathrm{v1}})(x_2 - x_1)]/e \\ c &= [(M_{\mathrm{v2}} - M_{\mathrm{v1}})(y_3 - y_1) - (M_{\mathrm{v3}} - M_{\mathrm{v1}})(y_2 - y_1)]/e \\ d &= [(M_{\mathrm{v2}} - M_{\mathrm{v1}})(x_3 - x_1) - (M_{\mathrm{v3}} - M_{\mathrm{v1}})(x_2 - x_1)]/e \\ e &= (x_2 - x_1)(y_3 - y_1) - (x_3 - x_1)(y_2 - y_1) \neq 0 \end{aligned} \tag{4}$$

where a, b, c, d, e are the parameters introduced to perform the linear fit. They have no physical meaning.

To validate the fitting, the coordinate (x_{ued},y_{ued}) is selected randomly to generate a fitted IPS. Then, the temperature rise values of the same position are compared with FEM simulation results, the comparison results and the error are shown in Fig. 10, $x_{\mathrm{r}}y_{\mathrm{r}}z$ coordinate system is used.

Fig. 10 draws the point-to-side projection to illustrate the accuracy of the method. It can be found that the temperature rise at the given points matches well, the prediction error at the isothermal point is within 0.5 °C. Thus, the effectiveness of the computation method is verified.

Usually, the isotherm produced by the chip heat source is approximately elliptical [21], so in this article, two points are inserted in each quadrant for each isothermal level to form an elliptical shape isotherm, the coordinate is ($\boldsymbol{A}^{\mathrm{p}}(m)\times\cos(\varphi)$, $\boldsymbol{A}^{\mathrm{q}}(m)\times\sin(\varphi)$), where p is W or E depending on the quadrant of the point, q is N or S depending on the quadrant of the point, m means the mth isotherm. φ is a multiple of 30° and its value depends on the quadrant of the point, the result after inserting the isothermal point is shown in Fig. 11. Different color represents different temperature level. Compared with the red dots in Fig. 10, it can be found Fig. 11 adds 40 points to form an isotherm shape in nonaxis region.

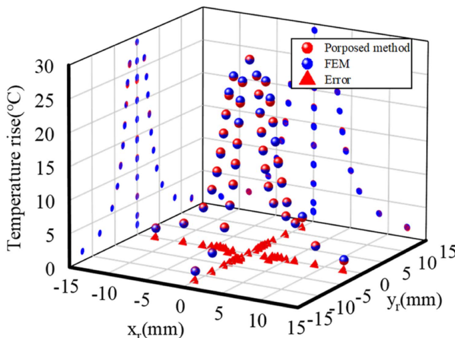


Fig. 10. Results comparison of the fitted isothermal point matrix and corresponding error.

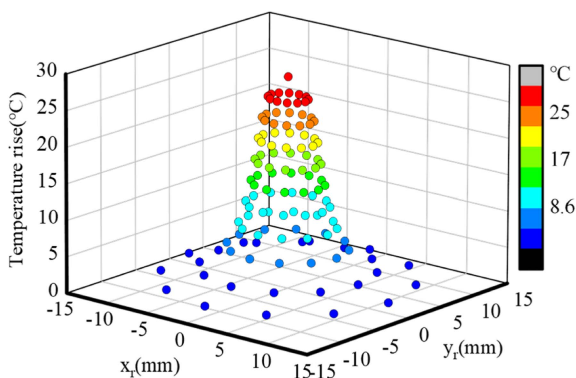


Fig. 11. Point set after elliptic expansion.

Then, a cubic spline interpolation is implemented to form the reconstructed field function F_{ued}, where F takes coordinates (x, y) as input and temperature rise as output. To verify the effect of this step, a reconstructed field when the chip is at a random position is generated and its results are compared with the field distribution of FEM, the result is shown in Fig. 12.

In Fig. 12, the top surface is the results of FEM, the middle surface is the results of the proposed approach, the bottom surface shows the area where the calculation error is less than 5% (Green color).

Fig. 12 shows that the reconstructed field is accurate at most positions, whether near the chip or slightly further away. Besides this, it also proves that the IPS is a valuable dimensionality reduction representation of the thermal field with unetched copper layer.

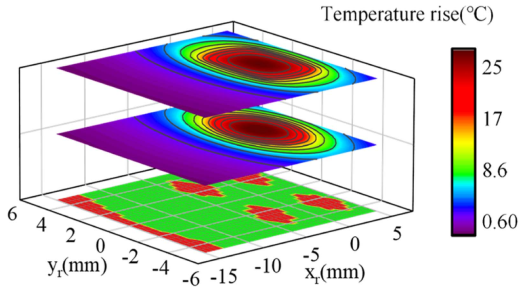


Fig. 12. Comparison result of the proposed approach and FEM.

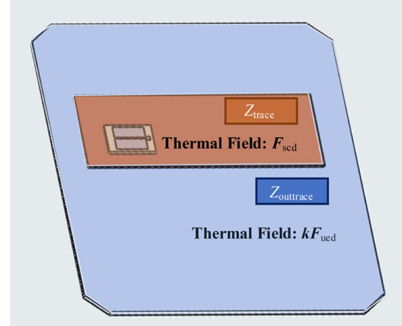


Fig. 13. Basic structure of the research object.

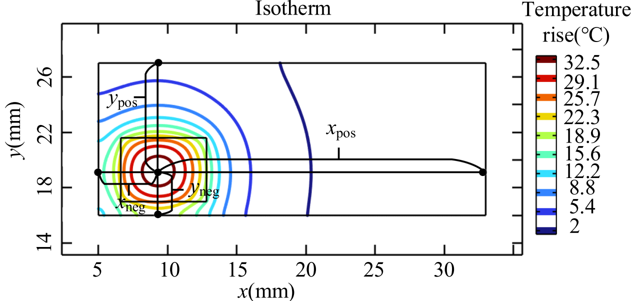


Fig. 14. Distance of the chip center to the edge of copper trace.

B. Field Reconstruction With Etched Copper Layer

The field reconstruction of the etched copper layer is the core content of this article. Fig. 13 shows the basic structure of the research object. This section consists of two parts, calculating the thermal field (F_{scd}) on the copper trace (Z_{trace} area, brown color) and estimating the thermal field (kF_{ued}) of the top ceramic isolator layer outside the trace (Z_{outtrace} area, blue color). It is based on the result of the unetched state F_{ued} and the dataset.

First, attention is focused on the evaluation of the temperature distribution at the top surface of the copper layer (Z_{trace} area). The distance of the chip center to the edge of the copper trace needs to be calculated, as shown in Fig. 14.

After that, entering the position of the chip center to the A segment of this section, the isothermal point matrix with unetched copper $\boldsymbol{A}_{\mathrm{ued}}$ can be obtained, and the isothermal point matrix ($\boldsymbol{A}_{\mathrm{scd}}$) of this case along each direction is modified based on the obtained $\boldsymbol{A}_{\mathrm{ued}}$.

Take the negative direction of the x-axis as an example, an isothermal point matrix with a $W_1 = 2x_{\mathrm{neg}}$ and $H_1 = y_{\mathrm{pos}}+y_{\mathrm{neg}}$ needs to be interpolated using the dataset of the second simulation stage. A linear interpolation is used as before. The interpolated matrix is denoted as $\boldsymbol{A}^{\mathrm{W}}{}_{\mathrm{xneg}}$. Let $\boldsymbol{A}_{\mathrm{full}}$ be the isothermal point matrix of the case when the trace is not etched and the chip is in the center. Treating each element of $\boldsymbol{A}^{\mathrm{W}}$ as a function of chip position $\mathbf{p} = (x_{\mathrm{cc}},y_{\mathrm{cc}})$ and copper layer information $\mathbf{t} = (x_{\mathrm{neg}},x_{\mathrm{pos}},y_{\mathrm{neg}},y_{\mathrm{pos}})$, i.e., $\boldsymbol{A}^{\mathrm{W}}{}_{\mathrm{scd}}(m) = g_{\mathrm{m}}(\mathbf{p},\mathbf{t})$, $\boldsymbol{A}^{\mathrm{W}}{}_{\mathrm{full}}(m) = g_{\mathrm{m}}(\mathbf{p}_0,\mathbf{t}_0)$, $m = 1$ to 10. The procedure uses the first-order term of the Taylor expansion of the function g_{m} to calculate the unknown $\boldsymbol{A}^{\mathrm{W}}{}_{\mathrm{scd}}$, as shown in (5).

Combing all the m terms in (5) forms the formula for calculating $\boldsymbol{A}^{\mathrm{W}}{}_{\mathrm{scd}}$, as shown in (6). Intuitively speaking, ($\boldsymbol{A}^{\mathrm{W}}{}_{\mathrm{xneg}}$-$\boldsymbol{A}^{\mathrm{W}}{}_{\mathrm{full}}$) is used as the correction factor of the etched copper layer. ($\boldsymbol{A}^{\mathrm{W}}{}_{\mathrm{ued}}$-$\boldsymbol{A}^{\mathrm{W}}{}_{\mathrm{full}}$) is used as the correction factor for changing chip position.

It should be noted that if $2x_{\mathrm{neg}}$ is larger than the width of the

$$\begin{aligned} g_m(\mathbf{p},\mathbf{t}) &\approx g_m(\mathbf{p}_0,\mathbf{t}_0) + \frac{\partial g_m(\mathbf{p}_0,\mathbf{t}_0)}{\partial \mathbf{p}_0} \bullet (\mathbf{p}-\mathbf{p}_0) + \frac{\partial g_m(\mathbf{p}_0,\mathbf{t}_0)}{\partial \mathbf{t}_0} \\ &\quad \bullet (\mathbf{t}-\mathbf{t}_0) \\ &\approx g_m(\mathbf{p}_0,\mathbf{t}_0) + \frac{\partial g_m(\mathbf{p}_\varepsilon,\mathbf{t}_0)}{\partial \mathbf{p}_\varepsilon} \bullet (\mathbf{p}-\mathbf{p}_\varepsilon) + \frac{\partial g_m(\mathbf{p}_0,\mathbf{t}_\xi)}{\partial \mathbf{t}_\xi} \\ &\quad \bullet (\mathbf{t}-\mathbf{t}_\xi) \\ &\approx g_m(\mathbf{p}_0,\mathbf{t}_0) + (g_m(\mathbf{p},\mathbf{t}_0) - g_m(\mathbf{p}_0,\mathbf{t}_0)) \\ &\quad + (g_m(\mathbf{p}_0,\mathbf{t}) - g_m(\mathbf{p}_0,\mathbf{t}_0)) \end{aligned} \tag{5}$$

$$\boldsymbol{A}^{\mathrm{W}}_{\mathrm{scd}} = \boldsymbol{A}^{\mathrm{W}}_{\mathrm{full}} + \left(\boldsymbol{A}^{\mathrm{W}}_{\mathrm{xneg}} - \boldsymbol{A}^{\mathrm{W}}_{\mathrm{full}}\right) + \left(\boldsymbol{A}^{\mathrm{W}}_{\mathrm{ued}} - \boldsymbol{A}^{\mathrm{W}}_{\mathrm{full}}\right) \tag{6}$$

unetched copper trace, then $W_1 = W_{\mathrm{bou}}$, where W_{bou} is the maximum width of the DBC's copper layer.

The correction of the matrix $\boldsymbol{A}_{\mathrm{scd}}$ in the other directions is the same, as shown in (7). After this process, the isothermal point matrix $\boldsymbol{A}_{\mathrm{scd}}$ is determined

$$\begin{aligned} \boldsymbol{A}^{\mathrm{E}}_{\mathrm{scd}} &= \boldsymbol{A}^{\mathrm{E}}_{\mathrm{xpos}} + \boldsymbol{A}^{\mathrm{E}}_{\mathrm{ued}} - \boldsymbol{A}^{\mathrm{E}}_{\mathrm{full}} \\ \boldsymbol{A}^{\mathrm{S}}_{\mathrm{scd}} &= \boldsymbol{A}^{\mathrm{S}}_{\mathrm{yneg}} + \boldsymbol{A}^{\mathrm{S}}_{\mathrm{ued}} - \boldsymbol{A}^{\mathrm{S}}_{\mathrm{full}} \\ \boldsymbol{A}^{\mathrm{N}}_{\mathrm{scd}} &= \boldsymbol{A}^{\mathrm{N}}_{\mathrm{ypos}} + \boldsymbol{A}^{\mathrm{N}}_{\mathrm{ued}} - \boldsymbol{A}^{\mathrm{N}}_{\mathrm{full}}. \end{aligned} \tag{7}$$

The maximum temperature rise at surface z = 0.3 mm also changes with the trace size and the chip position. The calculation process is based on the assumption that the maximum surface temperature rise is proportional to the thermal resistance underneath the chip solder. The thermal resistance from chip to ambient is studied first. Then, subtracting the 1-D thermal resistance of the chip and solder layer R_{cs} obtains the thermal resistance underneath the chip solder.

The thermal resistance from chip to ambient is equated to the parallel connection of four quadrant thermal resistances, as shown in Fig. 15(a). The four quadrant thermal resistances are calculated based on the geometry on the right side [see Fig. 15(b)]. They have the following characteristics.

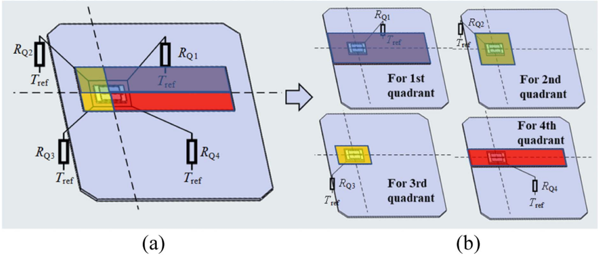


Fig. 15. Demonstration of the paralleled thermal resistance. (a) Structure to be analyzed. (b) Constructed structures for quadrant thermal resistance.

1) Identical to the structure on the left in given quadrant.
2) The copper layers are symmetric about the center of the chip.
3) If the copper layer is out of range when 1, 2 are satisfied, the copper layer is restricted to be within the possible range. (Geometry structure for quadrant 14)

After that, the quarter thermal resistance of Fig. 15(b) can be calculated based on the superimposed effect of chip position and copper layer size. The structure of the research object in this section is the same as the structure in Figs. 13 and 14. Using the geometry structure for first quadrant to illustrate the calculation step.

Supposing the average temperature rise of the chip with unetched copper and centered chip is

$$\theta_{\text{c}-\text{u}} = \theta_{\text{die}}(W_{\text{bou}}, H_{\text{bou}}) \tag{8}$$

where W_{bou} and H_{bou} is the size parameter of unetched copper layer, in this article, $W_{\text{bou}} = 38$ mm, $H_{\text{bou}} = 48$ mm.

Supposing the average temperature rise of the chip in the second simulation stage with $W_1 = 2x_{\text{pos}}$ and $H_1 = 2y_{\text{pos}}$ is

$$\theta_{c-G1} = \theta_{\text{die}}(2x_{\text{pos}}, 2y_{\text{pos}}). \tag{9}$$

Then, considering the influence of chip position by multiplying a correction factor $M_{\text{ued}}/\text{M}_{\text{c-u}}$, the average temperature rise of the chip in geometry structure for 1st quadrant can be estimated as

$$\theta_{G1} = (\theta_{c-G1} - R_{\text{cs}}P)\frac{M_{\text{ued}}}{M_{\text{c}-\text{u}}} + R_{\text{cs}}P \tag{10}$$

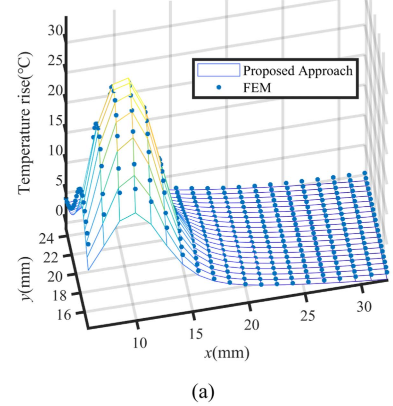
where $M_{\text{c-u}}$ is the maximum temperature rise of surface z = 0.3 with unetched copper and centered chip. Power loss is $P = 50$ W as mentioned before. R_{cs} is thermal resistance of the chip and solder layer.

After that, the quarter thermal resistance R_{Q1} of Fig. 15(b) can be calculated as

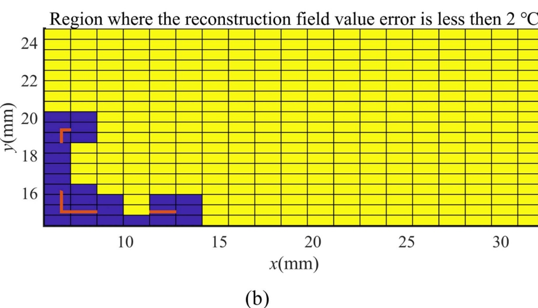
$$R_{\text{Q1}} = \frac{4\theta_{\text{G1}}}{P}. \tag{11}$$

Thus, the thermal resistance from chip to ambient in Fig. 13 can be calculated as

$$R_{\text{scd}} = \frac{1}{\frac{1}{R_{\text{Q1}}} + \frac{1}{R_{\text{Q2}}} + \frac{1}{R_{\text{Q3}}} + \frac{1}{R_{\text{Q4}}}}. \tag{12}$$



(a)



(b)

Fig. 16. Comparison result of the proposed approach and the FEM result. (a) Demonstration graph. (b) Region with absolute error <2 °C.

Subtracting R_{cs}, the thermal resistance underneath the chip solder can be obtained, as shown in

$$R_{\text{scdb}} = R_{\text{scd}} - R_{\text{cs}}. \tag{13}$$

Therefore, the modified maximum temperature rise in Fig. 14 at surface z = 0.3 mm is estimated by multiplying a correction factor. The correction factor is the ratio of thermal resistance in their respective structures

$$M_{\text{scd}} = \frac{R_{\text{scdb}}}{R_{\text{c}-\text{ub}}} M_{\text{c}-\text{u}} \tag{14}$$

where M_{scd} is the predicted maximum temperature rise of the surface z = 0.3 mm shown in Fig. 13; $R_{\text{c-u}}$ is the chip thermal resistance when the chip is centered and copper is unetched, and $R_{\text{c-u}} = \theta_{\text{c-u}}/P$, $R_{\text{c-ub}} = R_{\text{c-u}}$-$R_{\text{cs}}$ Afterward, the thermal field function F_{scd} can be reconstructed using A_{scd} and M_{scd}.

A single chip model is generated to verify the accuracy of this section's method, and the structure of the example is shown in Fig. 13. The comparison result between the proposed approach and the FEM result is shown in Fig. 16, only the thermal field on the copper is presented. It can be seen from Fig. 16 that the proposed approach can grasp the key parameter that influences the distribution of the thermal field. The error introduced by the approximation algorithm is within acceptable limits.

Then, the calculation of the thermal field in Z_{outtrace} area of Fig. 13 is demonstrated. First, an invariant $\theta_{\text{iso}}(x_{\text{c}},y_{\text{c}})$ is introduced. This variable is the average temperature rise of the ceramic isolator top surface, as mentioned in Section III.

$\theta_{\text{iso}}(x_{\text{c}},y_{\text{c}})$ basically does not change with the size of the trace, this can be verified by FEM simulation. Four simulations with

TABLE II
INFLUENCE OF TRACE SIZE TO THE TEMPERATURE RISE OF THE CERAMIC ISOLATOR LAYER

Chip position	Trace unetched	copper size =10mm×8mm	Difference
Center	1.86 °C	1.88 °C	0.78%
Bottom left corner	1.48 °C	1.47 °C	-0.57%

two chip positions and two copper trace sizes are conducted to verify this conclusion. The average temperature rise of the ceramic isolator top surface is recorded. The results are shown in Table II, and it can be found that the influence of the copper size on θ_{iso} is negligible.

It is known that the trace average temperature increases as the copper trace shrinks. An assumption is made that the top surface and bottom surface of the copper trace have the same temperature rise [20]. θ_{iso} is composed of the average temperature rise of the copper trace (Z_{trace} area, z = 0.3 mm) and the top surface of the ceramic isolator layer outside the copper trace ($\text{Z}_{\text{outtrace}}$ area, z = 0 mm). Therefore, the thermal field outside the copper trace can be estimated by multiplying a parameter k on the reconstructed thermal field F_{ued} to make θ_{iso} an invariant. Hence, the formula can be listed as (15), adding a formula (16) when copper is unetched and the chip is at specified position. Then, k can be calculated as (17). The integral is calculated using the trapezoidal formula

$$\iint_{T_{\text{trace}}} F_{\text{scd}} dS + k \iint_{Z_{\text{outtrace}}} F_{\text{ued}} dS = \theta_{\text{iso}} S_{\text{iso}} \tag{15}$$

$$\iint_{T_{\text{trace}}} F_{\text{ued}} dS + \iint_{Z_{\text{outtrace}}} F_{\text{ued}} dS = \theta_{\text{iso}} S_{\text{iso}} \tag{16}$$

$$k = \frac{\theta_{\text{iso}} S_{\text{iso}} - \iint_{Z_{\text{trace}}} F_{\text{scd}} dS}{\theta_{\text{iso}} S_{\text{iso}} - \iint_{Z_{\text{trace}}} F_{\text{ued}} dS} \tag{17}$$

where S_{iso} is the area of the top surface of the ceramic isolator layer.

C. Complete Reconstruction Demonstration of the Approach

Thermal conductivity can be considered constant when the temperature change is relatively small [12]. Evaluating the thermal distribution of different module layouts under a fixed operating condition fulfills this prerequisite. Thus, the superposition theorem can be used [22].

So far, a complete approach for modeling the thermal field has been proposed. A FEM thermal simulation and a thermal analysis using the proposed approach are conducted to verify the overall accuracy. The layout of the power module is shown in Fig. 2, the detailed layout is shown in Fig. 17. Obviously, the chips belong to two copper traces, so there are two types of thermal coupling, one is the thermal coupling in the same trace and the other is the thermal coupling in different traces.

The thermal field reconstruction result is shown in Fig. 18, to clearly show the accuracy of the approach proposed, the region in which reconstruction error is within 5% or 0.5 °C and 5% or 2 °C is painted yellow, as shown in Fig. 19 (red lines indicate chip edges).

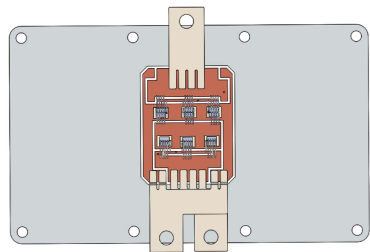


Fig. 17. Detailed layout of the power module.

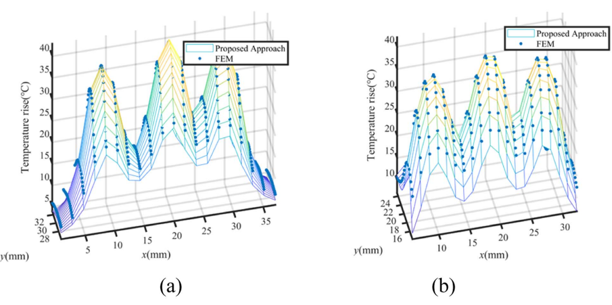


Fig. 18. Comparison between the proposed approach and the FEM result. (a) Upper bridge. (b) Lower bridge.

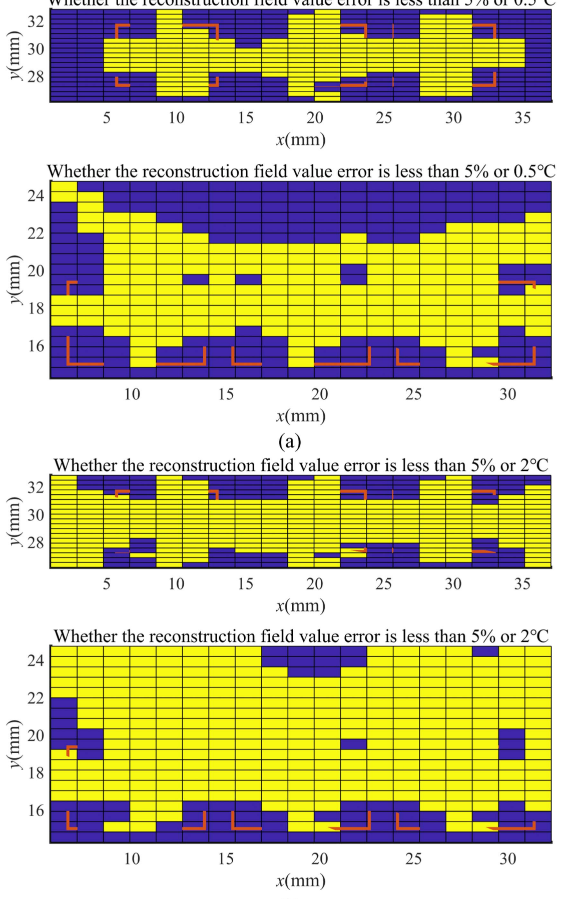


Fig. 19. Region in which a given error can be maintained. (a) When the given error level is 5% or 0.5 °C. (b) When the given error level is 5% or 2 °C.

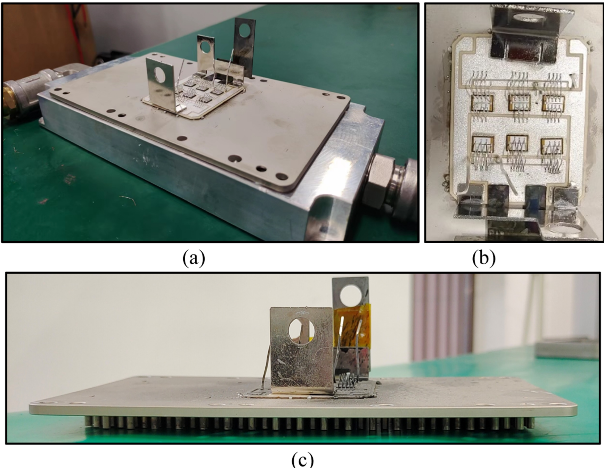


Fig. 20. Fabricated power module. (a) View 1. (b) View 2. (c) View 3.

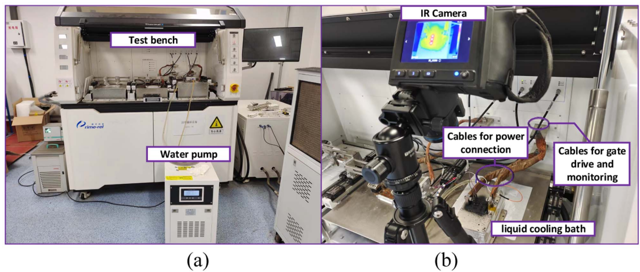


Fig. 21. (a) Overview of the test bench. (b) Test devices and measuring instruments.

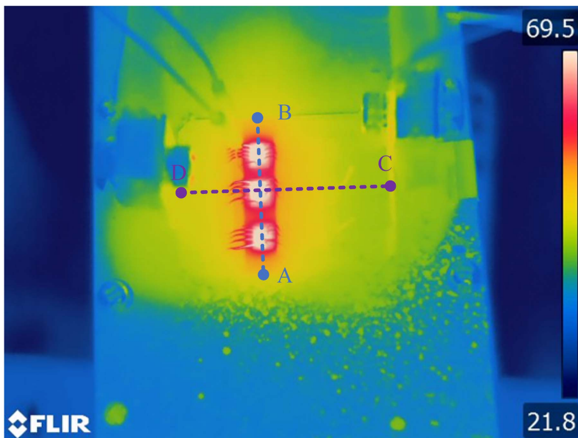


Fig. 22. Thermal image of the power module.

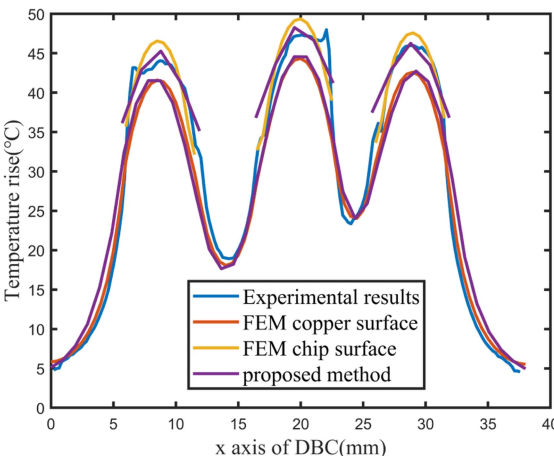


Fig. 23. Comparison among the experiment, FEM, and the proposed approach along line AB.

The comparison results verified the accuracy of the proposed approach. The calculation time using FEM is approximately 120 s with 1 million mesh number and a GMRES solver [23]. The time consumed by using the proposed approach is roughly 0.2 s. The temperature distribution inside the chip can be calculated using the FDM. With the temperature distribution at z = 0.3 surface as the boundary condition, the calculation speed can be very fast. If the chip temperature distribution is also calculated, the time consumed will be extended to roughly 0.35 s. The proposed approach can increase the calculation speed by roughly 300 times.

V. Verification of the Approach

A. Introduction of the Test Bench and Test Condition

An experiment is conducted to verify the feasibility of the proposed approach. A power module is fabricated, as shown in Fig. 20. The chips are taken from the same wafer to ensure parameter consistency. The silver-plated copper-clad ceramic substrate is used to reduce welding difficulty.

After that, black paint is sprayed over the top surface of the power module to unify the emissivity. The value of the emissivity setting used in this work is 0.94.

Then, the power module is placed on the test bench, as shown in Fig. 21(a). It is a multifunctional testing equipment for the thermal characteristics of power modules. The power module after black painting is put in a liquid cooling bath, as shown in Fig. 20(a), and the water pump is used to circulate the coolant.

The detailed view of the test bench is shown in Fig. 21, the temperature is measured using the infrared camera. The experiment is implemented on the upper bridge of the power module, and a dc current source is used to heat the power module. To reduce the self-heating effect of the bond wire, a constant $V_{gs} = 10$ V is held on the power module, in this condition, the voltage drop of the SiC MOSFET is larger than normal. The current value of the current source is set as 60 A, and the voltage drop of the power module is $V_{ds} = 2.843$ V. Hence, it can be calculated that $P_{\text{Chip1}} = P_{\text{Chip2}} = P_{\text{Chip3}} = 56.86$ W.

B. Comparison Among the Experiment, FEM, and the Proposed Approach

Fig. 22 shows the thermal image of the power module, the temperature rise along line AB(y = 29.41 mm) and its comparison with FEM and the proposed approach is shown in Fig. 23. The temperature rise comparison results along line CD(x = 19.5 mm) is shown in Fig. 24.

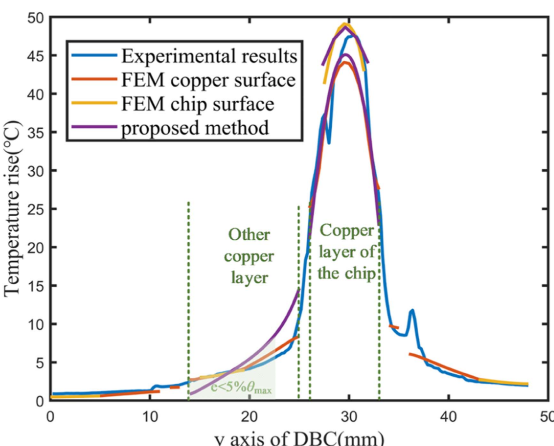


Fig. 24. Comparison among the experiment, FEM, and the proposed approach along line CD.

As can be seen from Fig. 23, over the copper layer, the results of the modeling method (FEM and the proposed approach) and the experiment match well, while over the chip surface, the thermal distribution differs. This is because the power loss distribution is uneven inside the chip, power loss is mostly concentrated near the source plate. Near the gate, chip loss is small [24]. Besides this, the self-heating effect of bond wires will also cause some temperature changes.

From Fig. 24, it can be found that the proposed approach has excellent prediction accuracy in the copper layer where the chips are located. it can also be found that the reconstruction of the thermal field over the copper layer at other trace have some errors, but the prediction accuracy is also sufficient for thermal analysis in the design phase. The shaded area indicates the point where the error is less than 5% of the highest temperature rise of the copper layer, which is 81.8% of the total length.

From the experiment result in Fig. 22, the temperature rise at the edge of the chip is about 70% of the temperature rise at the chip center. As power loss keep increasing, thermal distribution inside the module may requires more refined analysis. This is because the temperature imbalance inside the chip will influences the temperature-sensitive electrical parameters, like the value of internal gate resistance [25] and voltage drop [24], [26], [27], [28]. The approach proposed can be used for more precise modeling if the dataset is constructed with a metacellular structure or part of chip as the heat source [29]. The thermal distribution with uneven loss is obtained by superimposing the thermal field of each cell. Additionally, with the thermal distribution, the approach provides a foundation for mechanical stress calculations.

C. Comparison Among Different Approaches

A comparison with the approaches mentioned in the introduction is presented in Table III. The accuracy of the FEM is verified by the experiment. Therefore, FEM results are used as the reference for calculating error. The two power loss conditions are imposed on the power module, one is six chips with 50 W loss each, the other is three chips in upper bridge with 58.86 W loss each. Thus, the condition with uneven power loss between upper and lower bridge is considered. The maximum single chip thermal resistance calculation error is recorded in the error column in Table III. Due to the complexity of 3-D nodal resistor network method, its data are extracted from the reference paper. It is important to note that both the Fourier series based approach and the Green's function based approach have a high level of accuracy. In both approaches, the copper layer is subjected to a surface heat source with uniformly distributed normal heat flux, resulting in an overestimation of the temperature. This overestimation compensates for the underestimation caused by the neglect of layouts. As can be seen from Table III, the proposed approach has a high accuracy and speed.

TABLE III
COMPARISON OF CURRENT RAPID THERMAL MODELING APPROACHES

Types	Approach	Computation time	Maximum R_{th} Error	Thermal distribution availability
Numerical	Finite element method (FEM)	120 s	~	Yes
	Finite volume method (FVM)	213 s		
	3-D nodal resistor network method*	~60 s[30]	<5%[30]	Yes
		<1 s[9]	~10%[13]	
Analytical	Heat spreading angle	<1 s	17.36%	No
	Fourier series based approach	7.5 s	3.91%	Yes
	Green function based	<1 s	3.99%	Yes
Data-driven	Machine-learning based	<1 s	6.34%	Yes
Hybrid	Spreading resistance based	<1 s	8.00%	No
	Proposed approach	0.35 s	2.32%	Yes

*means the data is from the reference paper

VI. CONCLUSION

This article proposed a hybrid data-driven and mechanistic modeling approach for rapid thermal analysis. Its framework follows the sequence of dataset collection, dimensionality reduction, theoretical analysis, and thermal field reconstruction. By using this approach during the design stage, the calculation speed of the thermal field distribution can be increased by approximately 300 times, thereby improving design efficiency. The accuracy of the approach is verified by comparing it with FEM and experimental results. The approach presented in this article can provide an efficient and reliable tool for the design of power modules.

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