High-Precision Time-Domain Analysis Method Based on the Superposition Principle for CLLC Converter in Above-Resonant-Frequency Mode

Longteng Jiao, Lei Li, *Member, IEEE*, Cheng Wang, *Member, IEEE*, Shanlu Zhang, Borui Liu, and Xiongfeng Fang

***Abstract*—The CLLC converter is widely used in applications requiring highly efficient bidirectional power flows. However, multiple resonant components make its modeling and analysis quite challenging, hence, hard to reach a higher operating efficiency. In this article, the method based on the superposition principle is proposed to provide a more accurate analysis for CLLC converters in the above-resonant-frequency-mode (ARFM) and simplified time-domain analysis is employed for below-resonant-frequency mode. First, the principle of the novel method is analyzed within the introduction of the operating modes for CLLC converter. Then, the time-domain expressions regarding the voltage-gain, resonant currents, and resonant voltages are derived by using the proposed method in ARFM. Afterward, the soft-switching conditions are then redefined in a more accurate way. More detailed synchronous-rectification (SR) timings are derived, which is followed by the optimal hardware parameter design. The proposed concept is finally verified through a 1.5-kW resonant CLLC prototype. The experiment has confirmed that the voltage gain and peak values are consistent with the theoretical calculations. And the operating efficiency is improved by 1.8% with the accurate soft-switching and SR compared with the uncontrolled rectification as confirmed by experimental results. Furthermore, the proposed method surpasses the time-domain analysis method to implement SR considering the parasitic capacitance of switches.**

***Index Terms*—Above-resonant-frequency mode (ARFM), CLLC converter, simplified time-domain analysis (STDA), superposition principle (SP), synchronous rectification (SR).**

I. Introduction

ELECTRIC vehicles (EVs) with vehicle-to-grid capabilities are becoming an increasingly common choice due to their ability to store renewable energy, helping to achieve the supply-demand balance [1], [2], [3], [4], [5], [6]. These EVs are equipped with bidirectional dc–dc converters that enable power transmission to and from the grid. *LLC* converter is one of the potential resonant converters [7], [8] that can achieve high efficiency and high-power density. However, when it operates in reverse mode, the circuit is actually the same as an *LC* resonant converter and can only function in step-down conditions. Therefore, it is not commonly used in scenarios requiring bidirectional power flow [9]. To ensure optimal *LLC* characteristics in both forward and reverse operations, the CLLC converter was first derived in the literature [10], [11]. In either operation condition, it can be regarded as an *LLC* converter and has all the advantages of *LLC* converter, i.e., high power density and high operating efficiency [12].

The analysis of CLLC converter is typically conducted using the fundamental harmonic approximation (FHA) [11], [13], [14]. However, it results in higher voltage gain errors when the frequency significantly deviates from the resonant frequency. To address this issue, the extended harmonics approximation (EHA) method has been proposed as an improvement on the FHA [15], as it includes multiple harmonics in its calculation range and, thus, increases voltage gain calculation accuracy.

The study conducted in [16] suggested the use of time-domain analysis (TDA) for modeling the CLLC converter. Theoretically, the state variable values can be obtained by combining boundary conditions of different operating modes [17]. To cater to a wide voltage range, Zhao et al. [18] proposed the parameter equivalent principle. However, due to the transcendental equations of TDA, no formula can guide the design. To obtain the analytical solution of the CLLC converter, a precise analysis method based on state-plane analysis was proposed in above-resonant-frequency mode (ARFM) [19]. This method decouples the high-order system into two lower order systems. However, it is still quite complicated to calculate and solve the two decoupling equations. A method proposed by Wei et al. [20] simplified the analysis of design parameters by considering O-mode as flat and disregarding the transient N-mode. However, this approach only provides gain.

In recent years, researchers have focused on further improving the operating efficiency of CLLC converter. One newly emerging technique is synchronous rectification (SR), which can eliminate the voltage drop of each body diode, thus improving the converter's efficiency [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32]. SR uses switch channels as a replacement for body diode rectification. However, since the drive signal for SR of the secondary-side switches cannot be obtained directly, the implementation of SR normally uses voltage and current detection. Voltage detection relies on detecting voltage drops

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of body diodes [21]. However, the voltage drops across the semiconductors are often susceptible to external interference and parasitic parameters. In contrast, the current sensing method utilizes the current sensor to determine the SR signal based on its polarity [22]. The output signal amplitude of the current sensor is high, making it less susceptible to the interference and parasitic parameters. Chen et al. [23] proposed an SR method that utilizes the detection of the resonant inductor voltage to reflect the resonant current. The controller generates an SR signal based on the polarity of the resonant current. However, this method becomes less cost-effective due to the additional current and voltage sensors required. Various methods have been proposed by researchers to analyze the phase of the secondary-side current without additional sensors, i.e., the phase-shift-based SR scheme and the FHA method [24], [25], [26], [27]. The FHA method is an approximate analysis method that would lead to considerable switching errors, especially outside the resonance region. The EHA method can help to improve the accuracy but is difficult to calculate online [28]. Other methods such as the Fourier decomposition and three-order fitting models have also been suggested to reduce input ripple current and achieve a smooth response [29], [30]. However, these methods are majorly derived from the FHA method since the time-domain model requires numerical iteration, which is impractical for real-time calculation [31], [32].

This article proposes the superposition principle (SP) method that is done within an equivalent circuit that reflects a combination of steady-state response and transient response in ARFM. By replacing one normal mode with a quasi-operating mode, the method can simplify the time domain analysis. The proposed SP enables a comprehensive and detailed analysis of ARFM. The model SP becomes challenging due to structural changes in below-resonant-frequency mode (BRFM). Thus, simplified time-domain analysis (STDA) method is employed for solving BRFM by reasonably simplifying the O-mode. The accuracy of the calculated voltage gain and peak values of resonant current and voltage is superior to that of FHA, while its equations are simpler than those of TDA and EHA. Moreover, the method can calculate the switching time to achieve SR, thereby enhancing the overall efficiency of the system.

The rest of this article is organized as follows. In Section I, the modeling methods and the SR schemes of the CLLC converter have been reviewed and summarized in detail. Section II proposes method based on SP and employs STDA to obtain accurate voltage gain in BRFM and ARFM. Section III utilizes proposed method to analysis resonant current and voltage expressions, soft-switching conditions, SR timings, and loss calculations. Section IV presents the parameter design and control system. Afterwards, the validity of the proposed method is verified through experimental results. Finally, Section V concludes this article.

II. Operating Modes Derivation of the CLLC Converter

As shown in Fig. 1, there are five resonant elements in the CLLC converter topology, which are the resonant inductors L_{r1},

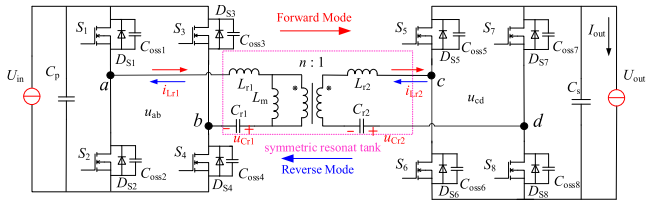

Fig. 1. Topology of the CLLC converter.

TABLE I
Exchanging the Notations for the Forward and the Reverse Power Transfer Modes

Forward		Reverse
$U_1 (= U_{in})$	↔	$U_2' (= U_{in} / n)$
$L_1 (= L_{r1})$	↔	$L_2' (= L_{r1} / n^2)$
$C_1 (= C_{r1})$	↔	$C_2' (= n^2 C_{r1})$
$L_m (= L_m)$	↔	$L_m' (= L_m / n^2)$
$L_2 (= n^2 L_{r2})$	↔	$L_1' (= L_{r2})$
$C_2 (= C_{r2} / n^2)$	↔	$C_1' (= C_{r2})$
$U_2 (= nU_{out})$	↔	$U_1 (= U_{out})$

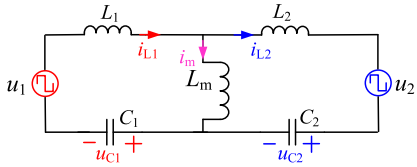

Fig. 2. Equivalent circuit of the CLLC converter in forward mode.

L_{r2} and the transformer excitation inductor L_m, the resonant capacitors C_{r1} and C_{r2}. The transformer turn-ratio is n:1. Exchanging the notations for the forward and the reverse power transfer mode is presented in Table I [19]. The equivalent circuit of the CLLC converter in forward mode is illustrated in Fig. 2. To unify the characteristics in charging and discharging mode, the symmetrical resonant parameters of CLLC converter should be satisfied [20]

$$\begin{cases} L_1 = L_2 = L_{r1} = n^2 L_{r2} \\ C_1 = C_2 = C_{r1} = C_{r2}/n^2 \end{cases}. \tag{1}$$

This symmetrical structure allows for the same analysis of forward and reverse power flow, then only the former being discussed in this article. The definition of the resonant frequency f_r, characteristic impedance Z_r, and inductance coefficient k is expressed as

$$\begin{cases} f_r = \frac{1}{2\pi\sqrt{L_{r1}\cdot C_{r1}}} = \frac{1}{2\pi\sqrt{L_{r2}\cdot C_{r2}}} \\ Z_r = \sqrt{\frac{L_{r1}}{C_{r1}}} = \sqrt{\frac{L_{r2}}{C_{r2}}} \\ k = \frac{L_m}{L_{r1}} = \frac{L_m}{n^2 L_{r2}}. \end{cases} \tag{2}$$

A. TDA Model Establishment

According to the different combinations of ON and OFF switches of the CLLC converter, the operational state can be divided into six modes. The CLLC converter has a half-cycle symmetric operating mode in one cycle. To simplify the analysis,

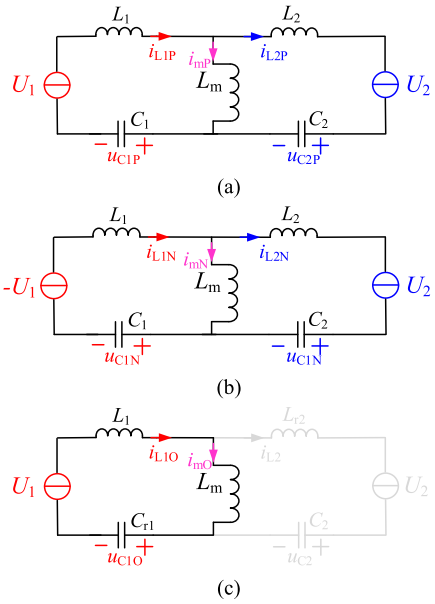

Fig. 3. Equivalent circuit of CLLC converter. (a) P-mode. (b) N-mode. (c) O-mode.

only three modes within half period are analyzed, as shown in Fig. 3.

1) P-mode [see Fig. 3(a)]: The primary and secondary-side switches S_1, S_4, S_5, and S_8 turn ON. The input voltage of the primary-side resonant tank u_{ab} is U_1, and the output voltage of resonant tank u_{cd} is U_2. According to the law of Kirchhoff, the circuit can be established as

$$\begin{cases} L_m \frac{di_{mP}}{dt} + L_1 \frac{di_{L1P}}{dt} + u_{C1P} = U_1 \\ L_2 \frac{di_{L2P}}{dt} + u_{C2P} + U_2 = L_m \frac{di_{mP}}{dt} \\ i_{L1P} = C_1 \frac{du_{C1P}}{dt} \\ i_{L2P} = C_2 \frac{du_{C2P}}{dt} \\ i_{L1P} = i_{L2P} + i_{mP}. \end{cases} \tag{3}$$

By solving (3), the time-domain equations of P-mode are derived as

$$\begin{cases} i_{L1P}(t) = P_1 \sin(\omega_r t + \varphi_1) + P_2 \sin(\omega_{k1} t + \varphi_2) \\ i_{L2P}(t) = P_1 \sin(\omega_r t + \varphi_1) - P_2 \sin(\omega_{k1} t + \varphi_2) \\ u_{C1P}(t) = -Z_r P_1 \cos(\omega_r t + \varphi_1) \\ \qquad\quad -P_2 \frac{Z_r}{k_1} \cos(\omega_{k1} t + \varphi_2) + U_1 \\ u_{C2P}(t) = -Z_r P_1 \cos(\omega_r t + \varphi_1) \\ \qquad\quad +P_2 \frac{Z_r}{k_1} \cos(\omega_{k1} t + \varphi_2) - U_2 \end{cases} \tag{4}$$

where $k_1 = 1 / \sqrt{1+2k}$; $\omega_r = 1 / Z_r$; $\omega_{k1} = k_1 \omega_r$; P_1, P_2, φ_1, and φ_2 are the unknown parameters related to the initial state of the circuit.

2) N-mode [see Fig. 3(b)]: The primary and secondary-side switches S_2, S_3, S_5, and S_8 turn ON. The input voltage of the primary-side resonant tank u_{ab} is $-U_1$, and the output voltage of resonant tank u_{cd} is U_2. By the same solution as P-mode, the time-domain equations of N-mode

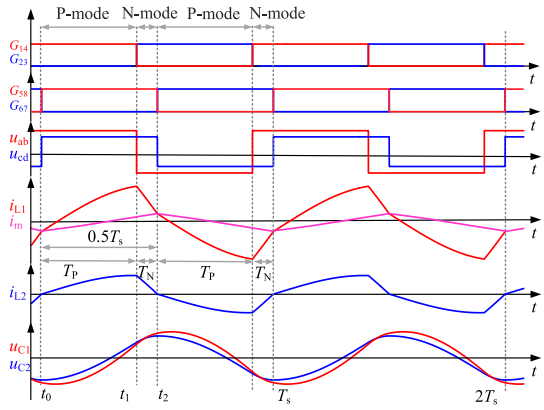

Fig. 4. Typical CLLC converter waveforms in ARFM.

are described as

$$\begin{cases} i_{L1N}(t) = P_3 \sin(\omega_r t + \varphi_1) + P_4 \sin(\omega_{k1} t + \varphi_2) \\ i_{L2N}(t) = P_3 \sin(\omega_r t + \varphi_1) - P_4 \sin(\omega_{k1} t + \varphi_2) \\ u_{C1N}(t) = -Z_r P_3 \cos(\omega_r t + \varphi_1) \\ \qquad\quad -P_4 \frac{Z_r}{k_1} \cos(\omega_{k1} t + \varphi_2) - U_1 \\ u_{C2N}(t) = -Z_r P_3 \cos(\omega_r t + \varphi_1) \\ \qquad\quad +P_4 \frac{Z_r}{k_1} \cos(\omega_{k1} t + \varphi_2) - U_2. \end{cases} \tag{5}$$

3) O-mode [see Fig. 3(c)]: The secondary-side switches turn OFF. The input voltage of the primary-side resonant tank u_{ab} is U_1. The expressions of state variables can be described as

$$\begin{cases} i_{L1O}(t) = i_{mO}(t) = I_{1O} \sin(\omega_{k2} t + \varphi_{1O}) \\ u_{C1O}(t) = -I_{1O} \frac{Z_r}{k_2} \cos(\omega_{k2} t + \varphi_{1O}) + U_1 \end{cases} \tag{6}$$

where $k_2 = 1 / \sqrt{1+k}$; $\omega_{k2} = k_2 \omega_r$; I_{1O} and φ_{1O} are the unknown parameters related to the initial state of the circuit.

As the switching frequency f_s varies, the CLLC converter can be divided into operation stages PO, PON, PN, NP, NOP, OP, OPO, P, and O-mode. Among them, the stages that contain O-stages without O-mode are continuous conduction mode (CCM) [19]. Moreover, the PO-mode is expected because of its soft-switching characteristics in BRFM ($f_s < f_r$) [33]. Besides, the required NP-mode works in ARFM ($f_s > f_r$), and P-mode only operates in resonant-frequency mode (RFM) ($f_s = f_r$).

B. Solving ARFM Based on Superposition Principle

The ARFM of CLLC converter works in CCM, as shown in Fig. 4. The structure remains unchanged except for the positive and negative terminals of the primary and secondary-side resonant cavity voltage u_{ab} and u_{cd}, which means that the N-mode can be decomposed by using SP. To solve the time-domain equation, N-mode can be separated as P-mode plus NO-mode, as shown in Fig. 5. This model decomposition, which utilizes the SP, is equivalent. The P-mode remains unchanged, maintaining consistency with the previous P-mode, while the NO-mode represents zero state response. The equivalent circuit waveforms are shown in Fig. 6.

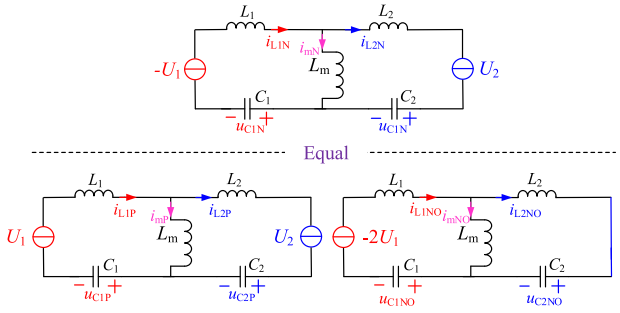

Fig. 5. Equivalent circuit of CLLC converter based on the SP in N-mode.

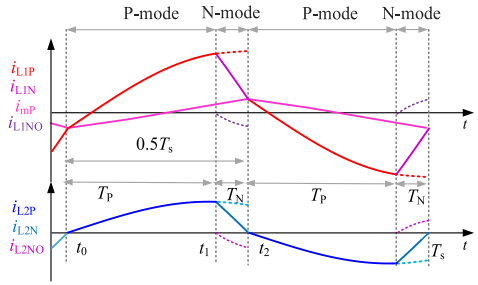

Fig. 6. Equivalent circuit waveforms of CLLC converter based on the SP in ARFM.

Assuming k is small, large cyclic nonactive power will be generated, resulting in increased loss and reduced efficiency. Therefore, k is generally larger than 3. The expressions of NO-mode are shown as follows:

$$\begin{cases} i_{\mathrm{L1NO}}(t) = -\frac{U_1}{Z_\mathrm{r}}\sin(\omega_\mathrm{r}t) - \frac{k_1U_1}{Z_\mathrm{r}}\sin(\omega_{\mathrm{k1}}t) \approx -\frac{U_1}{Z_\mathrm{r}}\sin(\omega_\mathrm{r}t) \\ i_{\mathrm{L2NO}}(t) = -\frac{U_1}{Z_\mathrm{r}}\sin(\omega_\mathrm{r}t) + \frac{k_1U_1}{Z_\mathrm{r}}\sin(\omega_{\mathrm{k1}}t) \approx -\frac{U_1}{Z_\mathrm{r}}\sin(\omega_\mathrm{r}t). \end{cases} \tag{7}$$

When time progresses from t_1 to t_2, the P-mode expressions can be obtained from (2) and NO-mode expressions can be derived by (4) after N-mode decomposition. Based on SP, the expressions of state variable in N-mode are presented as follows:

$$\begin{cases} i_{\mathrm{L1N}}(t) = i_{\mathrm{L1P}}(t) - \frac{U_1}{Z_\mathrm{r}}\sin\left(\omega_\mathrm{r}(t-t_1)\right) \\ i_{\mathrm{L2N}}(t) = i_{\mathrm{L2P}}(t) - \frac{U_1}{Z_\mathrm{r}}\sin\left(\omega_\mathrm{r}(t-t_1)\right) \\ u_{\mathrm{C1N}}(t) = u_{\mathrm{C1P}}(t) + U_1\cos\left(\omega_\mathrm{r}\left(t-t_1\right)\right) \\ u_{\mathrm{C2N}}(t) = u_{\mathrm{C2P}}(t) + U_1\cos\left(\omega_\mathrm{r}\left(t-t_1\right)\right) - U_1 - U_2. \end{cases} \tag{8}$$

Within half a period, i_m is described as follows:

$$i_\mathrm{m}(t) = i_{\mathrm{L1}}(t) - i_{\mathrm{L2}}(t) = 2P_2\sin\left(\omega_{\mathrm{k1}}t + \varphi_2\right). \tag{9}$$

According to the inductance current and capacitance voltage continuity and symmetry principles, the following conditions should be satisfied:

$$\begin{cases} i_{\mathrm{L2P}}(0) = i_{\mathrm{L2N}}\left(\frac{T_\mathrm{s}}{2}\right) = 0 \\ i_{\mathrm{mP}}(0) + i_{\mathrm{mN}}\left(\frac{T_\mathrm{s}}{2}\right) = 0 \\ u_{\mathrm{C1P}}(0) + u_{\mathrm{C2P}}(0) = -u_{\mathrm{C1N}}\left(\frac{T_\mathrm{s}}{2}\right) - u_{\mathrm{C2N}}\left(\frac{T_\mathrm{s}}{2}\right) \\ u_{\mathrm{C1P}}(0) - u_{\mathrm{C2P}}(0) = -u_{\mathrm{C1N}}\left(\frac{T_\mathrm{s}}{2}\right) + u_{\mathrm{C2N}}\left(\frac{T_\mathrm{s}}{2}\right). \end{cases} \tag{10}$$

In addition, the output current I_{out} is equal to the average value of the secondary-side current after rectification in half a cycle, where $R = n^2r$. r is the actual load resistance and R is the output resistance according to the transformer ratio n

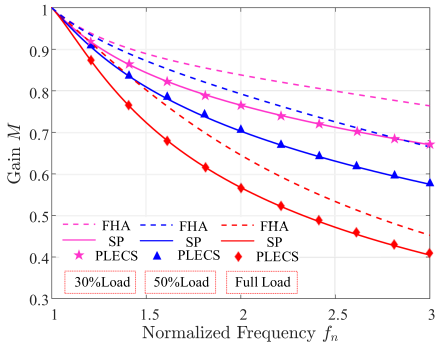

Fig. 7. Voltage gain M of FHA, SP, and PLECS.

$$\frac{2}{T_\mathrm{s}}\left(\int_{t_0}^{t_1} i_{\mathrm{L2P}}dt + \int_{t_1}^{t_2} i_{\mathrm{L2N}}dt\right) = \frac{U_2}{R}. \tag{11}$$

The implicit function of the voltage gain M is described as follows by combining (8)–(11):

$$\begin{aligned} 4 = &\left[A + A\cos\left(\frac{\pi}{f_\mathrm{n}}\right) + B(1+M)\sin\left(\frac{\pi}{f_\mathrm{n}}\right) + 2M\right]^2 \\ &+ \left[A\sin\left(\frac{\pi}{f_\mathrm{n}}\right) - B(1+M)\cos\left(\frac{\pi}{f_\mathrm{n}}\right) - B(1+M)\right]^2 \end{aligned} \tag{12}$$

where A, B, M and normalized frequency f_n are expressed as

$$\begin{cases} A = \left(\frac{\pi M Z_\mathrm{r}}{f_\mathrm{n}R} + 1 - M\right) \\ B = \frac{1}{\sqrt{1+2k}}\cdot\tan\left(\frac{\pi}{2\sqrt{1+2k}f_\mathrm{n}}\right) \\ M = \frac{U_2}{U_1} \\ f_\mathrm{n} = \frac{f_\mathrm{s}}{f_\mathrm{r}}. \end{cases} \tag{13}$$

Fig. 7 illustrates the comparison of the voltage gain M obtained from (12), FHA, and simulation by PLECS. According Fig. 7, the voltage gain of SP matches the actual voltage gain curve well. The error of FHA is 11%, while the error of the method in [20] is 18%. In contrast, the error of this article is 2% when $f_\mathrm{n} = 3$ under full load conditions.

C. Solving BRFM Based on Simplified Time-Domain Analysis

The BRFM of CLLC converter works in DCM. The primary-side resonant current i_{L1} rises in a sinusoidal form for half cycle lasting $0.5T_\mathrm{P}$, as shown in Fig. 8. Then, it intersects with the excitation current and entering O-mode. In O-mode, the excitation inductance participates in resonance, resulting in an extended resonance period and a gradual flattening. Solving for the O-mode primarily depends on the voltage of resonant capacitor at the end of P-mode. According to Appendix, the relationship of voltage at the end of P-mode can be expressed as

$$U_1 - u_{\mathrm{C1P}}(T_\mathrm{P}) \approx U_2 - u_{\mathrm{C2P}}(T_\mathrm{P}). \tag{14}$$

Because the extended resonance period of O-mode leads to a smoother change in excitation current, so O-mode can be

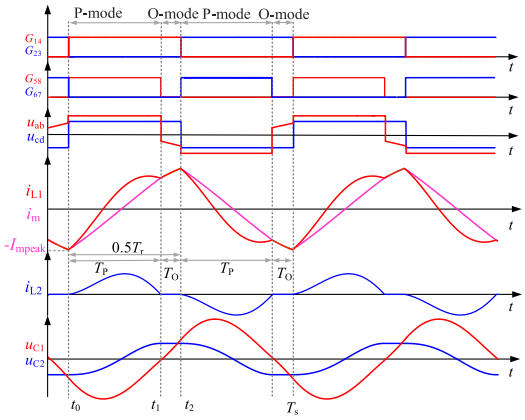

Fig. 8. Typical CLLC converter waveforms in BRFM.

simplified to a straight-line form. The expression of O-mode is derived by simplified time-domain as follows:

$$i_{\mathrm{L1O}}(t) = i_{\mathrm{mO}}(t) = i_{\mathrm{mP}}(t_1) + \frac{U_2 - u_{\mathrm{C2P}}(t_1)}{L_\mathrm{r} + L_\mathrm{m}}(t - t_1). \quad (15)$$

According to the capacitance calculation formula, it can be derived as

$$u_{\mathrm{C2O}}(t_2) - u_{\mathrm{C2P}}(t_0) = \frac{1}{C_2}\int_{t_0}^{t_2} i_{\mathrm{L2}} dt. \quad (16)$$

The u_{C2} remains constant during O-mode. Combining (10), $u_{C2}(t_1)$ is derived as

$$-u_{\mathrm{C2P}}(t_0) = u_{\mathrm{C2P}}(t_1) = u_{\mathrm{C2O}}(t_2) = \frac{\pi Z_\mathrm{r} U_2}{2 f_\mathrm{n} R}. \quad (17)$$

Additionally, u_{C1} is sufficiently charged during P-mode under heavy or full load conditions. Thus, the voltage across inductance L_1 is relatively small, which can be considered that the excitation current remains constant during O-mode [20].

According to the symmetry of the current, which should be satisfied as

$$\begin{cases} i_{\mathrm{L1P}}(0) + i_{\mathrm{L1P}}(T_\mathrm{P}) = 0 \\ i_{\mathrm{L2P}}(0) = i_{\mathrm{L2P}}(T_\mathrm{P}) = 0. \end{cases} \quad (18)$$

In heavy load, the duration time of P-mode is derived as

$$T_\mathrm{P} = \frac{T_\mathrm{r}}{2}. \quad (19)$$

The resonant capacitor requires to satisfy symmetry, which should be expressed as

$$\begin{cases} u_{\mathrm{C1P}}(0) + u_{\mathrm{C1O}}\left(\frac{T_\mathrm{s}}{2}\right) = 0 \\ u_{\mathrm{C2P}}(0) + u_{\mathrm{C2O}}\left(\frac{T_\mathrm{s}}{2}\right) = 0. \end{cases} \quad (20)$$

By solving (18)–(20), the voltage gain M of BRFM is described as

$$M = \frac{1}{1 - \frac{\pi}{\sqrt{1+2k}} \tan\left(\frac{\pi}{2\sqrt{1+2k}}\right)\left(\frac{1}{f_\mathrm{n}} - 1\right)}. \quad (21)$$

The voltage gain can be obtained by derivation formula under heavy load [20]. The variation of voltage gain is not obvious under PO-mode, as shown in Fig. 9. The calculated voltage gain matches the actual voltage gain curve well than FHA.

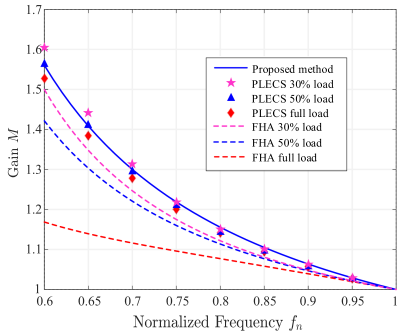

Fig. 9. Voltage gain M of FHA, STDA, and PLECS.

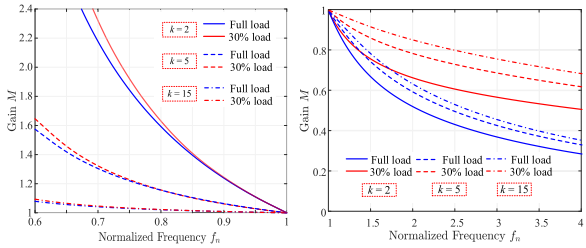

Fig. 10. Voltage gain M with different k. (a) $f_\mathrm{n} \le 1$. (b) $f_\mathrm{n} \ge 1$.

The analysis of PO-mode also applies to RFM.

Combining ARFM, the parameter k is related to the output gain. As the value of k increases, the frequency range for achieving the same gain becomes narrower. Conversely, as the value of k decreases, the frequency range for achieving the same gain becomes wider, as shown in Fig. 10.

III. Proposed Superposition Principle and TDA of the CLLC Converter

The waveforms of ARFM exhibit nonsinusoidal distortion, unlike BFRM, which possesses P-mode like the sine. Analyzing ARFM is more complex and achieving soft-switching is more challenging compared to BFRM [20]. The proposed method is conducted for analyzing soft-switching, efficiency analysis, and synchronous rectification.

A. Deriving Time-Domain Equations in ARFM

The voltage gain of ARFM is derived in (12). By solving (4), (8)–(12), the time-domain expressions in P-mode can be derived as

$$\begin{cases} i_{\mathrm{L1P}}(t) = A\sin(\omega_\mathrm{r} t) + B\cos(\omega_\mathrm{r} t) + C\sin(\omega_{\mathrm{k1}} t) \\ \qquad\qquad + B\cos(\omega_{\mathrm{k1}} t) \\ i_{\mathrm{L2P}}(t) = A\sin(\omega_\mathrm{r} t) + B\cos(\omega_\mathrm{r} t) - C\sin(\omega_{\mathrm{k1}} t) \\ \qquad\qquad - B\cos(\omega_{\mathrm{k1}} t) \\ u_{\mathrm{C1P}}(t) = -Z_\mathrm{r} A\cos(\omega_\mathrm{r} t) + Z_\mathrm{r} B\sin(\omega_\mathrm{r} t) \\ \qquad\qquad + \frac{Z_\mathrm{r} B}{k_1}\sin(\omega_{\mathrm{k1}} t) - \frac{Z_\mathrm{r} C}{k_1}\cos(\omega_{\mathrm{k1}} t) + U_1 \\ u_{\mathrm{C2P}}(t) = -Z_\mathrm{r} A\cos(\omega_\mathrm{r} t) + Z_\mathrm{r} B\sin(\omega_\mathrm{r} t) \\ \qquad\qquad - \frac{Z_\mathrm{r} B}{k_1}\sin(\omega_{\mathrm{k1}} t) + \frac{Z_\mathrm{r} C}{k_1}\cos(\omega_{\mathrm{k1}} t) - U_2 \end{cases} \quad (22)$$

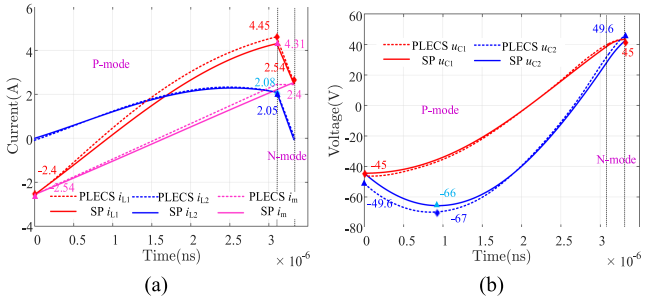

Fig. 11. Waveforms by SP and PLECS with $f_n = 1.5$ and load $= 214\ \Omega$. (a) Current i_{L1}, i_{L2}, i_m. (b) Voltage u_{C1}, u_{C2}.

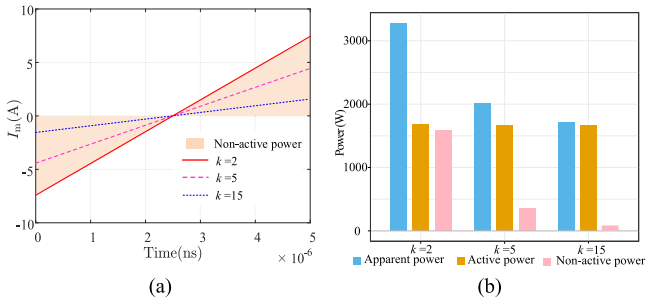

Fig. 12. Influence of excitation inductance ratio k on nonactive power. (a) Nonactive power region. (b) Amount of nonactive power.

where the unknown part A, B, and C of (22) can be obtained as follows:

$$\begin{cases} A = \frac{1}{2}\left(\frac{\pi U_2}{f_n R} + \frac{U_1}{Z_r} - \frac{U_2}{Z_r}\right) \\ B = -\frac{(U_1+U_2)}{2Z_r\sqrt{1+2k}} \tan\left(\frac{\pi}{2f_n\sqrt{1+2k}}\right) \\ C = \frac{(U_1+U_2)}{2Z_r\sqrt{1+2k}}. \end{cases} \tag{23}$$

The expressions derived by SP in N-mode are

$$\begin{cases} i_{L1N}(t) = i_{L1P}(t) - \frac{U_1}{Z_r}\sin(\omega_r(t-t_1)) \\ i_{L2N}(t) = i_{L2P}(t) - \frac{U_1}{Z_r}\sin(\omega_r(t-t_1)) \\ u_{C1N}(t) = u_{C1P}(t) + U_1\cos(\omega_r(t-t_1)) - U_1 \\ u_{C2N}(t) = u_{C2P}(t) + U_1\cdot\cos(\omega_r(t-t_1)) - U_1 - U_2. \end{cases} \tag{24}$$

The time of t_1 can be solved by (4), (8), and (10). It is described as follows:

$$t_1 = \frac{1}{2f_n f_r} - \frac{1}{\omega_r}\arcsin\left[\frac{1}{2}\left(\frac{\pi M Z_r}{f_n R} + 1 - M\right)\sin\left(\frac{\pi}{f_n}\right) - \frac{(1+M)}{2\sqrt{1+2k}}\cdot\tan\left(\frac{k_1\pi}{2f_n}\right)\left(\cos\left(\frac{\pi}{f_n}\right)+1\right)\right]. \tag{25}$$

The waveform diagram can be obtained based on (22)–(24). The SP method does not require initial values compared to the TDA. As illustrated in Fig. 11, the calculated waveforms are consistent with the simulated waveforms. The extreme error of current is within 0.15 A, and the extreme error of voltage is within 1 V. Therefore, this equation can be meaningful for device design, transformer magnetic simulation, and loss analysis.

Based on the acquired expression of current, the effective value of the current on primary and secondary-side can be obtained as expressed

$$\begin{cases} i_{rms,L1} = \sqrt{\frac{2}{T_s}\left(\int_0^{t_1} i_{L1P}^2 dt + \int_{t_1}^{\frac{T_s}{2}} i_{L1N}^2 dt\right)} \\ i_{rms,L2} = \sqrt{\frac{2}{T_s}\left(\int_0^{t_1} i_{L2P}^2 dt + \int_{t_1}^{\frac{T_s}{2}} i_{L2N}^2 dt\right)} \end{cases}. \tag{26}$$

Nonactive power is associated with the circulation on i_m, which can be obtained by (26). The nonactive power circulation increases as the k value decreases, as shown in Fig. 12.

B. TDA for Accurate Soft Switching

The proposed method is utilized to analyze the precise condition for soft switching. During the dead-time of switching

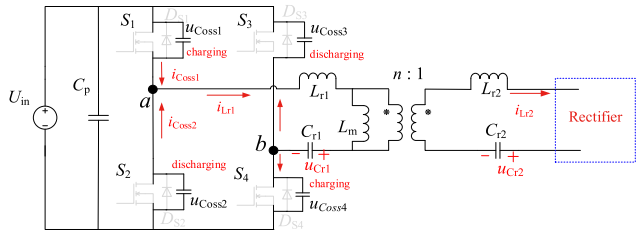

Fig. 13. Circuit condition for the ZVS analysis in dead-time.

duration, all switches are OFF and the primary-side current flows through the switch parasitic capacitances, as shown in Fig. 13.

This mode will keep until the voltages u_{Coss2} and u_{Coss3} is fully discharged. Once that happens, the S_2 and S_3 conduct in the reverse direction, which allows for the achievement of zero-voltage switching (ZVS). All the above capacitances are considered to be equivalent to the value of C_{oss}. Assuming the current remains constant because the dead-time is of short duration. Therefore, the formula for dead-time can be simplified as follows [19]:

$$Q = \int_{t_1}^{t_1+t_{dead}} i_{L1}dt \cong I_{L1(t=t_1+T_{dead})}t_{dead} \cong I_{L1(t=t_1)}t_{dead} \geq 2C_{oss}U_{in}. \tag{27}$$

The minimum dead-time can be calculated as

$$t_{dead} \geq \frac{2C_{oss}U_{in}}{I_{L1(t=t_1)}}. \tag{28}$$

After calculating the dead-time, it is essential to verify whether the designed excitation inductance value satisfies the requirements for achieving soft switching [20]. Therefore, the excitation inductance ratio k is calculated as

$$k \leq \frac{\pi t_{dead}}{4C_{oss}Z_r}. \tag{29}$$

C. Accurate Synchronous Rectification in ARFM and BRFM

For ARFM, the N-mode time can be calculated by (29), which refers to the delay in start-up time on the secondary-side switches for SR, as shown in Fig. 4

$$T_N = \frac{1}{\omega_r}\arcsin\left[\frac{1}{2}\left(\frac{\pi M Z_r}{f_n R} + 1 - M\right)\sin\left(\frac{\pi}{f_n}\right)\right.$$

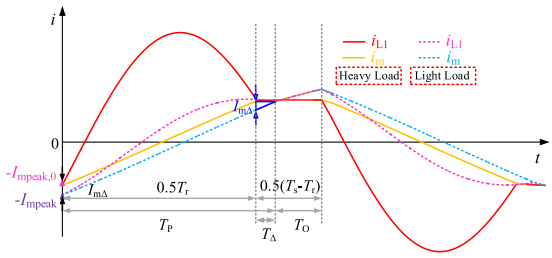

Fig. 14. Different load waveforms of CLLC converter in BRFM.

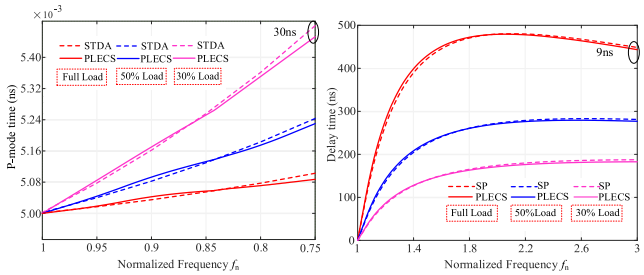

Fig. 15. Curves of SR time by PLECS and proposed methods at different loads. (a) $f_n \leq 1$. (b) $f_n \geq 1$.

$$-\frac{(1+M)}{2\sqrt{1+2k}} \cdot \tan\left(\frac{k_1\pi}{2f_n}\right)\left(\cos\left(\frac{\pi}{f_n}\right)+1\right)\Bigg]. \quad (30)$$

For BRFM, the duration of the P-mode (T_P) approximates $0.5T_r$ under heavy loads, as shown in Fig. 14. The $I_{mpeak,0}$ under heavy loads by solving (18)–(20) can be derived as

$$I_{mpeak,0} = \frac{2U_2k_1}{Z_r}\tan\frac{k_1\pi}{2}. \quad (31)$$

By taking (15), (17), (31) into (18). The I_{mpeak} can be deduced as

$$I_{mpeak} = \frac{2U_2k_1}{Z_r}\tan\frac{k_1\pi}{2} + \frac{2f_nRU_2 - \pi Z_rU_2}{8f_n(L_r+L_m)R}\left(\frac{1}{f_s}-\frac{1}{f_r}\right). \quad (32)$$

Based on the similar principle, the T_Δ be obtained as

$$T_\Delta = \frac{T_r}{2}\frac{(I_{mpeak}-I_{mpeak,0})R}{2I_{mpeak,0}R_L} \quad (33)$$

where R_L is light load. The time $0.5T_r + T_\Delta$ is the SR time. The P-mode SR time compared with PLECS is illustrated in Fig. 15(a). The calculation error of SR time is not significant compared to the value of PLECS.

In order to enhance the computational efficiency of DSP and compensate the errors. Fitting models were derived by taking U_{out} and f_s as the independent variables by implementing MATLAB *cf*tool (curve fitting toolbox). The proposed fitting model (34) and (35) were verified with different loads by comparing simulation, as shown in Fig. 14. The program calculation takes approximately 2.0 μs after performing the necessary calculations. Assuming a maximum frequency of 300 kHz, it is still able to complete the operation on time.

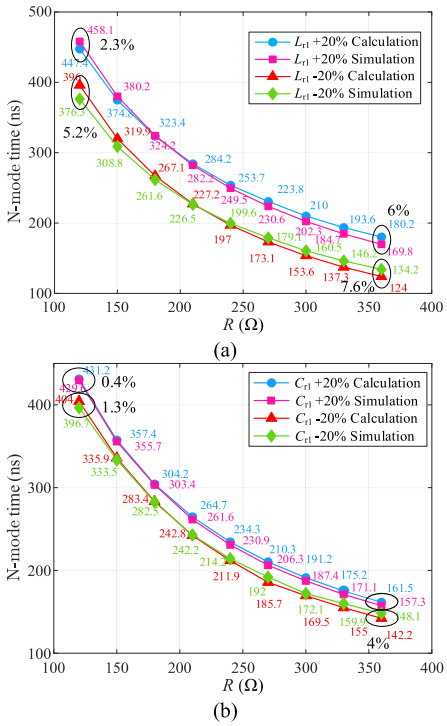

Fig. 16. Robustness analysis at 170 kHz. (a) Primary-side resonant inductance. (b) Primary-side resonant capacitance.

As the CLLC converter works in ARFM, the fitting model of SR delay-time is expressed as

$$F(f_s,U_{out}) = p_{00} + p_{10}f_s + p_{01}U_{out} + p_{20}{f_s}^2 + p_{11}f_sU_{out} + p_{02}U_{out}^2 + p_{30}{f_s}^3 + p_{21}{f_s}^2U_{out} + p_{12}f_sU_{out}^2 + p_{03}U_{out}^3 \quad (34)$$

where p_{00} is 4.0232×10^{-05}, p_{10} is -1.899×10^{-10}, p_{01} is -2.85×10^{-07}, p_{20} is 2.6515×10^{-16}, p_{11} is 9.045×10^{-13}, p_{02} is 7.12×10^{-10}, p_{30} is -1.854×10^{-22}, p_{21} is -4.602×10^{-19}, p_{12} is -1.247×10^{-15}, and p_{03} is -5.939×10^{-13}.

As the CLLC converter works in BRFM, the fitting model of SR on-time is given by

$$F(f_s,U_{out}) = p_{00} + p_{10}f_s + p_{01}U_{out} + p_{20}{f_s}^2 + p_{11}f_sU_{out} + p_{02}U_{out}^2 + p_{30}{f_s}^3 + p_{21}{f_s}^2U_{out} + p_{12}f_sU_{out}^2 + p_{03}U_{out}^3 \quad (35)$$

where p_{00} is -0.035425, p_{10} is 4.896×10^{-7}, p_{01} is 0.000146, p_{20} is -2.232×10^{-12}, p_{11} is -1.355×10^{-09}, p_{02} is -1.996×10^{-7}, p_{30} is 3.345×10^{-18}, p_{21} is 3.114×10^{-15}, p_{12} is 9.339×10^{-13}, and p_{03} is 9.05×10^{-11}.

The impact of component tolerance on the SR time is examined through the utilization of the Monte Carlo method. Fig. 16(a) illustrates the effect of the variation of the resonant inductor L_{r1} on the SR time t_{SR} when the output load changes in ARFM. Similarly, Fig. 16(b) demonstrates the influence of the deviation of the resonant capacitor C_{r1} on the time t_{SR} when the output load changes. The maximum error of SR time is 7.6%

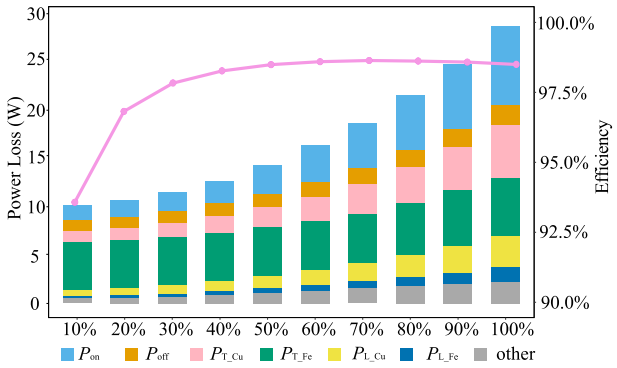

Fig. 17. Power loss distribution and efficiency curve under different load conditions.

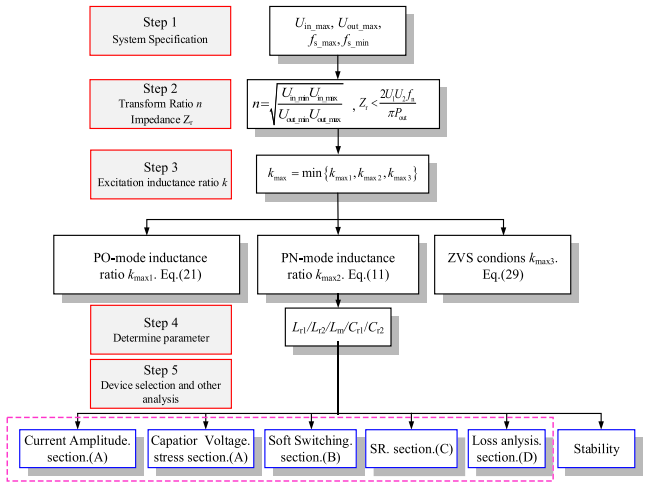

Fig. 18. Parameter design procedure of the CLLC converter.

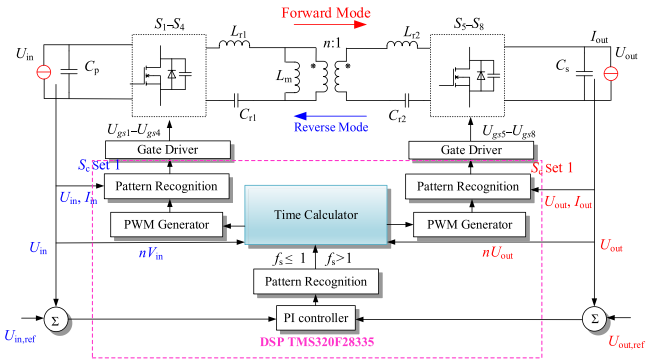

Fig. 19. Diagram of the proposed SR method for CLLC converter.

with a 20% tolerance of the primary-side resonant inductance at different load. SR time is not larger than 4%, as long as the primary-side capacitance is within 20% of the expected value. Moreover, the same analysis is employed for SR strategies in BRFM. The influence of the deviation of the L_{r1} and C_{r1} is 4.2% and 1.6%. Thus, the proposed SR control is robustness as the CLLC converter parameters have a certain degree of tolerance.

D. Loss Analysis With Synchronous Rectification

ZVS of all switches can be achieved. At the same time, SR can be achieved by appropriately turning ON and OFF the secondary-side switches. Therefore, the losses mainly include turn-OFF loss (P_{OFF}), conduction loss (P_{ON}), copper loss (P_{T_Cu} and P_{L_Cu}), and core loss (P_{T_Fe} and P_{L_Fe}). In addition, losses also include other losses (P_{other}) such as capacitor losses, PCB losses and switch conduction losses. Since the specific expressions of current and voltage have been derived, all loss parts can be calculated by referring to [26] and [34]. To sum up, the total system loss can basically be calculated using the following formula:

$$P_{Loss} = P_{on} + P_{off} + P_{T\_Fe} + P_{T\_Cu} + P_{L\_Fe} + P_{L\_Cu} + P_{other}. \quad (36)$$

The composition and efficiency of losses for various loads are shown in Fig. 17.

IV. System Design and Experimental Verification

A. Parameter Design and SR Control System

In conjunction with the above analysis content, Fig. 18 illustrates the primary process for parameter design. The calculation of n and Z_r in this study referred to [18] and [20].

Fig. 19 shows the diagram of the proposed digital SR scheme. For the forward mode, the primary-side switches $S_1 - S_4$ are controlled by traditional digital PI voltage closed-loop control, while the secondary-side switches $S_5 - S_8$ are mainly determined by the SR time calculated through the method described in this article. The sampling delay of U_{in} and U_{out} can be ignored. The f_s is the calculation result of the PI controller, which has no sampling delay. To calculate the SR time of $S_5 - S_8$, two variables of output voltage U_{out} and switching frequency f_s are used. The analysis of reverse mode is same with forward mode. A pattern analysis module has been added to the program for different modes. For ARFM and BRFM, there are two ways in time calculator. In addition, when pattern recognition detects light-load burst or short-circuit load or open-circuit load, the module output S_C is 1, enabling SR control through the secondary-side switches. Instead, if S_C goes to 0, a turn-OFF signal is issued immediately to prevent major errors in calculating SR and, thus misleading the switches to turn ON.

B. Verification of the Voltage Gain

To verify the proposed theory, a 1.5 kW bidirectional CLLC converter is developed, as shown in Fig. 20. The specific parameters of the converter are list by Table II. The CLLC converter is controlled with a digital signal processor TMS320F28335. And the size of switches is C3M0065090D. The parallel parasitic capacitance C_{oss} is about 100 pF. An antiparallel diode is added to bypass the switches ON the secondary-side. To verify the accuracy of the proposed model, the voltage gains calculated by the proposed method were compared with those of the FHA method and the experiment results.

The voltage gain of the CLLC converter prototype was tested by keeping the input voltage constant at 400 V, under three different loads – full load (load = 107 Ω), half load (load = 214 Ω),

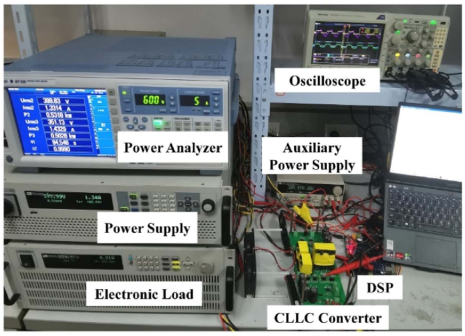

Fig. 20. Experimental setup including the prototype1.5 kW CLLC converter.

TABLE II
KEY PARAMETERS OF CLLC CONVERTER

Parameters	Values
Input voltage U_{in}	400 V
Output voltage U_{out}	270 – 480 V
Switching frequency f_s	75 – 300 kHz
Rated power	1.5 kW
Resonant inductor L_{r1} and L_{r2}	44.44 μH
Resonant capacitor C_{r1} and C_{r2}	57 nF
Magnetizing inductor L_m	222.2 μH
Turns ratio n	1:1
Dead time	200 ns

and 30% light load (load = 350 Ω). The comparison between the experimental voltage gain and the theoretical voltage gain is shown in Fig. 21. The results indicate that the calculated values are consistent with the experimental results.

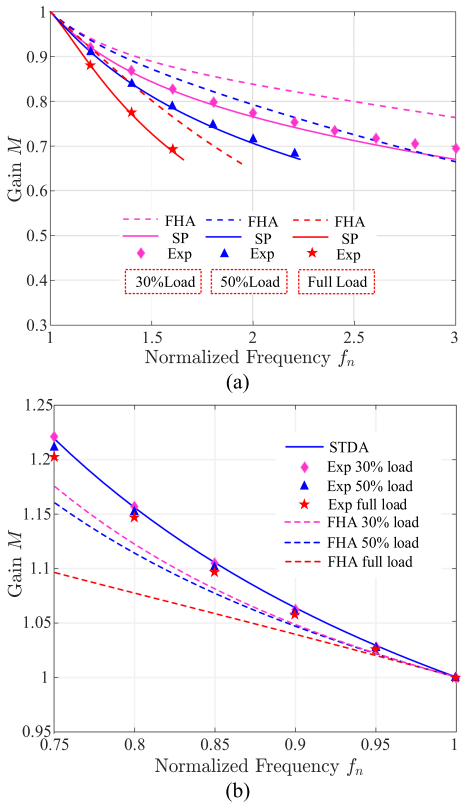

Fig. 21. Voltage gain M of FHA, experiment (Exp) and this article method (SP and STDA) in different stage. (a) $f_n \leq 1$. (b) $f_n \geq 1$.

C. Verifying the Peak Values of Voltage and Current and N-Model Time in ARFM

The formula in Section III can be used to obtain the peak values and the N-mode time. To validate the theory, this section uses the same experimental setup as Section IV-B, which employs the diode on the secondary-side. As depicted in Fig. 22, the peak values obtained from the SP analysis are highly consistent with both the experimental results and simulation by PLECS. The predicted peak values by the FHA under different loads at the same frequency also closely approximate the actual values, except for the peak current on the primary-side. Additionally, the SP calculates the peak value slightly lower than the simulation and closer to the experimental results, as indicated in Table III. Moreover, the proposed approach accurately computes N-mode time in line with experimental data, whereas FHA calculation yields a higher SR time with significant error.

As depicted in Fig. 23, experiments were conducted on the CLLC converter with an output voltage set at 270 V. The control frequencies for Fig. 23(a) and (b) were, respectively, set to 167 kHz and 237 kHz. The peak values and N-mode time obtained through the proposed analysis are in agreement with both experimental results and simulation results, demonstrating a strong correlation. However, it should be noted that the FHA analysis predicts lower peak values compared to actual

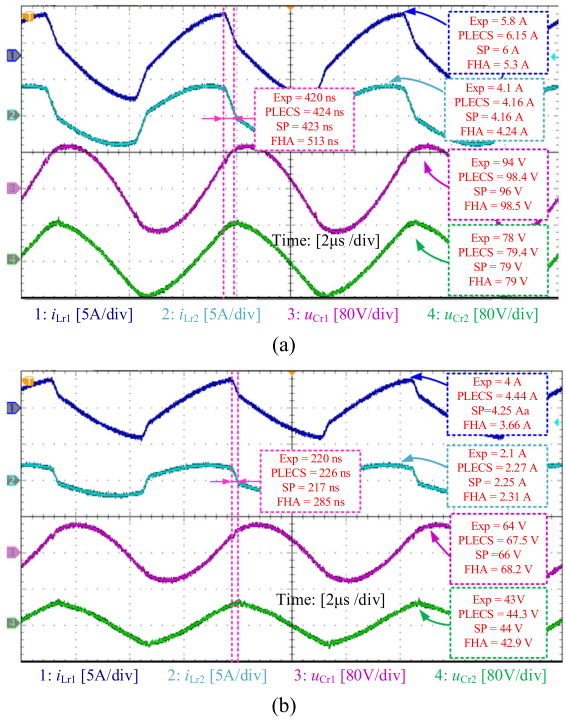

Fig. 22. Resonant current and voltage waveforms of the resonant elements under. (a) Load = 107 Ω, f_s = 150 kHz. (b) Load = 214 Ω, f_s = 150 kHz.

TABLE III
COMPARISON OF THE EXPERIMENT (EXP.), PLECS SIMULATION (SIM.), SP, AND FHA RESULTS FOR FORWARD POWER TRANSFER

Parameter	Load = 107 Ω, f_s = 150 kHz							Parameter	Load = 214 Ω, f_s = 150 kHz						
	Exp	Sim	Error	SP	Error	FHA	Error		Exp	Sim	Error	SP	Error	FHA	Error
U_{out} (V)	294	292	0.68%	293	0.34%	320.7	8.33%	U_{out} (V)	330	325	1.52%	326	1.21%	348.85	5.40%
I_{out} (A)	2.75	2.73	0.64%	2.74	0.28%	3	9.18%	I_{out} (A)	1.59	1.52	4.40%	1.52	4.40%	1.63	2.45%
i_{L1max} (A)	5.8	6.15	6.03%	6	3.45%	5.3	8.62%	i_{L1max} (A)	4.1	4.44	8.29%	4.25	3.67%	3.66	12.02%
i_{L2max} (A)	4.1	4.16	1.46%	4.16	1.46%	4.24	3.41%	i_{L2max} (A)	2.1	2.27	8.10%	2.25	7.14%	2.31	9.09%
u_{C1max} (V)	94	98.4	4.68%	94	2.13%	98	4.26%	u_{C1max} (V)	64	67.5	5.47%	67	4.69%	68.2	6.16%
u_{C2max} (V)	78	79.4	1.79%	79	1.28%	79	1.28%	u_{C2max} (V)	43	44.3	3.02%	44	2.33%	42.9	0.23%
N-mode(ns)	420	424	0.95%	423	0.71%	520	23.81%	N-mode(ns)	220	226	2.73%	217	1.36%	311	29.26%
Parameter	U_{out} = 270 V, Load = 107 Ω							Parameter	U_{out} = 270 V, Load = 214 Ω						
	Exp	Sim	Error	SP	Error	FHA	Error		Exp	Sim	Error	SP	Error	FHA	Error
U_{out} (V)	270	270	0	270	0	270	0	U_{out} (V)	270	270	0	270	0	270	0
f_s (kHz)	167	163.3	2.22%	164	1.80%	189	13.17%	f_s (kHz)	237	219.6	7.34%	220	7.17%	291	22.78%
i_{L1max} (A)	5.5	5.86	6.55%	5.44	1.09%	4.28	22.18%	i_{L1max} (A)	3.2	3.6	12.50%	3.43	7.19%	2.24	30.00%
i_{L2max} (A)	3.9	4	2.56%	4	2.56%	3.57	8.46%	i_{L2max} (A)	2.1	2.2	4.76%	2.22	5.71%	1.8	14.29%
u_{C1max} (V)	78	84	7.69%	77	1.28%	99	26.92%	u_{C1max} (V)	34	35	2.94%	33.4	1.76%	52	52.94%
u_{C2max} (V)	62	68	9.68%	66	6.45%	83	33.87%	u_{C2max} (V)	25.6	25.2	1.56%	25.2	1.56%	41	60.16%
N-mode(ns)	440	446	1.36%	452	2.73%	585	32.95%	N-mode(ns)	270	279	3.33%	271	0.37%	435	61.11%

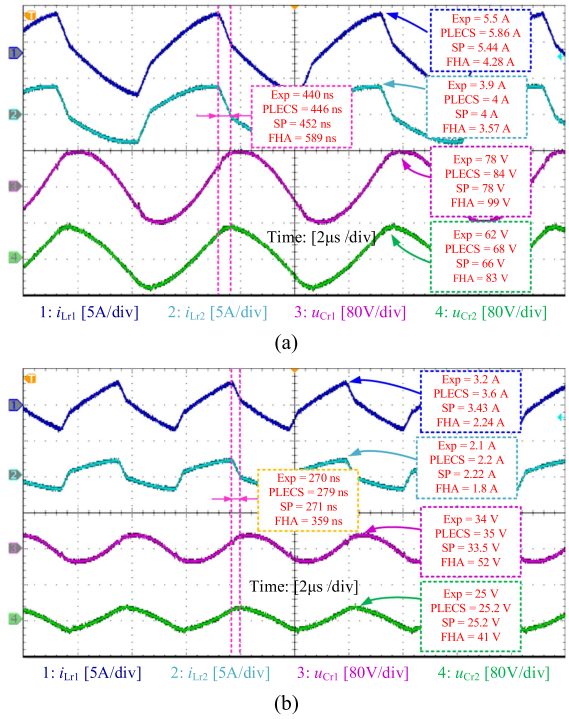

Fig. 23. Resonant current and voltage waveforms of the resonant elements under. (a) $U_{\rm out}$ = 270 V, load = 107 Ω. (b) $U_{\rm out}$ = 270 V, load = 214 Ω.

measurements, which may result in improper component selection. Additionally, the N-mode time exhibits significant discrepancies when compared to theoretical calculations and real-world data, as indicated in Table III.

The recommended approach is to set a slightly longer dead time than the calculated theoretical value, taking into account potential errors in controlling the driver and prototype parameters. The CLLC converter achieved soft switching on the primary-side switches, as illustrated in Fig. 24. This was accomplished by

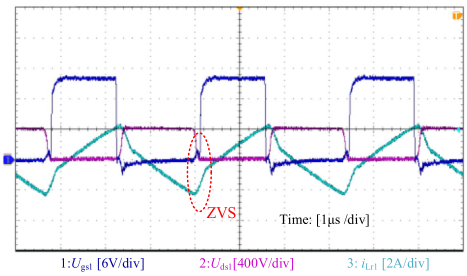

Fig. 24. Waveforms corresponding to calculated dead-time that ensures ZVS.

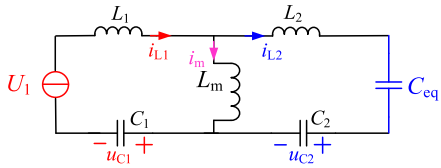

Fig. 25. Equivalent circuit of CLLC converter in the charging and discharging mode of the switch parasitic capacitors.

incorporating a calculated dead time and operating at a maximum set frequency of 300 kHz under light load conditions. The output voltage is 270 V.

D. Precise Implementation of Synchronous Rectification

Despite the fact that the charging and discharging time of the secondary-side switch parasitic capacitors are not taken into account during the theoretical analysis, it is essential to take the under load = 350 Ω and f_s = 300 kHz. Times into account for practical applications. The charging and discharging PC-mode of the switch parasitic capacitors can be seen in Fig. 25. The waveforms of ARFM are depicted in Fig. 26.

After the parallel capacitor charging and discharging of the secondary-side switches, the body diodes will be activated and

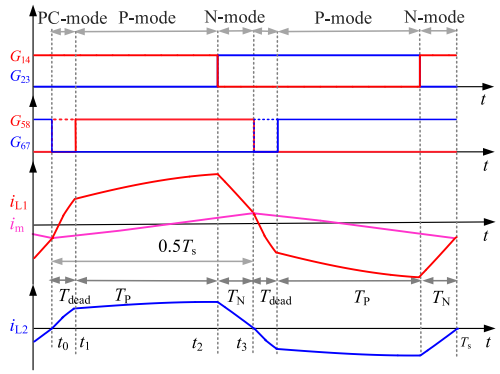

Fig. 26. Waveforms in ARFM considering parasitic capacitors.

a SR signal must be given once the capacitor charging and discharging is finished. If not, early activation will cause hard switching, thus decreasing efficiency and increasing the switches temperature.

The time for charging and discharging parasitic capacitors of the switches needs to be calculated, which can be achieved by altering the dead-time. For BRFM, due to the oscillation of the parasitic capacitors, the parasitic capacitor of the secondary-side switches will be charged in O-mode. Therefore, the dead-time is not large, and a fixed dead-time can be given [35]. For ARFM, calculating dead-time is more important without advanced charge. The actual calculated time for driving activation is the sum of N-mode time and dead-time in ARFM

Defining T_{dead} as the time required for complete charging and discharging, the following equation can be derived as:

$$\int_0^{T_{\text{dead}}} |i_{\text{L2}}|\, dt \geq U_2 C_{\text{eq}} \tag{37}$$

where C_{eq} is as large as C_{oss}.

It is possible to view the resonant current i_{L2} as a sine waveform, which is got as

$$i_{\text{Lr2}} = I_{\text{Lr2}} \sin(2\pi f_s t)\,. \tag{38}$$

As the curve is almost a straight line when charging and discharging when frequency is resonant. By taking (11) into (38), the (38) can be simplified as

$$\int_{t_2}^{t_3} I_{\text{Lr2}} \sin(2\pi f_s t)\, dt \approx \int_0^{T_{\text{dead}}} \frac{I_{\text{out}}\pi}{2} (2\pi f_s t)\, dt \geq U_{\text{out}} C_{\text{oss}}. \tag{39}$$

The minimum time T_{dead} for charging and discharging parallel capacitors of the switches can be obtained as

$$T_{\text{dead}} \geq \frac{1}{n\pi} \sqrt{\frac{2C_{\text{oss}} U_{\text{out}}}{f_s I_{\text{out}}}}. \tag{40}$$

The presence of dead-time leads to a difference between the waveform used for SR time calculation and the ideal conditions. However, the method of calculation outlined is still applicable for calculating SR time in experiments. Due to the potential deviation of passive components and the influence of parasitic parameters on switching devices. The value of the theoretical

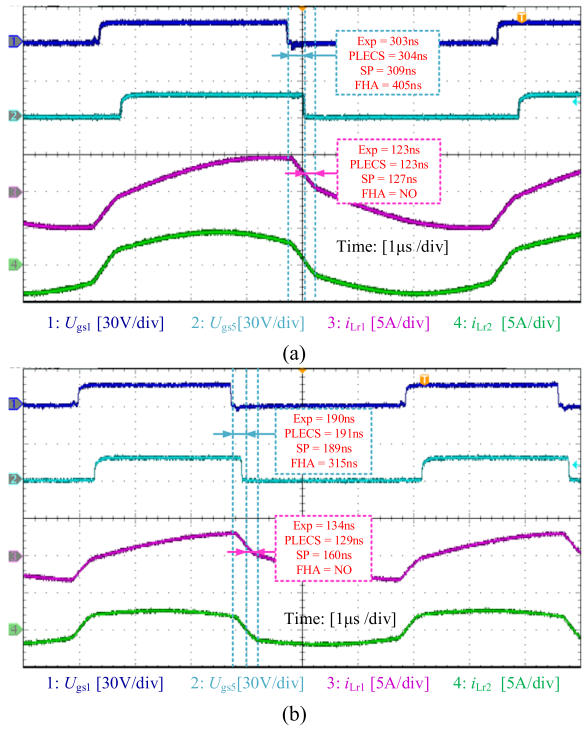

Fig. 27. Waveforms of CLLC converter. (a) $U_{\text{out}} = 340$ V, load $= 107\ \Omega$. (b) $U_{\text{out}} = 340$ V, load $= 214\ \Omega$.

formula is adjusted to prevent premature activation or deactivation of the calculated secondary SR signal.

Experiments were conducted on the CLLC converter with an output voltage set at 340 V, as shown in Fig. 27. The control frequencies for Fig. 27(a) and (b) were, respectively, set to 137 kHz and 168 kHz. The proposed SP analysis accurately calculates the SR time consistent with experimental data and PLECS, while the FHA calculation yields a higher SR time with significant discrepancy. The calculation of dead-time is also closely aligned with both experimental and theoretical calculations.

The SR waveforms of BRFM are depicted in Fig. 28. The O-mode values are consistent with experimental data and PLECS, which verified the proposed analysis. The SR time calculated by the proposed approach is accurately in accordance with experiment and PLECS (the output voltage of Fig. 28(a) and (b) is 470 V), while the FHA calculation yields a higher SR time with significant discrepancy.

The dynamic waveforms during load switching, as shown in Fig. 29, demonstrate the excellent dynamic response capability of the proposed SR scheme. Fig. 29(a) and (b) demonstrates the smooth operation during load switching in ARFM. Fig. 29(c) and (d) illustrates the smooth transition between BRFM and ARFM when output voltage changed.

The comparison with other methods has been summarized in Table IV. The proposed SP model significantly enhances accuracy compared to FHA methods. TDA methods require iteration. TDA and EHA methods are quite complex. Moreover, by SP analysis and STDA, we can obtain voltage gain expressions that strike a balance between simplicity and accuracy in calculations. The current and voltage expressions do not require initial

TABLE IV
COMPARISON WITH PREVIOUS CLLC CONVERTER METHODS

References	[11]	[14]	[15]	[16]	[18]	[19]	[20]	This paper
Topology	CLLC	CLLC	CLLC	CLLC	CLLC	CLLC	CLLC	CLLC
Model	FHA	FHA	EHA	TDA	TDA	TDA	TDA	SP and TDA
Accuracy	★	★★★	★★★★	★★★★	★★★★	★★★	★★	★★★
Iteration required	Yes	No	Yes	Yes	Yes	No	No	No
Voltage gain expression	Yes	Yes	Yes	No	No	Yes	Yes	Yes
Current and Voltage expression visualization	No	No	No	No	No	Yes	No	Yes
Current effective value	No	Yes	Yes	Yes	No	No	No	Yes
Complexity	★	★★★	★★★★	★★★★	★★★★	★★★★	★★	★★

TABLE V
V EFFICIENCY COMPARISON WITH PREVIOUS CLLC CONVERTER METHODS

References	[24], [25], [26], [27]	[28]	[31], [32]	This paper
Topology	CLLC	CLLC	CLLC	CLLC
Method	FHA	EHA	TDA	SP and TDA
Iteration required	No	No	Yes	No
Calculation	fitting model	look-up tables	look-up tables	fitting models
Complexity	★	★★★★	★★★★	★★
SR accuracy	★	★★★★	★★★★	★★★★
The peak efficiency/ efficiency improvement	97.29%/1.59%	97.40%/1.70%	97.40%/1.70%	97.5%/1.8%

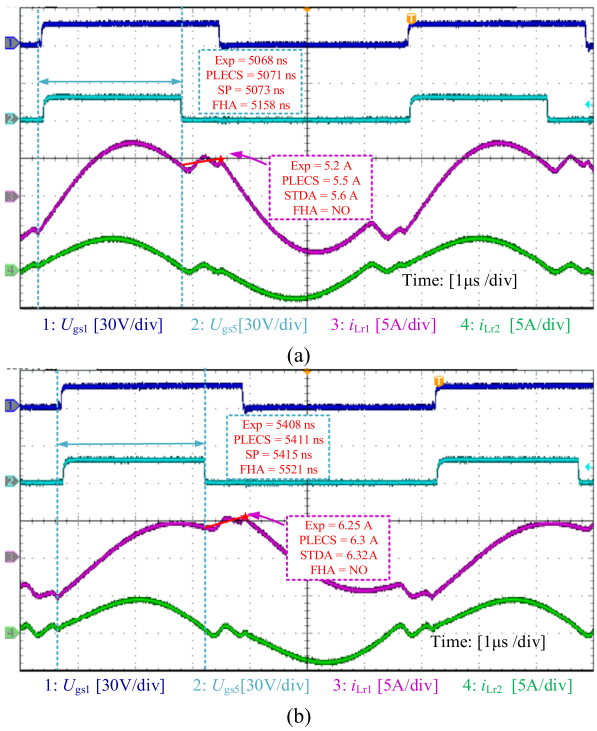

Fig. 28. Waveforms of CLLC converter. (a) $U_{\text{out}} = 470$ V, load $= 107\ \Omega$. (b) $U_{\text{out}} = 470$ V, load $= 214\ \Omega$.

values and can visualize easily as well. Finally, the proposed method proves to be highly efficient and reliable for CLLC converter.

To enhance the efficiency comparison, Table V has been included for efficiency analysis. Among them, FHA exhibited errors, EHA and TDA methods utilized a complex algorithm that required building look-up tables to generate phase shifts between gate signals on the primary and secondary-sides. These tables needed to be reconstructed whenever CLLC parameters changed, resulting in poor universality. Additionally, the impact accuracy on SR of parasitic capacitance is taken into account to achieve higher

The efficiency of uncontrolled rectifier, TDA and proposed method is illustrated in Fig. 30. Different load at resonant frequency was selected to achieve the peak efficiency, as shown in Fig. 30(a). The proposed control has resulted in improved overall efficiency across various load ranges. In particular, there has been a 1.8% increase in efficiency (at 900 W), reaching a peak of 97.5% between the proposed SR method and the uncontrolled rectification (maximum efficiency difference is 2.27%). Compared with TDA method [31], [32], the converter full load efficiency is improved by 0.1% with the proposed strategy. Consequently, the proposed method exhibits superior overall efficiency compared to uncontrolled rectification. According to Fig. 30(b), the proposed SR method shows a significant efficiency increase (1.42% – 2.3%) compared to the uncontrolled rectification with constant output voltage ($U_{\text{out}} = 340$ V). The proposed SR method demonstrates higher efficiency compared to the TDA [32] (with a maximum efficiency difference of 0.17%). Similarly, as shown in Fig. 30(c), there is also a significant improvement in efficiency when comparing the proposed SR method with uncontrolled rectification (1.34% – 2.16%) at discharge condition and constant output voltage ($U_{\text{out}} = 450$ V). The proposed SR method is more efficient than the TDA [32] (with a maximum efficiency difference of 0.13%). Experimental results confirm the high efficiency achieved by the proposed SR method in CLLC converters.

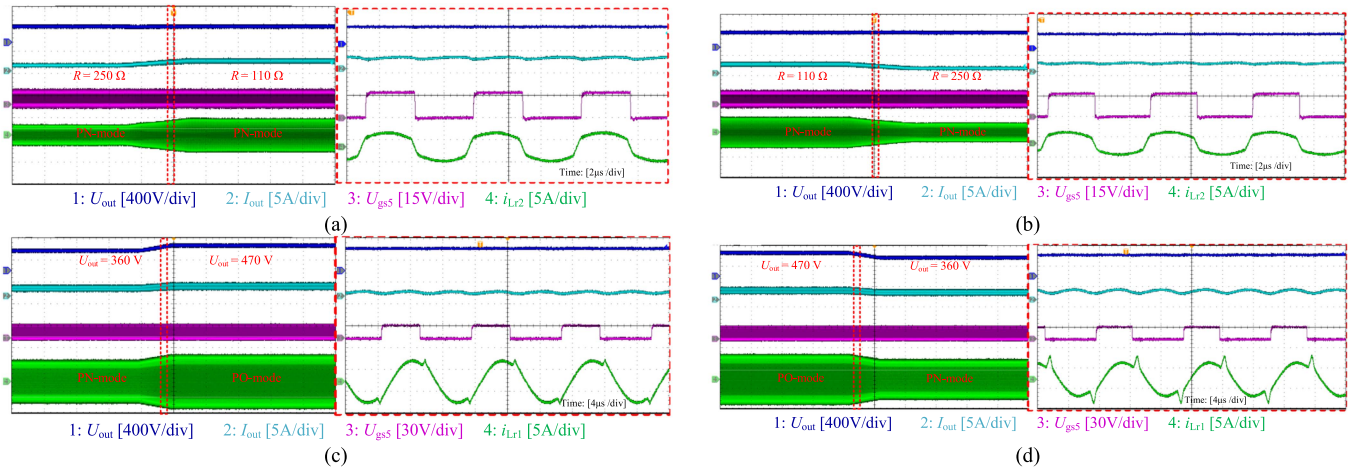

Fig. 29. Dynamic waveforms. (a) Increase load from 250 Ω to 110 Ω at constant output voltage 330 V. (b) Decrease load from 110 Ω to 250 Ω at constant output voltage 330 V. (c) Increase output voltage from 360 V to 470 V at constant load 214 Ω. (d) Decrease output voltage from 470 V to 360 V at constant load 214 Ω.

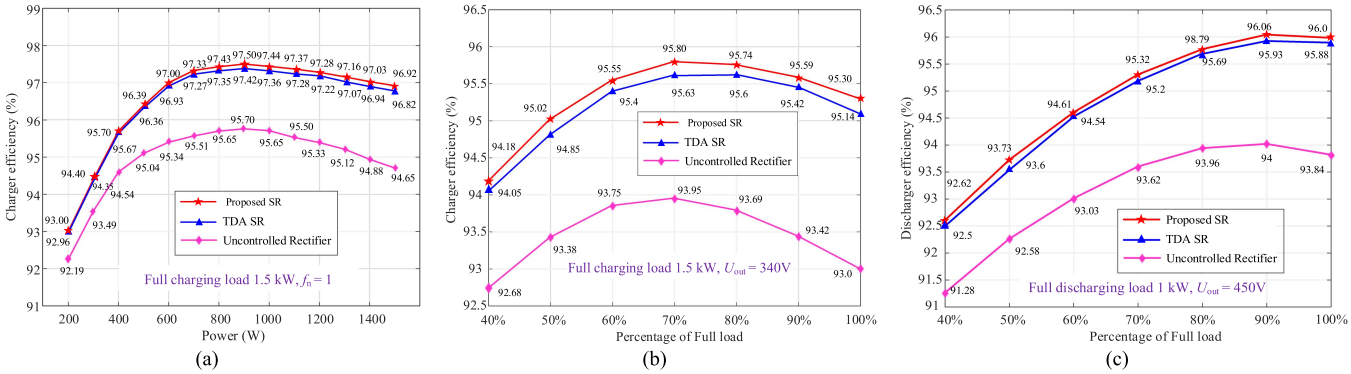

Fig. 30. Efficiency comparison among proposed SR strategy, TDA, and uncontrolled rectifier. (a) Different load at resonant frequency. (b) Overall charging efficiency at constant output voltage (340 V). (c) Overall discharging efficiency at constant output voltage (450 V).

V. Conclusion

This article proposes a superposition principle-based method applied to CLLC converters under the above-resonant-frequency-mode and employs simplified TDA method for BRFM. First, it helps to simplify the time-domain expression analysis, thereby obtaining an expression of the voltage gain and the resonant currents and voltages. Second, through the proposed analysis method, the analytical expression of the synchronous rectification time is determined, thereby achieving precise synchronous rectification. Simulation verified the correctness of the proposed theory. Both simulation and experimental results show that the proposed method is not only less complex than the EHA method but also derives the peak value of the resonant current and voltage more accurately than the FHA. Through precise soft switching and synchronous rectification, the operating efficiency of the CLLC converter is improved by 1.8%, with a peak value of 97.5%.

Appendix

Assuming that the transformer operates in heavy load, the excitation current of O-mode remaining unchanged in BRFM. the output voltage gain and peak value of excitation current has been derived in (21) and (31).

The voltage across capacitors is related within half a cycle, which is expressed as

$$u_{C1}(T_p) + u_{C1}(0) = -u_{C2}(T_p) - u_{C2}(0) - \frac{I_{mpeak}}{C_1}\left(\frac{T_s}{2} - T_P\right). \quad (41)$$

Due to the symmetry of magnetic current in P-mode, which can be derived as

$$u_{C1}(T_P) - u_{C1}(0) = \frac{1}{C_1}\int_{t_0}^{t_1} i_{L1}dt = \frac{1}{C_1}\int_{t_0}^{t_1}(i_{L2} + i_m)\,dt = \frac{1}{C_2}\int_{t_0}^{t_1} i_{L2}dt = u_{C2}(T_P) - u_{C2}(0). \quad (42)$$

Combining (41) and (42), which can be got that

$$u_{C1}(T_P) = -u_{C2}(0) - \frac{I_{mpeak}}{C_1}\left(\frac{T_s}{2} - T_P\right). \quad (43)$$

Therefore, the primary-side voltage at the end of the P-mode can be obtained as

$$U_1 - u_{C1}(T_P) = U_1 + u_{C2}(0) + \frac{I_{mpeak}}{C_r}\left(\frac{T_s}{2} - T_P\right). \quad (44)$$

Combining (21) and (31), which can be derived as

$$U_2 - u_{C2}(T_P) = U_1 + u_{C2}(0) + \frac{I_{mpeak}}{C_r}\left(\frac{T_s}{2} - T_P\right). \quad (45)$$

Therefore, (46) is satisfied in heavy load

$$U_1 - u_{C1}(T_P) = U_2 - u_{C2}(T_P). \quad (46)$$

In order to verify whether (46) meets the light load condition, simulation verification is carried out. The error of (43) and (44) is 4% when the CLLC converter works at 30% light load and $f_n = 0.75$. Then, (47) can be employed simplifying the TDA

$$U_2 - u_{C2}(T_P) \approx U_2 + u_{C2}(0). \quad (47)$$

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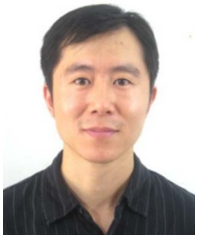

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