Fault-Tolerant Five-Level Switching-Cell Current Source Inverter

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***Abstract*—A topology with a reduced component count, referred to as the different multilevel current source inverter (DML-CSI), has been introduced in the literature. However, similar to other CSIs, DML-CSI also suffers from the issue of open-circuit faults (OCFs), which are reported to be the most common and destructive failures in industrial settings. In addressing this significant drawback, this article introduces a new configuration termed the fault-tolerant switching-cell CSI (FT-SC^{2}SI), derived from the DML-CSI circuit. To enhance the proposed topology's resilience against severe OCF scenarios and avoid the need for an additional closed-loop controller, the phase-shifted pulsewidth modulation (PS-PWM) method is employed. Notably, the proposed solution is straightforward and does not necessitate any fault diagnosis or other complex controllers. Furthermore, the PS-PWM operation under faulty conditions does not require modification. Likewise, the quality of the waveforms is not compromised during the faulty operating conditions. Experimental results are provided to substantiate the findings.**

***Index Terms*—Current source inverter, multilevel converter, open-circuit fault (OCF), phase-shifted pulsewidth modulation (PS-PWM), reliability.**

I. Introduction

RELIABILITY has consistently ranked among the primary characteristics for assessing power converters. Given its expansive nature, numerous studies have explored reliability from various angles. These include approaches such as junction temperature control employing thermal management and modulation methods, condition monitoring, robustness validation, reduced switch count, and the utilization of fault-tolerant topologies, all of which are well-recognized methods aimed at enhancing the reliability of power converters [1]. The fault-tolerant multilevel voltage and current source converters (VSCs/CSCs) are of interest due to their incorporation of numerous power devices in their structure, as well as their pivotal roles in industrial settings. Failures in power devices, categorized into shoot-through issues, also known as leg short-circuit faults (SCF), and open-circuit faults (OCF), seriously endanger the reliability of power converters [2]. According to industrial reports, OCFs and SCFs caused by faulty semiconductor gate driving are identified as the most prevalent and consequential failures observed in current source and voltage source converters, respectively [2]. Industrial gate drivers incorporate SCF protection mechanisms that promptly deactivate power switches or the converter upon detecting such failures. While shutting down the power devices during an SCF event prevents potential damage to the converter, it may result in an undesirable loss of power supply for critical applications. However, this concern does not apply to CSCs, as they inherently possess SCF handling capability. This key feature makes CSCs appealing topologies for applications where reliability and fault tolerance are paramount. When it comes to OCFs, there is a notable contrast between CSCs and VSCs. While OCFs in VSCs may not pose an immediate danger and can be detected and managed to some extent, in CSCs, such faults can swiftly lead to significant damage to the converter. Overall, there are two approaches to addressing OCFs in VSCs: hardware and software solutions. In hardware remedies, additional components, power devices, and even extra legs or converters are integrated into the main converter. Even so, the hardware approach not only results in a bulky, expensive, and complex system but may also have adverse effects on reliability. While the control solution eliminates the need for additional equipment, it does possess certain limitations. For instance, most control solutions mandate a fault detection process prior to any action. This results in a complex fault-tolerant control structure and modeling process. Furthermore, diagnosing OCFs requires time, thereby delaying the return to both healthy and postfault (PF) conditions [3]. In addition, misdiagnosis may arise from faults sharing similar characteristics. While software methods simplify the hardware implementation of the converter, they simultaneously complicate the control system. In addition, although control-based OCF techniques may appear cheaper than hardware strategies, they may require additional voltage and current sensors, which would increase the cost of software solutions. Another major limitation associated with the previous OCF hardware/software methods is that during faulty operation of the converter, the quality of output waveforms deteriorates.

Despite the numerous benefits associated with CSCs, such as voltage boosting capability, short-circuit immunity, and the provision of motor-friendly waveforms there has been a notable absence of extensive research and studies aimed at enhancing

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their performance relative to the voltage source multilevel inverter counterpart, particularly from a fault-tolerant perspective. In contrast to VSCs, the consequence of the OCF issue in CSCs is irreversible. When an OCF occurs on complementary switches in CSCs, it interrupts the input dc choke current, resulting in a significant voltage spike or overvoltage on power devices within a very short time, leading to severe damage to the converter. Hence, the OCF software solution discussed for VSCs is ineffective for CSCs, as diagnosing faults takes time and protection requires a nanosecond-level response time to safeguard the devices [4]. The primary causes of OCF are faults in the gate driver [2]. Until recently, there has been limited research dedicated to addressing OCFs in CSIs. Previous studies primarily focused on employing voltage clamp circuits, such as a diode bridge circuit [5]. However, these methods resulted in an increased number of power devices within the main topology, rendering the system more complex, costly, bulky, and less reliable. In [6], a novel ML-CSI topology is introduced to address OCF occurrences, even if they happen simultaneously among all power devices. This remarkable capability is achieved by integrating only small film capacitors into the circuit. However, if OCF incidents are frequent, the proposed converter may not be able to withstand them. In addition, an additional closed-loop controller is needed to maintain a balanced current in the intermediate inductor, adding complexity to the system. Building upon this concept, another enhanced ML-CSI is proposed in [7]. However, the effectiveness of this proposed solution under frequent or severe faulty operating conditions has not been investigated. Moreover, the proposed topology includes two intermediate and one input dc smoothing inductors, which could potentially result in a bulky, heavy, and costly circuit. Similar to conventional ML-CSIs, such as the single rating ML-CSI (SR-ML-CSI), multirating ML-CSI (MR-ML-CSI), paralleled H-bridge ML-CSI (PHB-ML-CSI), and multicell ML-CSI (MC-ML-CSI), the two converters mentioned last also incorporate a higher number of power devices in their structures. This increase not only affects the reliability of the converter but also raises concerns regarding cost, size, and controller or pulsewidth modulation (PWM) complexity. In [8], a new topology called different multilevel current source inverter is introduced, derived from the MC-ML-CSI [see Fig. 1(a)]. This topology not only reduces the number of power semiconductor devices by 25% but also decreases the number of input dc inductors by 50% compared to the MC-ML-CSI. While the D-5LCSI configuration offers advantages such as fewer devices and chokes, it is important to note that OCF also poses a threat to the D-5LCSI. Furthermore, the PWM employed in [8] cannot balance the inductor current, requiring an additional closed-loop controller.

Considering the discussed limitations for CSIs, this article proposes a new topology called fault-tolerant switching-cell (SC) CSI (FT-SC^{2}SI) for the sake of simplicity. The circuit diagram of the proposed topology is depicted in Fig. 1(b) and has the same number of power devices as the D-5LCSI. Three small SC capacitors C_1, C_2, and C_3 are incorporated in the proposed inverter, and the position of some power semiconductor devices are interchanged. By doing so, the SC capacitors can provide an uninterrupted current path for the input dc currents even if

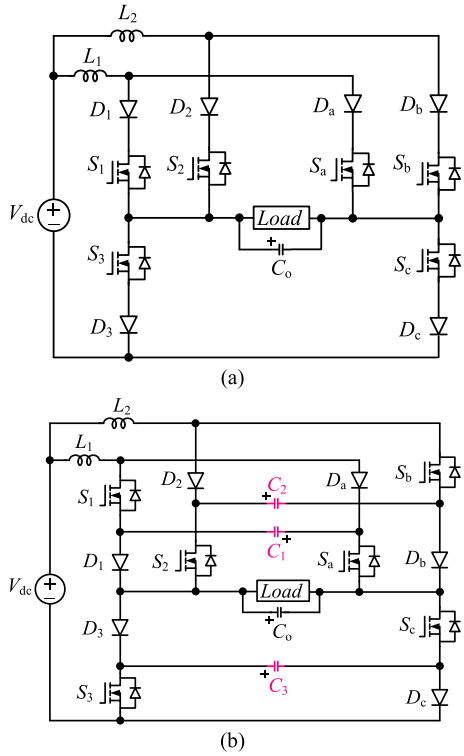

Fig. 1. (a) D-5LCSI. (b) Proposed FT-SC^{2}SI.

all switches are turned OFF simultaneously and frequently. Even under faulty operating conditions, there is no compromise in the quality of waveforms. The proposed solution is both simple and efficient, as it does not necessitate fault diagnosis or the use of complex controllers. In addition, no additional voltage or current sensors are required. Furthermore, the phase-shifted PWM (PS-PWM) does not require modification in scenarios involving OCF.

It is noteworthy that the practice of integrating capacitors between legs in CSCs is not a recent development and has origins dating back to 1972 [9]. During this period, capacitors were introduced between the phase legs in force commutation thyristor-based CSIs, commonly referred to as autosequential current-fed inverters (ASCIs). This implementation was intended to streamline the commutation process in motor drive applications [10], [11]. The utilization of series diodes and capacitor banks, each with identical values, linked to both the upper and lower sets of thyristors, serves the function of forced commutation. These capacitors, storing charge of the correct polarity, along with isolating diodes, aid in the process of forced commutation. However, the operational mode of ASCI produces a square wave phase current waveform, potentially resulting in considerable core loss within the motor [10], [11]. During commutation, the rapid fluctuations in current induce a voltage spike at the output waveforms, posing risks to winding insulation in motor drive applications and generating electromagnetic interference. This presents a notable challenge for ASCI topology. To address this issue, either thyristor voltage should be rated higher, or the machine should be designed with low leakage inductance [10], [11]. Alternatively, an external clamping circuit can absorb

TABLE I
SWITCHING PATTERN OF THE PROPOSED FT-SC^{2}SI

Modes	Switching States						Inverter Current (i_{inv})
	S_1	S_2	S_3	S_a	S_b	S_c	
1	1	1	0	0	0	1	I_{dc}
2	0	1	0	1	0	1	$0.5I_{dc}$
3	1	0	0	0	1	1	
4	1	1	1	0	0	0	0
5	0	0	0	1	1	1	
6	1	0	1	0	1	0	$-0.5I_{dc}$
7	0	1	1	1	0	0	
8	0	0	1	1	1	0	$-I_{dc}$

the spike voltage. In addition, due to the intricate nature of the circuit, the dc-link inductor should be adequately sized to ensure effective smoothing of the dc current. Once a commercial offering by Cutler Hammer, this inverter has now been rendered obsolete with the rise of fast-switching IGBT-based VSIs dominating the market. There exist notable distinctions between the ASCI and the proposed topology. In ASCI, the capacitors employed are incapable of safeguarding the converter against OCF, even in the event of a failure occurring in just one switch. In addition, augmenting the number of phases in ASCI results in a proportional increase in the quantity of capacitors. Furthermore, the capacitors in ASCI should have large capacitance values.

The rest of this article is organized as follows. The PS-PWM approach, along with the operation of the proposed inverter under normal, faulty, and parameter mismatch conditions, is elaborated in Section II. This section also covers the design guidelines for the passive components in the suggested circuit. Section III encompasses experimental results and a comparison between the proposed topology and several other ML-CSIs. Finally, Section IV concludes this article.

II. PROPOSED FT-SC^{2}SI

A. Modulation Strategy

The implementation of PWM methods, such as level-shifted and phase-shifted, in an ML-CSI, is not as straightforward as in an ML-VSI. In several previous studies related to ML-CSIs, the gating signals generated by PWM schemes involve blanking times/intervals, which do not allow for the continuity of the inductor's current [12], [13], [14], [15], [16]. These intervals must be recognized and replaced by zero states using additional logic to maintain continuous current in the inductor(s). This process results in increased complexity in PWM implementation, particularly from a practical standpoint. Another limitation of the mentioned PWM techniques is that they may not naturally provide optimal switching states, adding further complexity to the PWM/controller [13].

In contrast to the complex PWM methods discussed above, this work applies the switching states shown in Table I (where "0" indicates the OFF state and "1" indicates the ON state of the power switches) to the proposed FT-SC^{2}SI using PS-PWM in the same simplified manner as in [17] and [18]. Thus, not only is the blanking time in previous methods avoided, but optimized switching states are also naturally produced. It should also be mentioned that the PWM/control simplicity can be attributed to the straightforwardness of the proposed inverter. Fig. 2(a) depicts the gating signals of switches (S_1, S_2, S_3, S_a, S_b, and S_c) produced by the PS-PWM method. In this figure, W_{ref} denotes the reference signal and W_{cr1}, W_{cr2}, and W_{cr3} are the carrier signals. Comparing the reference signal, W_{ref} with carrier1, W_{cr1} drives switches S_1 and S_a. When W_{ref} is compared with W_{cr2}, the switches S_2 and S_b are driven. And finally, the gating signals for switches S_3 and S_c are generated by comparing W_{ref} and W_{cr3}. The switches pair (S_1, S_a), (S_2, S_b), and (S_3, S_c) operate in a complementary manner. The gating signals, along with the overlap time/commutation intervals/transients (δ) illustrated in Fig. 2, are applied to the hardware prototype by programming a description language in Code Composer Studio and using it in DSP. Furthermore, unlike the traditional MLCs, which require (n – 1) carrier signals (where n denotes the number of output levels), the suggested circuit only needs (n – 2) carrier signals. This requirement reduces the number of switching states, significantly simplifying the control of the proposed converter [19].

B. Operation Principle of the Proposed Inverter Under Normal Condition

Considering that the operation modes of the proposed topology are symmetrical in the positive and negative half-cycles, only its functioning in the positive half-cycle is elaborated here. Overall, during the positive half-cycle, C_1's voltage remains at zero volts, while C_2 and C_3 undergo a progressive charging process in the first half and a discharging process in the second half of the positive phase. The parts highlighted in red in Fig. 2(b) pertain to OCF analysis, which will be elaborated on in Section II-C.

Mode 1 [Table I, Figs. 2 and 3(a)]: Switches S_1, S_2, and S_c are ON, and their complementary switches S_a, S_b, and S_3 are OFF. The inverter current (i_{inv}) is the sum of the I_{dc1} and I_{dc2}. In other words, $i_{inv} = I_{dc1} + I_{dc2}$ where $I_{dc1} = I_{dc2} = 0.5I_{dc}$.

Commutation from Mode 1 to Mode 2 [Figs. 2 and 3(b)]: Switch S_a, which is complementary of S_1 is turned ON. Thus, S_1, S_2, S_a, and S_c are ON, and remaining switches are OFF. The inverter current is equal to $i_{inv} = I_{dc2} = 0.5I_{dc}$.

Mode 2 [Table I, Figs. 2 and 3(c)]: Switches S_a, S_2, and S_c are ON, and their complementary switches S_1, S_b, and S_3 are OFF. The inverter current is equal to $i_{inv} = I_{dc2} = 0.5I_{dc}$.

Commutation from Mode 1 to Mode 3 [Figs. 2 and 3(d)]: Switch S_b, which is complementary of S_2 is turned ON. Thus, S_1, S_2, S_b, and S_c are ON, and the remaining switches are OFF. The inverter current is equal to $i_{inv} = I_{dc1} = 0.5I_{dc}$.

Mode 3 [Table I, Figs. 2 and 3(e)]: Switches S_1, S_b, and S_c are ON, and their complementary switches S_a, S_2, and S_3 are OFF. The inverter current is equal to $i_{inv} = I_{dc1} = 0.5I_{dc}$.

Commutation from Mode 1 to Mode 4 [Figs. 2 and 3(f)]: Switch S_3, which is complementary of S_c is turned ON. Thus,

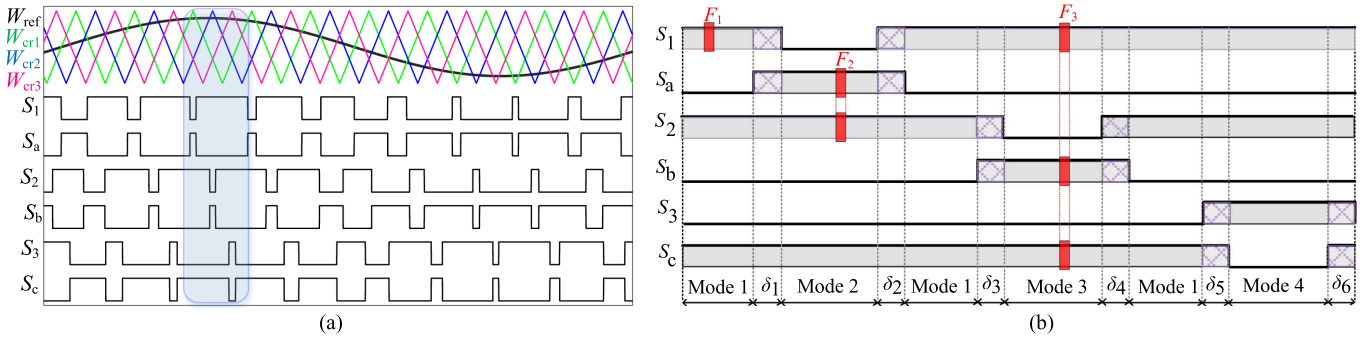

Fig. 2. (a) Reference, carrier, and gating signals generated by the PS-PWM for the proposed FT-SC^{2}SI. (b) Zoomed view of the highlighted part in (a).

TABLE II
ABBREVIATIONS USED IN TABLES III–VIII

OFF S-H: OFF switches under healthy condition	OFF S-OCF: OFF switches under OCF condition	CP-H: current path under healthy condition
CP-OCF: current path under OCF	MVS_C-H: maximum voltage stress on CS capacitor under healthy operating condition	
MVS_C-OCF: maximum voltage stress on CS capacitor under OCF	MVS_S-H: maximum voltage stress on switch under normal/healthy condition	
MVS_S-OCF: maximum voltage stress on switch under OCF	OFF S-PF: OFF switches under PF condition	
OFF S-δ_X (X = 1, 2, 3, …): OFF switches under commutation (overlap-time) intervals	CP-PF: current path under PF condition	
CP-δ_X: current path under commutation intervals	MVS_C-PF: maximum voltage stress on CS capacitor under PF condition	
MVS_C-δ_X: maximum voltage stress on CS capacitor under commutation intervals	MVS_S-PF: maximum voltage stress on switch under PF condition	
MVS_S-δ_X: maximum voltage stress on switch under commutation intervals		

S_1, S_2, S_3, and S_c are ON, and the remaining switches are OFF. The inverter current is equal to zero.

Mode 4 [Table I, Figs. 2 and 3(g)]: Switches S_1, S_2, and S_3 are ON, and their complementary switches S_a, S_b, and S_c are OFF. The inverter current is equal to zero.

C. Operation of the Proposed Topology Under Faulty Condition

There are six possibilities of harmful OCF occurrences in each operation mode/state, leading to a total of 48 occurrences throughout one fundamental period, plus one worst-case OCF scenario involving all switches, resulting in 49 OCF occurrences in total. The proposed topology should be safeguarded against these.

During the faulty operating condition, the SC capacitors are charged through input dc current. By presuming that all SC capacitors enjoy the same capacitance $C_1 = C_2 = C_3 = C$ the increase in the voltage of the capacitors is calculated as

$$\Delta V_{C1} = \Delta V_{C2} = \Delta V_{CA} = \frac{0.5 I_{dc}}{C} \Delta t_d \tag{1}$$

$$\Delta V_{C3} = \Delta V_{CB} = \frac{I_{dc}}{C} \Delta t_d \tag{2}$$

in which ΔV_{C1}–ΔV_{C3} represent the permissible increase in voltages of the SC capacitors under faulty conditions, while Δt_d is the duration time of the faulty operating conditions. Based on Figs. 2(b) and 3, which show the zoomed view of the highlighted region in Fig. 2(a), the fault-tolerant operation of the proposed topology under OCF occurrences on different switches in Modes 1–3 is explained here. The performance of the proposed inverter under the remaining modes and different fault scenarios can be analyzed similarly. The abbreviations used in Tables III–VIII are summarized in Table II.

OCF on S_1 at point F_1 in Mode 1 [Table III, Figs. 2(b), and 3(a), (h)]: Before the occurrence of the fault, the proposed inverter operates in Mode 1, wherein switches S_1, S_2, and S_c are ON, while their complementary switches S_a, S_b, and S_3 are OFF [see Fig. 3(a)]. In this state, the inverter's current (i_{inv}) flows through S_1, S_2, S_c, D_1, D_2, and D_c. However, once an OCF occurs at S_1, denoted as point F_1 in Fig. 2(b), the current path of the I_{dc1} shifts from S_1 to C_1 and D_a [see Fig. 3(h)]. During this fault condition, the voltage across capacitor C_1 increases from zero to ΔV_{CA}, affecting switches S_1 and S_a. Consequently, the stress voltage on S_1 increases from zero to ΔV_{CA}, while the voltage on S_a rises from V_o to $V_o + \Delta V_{CA}$. No changes are observed in the remaining power devices and SC capacitors. Further details of this scenario are provided in Table III.

PF and recovery period after point F_1 [Table IV, Figs. 2(b), and 3(a), (i)]: After the fault at point F_1, the operation of the proposed inverter returns to a healthy/normal condition in Mode 1, as depicted in Fig. 2(b). Nevertheless, the previous conditions regarding stress voltage on power devices and SC capacitors remain unchanged in the PF condition. The proposed inverter continues to function until the operation enters the commutation/overlap-time interval, δ_1 [see Fig. 3(i) and δ_1 in Fig. 2(b)]. During the overlap-time/commutation interval (δ_1), S_a, which is the complementary switch of S_1, is switched ON [see Fig. 3(i)]. Diodes D_1 and D_a are reverse-biased through C_1. Consequently, the voltage ΔV_{CA} on C_1 is discharged through S_1, S_a, S_c, and D_c, allowing the converter to continue operating under

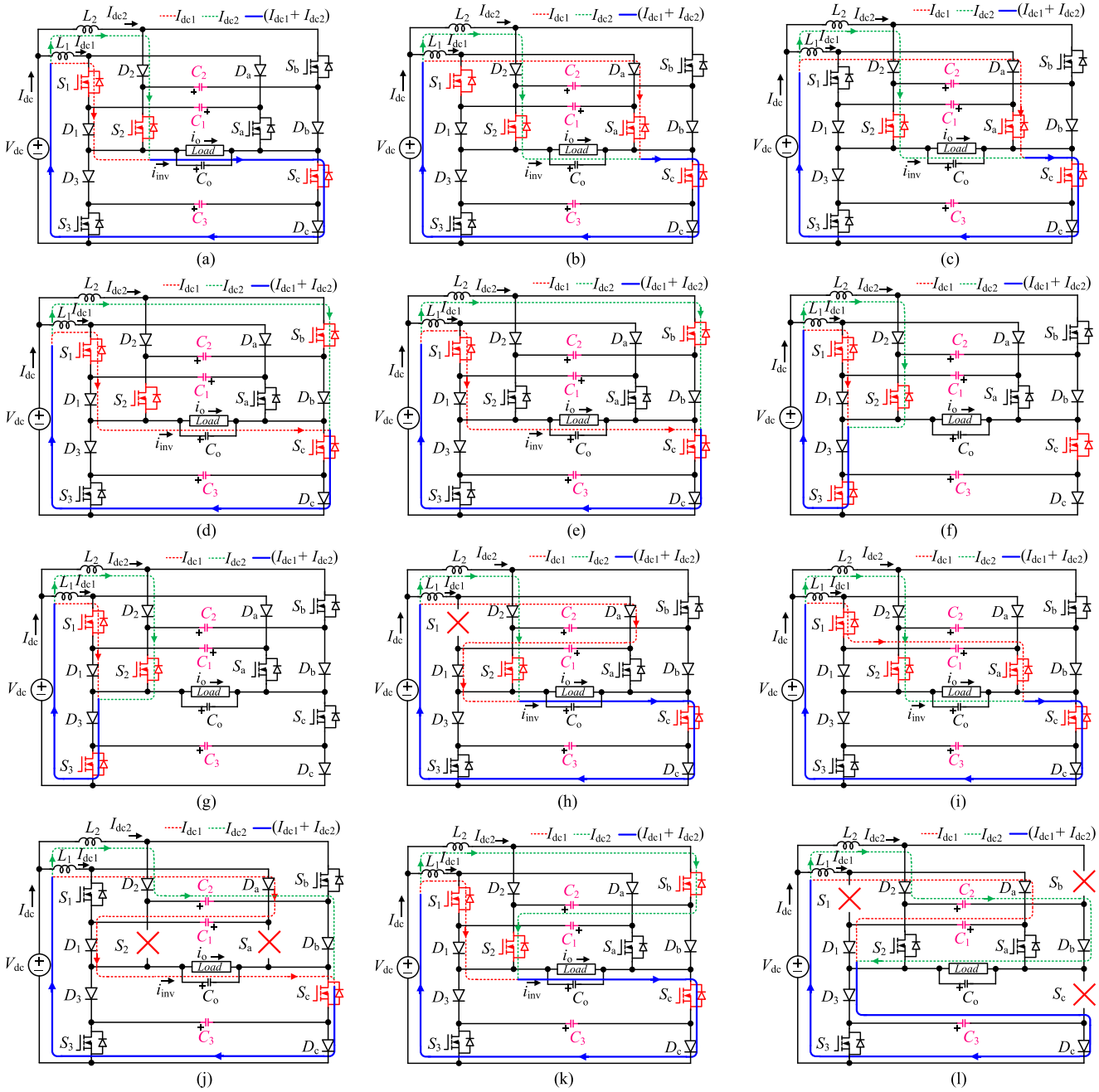

Fig. 3. Operation modes of the proposed topology. Under healthy condition: (a) Mode 1. (b) δ_1&δ_2. (c) Mode 2. (d) δ_3&δ_4. (e) Mode 3. (f) δ_5&δ_6. (g) Mode 4. Under faulty condition: (h) OCF on S_1 in Mode 1. (i) δ_1 and δ_2 after PF. (j) OCF on S_a and S_2 in Mode 2. (k) δ_3 after PF. (l) OCF on all switches in Mode 3.

TABLE III
OCF AT F_1 IN MODE 1

OFF S-H	OFF S-OCF	CP-H	CP-OCF	MVS$_C$-H	MVS$_C$-OCF	MVSs-H	MVSs-OCF
S_3, S_a, S_b	S_1, S_3, S_a, S_b	S_1, S_2, S_c D_1, D_2, D_c	S_2, S_c, C_1 D_1, D_2, D_a, D_c	$V_{C1} = 0$ $V_{C2} = V_{C3} = V_o$	$V_{C1} = \Delta V_{CA}$ $V_{C2} = V_{C3} = V_o$	$V_{S1} = V_{S2} = V_{Sc} = 0$ $V_{Sa} = V_{Sb} = V_{S3} = V_o$	$V_{S1} = \Delta V_{CA}$, $V_{Sa} = V_o + \Delta V_{CA}$ $V_{S2} = V_{Sc} = 0$, $V_{Sb} = V_{S3} = V_o$

TABLE IV
PF AFTER F_1 AND RECOVERY AT δ_1

OFF S-PF	OFF S-δ_1	CP-PF	CP-δ_1	MVS$_C$-PF	MVS$_C$-δ_1	MVSs-PF	MVSs-δ_1
S_3, S_a, S_b	S_3, S_b	S_1, S_2, S_c D_1, D_2, D_c	S_1, S_2, S_a, S_c C_1, D_2, D_c	$V_{C1} = \Delta V_{CA}$ $V_{C2} = V_{C3} = V_o$	$V_{C1} = 0$ $V_{C2} = V_{C3} = V_o$	$V_{S1} = \Delta V_{CA}$, $V_{Sa} = V_o + \Delta V_{CA}$ $V_{S2} = V_{Sc} = 0$, $V_{Sb} = V_{S3} = V_o$	$V_{S1} = V_{S2} = V_{Sc} = 0$ $V_{Sa} = V_{Sb} = V_{S3} = V_o$

TABLE V
OCF AT F_2 IN MODE 2

OFF S-H	OFF S-OCF	CP-H	CP-OCF	MVS$_C$-H	MVS$_C$-OCF	MVSs-H	MVSs-OCF
S_3, S_1, S_b	S_1, S_3, S_a, S_b, S_2	S_a, S_2, S_c D_a, D_2, D_c	S_c, C_1, C_2 D_1, D_2, D_a, D_b	$V_{C1} = 0$ $V_{C2} = V_{C3} = V_o$	$V_{C1} = \Delta V_{CA}$ $V_{C2} = V_o + \Delta V_{CA}$ $V_{C3} = V_o$	$V_{Sa} = V_{S2} = V_{Sc} = 0$ $V_{S1} = V_{Sb} = V_{S3} = V_o$	$V_{S2} = V_{Sa} = \Delta V_{CA}$ $V_{S1} = V_{Sb} = V_o + \Delta V_{CA}$ $V_{S3} = V_o$, $V_{Sc} = 0$

TABLE VI
PF AFTER F_2 AND RECOVERY AT δ_2

OFF S-PF	OFF S-δ_2	CP-PF	CP-δ_2	MVS$_C$-PF	MVS$_C$-δ_2	MVSs-PF	MVSs-δ_2
S_3, S_1, S_b	S_3, S_b	S_a, S_2, S_c D_a, D_2, D_c	S_1, S_2, S_a, S_c C_1, D_2, D_c	$V_{C1} = \Delta V_{CA}$ $V_{C2} = V_o + \Delta V_{CA}$ $V_{C3} = V_o$	$V_{C1} = 0$ $V_{C2} = V_o + \Delta V_{CA}$ $V_{C3} = V_o$	$V_{Sb} = V_o + \Delta V_{CA}$ $V_{Sa} = V_{S2} = V_{Sc} = 0$ $V_{S1} = V_{S3} = V_o$	$V_{Sb} = V_o + \Delta V_{CA}$ $V_{S1} = V_{Sa} = V_{S2} = V_{Sc} = 0$ $V_{S3} = V_o$

TABLE VII
PF AFTER F_2 AND RECOVERY AT δ_3

OFF S-H	OFF S-δ_3	CP-PF	CP-δ_3	MVS$_C$-PF	MVS$_C$-δ_3	MVSs-PF	MVSs-δ_3
S_3, S_a, S_b	S_3, S_a	S_1, S_2, S_c D_1, D_2, D_c	S_1, S_2, S_b, S_c, D_1, D_c, C_2	$V_{C1} = 0$ $V_{C2} = V_o + \Delta V_{CA}$ $V_{C3} = V_o$	$V_{C1} = 0$ $V_{C2} = V_o$ $V_{C3} = V_o$	$V_{Sb} = V_o + \Delta V_{CA}$ $V_{Sa} = V_{S2} = V_{Sc} = 0$ $V_{S1} = V_{S3} = V_o$	$V_{S1} = V_{S2} = V_{Sb} = V_{Sc} = 0$ $V_{Sa} = V_{S3} = V_o$

normal conditions. More details of this scenario are highlighted in Table IV.

OCF on S_a and S_2 at point F_2 in Mode 2 [Table V, Figs. 2(b), and 3(c), (j)]: Prior to the fault event, the proposed inverter operates in Mode 2, where switches S_a, S_2, and S_c are in the ON state, while their complementary switches S_1, S_b, and S_3 remain in the OFF state [see Figs. 2(b) and 3(c)]. Upon the occurrence of an OCF at S_a and S_2, identified as point F_2 in Fig. 2(b), the current path of I_{dc2} transitions from S_2 to C_2 and D_b, while the current path of I_{dc1} transitions from S_a to C_1 and D_1 [see Fig. 3(j)]. Throughout this fault condition, the voltage across capacitor C_2 escalates from V_o to $V_o + \Delta V_{CA}$, while the voltage across capacitor C_1 increases from zero to ΔV_{CA}, impacting switches S_a, S_1, S_2, and S_b. Consequently, the stress voltage on S_a and S_2 escalates from zero to ΔV_{CA}, whereas the voltage on S_1 and S_b escalates from V_o to $V_o + \Delta V_{CA}$. No alterations are discernible in the C_3. Additional details pertaining to this scenario are furnished in Table V.

PF condition after point F_2 [Table VI and VII, Figs. 2(b), and 3(c), (i), (k)]: Following the fault occurrence at point F_2, the proposed inverter's operation reverts to a healthy/normal state in Mode 2, as illustrated in Figs. 2(b) and 3(c). However, the preceding conditions pertaining to stress voltage on power devices and SC capacitors remain unaltered in the PF state. The proposed inverter continues its functioning until it progresses into the commutation/overlap-time interval, δ_2 [see Fig. 3(i) and δ_2 in Fig. 2(b)]. During the overlap-time/commutation interval (δ_2), S_1, the complementary switch of S_a, is switched ON [see Fig. 3(i)]. Diodes D_1 and D_a are reverse-biased through C_1. Consequently, the voltage ΔV_{CA} on C_1 is discharged through S_1, S_a, S_c, and D_c. Table VI provides more details about this period. After δ_2, the operation mode of the proposed inverter enters Mode 1 [see Fig. 2(b)]. However, $V_o + \Delta V_{CA}$ on C_2 still exists. This condition continues until the operation of the suggested inverter enters δ_3, as depicted in Fig. 2(b) and the equivalent circuit diagram shown in Fig. 3(k). Upon entering δ_3, S_b, the complementary switch of S_2, is also turned ON [see Fig. 3(k)]. Diodes D_2 and D_b are reverse-biased through C_2. Consequently, the voltage $V_o + \Delta V_{CA}$ on C_2 is discharged through S_2, S_b, S_c, and D_c, facilitating the converter's continued operation under normal conditions. Further elucidation of this scenario is presented in Table VII.

OCF on S_1, S_2, S_c, (all switches are OFF) at point F_3 in Mode 3 [Table VIII, Figs. 2(b), and 3(e), (l)]: Before the fault occurs, the proposed inverter operates in Mode 3, with switches S_1, S_b, and S_c turned ON while the others are OFF [see Fig. 3(e)]. When switches S_1, S_b, S_c face OCF (all switches are OFF), the input dc inductors' currents I_{dc1} and I_{dc2} are not interrupted and flow via the SC capacitors C_1, C_2, and C_3 and diodes D_1, D_2, D_3, D_a, D_b, and D_c [see Fig. 3(l)]. The voltage across C_1, C_2, and C_3 increases from zero to ΔV_{CA}, from V_o to $V_o + \Delta V_{CA}$, and from V_o to $V_o + \Delta V_{CB}$, respectively. The analysis of PF conditions, with all switches in the OFF position, can be conducted based on the previous PF investigation. More details about this situation can be found in Table VIII. While it is also possible that the OCF may not occur simultaneously among switches, the overall consequence is similar to when they do if the OCF happens within a single mode. If the OCF on switches is distributed across different modes, the faulty condition can be considered as a single switch fault and can be analyzed for each faulty point separately, following the same approach used for OCF at point F_1. Unlike the proposed topology, if the same fault occurs in traditional CSIs, the currents of the inductors are interrupted, resulting in significant overvoltage on the power devices, which could cause severe damage to the converter.

D. Sensitivity Analysis for Parameter Mismatch Between L_1 and L_2

To simplify the sensitivity analysis of the proposed inverter under parameter mismatch conditions, it is assumed that due to the unequal inductance values of the input dc chokes, their

TABLE VIII
OCF AT F_3 IN MODE 3

OFF S-H	OFF S-OCF	CP-H	CP-OCF	MVS$_C$-H	MVS$_C$-OCF	MVSs-H	MVSs-OCF
S_3, S_a, S_2	all switches	S_1, S_b, S_c D_1, D_b, D_c	C_1, C_2, C_3 D_1, D_2, D_3, D_a, D_b, D_c	$V_{C1} = 0$ $V_{C2} = V_{C3} = V_o$	$V_{C1} = \Delta V_{CA}$ $V_{C2} = V_o + \Delta V_{CA}$ $V_{C3} = V_o + \Delta V_{CB}$	$V_{S1} = V_{Sb} = V_{Sc} = 0$ $V_{Sa} = V_{S2} = V_{S3} = V_o$	$V_{S1} = V_{Sb} = \Delta V_{CA}$ $V_{Sa} = V_{S2} = V_o + \Delta V_{CA}$ $V_{S3} = V_o + \Delta V_{CB}$ $V_{Sc} = \Delta V_{CB}$

TABLE IX
INVERTER CURRENT IN THE PROPOSED TOPOLOGY UNDER NORMAL AND PARAMETER MISMATCH CONDITIONS

Operation condition	Mode 1	Mode 2	Mode 3	Mode 4
Normal	$I_{dc1} = I_{dc2} = 0.5I_{dc}$ $i_{inv} = I_{dc1} + I_{dc2} = I_{dc}$	$I_{dc1} = I_{dc2} = 0.5I_{dc}$ $i_{inv} = I_{dc2} = 0.5I_{dc}$	$I_{dc1} = I_{dc2} = 0.5I_{dc}$ $i_{inv} = I_{dc1} = 0.5I_{dc}$	$I_{dc1} = I_{dc2} = 0.5I_{dc}$ $i_{inv} = 0$
Mismatch	$I_{dc1} = 0.6I_{dc}$, $I_{dc2} = 0.4I_{dc}$ $i_{inv} = I_{dc1} + I_{dc2} = I_{dc}$	$I_{dc1} = 0.6I_{dc}$, $I_{dc2} = 0.4I_{dc}$ $i_{inv} = I_{dc2} = 0.4I_{dc}$	$I_{dc1} = 0.6I_{dc}$, $I_{dc2} = 0.4I_{dc}$ $i_{inv} = I_{dc1} = 0.6I_{dc}$	$I_{dc1} = 0.6I_{dc}$, $I_{dc2} = 0.4I_{dc}$ $i_{inv} = 0$

currents experience a $\pm 20\%$ difference. In other words, it is presumed that $I_{dc1} = 0.6I_{dc}$ and $I_{dc2} = 0.4I_{dc}$, instead of the normal condition where $I_{dc1} = I_{dc2} = 0.5I_{dc}$. Again, due to the symmetry in the operational modes of the proposed inverter, parameter mismatch is analyzed in the positive half-cycle. Even though the mismatch condition may cause some deviation between the inductor currents, the inverter current (i_{inv}) and output waveforms are not impacted in Modes 1 and 4. In Mode 4, the inductor currents are bypassed, and the inverter current is zero regardless of whether the inductor currents are different or equal [see Fig. 3(g)]. Similarly, in Mode 1, the inverter current is equal to the input dc current regardless of whether the inductor currents are equal or not, as the inverter current is the sum of these two inductor currents [see Fig. 3(a)]. Although the inverter current is reduced by 20% in Mode 2, its value is compensated in the subsequent mode (Mode 3) [see Fig. 2(b)]. Table IX provides more details about normal and mismatch conditions in the proposed inverter, following Figs. 2 and 3(a), (c), (e), and (g) step-by-step. From this theoretical analysis, it can be concluded that the performance of the proposed topology is not affected under mismatch conditions unless the current mismatch exceeds the saturation current of the inductors. This analysis is verified by experimental results Section III.

E. Design Guideline

Commonly, the input dc choke is designed to maintain the inductor's current fluctuation within the range of 10%–30% of its rated current

$$L_1 = L_2 = L = \frac{V_{in}\sqrt{2}}{4f_o\Delta I_L} \times 0.1 \tag{3}$$

in which L represents the value of inductance, V_{in} is the input dc voltage, f_o denotes the fundamental frequency, and ΔI_L is the allowable current ripple on inductor L.

The capacitance value of SC capacitors (C_1–C_3) is designed based on their ΔV_C and Δt_d. The ΔV_C can be determined as

$$\Delta V_C \leq V_{SWR} - V_{SA} \tag{4}$$

where V_{SA} represents the theoretical/ideal/actual stress voltage on power devices, which is generally equal to V_o in nearly all CSIs and similarly holds true for the suggested inverter. The

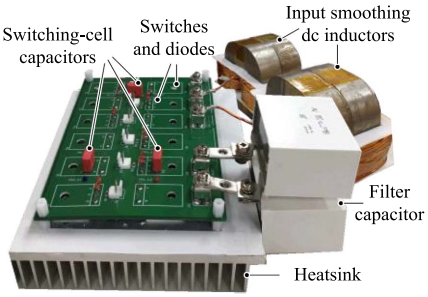

Fig. 4. Hardware prototype of the proposed inverter.

V_{SWR} denotes the voltage rating of selected semiconductor devices, which is typically equal to 150%–200% of V_{SA} for a safety margin. Then, the capacitance value for the SC capacitors is determined using

$$C_1 = C_2 = C_3 = C = \frac{I_{dc}}{\Delta V_C}\Delta t_d m \tag{5}$$

where m represents the number of possible OCF occurrences in a single operation mode, which in the present work is one. However, if it is likely that OCF may occur multiple times during one operation mode, the capacitance value of the SC capacitors will be increased by a factor of m.

To keep the output voltage ripple within the recommended range of less than 5% of its peak value, the output capacitor should be selected as follows:

$$C_o = \frac{I_{dc}}{4f_{sw}\Delta V_{Co}} \tag{6}$$

where C_o is the capacitance value of the output filter capacitor, I_{dc} represents the input dc current, and ΔV_{Co} is the permissible voltage ripple across C_o.

III. EXPERIMENTAL VERIFICATION

Using MOSFETs (IPW60R040C7) in series with diodes (APT30D60BG), and SC capacitors (MKS4G032203G), a prototype was constructed in the laboratory as illustrated in Fig. 4. The PS-PWM strategy along with the overlap-time and OCF was programmed in DSP TMS320F28335. In waveforms shown

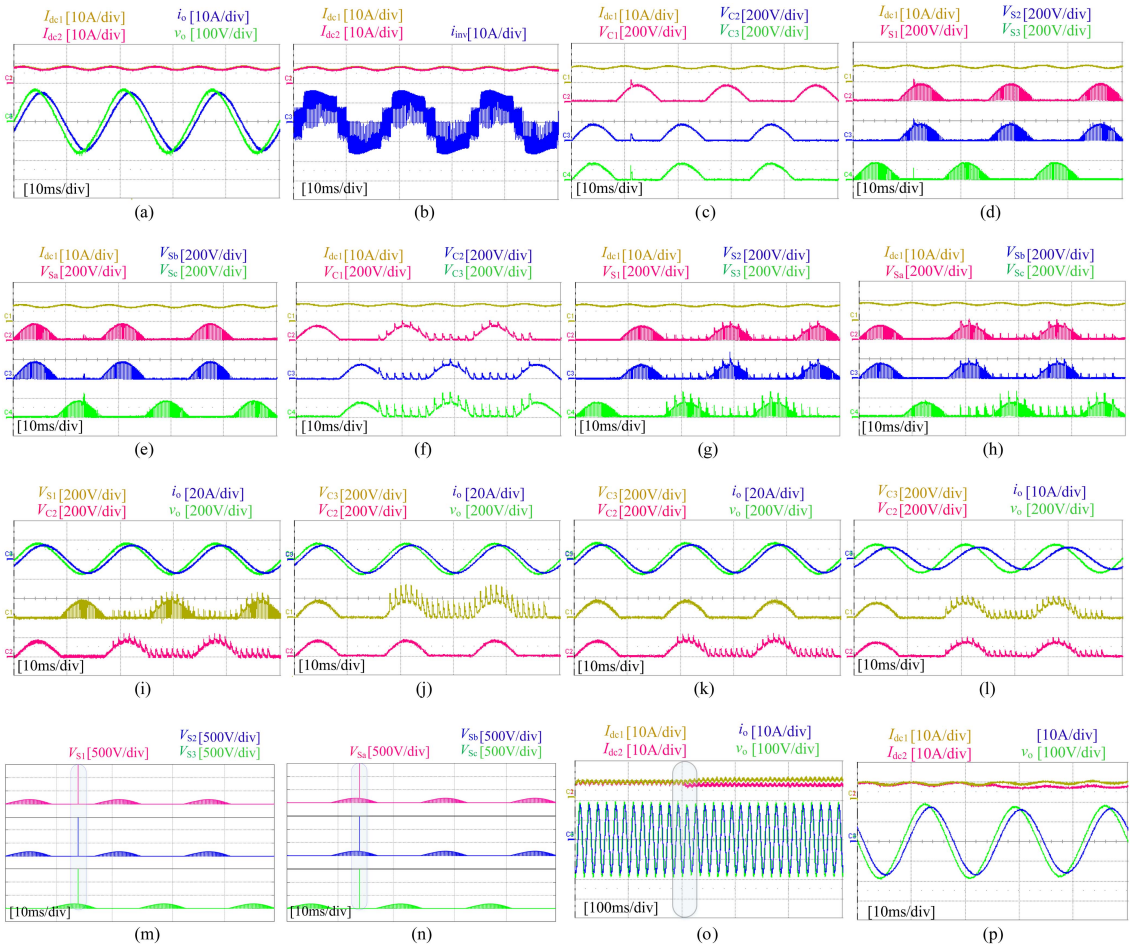

Fig. 5. Experimental and simulation results. (a) Input DC inductors' currents, output current, and output voltage under normal condition. (b) Input DC inductors' currents, and unfiltered inverter's current under normal condition. (c) Stress voltage on SC capacitors and the input DC inductor current under single OCF. (d) and (e) Stress voltage on switches under single OCF. (f) Stress voltage on SC capacitors and the input DC inductor current under frequent OCF. (g) and (h) Stress voltage on switches under frequent OCF. (i) Output current, output voltage, and stress voltage on C_2, and S_1 under frequent OCF. (j)–(l) Output current, output voltage, and stress voltage on C_2, and C_3 under frequent OCF. (m) and (n) Stress voltage on switches under single OCF in D-5LCSI. (o) Input DC inductors' currents, output current, and output voltage under mismatch conditions. (p) Enlarged view of the highlighted part in Fig. 5(o).

TABLE X
EXPERIMENTAL SPECIFICATIONS

Variable	Description	Values
P_o	Output power (kW)	1.2
I_{dc}	Input dc current (A)	18
v_o	Output ac voltage (V_{RMS})	120
f_{sw}	Switching frequency (kHz)	20
f_o	Output frequency (Hz)	60
C_1 to C_3	SC capacitors (μF)	0.22
C_o	Output capacitor (μF)	40
R, L	Load (Ω, mH)	10, 11
δ	Overlap-time (μs)	0.3

in Fig. 5, I_{dc1} and I_{dc2} are dc input inductors' currents; i_o represents output current; v_o is output voltage; i_{inv} denotes inverter's five-level current (before filter); V_{C1}–V_{C3} are stress voltages on SC capacitors; V_{S1}–V_{S3} and V_{Sa}–V_{Sc} demonstrate the voltage stress on switches. The experimental parameters are detailed in Table X. It should be noted that all waveforms shown in Fig. 5 are experimental results, except for Fig. 5(m) and (n), which are simulation waveforms of the D-5LCSI under a single OCF operating condition.

A. Performance of the Proposed Topology Under Normal Condition

The input dc currents, output current and voltage, and the five-level inverter current of the proposed topology are depicted in Fig. 5(a) and (b). As can be seen from these waveforms, the output voltage and current exhibit sinusoidal behavior, and the PS-PWM strategy maintains well-balanced conditions for the inductors' currents [18].

B. Performance of the Proposed Topology Under Faulty Condition

1) Under Single OCF on All Switches: Fig. 5(c) illustrates one of the input inductors' currents (I_{dc1}) together with the stress voltage on SC capacitors in the proposed topology. Initially, the proposed inverter operates under normal conditions, and SC capacitors withstand a voltage stress equal to the peak value of

the output voltage. At approximately 12 ms, a single OCF occurs simultaneously among all power switches with time duration of 1.5 μs. During this faulty interval, the input dc currents are not interrupted, and they charge the SC capacitors by the values of (1) and (2), confirming the theoretical analysis. These extra voltages (ΔV_{CA} and ΔV_{CB}) are mirrored in power devices as illustrated in Fig. 5(d) and (e). It is important to note that these supplementary voltages, occurring during faulty conditions, do not pose a threat to the converter. Generally, power devices are selected with ratings set at 150%–200% higher than their theoretical voltage values.

2) Under Frequent OCF on All Switches: Fig. 5(f) illustrates the voltage across the SC capacitors in the suggested circuit when it is subjected to frequent OCF. At approximately 16 ms, frequent OCF occurs simultaneously among all power switches with a time duration of 1.5 μs. During this faulty interval, the input dc currents are not interrupted, and they charge the SC capacitors by the same value discussed before. As observed in Fig. 5(f), PS-PWM effectively safeguards the proposed topology during frequent OCF occurrences in all power devices. Fig. 5(g) and (h) depicts the stress voltage on switches when the proposed inverter operates under frequent OCF conditions with PS-PWM. No harmful stress voltage is evident in these waveforms. In order to ensure that the quality of output waveforms remains unaffected in the proposed topology under frequent and simultaneous OCF among all switches, an additional test was conducted under more stringent conditions, increasing the fault duration time from 1.5 to 2 μs. This increased fault duration is also applied in the subsequent OCF tests presented in Fig. 5(j)–(l). Fig. 5(i) displays the waveforms of the output voltage, output current, and stress voltage on S_1, and capacitor C_2 under this faulty operating condition. As demonstrated in Fig. 5(i), the quality of the output waveforms remains uncompromised even under such severe faulty conditions.

3) Under Frequent OCF on One Switch (S_3): A less severe OCF test compared to the previous faulty condition is performed, where frequent OCF occurs solely on switch S_3. Fig. 5(j) shows the voltages across capacitors C_3 and C_2, along with the output current and voltage in this fault scenario. As indicated in this figure, only capacitor C_3 undergoes ΔV_{CB} in this OCF condition.

4) Under Frequent OCF on Two Switches (S_1 and S_2): Fig. 5(k) illustrates the situation where frequent OCF occurs concurrently on S_1 and S_2. The figure clearly shows that capacitor C_3 does not experience increased voltage. These tests corroborate the theoretical OCF analysis outlined in Section II-C.

5) Under Frequent OCF on All Switches in a Highly Inductive Load: To evaluate the performance of the proposed topology under conditions of frequent and simultaneous OCF across all devices with various loads, a highly inductive load with values of $RL = 20\ \Omega$ and 62.5 mH (PF = 0.65) was connected to the circuit, and the results are shown in Fig. 5(l). Due to the high inductance of the load and the adjustment of the output voltage to its nominal value, the load current is reduced by nearly half. Consequently, the input dc current drawn from the dc source also decreases. Since the charged voltage of the SC capacitors under OCF scenarios is directly related to the input dc current, as formulated in (1) and (2), the values of ΔV_{CA} and ΔV_{CB} are nearly halved compared to the previous load condition, thereby validating the theoretical analysis. This conclusion is further supported by comparing the stress voltage across capacitors shown in Fig. 5(l) with those in Fig. 5(j) and (k).

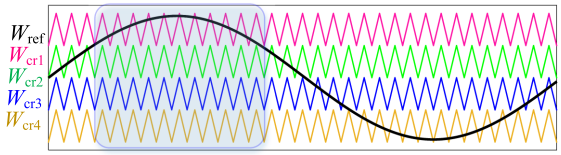

Fig. 6. Reference and carrier waveforms using level-shifted PWM for the topology introduced in [6].

C. Performance of the D-5LCSI Under Faulty Condition

To provide further insight into the significance of the proposed solution, a scenario where a single occurrence of OCF affects all switches with a fault duration ten times smaller (0.15 μs) is also examined on the previously proposed D-5LCSI topology. This examination is conducted through simulation using the MATLAB/Simulink environment, as practical testing could result in damage to the converter. As depicted in Fig. 5(m) and (n), a significant overvoltage is observed on the power devices immediately after the OCF event. Even if this fault occurs in only one switch, severe damage to the D-5LCSI topology is expected due to the disruption of the inductor current.

D. Performance of the Proposed Inverter Under Mismatch Condition

To validate the theoretical sensitivity analysis for parameter mismatch conducted earlier, a significant tolerance of approximately 17.5% in the inductance value of the input dc inductors is deliberately introduced in an experimental setup. As depicted in Fig. 5(o) and (p), the proposed topology initially operates under normal conditions with both inductors, L_1 and L_2, set to 26 mH. Subsequently, an additional 5.5 mH inductor is introduced to L_2, raising its inductance to 31.5 mH, while L_1 remains at 26 mH. Despite this substantial mismatch, the output waveforms remain unaffected, although the inductor currents exhibit slight deviations from their reference values. These findings closely match the theoretical analysis. It is worth noting that such a significant mismatch with dynamic changes was intentionally introduced to clarify the visibility of the results. However, in real-world scenarios, encountering such a large mismatch, even under unfavorable design or manufacturing processes, is unlikely.

Table XI presents a comparison between the proposed topology and five other 5L-CSIs. It should be mentioned that except for OCF handling capability, all remaining comparisons in Table XI assume normal operating conditions. While CSIs in [6] and [7] demonstrate the capability to mitigate single OCF, the proposed topology excels by offering handling capabilities for both single and frequent OCF occurrences. To elaborate on why the CSIs proposed in [6] cannot manage frequent OCF scenarios, Fig. 6 depicts the reference and carrier waveforms of the PWM employed in the topology introduced in [6] as an

TABLE XI
COMPARISON BETWEEN THE PROPOSED AND OTHER 5L-CSI TOPOLOGIES

CSIs	S	D	L_i	L_{sh}	C	MVS_S	MVS_D	MVS_C	MCS_S	MCS_D	MCS_{Li}	MCS_{Lsh}	$SOCF_h$	$FOCF_h$	Di	$	Con.
[20]	8	8	1	2	—	V_o	V_o	—	I_{dc}	I_{dc}	I_{dc}	$0.5I_{dc}$	No	No	**	**	—
[7]	8	8	1	2	4	V_o	V_o	V_o	I_{dc}	I_{dc}	I_{dc}	$0.5I_{dc}$	Yes	—	**	**	Yes
[21]	8	8	1	1	—	V_o	V_o	—	I_{dc},$0.5I_{dc}$	I_{dc},$0.5I_{dc}$	I_{dc}	$0.5I_{dc}$	No	No	*	**	Yes
[6]	8	8	1	1	4	V_o	V_o	V_o	I_{dc},$0.5I_{dc}$	I_{dc},$0.5I_{dc}$	I_{dc}	$0.5I_{dc}$	Yes	No	*	**	Yes
[8]	6	6	2	—	—	V_o	V_o	—	I_{dc},$0.5I_{dc}$	I_{dc},$0.5I_{dc}$	$0.5I_{dc}$	—	No	No	*	**	Yes
Prop.	6	6	2	—	3	V_o	V_o	V_o	I_{dc},$0.5I_{dc}$	I_{dc},$0.5I_{dc}$	$0.5I_{dc}$	—	Yes	Yes	*	*	No

Note: S: number of (No.) switches; D: No. diodes; L_i: No. input dc chocks; L_{sh}: No. sharing/intermediate inductors; C: No. capacitors; MVS_S: maximum voltage stress on switch; MVS_D: maximum voltage stress on diode; MVS_C: maximum voltage stress on capacitor; MCS_S: maximum current stress on switch; MCS_D: maximum current stress on diode; MCS_{Li}: maximum current stress on input dc chock; MCS_{Lsh}: maximum current stress on sharing/intermediate inductor; SOCFh: single OCF handling capability; FOCFh: frequent OCF handling capability; Di: Dimension/volume/size [**: large, *: medium]; $: cost [**: expensive, *: cheap] *: cheap]; Con.: controller.

TABLE XII
LOSS BREAKDOWN BETWEEN THE PROPOSED AND OTHER 5L-CSI TOPOLOGIES

CSIs	PS_{SW}	PC_{SW}	PC_D	P_L	P_{Co}	P_{ot}	η
[20], [7]	13.9 W	5.3 W	10.6 W	26 W	0.4 W	1.3 W	95.2%
	24.2%	9.2%	18.4%	45.2%	0.7%	2.3%	
[21], [6]	20.9 W	13.2 W	17.53 W	14.34 W	0.4 W	1.3 W	94.3%
	30.8%	19.5%	25.9%	21.2%	0.6%	2%	
[8] and proposed	13.9 W	7.92 W	11.42 W	23.5 W	0.4 W	1.3 W	95.1%
	23.8%	13.6%	19.5%	40.2%	0.68%	2.2%	

Note: PS_{sw}: switching loss in the switch; PC_{sw}: conduction loss in the switch; PC_D: conduction loss in the diode; P_L: loss in the inductor; P_{Co}: loss in the output capacitor; P_{ot}: loss caused by overlap-time; and η: efficiency.

example. Within the highlighted region indicated in Fig. 6, the reference signal (W_{ref}) is solely compared with carrier1 (W_{cr1}). Consequently, only two out of the eight switches are turned ON and OFF during this interval, while the remaining six switches remain inactive. Therefore, in the event of frequent OCFs during this period, the absence of switching and overlapping times for these six switches causes a gradual increase in voltage across the capacitors, thereby affecting the power devices. This sustained voltage rise across the SC capacitors and power devices may exceed the voltage rating of the semiconductor devices, potentially resulting in damage to the converter. Traditional CSIs [8], [20], [21] will be severely damaged even if a single switch encounters a single OCF, as the inductor current is interrupted. In almost all converters, an extra controller is employed to balance the current of inductors, except in the proposed inverter, which can achieve this through PS-PWM [18]. The natural balancing capability of PS-PWM for inductor currents depends on the specific configuration of the converter. This modulation scheme may not be applicable to all topologies and may fail to generate desirable waveforms. For instance, applying PS-PWM does not produce desirable waveforms for the topology proposed in [6] and [21] necessitating the implementation of an additional closed-loop controller or an improved/new PWM technique. As shown in Table XI, the configurations of both the proposed topology and the one described in [8] feature a reduced number of active and passive power devices, which also require two fewer gating channels in the gate driver and their associated expensive components (e.g., gate driver ICs). In addition, this decrease in the number of switches in the proposed topology not only lowers its cost but also simplifies the PWM/controller. Although the proposed and other SC CSI structures presented in [6] and [7] incorporate additional SC capacitors, these do not require extra space on the PCB layout (see Fig. 4). Moreover, the cost of these SC capacitors in the proposed inverter is considerably less than the cost associated with the four additional semiconductor devices and the two extra gate driver channels found in [6], [7], [20], and [21]. It may seem that the proposed inverter is more expensive than the topology in [8]; however, the PWM in [8] lacks the ability to naturally balance the inductors' current, which necessitates the use of expensive current sensors. Moreover, in the event of a single OCF affecting only one switch in the topologies discussed in [8], [20], and [21] throughout their lifespan, these converters may incur significant damage. As a result, there may be a need to replace the inverter, leading to a doubling of the converter's cost. The configurations introduced in [20] (MR-ML-CSI) and [7] contain the greatest quantity of inductors, which may lead to a larger physical size compared to other topologies. The power loss for each topology is calculated according to [6], [22], [23], [24], [25], [26], with the breakdown of losses and efficiency detailed in Table XII. While no difference is observed in stress voltage on devices across the various topologies under normal operating conditions, the current stress on power devices varies among the compared converters (see Table XI). Consequently, the distribution of losses among power devices in the proposed topology and those in [6], [8], and [21] may not be equal. As a result, the efficiency of the proposed inverter is not higher than that of [7] and [20]. To overcome this limitation in the proposed topology, new or modified PWM/control strategies can be explored as part of future work. Moreover, the efficiency of the proposed inverter can be further enhanced by considering software/hardware decoupling techniques [27] and [28].

IV. CONCLUSION

In this article, a new 5L-CSI has been introduced to address the issue of OCF associated with traditional CSC topologies. The proposed remedy, both simple and effective, protects the

suggested inverter against frequent OCF, even if it occurs simultaneously on all switches. The PS-PWM method has been employed to control the suggested inverter for two reasons: 1) other modulation approaches cannot protect the FT-SC^{2}SI under frequent OCF scenarios, and 2) it provides natural current balancing of the paralleled input dc chokes, eliminating the need for an extra controller. The functionality of the proposed topology has been thoroughly examined under normal, faulty, and parameter mismatch conditions, with experimental tests confirming its efficacy. Moreover, a comparative analysis has been conducted between the proposed solution and five other five-level CSI configurations to elucidate their unique attributes and limitations. The proposed topology is well-suited for PV applications because it inherently boosts voltage. This feature eliminates the need for an additional front-end dc–dc converter, which is commonly used in VSIs, thereby simplifying control and implementation. In addition, the proposed inverter overcomes the shoot-through issue found in VSIs and the OCF problem in conventional CSIs, enhancing its fault tolerance and reliability.

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