Dynamic Analytical Switching Loss Model of SiC MOSFET Considering Threshold Voltage Instability

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***Abstract*—Accurate modeling of switching loss is critical for silicon carbide MOSFETs as well as power converters. However, previous "static" time-independent models did not consider the impact of gate oxide degradation on switching performance during long-term operation. This article proposes a "dynamic" time-dependent analytical model considering threshold voltage ($V_{\rm TH}$) instability caused by gate oxide degradation to predict switching loss. The influence of $V_{\rm TH}$ instability on the turn-ON and turn-OFF $V_{\rm TH}$, as well as on switching loss during continuous operation is revealed first. Moreover, the problems suffered in the existing analytical model are investigated, and an improved switching loss model is presented. A measurement-based method to obtain the $V_{\rm TH}$ instability parameters for modeling is provided. Furthermore, a buck converter is built and operated under different conditions. Comparisons of switching waveforms and switching losses between experiments and the proposed model are given to validate the model. The results indicate that the proposed analytical model can effectively evaluate the switching loss, with an error within 7% under different continuous operating conditions. Finally, the universality of the proposed model for devices with different structures is verified, and a predication application of the model in operation is demonstrated.**

***Index Terms*—Analytical model, buck, dynamic, SiC MOSFETs, switching loss, threshold voltage instability.**

I. Introduction

THE power losses of the semiconductors are typically the largest loss contributors in power converters [1]. Especially, the switching losses become dominant for silicon carbide (SiC) MOSFETs with high switching frequency. These may have a significant impact on the cooling system [2]. Therefore, an accurate modeling of switching loss is critical for evaluating and optimizing converter design.

The existing models for predicting switching loss can be mainly divided into three categories: 1) simulation model, 2) numerical model, and 3) analytical model. For the simulation model, Mantooth et al. [3] and Santi et al. [4] reviewed a lot of physical models and discussed the basic physical principles of the corresponding semiconductor devices. Mukunoki et al. [5] presented an improved compact model for a discrete SiC MOSFETs with a new behavioral model of output characteristics and new nonlinear models of internal capacitors. The improved model showed better reproducibility of the high-frequency transient characteristics. Moreover, Rødal and Peftitsis [6] proposed a discrete and real-time capable dynamic model of high-voltage and high-current SiC MOSFET half-bridge power modules to identify the switching loss, which provided good accuracy with reduced simulation time.

For the numerical model, typically, Ahmed et al. [7] analyzed the switching process of the SiC MOSFET through time segmentation, which is similar to the silicon (Si) MOSFET analytical models in [8]. The difference is that no assumptions were used in SiC MOSFET model and the numerical solutions of the switching loss were given finally. For the analytical model, Chen et al. [9], Wang et al. [10] and Sun et al. [11] conducted a series of research, including a simple model accounting for the nonlinear junction capacitance [9], a comprehensive analytical loss model based on energy conservation [10], and a semiphysical semibehavioral analytical model for the applications in design automation to balance accuracy and efficiency [11]. Dong et al. [12] pointed out that due to the short channel effect and drain-induced barrier lowering (DIBL) effect of SiC MOSFET, the transfer curve varies with the drain-source voltage ($V_{\rm DS}$). The gate-drain capacitance ($C_{\rm GD}$) during the actual switching period is also different from that in the datasheet. Therefore, they proposed an analytical switching-ON loss model considering dynamic transfer characteristics and gate-drain charge ($Q_{\rm GD}$). Qian et al. [13] derived an analytical switching loss equation intuitively based on charge conservation and flux conservation.

The abovementioned research improves the accuracy and efficiency of switching loss prediction from the perspectives of various modeling. However, the effect of the long-term operation of the device on switching performance has yet not been considered in existing "static" time-independent models. Especially, for SiC MOSFETs with high interface state density ($D_{\rm it}$) at

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the SiC/SiO_2 interface, the threshold voltage (V_{TH}) instability caused by gate oxide degradation due to long-term operation is a serious reliability issue [14]. Tanimoto et al. [15] developed a compact SiC MOSFET model including carrier-trap influences and predicted power loss. However, they did not consider the V_{TH} instability. Obviously, the V_{TH} instability directly affects the switching behavior of the device. Therefore, it is important to take this into consideration in the modeling of switching loss.

The V_{TH} instability includes both a permanent V_{TH} shift and a recoverable V_{TH} hysteresis [16]. The impact of V_{TH} hysteresis on switching loss has been investigated recently [17], [18], and it is normally considered in conjunction with the DIBL effect due to the interaction of both effects [19], [20]. The specific method is to obtain the dynamic turn-ON and turn-OFF transfer characteristics, respectively, under positive gate voltage ($V_{\mathrm{GS}}{}^{\mathrm{ON}}$), negative gate voltage ($V_{\mathrm{GS}}{}^{\mathrm{OFF}}$), and V_{DS} of the target switching condition, and then bring them into the switching loss model. However, the permanent V_{TH} shift has not been taken into account. Moreover, an increase in V_{TH} hysteresis with the permanent V_{TH} shift was observed in the devices sensitive to $V_{\mathrm{GS}}{}^{\mathrm{OFF}}$ [21].

To this end, this article considers the V_{TH} instability caused by the long-term operation and proposes a "dynamic" time-dependent switching loss model of SiC MOSFETs. First, the influence of V_{TH} instability on the turn-ON and turn-OFF processes is revealed, respectively. Second, the problems of the existing analytical model are analyzed, and an accurate modeling of dynamic switching loss during continuous operation is proposed. Then, a buck converter is built and operated under different conditions to verify the accuracy of the proposed model. Moreover, the universality of the proposed model for SiC MOSFETs with different gate structures is verified. Finally, a case of the prediction application of the proposed model in actual operation is provided. The improved switching loss model in this article is favorable to effectively evaluate the switching loss of the device and optimize the design of the converter system.

II. Effect of V_{TH} Instability

A. V_{TH} Instability

The V_{TH} instability consists of two parts: 1) a long-term portion $V_{\mathrm{TH}}{}^{\mathrm{SHIFT}}$ and 2) a short-term part V_{TH} hysteresis ($V_{\mathrm{TH}}{}^{\mathrm{HYST}}$). The $V_{\mathrm{TH}}{}^{\mathrm{SHIFT}}$ is a permanent shift in V_{TH} with long-term operation, which is generally considered to be caused by an inelastic charge effect of border traps within SiO_2 close to the SiC/SiO_2 interface [16]. The inelastic tunneling process is triggered not only by the substrate Fermi level position but also by a thermodynamic energy barrier. The barrier may be widely distributed and is typically different for trapping and detrapping. Border traps may undergo a relaxation upon capturing or emitting carriers thereby stabilizing the charge state of a trap for much longer times, and consequently, a permanent $V_{\mathrm{TH}}{}^{\mathrm{SHIFT}}$ occurs [22].

The V_{TH} hysteresis phenomenon refers to the fact that the upward sweep threshold voltage when the device turns ON, $V_{\mathrm{TH}}{}^{\mathrm{UP}}$, is typically lower than the downward sweep threshold voltage $V_{\mathrm{TH}}{}^{\mathrm{DOWN}}$, which is measured when the device turns OFF. This

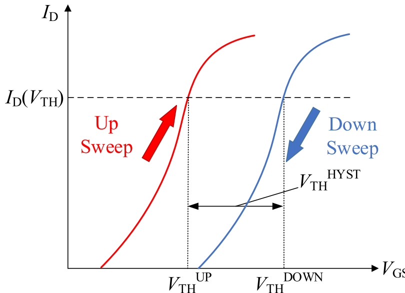

Fig. 1. Schematic of subthreshold V_{TH} hysteresis.

phenomenon depends on the charging and discharging of the interface states located energetically within SiC bandgap, and is triggered by the position of the trap level and the Fermi level at the interface. Moreover, the trap level energy of interface states is invariant, which means they do not undergo relaxation upon capturing or emitting carriers. Therefore, the V_{TH} hysteresis is recoverable during switching process of SiC MOSFETs.

The V_{TH} hysteresis $V_{\mathrm{TH}}{}^{\mathrm{HYST}}$ is defined as the difference between $V_{\mathrm{TH}}{}^{\mathrm{UP}}$ and $V_{\mathrm{TH}}{}^{\mathrm{DOWN}}$. Generally, the V_{TH} hysteresis effects can be observed by measuring the transfer characteristics of SiC MOSFETs, especially in the subthreshold regime [23]. The schematic of subthreshold V_{TH} hysteresis is shown in Fig. 1, and the expression is given as follows:

$$V_{\mathrm{TH}}{}^{\mathrm{HYST}} = V_{\mathrm{TH}}{}^{\mathrm{DOWN}} - V_{\mathrm{TH}}{}^{\mathrm{UP}}. \quad (1)$$

Moreover, the V_{TH} hysteresis is related to $V_{\mathrm{GS}}{}^{\mathrm{OFF}}$ [16]. When $V_{\mathrm{GS}}{}^{\mathrm{OFF}}$ is negative, the device is in accumulation and the donor traps capture holes. Moreover, the lower $V_{\mathrm{GS}}{}^{\mathrm{OFF}}$ is, the more holes are captured. When the device is changed from the accumulation to depletion and then to inversion, the Fermi level quickly moves across the SiC bandgap, which drives the interface states into a nonsteady state, and the discharging of donor traps occurs, causing $V_{\mathrm{TH}}{}^{\mathrm{UP}}$ to decrease. Additionally, the lower $V_{\mathrm{GS}}{}^{\mathrm{OFF}}$ is, the more donor traps discharge and the smaller $V_{\mathrm{TH}}{}^{\mathrm{UP}}$ is [24]. However, the Fermi level changes only slightly, and the thermal equilibrium is restored quickly when V_{GS} is switched from deep inversion to $V_{\mathrm{TH}}{}^{\mathrm{DOWN}}$. $V_{\mathrm{TH}}{}^{\mathrm{DOWN}}$ changes only minimally with changing $V_{\mathrm{GS}}{}^{\mathrm{OFF}}$ during this process. Therefore, the quantity $V_{\mathrm{TH}}{}^{\mathrm{UP}}$ decreases with the lower $V_{\mathrm{GS}}{}^{\mathrm{OFF}}$, and $V_{\mathrm{TH}}{}^{\mathrm{DOWN}}$ is almost not affected, and consequently, $V_{\mathrm{TH}}{}^{\mathrm{HYST}}$ increases.

The evolution of V_{TH} in the continuous operation of the device is shown in Fig. 2.

The quantities $V_{\mathrm{TH}}{}^{\mathrm{UP}}(0)$ and $V_{\mathrm{TH}}{}^{\mathrm{DOWN}}(0)$ shown in Fig. 2 represent the initial V_{TH} of the turn-ON and turn-OFF processes, respectively. It is assumed that $V_{\mathrm{TH}}{}^{\mathrm{UP}}(0)$ and $V_{\mathrm{TH}}{}^{\mathrm{DOWN}}(0)$ have taken into account the influence of the DIBL effect. According to (1), the relationship between $V_{\mathrm{TH}}{}^{\mathrm{UP}}(0)$ and $V_{\mathrm{TH}}{}^{\mathrm{DOWN}}(0)$ can be expressed as

$$V_{\mathrm{TH}}{}^{\mathrm{UP}}(0) = V_{\mathrm{TH}}{}^{\mathrm{DOWN}}(0) - V_{\mathrm{TH}}{}^{\mathrm{HYST}}(0) \quad (2)$$

where $V_{\mathrm{TH}}{}^{\mathrm{HYST}}(0)$ is the initial V_{TH} hysteresis.

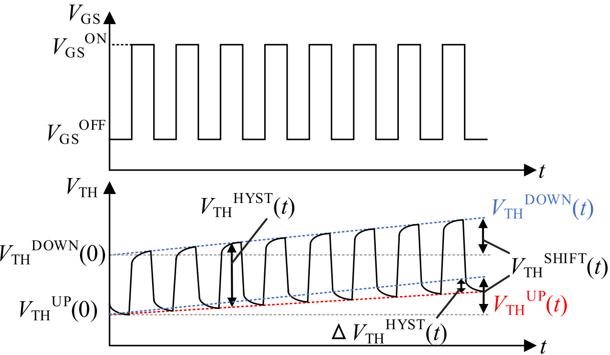

Fig. 2. Schematic evolution of the V_{TH} instability in application.

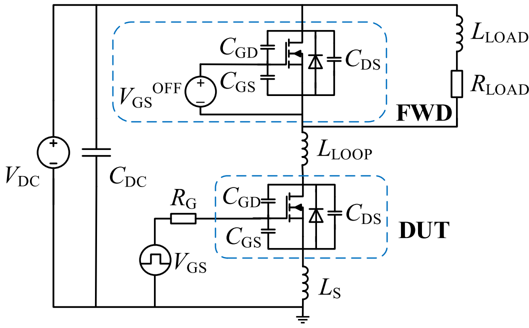

Fig. 3. Typical half-bridge circuit.

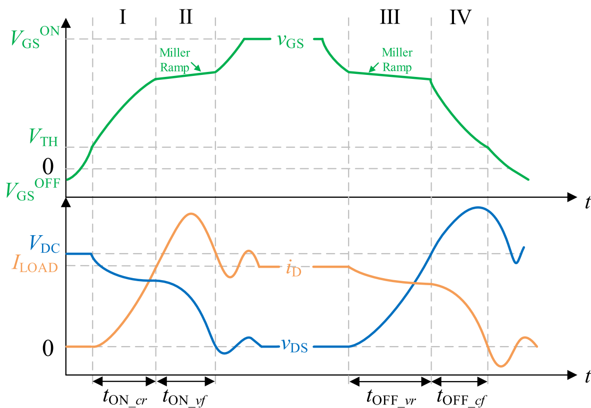

Fig. 4. Switching waveforms.

With the long-term operation of the device, there is a permanent $V_{TH}{}^{SHIFT}(t)$, which is typically positive [25], and consequently, the V_{TH} of both turn-ON and turn-OFF processes increases. However, there is a different magnitude of the increase in $V_{TH}{}^{UP}(t)$ and $V_{TH}{}^{DOWN}(t)$, which comes from the variation of the V_{TH} hysteresis ($\Delta V_{TH}{}^{HYST}(t)$) due to a permanent V_{TH} shift. The positive permanent V_{TH} shift in turn leads to a negative shift in the effective gate voltage value [$V_{GS}{}^{OFF}$- $V_{TH}{}^{UP}(t)$] applied during the V_{TH} hysteresis measurement, thereby causing $V_{TH}{}^{UP}(t)$ to decrease [21]. For example, $V_{GS}{}^{OFF} = -4$ V before any positive V_{TH} shift, but a 2 V positive shift in V_{TH} would result in [$V_{GS}{}^{OFF}$- $V_{TH}{}^{UP}(t)$] changing, such that $V_{GS}{}^{OFF}$ effectively becomes -6 V instead, thus increasing the V_{TH} hysteresis (the change in effective gate voltage value [$V_{GS}{}^{OFF}$- $V_{TH}{}^{DOWN}(t)$] caused by V_{TH} shift does not affect $V_{TH}{}^{DOWN}(t)$).

Therefore, the degraded V_{TH} of the turn-ON and turn-OFF processes in operation can be expressed as

$$V_{TH}{}^{DOWN}(t) = V_{TH}{}^{DOWN}(0) + V_{TH}{}^{SHIFT}(t) \tag{3}$$

$$V_{TH}{}^{UP}(t) = V_{TH}{}^{UP}(0) + V_{TH}{}^{SHIFT}(t) - \Delta V_{TH}{}^{HYST}(t). \tag{4}$$

It can be seen from (3) and (4) that $V_{TH}{}^{DOWN}(t)$ is only affected by $V_{TH}{}^{SHIFT}(t)$, while $V_{TH}{}^{UP}(t)$ is affected by both $V_{TH}{}^{SHIFT}(t)$ and $\Delta V_{TH}{}^{HYST}(t)$, which have opposite effects. Therefore, $V_{TH}{}^{DOWN}(t)$ increases continuously with the gate oxide degradation during long-term operation. However, the change in $V_{TH}{}^{UP}(t)$ depends on the values of $V_{TH}{}^{SHIFT}(t)$ and $\Delta V_{TH}{}^{HYST}(t)$.

B. Effect of V_{TH} Instability on Switching Loss

As mentioned in Section I, the gate oxide degradation of SiC MOSFET due to long-term operation leads to V_{TH} instability, which will affect the switching loss. However, its impact on turn-ON and turn-OFF is different. A typical half-bridge circuit shown in Fig. 3 is used for the analysis and the bottom switch is selected as the device under test (DUT). The top device is in OFF-state and used as a freewheeling diode. L_{LOOP} and L_S are the commutation loop parasitic inductance and source parasitic inductance, respectively. C_{GS} is the gate-source capacitance, C_{DS} is the drain-source capacitance, and R_G is the gate resistance. R_{LOAD} and L_{LOAD} represent the load.

Fig. 4 shows the switching trajectory waveforms of the gate voltage v_{GS}, the drain current i_D, and the drain-source voltage v_{DS} in the switching processes, where "Miller ramp" is caused by the DIBL effect, V_{dc} is the bus voltage, and I_{LOAD} is the load current. t_{ON_cr} and t_{ON_vf} are the durations of current-rise period I and voltage-fall period II of the turn-ON process, and the integral of the product of v_{DS} and i_D in periods I and II is the turn-ON loss (E_{ON}). t_{OFF_vr} and t_{OFF_cf} are the durations of voltage-rise period III and current-fall period IV of the turn-OFF process, and the integral of the product of v_{DS} and i_D in periods III and IV is the turn-OFF loss (E_{OFF}).

The duration of switching periods of the switching process determines the switching loss, and they can be expressed as follows [26]:

$$t_{ON_cr} = R_G\,(C_{GS} + C_{GD}) \ln \left(\frac{V_{GS}{}^{ON} - V_{TH}}{V_{GS}{}^{ON} - V_{GP}} \right) \tag{5}$$

$$t_{ON_vf} = \frac{R_G Q_{GD}}{V_{GS}{}^{ON} - V_{GP}} \tag{6}$$

$$t_{OFF_vr} = \frac{R_G Q_{GD}}{V_{GP} - V_{GS}{}^{OFF}} \tag{7}$$

$$t_{OFF_cf} = R_G\,(C_{GS} + C_{GD}) \ln \left(\frac{V_{GP}}{V_{TH} - V_{GS}{}^{OFF}} \right) \tag{8}$$

where Q_{GD} is the total charge of C_{GD}, and V_{GP} is the Miller ramp voltage, which can be expressed as

$$V_{\mathrm{GP}} = V_{\mathrm{TH}} + \frac{I_{\mathrm{LOAD}}}{G_{\mathrm{m}}} \tag{9}$$

where G_{m} is the transconductance.

It can be seen from (5)–(9) that the parameters affecting the switching times can be divided into two categories: 1) circuit parameters and 2) device parameters. The former refers to R_{G}, $V_{\mathrm{GS}}{}^{\mathrm{ON}}$, and $V_{\mathrm{GS}}{}^{\mathrm{OFF}}$, which are fixed during device operation. The latter includes V_{TH}, V_{GP}, C_{GS}, C_{GD}, and Q_{GD}. Obviously, V_{TH} will degrade in the long-term operation of the device, as well as V_{GP}. In addition, the portions of C_{GS} and C_{GD} are found to be aging-sensitive in low v_{DS} and $v_{\mathrm{GS}} \leq V_{\mathrm{TH}}$ [27], [28]. Therefore, C_{GS} and C_{GD} degrade with time when operation point is at low v_{DS} and v_{GS}. Obviously, the operation point is high v_{DS} and v_{GS} during t_{ON_cr} in (5) and t_{OFF_cf} in (8), and consequently, there is almost no change over time in C_{GS} and C_{GD}.

As for Q_{GD} used in calculating t_{ON_vf} and t_{OFF_vr} in (6) and (7), the Miller "ramp" is transposed to a "plateau" and v_{GS} is in the static Miller plateau voltage when extracting dynamic Q_{GD} according to JEP192 [29]. Since Q_{GD} is the integral of C_{GD} over the Miller plateau time, it can be considered as constant since C_{GD} at $v_{\mathrm{GS}} = V_{\mathrm{GP}}$ hardly changes with the operation. Therefore, it can be concluded that the V_{TH} instability caused by gate oxide degradation under the long-term operation of the device is the vital factor affecting the switching loss.

However, the degradation mechanism of the V_{TH} of turn-ON and turn-OFF processes is different. It can be obtained from (3) that the variation in V_{TH} of the turn-OFF process $V_{\mathrm{TH}}{}^{\mathrm{DOWN}}(t)$ only depends on $V_{\mathrm{TH}}{}^{\mathrm{SHIFT}}(t)$, and it increases with degradation, which causes t_{OFF_vr} and t_{OFF_cf} decrease, and consequently, E_{OFF} decreases. However, the V_{TH} of the turn-ON process $V_{\mathrm{TH}}{}^{\mathrm{UP}}(t)$ varies depending on the values of $V_{\mathrm{TH}}{}^{\mathrm{SHIFT}}(t)$ and $\Delta V_{\mathrm{TH}}{}^{\mathrm{HYST}}(t)$. If $V_{\mathrm{TH}}{}^{\mathrm{UP}}(t)$ increases, t_{ON_cr} and t_{ON_vf} increase, and thus $E_{\mathrm{_ON}}$ increases. On the contrary, $E_{\mathrm{_ON}}$ decreases.

Therefore, the V_{TH} instability caused by the long-term degradation of the device has an important and complicated influence on the switching loss. To accurately evaluate and predict device performance, it is necessary to account for the V_{TH} instability in turn-ON and turn-OFF loss modeling separately.

III. Improved Dynamic Analytical Switching Loss Model

A. Existing Static Analytical Model

Since analytical model provides the most intuitive explanation and the highest calculation efficiency compared to other prediction methods of switching loss, an analytical switching loss model [13] is adopted in this article. The model is derived intuitively by linearizing the switching transients, and the linearized switching waveforms are shown in Fig. 5, where V_1 is the v_{DS} at the end of the current-rise period I, I_1 is the i_{D} at the end of the voltage-rise period III, and $\Delta V_{\mathrm{DSMAX}}$ is the turn-OFF overvoltage.

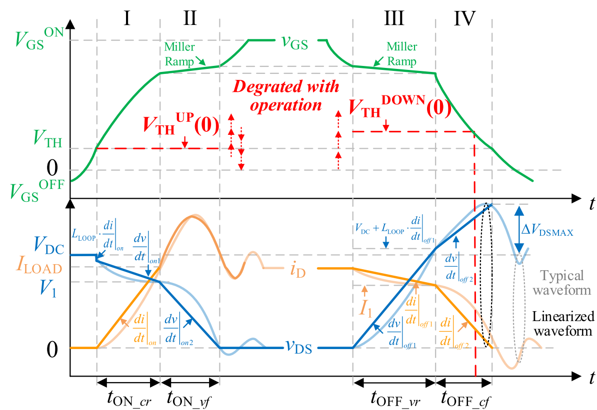

Fig. 5. Linearized switching waveforms.

Based on the simplification method, the duration of each period can be derived by combining the gate charge conservation equation in integral form and the charge/flux conservation equation shown in Table I. It is worth pointing out that since the gate loop equation is in integral form in this model, the charge characteristics, such as Q_{GD} and output capacitance charge Q_{OSS}, can be obtained from the device datasheet or measurement, and the influences of nonlinearity of parasitic capacitance have been included. Furthermore, the slew rate of the drain current di/dt and the slew rate of the drain-source voltage dv/dt can be described separately, and the expressions of v_{DS} and i_{D} are obtained. Finally, the predicted switching loss is the time integral of the product of v_{DS} and i_{D}.

In the above derivation process, ΔV_{TH1} was introduced considering the dynamical lower V_{TH} caused by the DIBL effect and interface state effect, which can be approximated as the difference between V_{GP} read from the static transfer curve (the V_{GS} at load current) and the gate charge (Q_{G}) curve (the V_{GS} at the first turning point) provided in the device datasheet. Consequently, (V_{TH}-ΔV_{TH1}) represents the dynamic V_{TH}. However, the model suffers from the following problems when predicting switching loss during long-term operation.

1) There is an error in the initial V_{TH} for the turn-OFF transient.

The presence of V_{TH} hysteresis leads to different V_{TH} for turn-ON and turn-OFF processes, and thus, different V_{GP}, as well as different Q_{G} curves shown in Fig. 6. It is necessary to define $V_{\mathrm{GS}}{}^{\mathrm{OFF}}$ of Q_{G} measurement. Generally, the Q_{G} curve provided in the datasheet is obtained during device turn-ON at the recommended $V_{\mathrm{GS}}{}^{\mathrm{OFF}}$. Therefore, ΔV_{TH1} reflects the influence of the DIBL and V_{TH} hysteresis effects on the V_{TH} of turn-ON transient. However, it does not apply to the turn-OFF transient, which is only affected by the DIBL effect ($V_{\mathrm{TH}}{}^{\mathrm{DOWN}}$ is not affected by $V_{\mathrm{GS}}{}^{\mathrm{OFF}}$).

2) There is an error in the long-term V_{TH} for both turn-ON and turn-OFF transients.

The V_{TH} will change over time as the gate oxide degrades, which is not considered in the model.

TABLE I
ANALYTICAL PROCESS OF SWITCHING TRANSIENT

Period	Gate charge conservation equation	Charge/Flux conservation equation
Turn-ON current-rise I	$I_{G_cr} t_{ON_cr} = C_{GD}(V_{DC}-V_1)+C_{GS}\frac{I_{LOAD}}{G_{ml}}$	$\frac{1}{2}t_{ON_cr}\left(L_{LOOP}\frac{I_{LOAD}}{t_{ON_cr}}+V_{DC}-V_1\right)=L_{LOOP}I_{LOAD}$
Turn-ON voltage-fall II	$I_{G_vf}t_{ON_vf}=Q_{GD}-C_{GD}(V_{DC}-V_1)+C_{GS}\Delta V_{TH1}$	–
Turn-OFF voltage-rise III	$I_{G_vr}t_{OFF_vr}=Q_{GD}+C_{GD}L_{LOOP}\frac{I_{LOAD}-I_1}{t_{OFF_vr}}+C_{GS}\frac{I_{LOAD}-I_1}{G_{ms}}+C_{GS}\frac{C_{DS}V_{DC}}{G_{ms}t_{OFF_vr}}$	$\frac{1}{2}t_{OFF_vr}(I_{LOAD}-I_1)=Q_{OSS}$
Turn-OFF current-fall IV	$I_{G_cf}t_{OFF_cf}=C_{GS}\left(\frac{I_{LOAD}}{G_{ml}}-\frac{I_{LOAD}-I_1}{G_{ms}}\right)+C_{GD}\left(\Delta V_{DSMAX}-\frac{L_{LOOP}(I_{LOAD}-I_1)}{t_{OFF_vr}}\right)$	$\frac{1}{2}t_{OFF_cf}\left(L_{LOOP}\frac{I_{LOAD}-I_1}{t_{OFF_vr}}+\Delta V_{DSMAX}\right)=L_{LOOP}I_1$

Note: G_{ml} and G_{ms} represent large-signal transconductance and small-signal transconductance, respectively. The gate current I_G for each period can be expressed by the KVL equation of the gate drive loop.

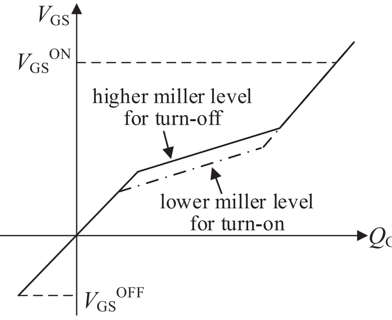

Fig. 6. Difference in turn-ON and turn-OFF Q_G curves due to V_{TH} hysteresis. [29].

B. Improved Dynamic Analytical Model

To address the above problems, the V_{TH} for turn-ON and turn-OFF processes is modeled separately in this article. The red marks in Fig. 5 visually represent the correction of the V_{TH} during long-term operation by the model proposed in this article. First, $V_{TH}{}^{UP}(0)$ and $V_{TH}{}^{DOWN}(0)$ are determined according to (2). Furthermore, (3) and (4) are introduced to describe the influence of V_{TH} instability on $V_{TH}{}^{UP}(t)$ and $V_{TH}{}^{DOWN}(t)$ during long-term operation.

For the quantity $V_{TH}{}^{HYST}(0)$ in (2), it is necessary to be decoupled from the influence of the DIBL effect on the V_{TH} ($V_{TH}{}^{DIBL}$), which is related to V_{DS}. Note that there is no V_{TH} hysteresis when $V_{GS}{}^{OFF} = 0$ V, this condition can be used to separate $V_{TH}{}^{HYST}(0)$ and $V_{TH}{}^{DIBL}$. The quantity $V_{TH}{}^{SHIFT}(t)$ in (3) is a function of the relevant parameters experienced in typical applications such as $V_{GS}{}^{ON}$, $V_{GS}{}^{OFF}$, switching frequency, stress time, and operation temperature. It is found that $V_{TH}{}^{SHIFT}(t)$ follows a power law with the number of switching cycles (N_{cycles}) under certain operating conditions, which can be expressed as [25]

$$V_{TH}{}^{SHIFT}(t) = a \cdot N_{cycles}{}^{b} \tag{10}$$

where a and b are constants. Moreover, $\Delta V_{TH}{}^{HYST}(t)$ in (4) is related to $V_{GS}{}^{OFF}$ and switching speed.

Due to the complex influencing factors, a measurement-based method is adopted in this article to obtain the related parameters for modeling V_{TH}. The method is shown in the flowchart in

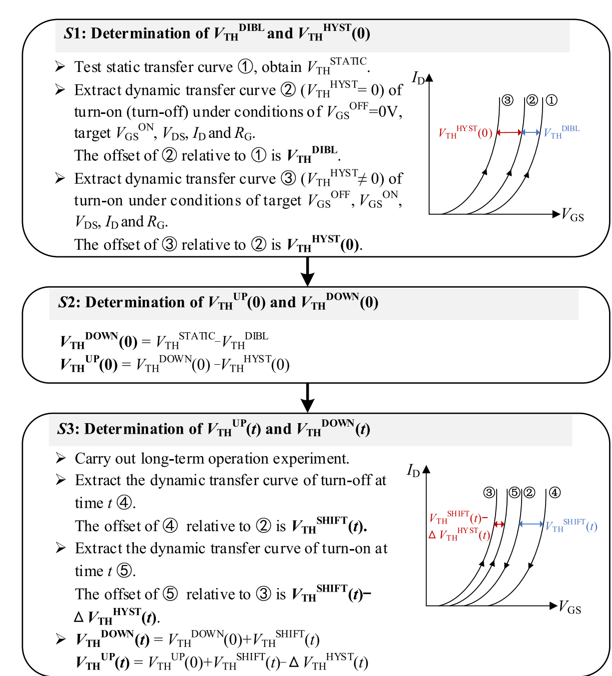

Fig. 7. Flowchart for modeling the V_{TH} during long-term operation.

Fig. 7, where $V_{TH}{}^{STATIC}$ is the V_{TH} extracted from the measured static transfer curve.

IV. EXPERIMENTAL VERIFICATION

A. Experimental Platform

In order to demonstrate the switching loss in real operation, a buck converter is built in this article, which is shown in Fig. 8. It is worth pointing out that the buck converter setup can also be operated as a double-pulse test (DPT) platform, which is controlled through the pulses from the gate driver.

The buck converter runs at continuous switching operation and constant high temperature, which is exactly the electrothermal stress condition that causes gate oxide degradation and will not introduce package degradation. The DUT is a 1200 V/31 A double trench gate SiC MOSFET (DT-MOSFET). Since the junction temperature (T_j) of the chip cannot be measured directly, the case temperature (T_c) is measured by a temperature sensor placed

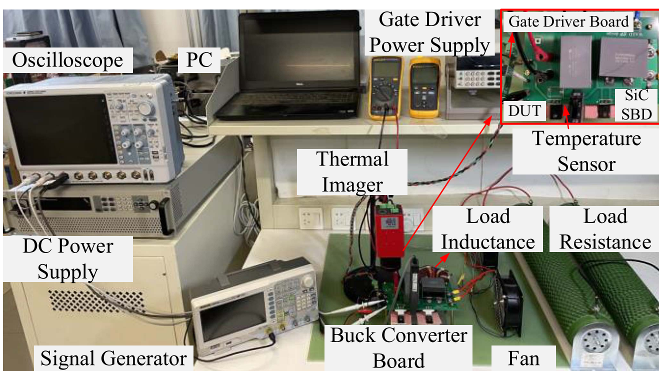

Fig. 8. Photograph of the buck converter setup.

TABLE II
SPECIFICATIONS OF THE BUCK CONVERTER EXPERIMENTS

Parameter	Test A	Test B	Test C	Test D
f	500 kHz			
D	0.3	0.3	0.3	0.7
R_G	10 Ω	10 Ω	20 Ω	10 Ω
V_{GS}	+22/-12 V	+22/-4 V	+22/-12 V	+22/-12 V
V_{DC}	220 V	200 V	210 V	135 V

under the DUT to estimate T_j by the equation

$$Z_{thjc} = \frac{T_j - T_c}{P_{pul}} \tag{11}$$

where Z_{thjc} is the junction to case thermal impedance, which is related to the pulse width and can be obtained from the datasheet of the device. P_{pul} is the average heating power per pulse. Moreover, a thermal imager is used to monitor the temperature on top of the TO package as an aid in verification.

To accelerate the degradation process, a more stressful operating point of the converter is selected. The gate voltage is set to be $+22/-12$ V first, and the switching frequency is chosen as 500 kHz. R_G is 10 Ω, and duty cycle (D) is set as 0.3. The input dc voltage (V_{dc}) is determined by achieving $T_j = 150\,°$C. Moreover, since V_{TH} instability is related to $V_{GS}{}^{OFF}$, switching speed, bus voltage and load current, test A is used as the control group, and experiments are carried out under different $V_{GS}{}^{OFF}$ (test B), R_G (test C), and D (test D, equivalent to changing I_{LOAD} and V_{dc}) to verify the universality of the proposed analytical model under different operating conditions. The specifications of the four groups of buck experiments are summarized in Table II. The four DUTs in the experiments are the same device from the same manufacturer and the same batch.

During the operation of buck converter, the variation in V_{TH} caused by gate oxide degradation will affect switching loss of the DUT, thereby affecting T_j. T_j in turn affects V_{TH} and other temperature-dependent parameters, which changes switching loss again. Therefore, it is difficult to decouple the influence of V_{TH} degradation and T_j on device switching behavior in buck converter due to electrothermal bidirectional coupling in operation. Moreover, limited by T_j, the voltage and current level of the buck converter are low. Therefore, in order to investigate the impact of V_{TH} instability on switching loss and effectively reflect the switching loss under the real operating level, a

600 V/20 A DPT at room temperature is performed when the buck converter setup is interrupted every 24 h. Moreover, the static V_{TH} is monitored as a reference.

TABLE III
TYPE NUMBERS AND SPECIFICATIONS OF THE EQUIPMENT

Equipment	Type Numbers	Specification	Delay
Oscilloscope	YOKOGAWA DLM5058	500 MHz 2.5 GS/s	-
Voltage probe	YOKOGAWA 701939	500 MHz 600 V	-
Current probe	HIOKO CT3276	100 MHz 30 A	7 ns

TABLE IV
INITIAL V_{TH} OF THE BUCK CONVERTER EXPERIMENTS

Parameter	Test A	Test B	Test C	Test D
$V_{TH}{}^{HYST}(0)$	3.5 V	1.3 V	1.0 V	3.4 V
$V_{TH}{}^{UP}(0)$	0.4 V	1.8 V	1.9 V	0.3 V
$V_{TH}{}^{DOWN}(0)$	3.9 V	3.1 V	2.9 V	3.7 V

Since the accurate acquisition of switching loss depends on the parameters of the test equipment, a high bandwidth test system is established to ensure accuracy and the detailed specifications are shown in Table III. It should be noted that probe propagation delay has significant impact on loss measurement [30] and it is calibrated in this article through the Deskew correction signal source [31].

B. Parameter Extraction of V_{TH} Instability

1) In the Initial State: As presented in *S*1 and *S*2 in the flowchart in Fig. 7, the V_{TH} for turn-ON and turn-OFF processes in the initial state is extracted and shown in Table IV. It can be seen from Table IV that the DUTs in tests A and D have almost the same $V_{TH}{}^{HYST}(0)$, which indicates that the devices of the same batch in this article have almost the same interface state density, supporting the fact that the device process is under control. Moreover, it is obvious that the $V_{TH}{}^{HYST}(0)$ of the DUTs in tests A and D is larger than that in tests B and C. This is because of the lower $V_{GS}{}^{OFF}$ and R_G of tests A and D [32].

2) During the Operation of the Buck Converter: Taking the control group A as an example, Fig. 9 presents the switching waveforms of the device in DPT during long-term operation.

It can be seen from Fig. 9 that there is a variation in the switching waveforms of the device during long-term operation, resulting in a change in the switching loss. For the turn-ON process, after 24 h operation of the buck converter, the rise time of i_D is delayed, and the value of di/dt is decreased. Moreover, V_{GP} increases and consequently, the fall time of v_{DS} is delayed. This is directly caused by the increase of $V_{TH}{}^{UP}$(24 h). With the increase of the operation time, the turn-ON waveform at 48 h basically overlaps with that at 24 h, while it shows the opposite change at 72 h, which indicates that $V_{TH}{}^{UP}$(72 h) decreases. However, the V_{GP} for the turn-OFF process increases, and both the time when i_D starts to fall and v_{DS} starts to rise are advanced

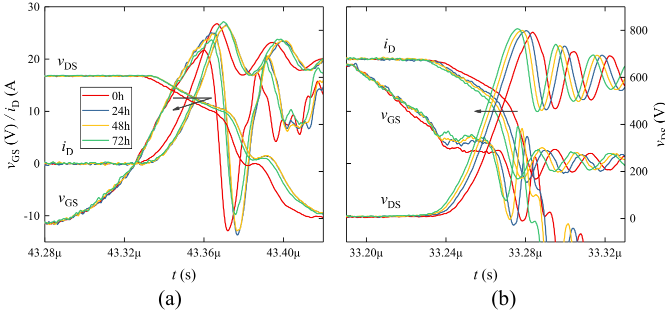

Fig. 9. Switching waveforms of test A during buck operation. (a) Turn-ON. (b) Turn-OFF.

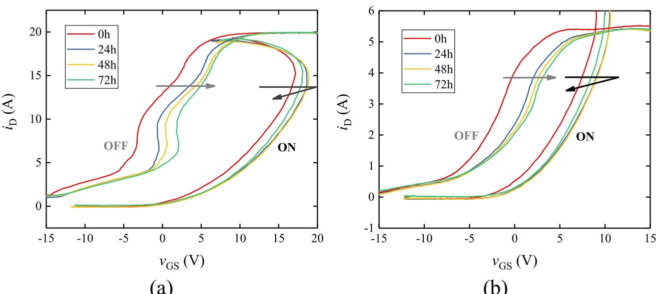

Fig. 10. Dynamic transfer characteristics of test A. (a) DPT. (b) Buck.

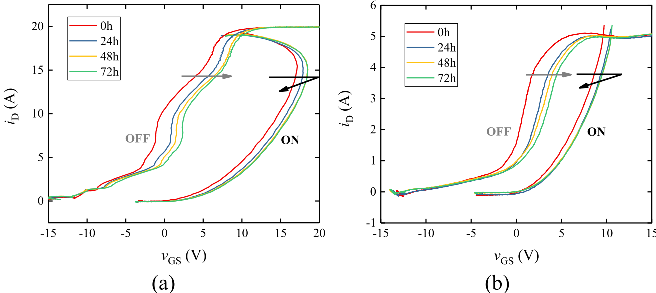

Fig. 11. Dynamic transfer characteristics of test B. (a) DPT. (b) Buck.

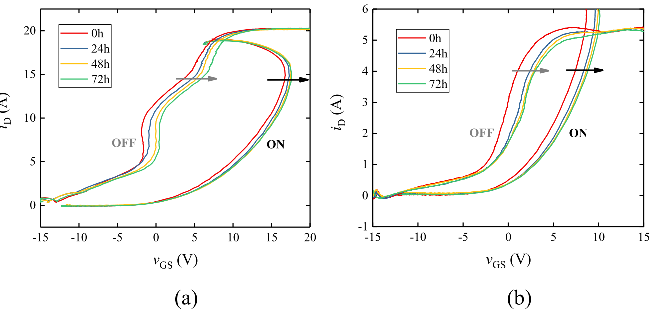

Fig. 12. Dynamic transfer characteristics of test C. (a) DPT. (b) Buck.

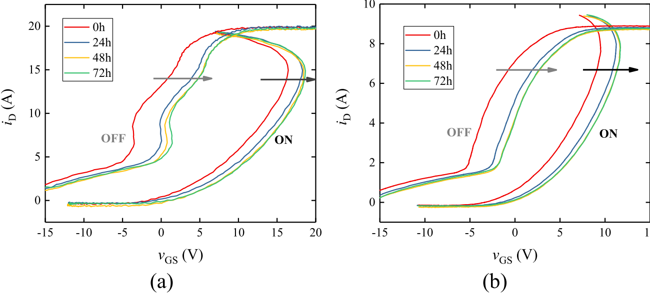

Fig. 13. Dynamic transfer characteristics of test D. (a) DPT. (b) Buck.

with the increase of the operation time. This demonstrates that $V_{TH}^{DOWN}(t)$ has been increasing.

As illustrated in $S3$ of the flowchart in Fig. 7, $V_{TH}^{UP}(t)$ and $V_{TH}^{DOWN}(t)$ are qualified by the dynamic transfer curve method [32]. Fig. 10 presents the dynamic transfer characteristics of the DUT in test A. The results of DPT and buck are shown together for verification. Due to the large current range of the dynamic transfer curves and the difference in turn-ON and turn-OFF processes, the behavior of the turn-ON and turn-OFF transfer curves shown in Fig. 10 is different from the typical static subthreshold transfer characteristics shown in Fig. 1. It should be noted that there is remaining current when v_{GS} reaches V_{TH} and far below 0 for the turn OFF curves in the dynamic transfer characteristics, which is the charging current of the parasitic output capacitance C_{GD} and C_{DS}. Moreover, the shape of the dynamic hysteresis curves is closely related to the circuit parameters due to their influence on switching characteristics [32]. However, it can be seen from Fig. 10 that the V_{GP} of turn-ON process is located to the left of that of turn-OFF process, which indicates that V_{TH}^{UP} is lower than V_{TH}^{DOWN}. Moreover, the shift in the saturation regions of the turn-ON and turn-OFF transfer curves with operation represents the degradation in V_{TH}^{UP} and V_{TH}^{DOWN}, respectively.

As shown in Fig. 10, there is the same variation trend in turn-ON (turn-OFF) transfer curves of buck and DPT with aging, which reflects the consistency of the V_{TH} instability at high temperature and room temperature. Moreover, the turn-OFF transfer curves all shift to the right. The turn-ON transfer curve first shifts to the right and then shifts to the left at 72 h. The behavior of the dynamic transfer curve is consistent with the switching characteristics shown in Fig. 9, indicating that $V_{TH}^{DOWN}(t)$ increases all the time, while $V_{TH}^{UP}(t)$ first increases and then decreases, i.e., $V_{TH}^{SHIFT}(72\ \text{h}) < \Delta V_{TH}^{HYST}(72\ \text{h})$ under the condition of test A.

Figs. 11–13 demonstrate the dynamic transfer curves of the DUTs in tests B, C and D, respectively. It can be obtained that the turn-OFF transfer curve always shifts to the right with the increase of the operation time in different conditions, indicating a positive $V_{TH}^{SHIFT}(t)$ from (3). However, the performance of the turn-ON transfer curve varies under different operating conditions. The dynamic transfer curve of the turn-ON process in test B has a similar trend to that in test A, while it always shifts to the right in tests C and D. This implies that the relative value of $V_{TH}^{SHIFT}(t)$ and $\Delta V_{TH}^{HYST}(t)$ in (4) depends on the operating conditions.

According to Figs. 10(a)–13(a), the V_{TH} instability parameters of DPT are extracted from the variation of v_{GS} at a certain current in the saturation regions of the turn-ON and turn-OFF transfer curves with operation. The results are shown in Fig. 14, where $\Delta V_{TH}^{STATIC}(t)$, $\Delta V_{TH}^{UP}(t)$, and $\Delta V_{TH}^{DOWN}(t)$,

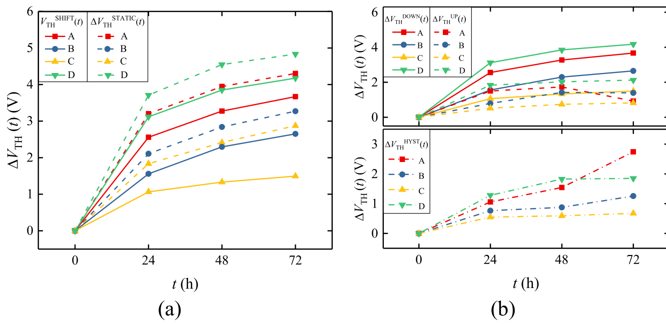

Fig. 14. V_{TH} instability in long-term operation. (a) $V_{TH}{}^{SHIFT}(t)$. (b) $\Delta V_{TH}{}^{HYST}(t)$.

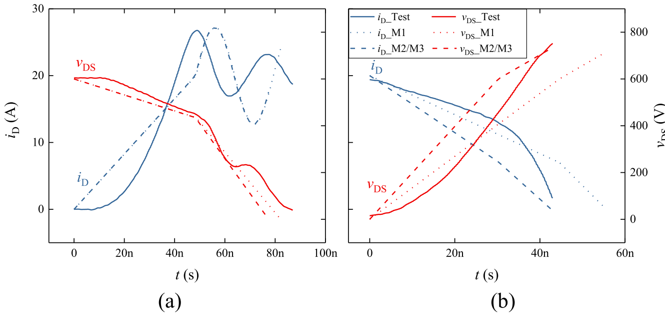

Fig. 16. Comparison results of initial switching waveforms for test A. (a) Turn-ON. (b) Turn-OFF.

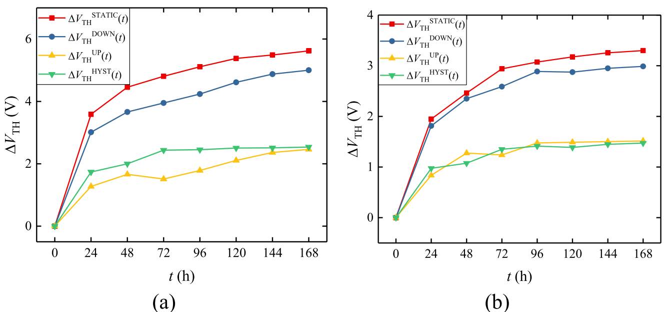

Fig. 15. V_{TH} instability with longer operation time. (a) Test A. (b) Test B.

respectively, represent the variation of $V_{TH}{}^{STATIC}$, $V_{TH}{}^{UP}$, and $V_{TH}{}^{DOWN}$ at time *t* relative to the initial state.

It can be seen from Fig. 14(a) that the $V_{TH}{}^{SHIFT}(t)$ characterized by the turn-OFF process of DPT and the static results have the same increasing trend with operation, but the value of the dynamic turn-OFF process is lower. It is, therefore, concluded that $V_{TH}{}^{SHIFT}(t)$ represents a real degradation, due to a permanent charge effect. Obviously, $V_{TH}{}^{SHIFT}(t)$_A $>$ $V_{TH}{}^{SHIFT}(t)$_B$>$ $V_{TH}{}^{SHIFT}(t)$_C, verifying that $V_{TH}{}^{SHIFT}(t)$ increases with lower $V_{GS}{}^{OFF}$ and R_G. Moreover, $V_{TH}{}^{SHIFT}(t)$_D $>$ $V_{TH}{}^{SHIFT}(t)$_A. This phenomenon is due to the influence of different dc voltage and load current on gate oxide degradation from the related research we are conducting. Fig. 14(b) shows that $\Delta V_{TH}{}^{HYST}(t)$ increases significantly at 72 h in both tests A and B, especially in A, which can explain that $V_{TH}{}^{UP}(t)$ first increases and then decreases. This indicates that $\Delta V_{TH}{}^{HYST}(t)$ increases dramatically with $V_{TH}{}^{SHIFT}(t)$ at low $V_{GS}{}^{OFF}$ and high switching speed.

Since $V_{TH}{}^{UP}$ of tests A and B first increases and then decreases within 72 h, in order to further investigate its behavior under longer-term stress, buck experiments with longer operation time (168 h) are conducted. Fig. 15 presents the V_{TH} parameters extracted from the experimental results. It can be obtained from Fig. 15 that under conditions A and B, the V_{TH} hysteresis is almost stable after 72 h, and both $V_{TH}{}^{UP}(t)$ and $V_{TH}{}^{DOWN}(t)$ continue to have small shifts and gradually saturate. This phenomenon demonstrates that there is saturation in both V_{TH} shift and V_{TH} hysteresis for the double trench gate DUT tested in this article. The permanent V_{TH} shift reaches saturation after reaching a certain number of switching cycles. Moreover, as the effective gate voltage [$V_{GS}{}^{OFF}$- $V_{TH}{}^{UP}(t)$] caused by the positive permanent V_{TH} shift reaches a certain value, the donor traps are all filled and the V_{TH} hysteresis is saturated.

C. Model Verification

1) Switching Waveform: Taking test A as an example, Fig. 16 shows the comparison results of switching waveforms in the initial state between the experiment and three analytical models, which are the existing analytical model in [13] (M1), the model only accounts initial V_{TH} hysteresis (M2), and the model proposed in this article that comprehensively considers V_{TH} instability (M3). $V_{TH} = 4.2$ V and $\Delta V_{TH1} = 3.7$ V in M1 for the DUT in this article. The parameters involved in M2 are the same as those in Table IV, i.e., the initial state of M3. Moreover, since the long-term operation has not been carried out, there is no permanent V_{TH} shift, the results of M2 and M3 are the same, and they are shown as one curve in Fig. 16.

It can be seen from Fig. 16(a) that during the turn-ON process, the waveforms of M1 and M3(M2) are consistent for the current-rise period, while M1 has a longer voltage-fall period and a lower slew rate of d*v*/d*t*. This is because the ΔV_{TH1} used in the voltage-fall period of M1 should be the change in V_{GP} for the Miller ramp phase caused by the DIBL effect $V_{TH}{}^{DIBL}$, while the actual extracted ΔV_{TH1} is the joint effect of DIBL and interface states. Since the adopted ΔV_{TH1} is higher than $V_{TH}{}^{DIBL}$, resulting in a longer voltage-fall period. For the turn-OFF process shown in Fig. 16(b), the duration of voltage-rise period and current-fall period of M1 is longer than that of M3(M2), which is due to the same V_{TH} used for turn-ON and turn-OFF processes in M1 without considering V_{TH} hysteresis, i.e., there is a lower turn-OFF V_{TH} in M1.

Furthermore, Fig. 17 presents the switching waveforms during long-term operation for the experiment and M3. Since M1 and M2 do not account for the effect of continuous operation on the switching process, their results do not vary with time and are always the same as the initial state shown in Fig. 16.

As shown in Fig. 17, the analyzed switching waveforms of M3 present a trend consistent with the experimental results as the operation time increases. This indicates that the proposed analytical model can effectively track the change of switching characteristics during long-term operation.

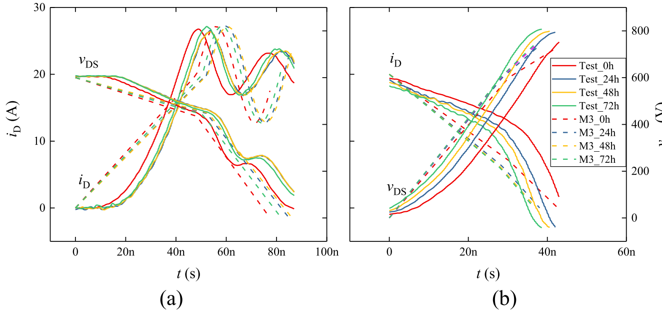

Fig. 17. Comparison results of long-term switching waveforms for test A. (a) Turn-ON. (b) Turn-OFF.

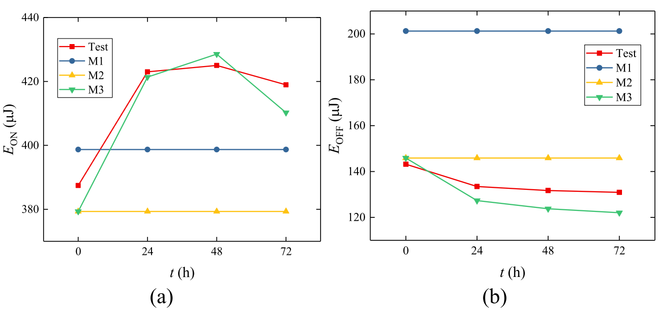

Fig. 18. Comparison results of switching loss for test A. (a) E_{ON}. (b) E_{OFF}.

However, it is obvious from Figs. 16 and 17 that the switching waveforms obtained from the analytical model do not exactly agree with the experimental results. There are two main causes. On the one hand, approximation and linearization are adopted to improve the intuitiveness of the analytical model, which will inevitably sacrifice accuracy. On the other hand, for M3, there is an error in the V_{TH} extracted from the dynamic transfer curve during long-term operation. Therefore, it is necessary to quantify the switching loss to further evaluate the accuracy of the proposed model.

2) Switching Loss: Fig. 18 gives the comparison results of switching losses for test A between M1, M2, M3, and the experiment. It can be found that M1 has the largest error, especially for E_{OFF}, and M2 has a more accurate initial state compared with M1 since it introduces different $V_{TH}{}^{DOWN}(0)$ and $V_{TH}{}^{UP}(0)$ from the dynamic test. Nonetheless, M2 remains problematic for predicting switching loss in real operation. On the contrary, the proposed M3 can track the variation of the long-term switching loss since it considers V_{TH} instability. This is consistent with the analysis of the switching waveforms in Figs. 16 and 17.

Furthermore, Fig. 19 presents the results of experiment and M3 for tests B, C, and D, and the relative errors of the switching losses in M3 and experiment under different operating conditions are listed in Table V. It is found that the proposed model can effectively evaluate the switching loss within 7% error under different operating conditions ($V_{GS}{}^{OFF}$, R_G, V_{dc}, and I_{LOAD}). This result indicates that although there are some differences between the switching waveforms of the proposed analytical model and the experimental results, the relative error of the

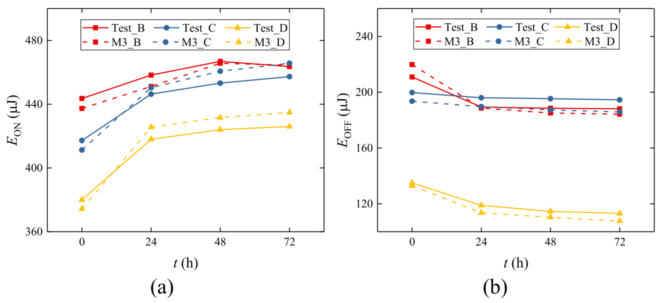

Fig. 19. Switching loss of the proposed model and experiments for tests B, C, and D. (a) E_{ON}. (b) E_{OFF}.

TABLE V
ERROR ANALYSIS FOR THE PROPOSED MODEL

Test		Error (%)			
		0 h	24 h	48 h	72 h
A	E_{ON}	-2.10	-0.39	0.84	-2.08
	E_{OFF}	1.89	-4.62	-6.04	-6.79
B	E_{ON}	-1.40	-1.56	-0.25	0.19
	E_{OFF}	4.22	-0.40	-1.80	-2.08
C	E_{ON}	-1.42	0.91	1.64	1.84
	E_{OFF}	-3.09	-3.24	-4.13	-4.46
D	E_{ON}	-1.5	1.81	1.79	2.08
	E_{OFF}	-1.54	-4.48	-3.73	-4.88

TABLE VI
SPECIFICATIONS OF DUTS AND TEST CONDITIONS

Parameter	AT-MOSFET	VD-MOSFET
Specification	1200 V/36 A	1200 V/32 A
$V_{TH}{}^{HYST}(0)$	3.0 V	0.3 V
$V_{TH}{}^{UP}(0)$	0.9 V	2.8 V
$V_{TH}{}^{DOWN}(0)$	3.9 V	3.1 V
V_{DC} (buck)	260 V	265 V

switching loss calculation is acceptable. Moreover, the proposed model can effectively reflect the change of the switching loss during continuous operation, which further verifies the validity of the proposed analytical model.

V. DISCUSSION

A. Universality of the Model for Devices With Different Structures

In order to verify the universality of the proposed model for SiC MOSFETs with different gate structures, long-term buck experiments under condition A of Section IV are also carried out on the other two devices, which have asymmetric trench gate structure (AT-MOSFET) and planar gate structure (VD-MOSFET), respectively. The input dc voltage V_{dc} in each set of experiments is determined by achieving $T_j = 150\,°C$. Similarly, a 600 V/20 A DPT is carried out and the switching loss is calculated when the buck converter is interrupted. The specifications of the DUTs and the conditions for buck converter experiments are shown in Table VI. Observing the initial state of V_{TH} under condition A of the three devices in Tables IV and VI, it can be found that the $V_{TH}{}^{HYST}(0)$ of AT-MOSFET and DT-MOSFET is much larger

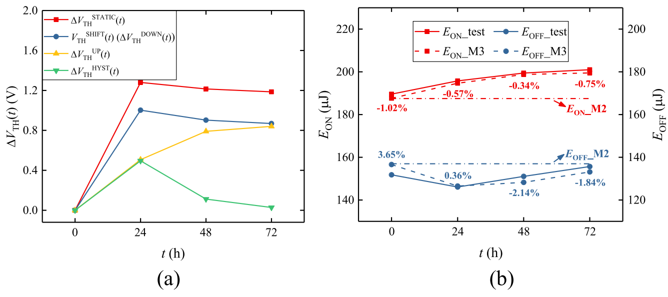

Fig. 20. V_{TH} instability parameters and switching losses of AT-MOSFET. (a) V_{TH} instability parameters. (b) Switching losses.

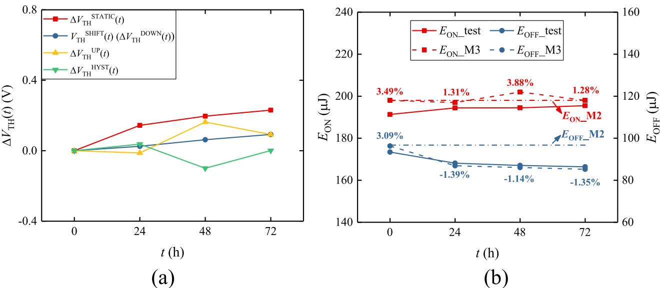

Fig. 21. V_{TH} instability parameters and switching losses of VD-MOSFET. (a) V_{TH} instability parameters. (b) Switching losses.

than that of VD-MOSFET. This phenomenon is due to the fact that the D_{it} of trench gate devices is higher than that of planar gate devices [24].

Figs. 20 and 21 present the results of long-term operation experiments of AT-MOSFET and VD-MOSFET, respectively, including the variation in V_{TH}, as well as the comparison results of switching losses in the experiment and calculated by the proposed analytical model M3.

As can be seen from Figs. 20(a) and 21(a) that the V_{TH} instability parameters of AT-MOSFET and DT- MOSFET have different behaviors compared to that of VD-MOSFET shown in Fig. 14. For AT-MOSFET, the $V_{TH}^{SHIFT}(t)$ first increases within 24 h, then decreases and gradually saturates. Therefore, the effective gate voltage value (V_{GS}^{OFF}- $V_{TH}^{UP}(t)$) applied during the V_{TH} hysteresis measurement first decreases and then increases, and consequently, $\Delta V_{TH}^{HYST}(t)$ has similar performance to $V_{TH}^{SHIFT}(t)$. While the $V_{TH}^{SHIFT}(t)$ of VD-MOSFET have a consistent increasing behavior with DT-MOSFET but a smaller amplitude, which results in a smaller $\Delta V_{TH}^{HYST}(t)$. Therefore, both $V_{TH}^{SHIFT}(t)$ and $\Delta V_{TH}^{HYST}(t)$ are almost negligible in long-term operation. It should be noted that the different behavior in V_{TH} instability of the three devices is related to the different gate structure and the fabrication process of the device manufacture [24].

Moreover, Fig. 20(b) indicates that for AT-MOSFET, the variation in switching loss evaluated by the proposed analytical model is consistent with experiment, and the prediction error is within 4%. For the VD-MOSFET presented in Fig. 21(b), the E_{OFF} of both experiment and M3 decreases monotonically and the prediction error is within 4%. However, the predication advantage of M3 is not reflected for E_{ON} since there is almost no degradation.

The predicted result lines for E_{ON} and E_{OFF} of M2, which only accounts initial V_{TH} hysteresis, are also marked in Figs. 20(b) and 21(b). It is worth pointing out that depending on the degradation behavior of switching loss during device long-term operation, the result of M2 may be closer to the experiment at certain times, such as E_{OFF} (72 h) for AT-MOSFET. However, the M3 proposed in this article is essentially different from M2. M3 is a time-varying model that takes aging into account, while M2 is independent of time.

Therefore, the proposed analytical model is universally applicable to devices with different structures. This model can effectively characterize the switching losses evolution during long-term operation for different degradation behaviors of different devices. Furthermore, this model can be used to predict the long-term switching losses of devices with different processes and voltage levels. Especially for devices with severe gate oxide degradation, the prediction error using the proposed model will be much lower than that of the traditional model.

B. Prediction Application of the Model in Operation

It is worth pointing out that, compared with the traditional "static" model, only "dynamic" V_{TH} is introduced in the proposed "dynamic" analytical model for predicting switching loss during long-term operation. This is due to the intuitive analysis of the switching loss model adopted in this article. The impact of a certain parameter on the switching loss can be obtained from the analytical expression directly. In addition, the integral processing of the equations describing the switching behavior in this analytical model is also very important, which allows the nonlinear characteristics of the capacitance to be included in the charge parameters. Therefore, the proposed analytical model is versatile and convenient from instantaneous prediction to realizing long-term prediction. However, the V_{TH} instability is related to the manufacturing process, gate structure, and operating condition of the device. The degradation mechanism of the permanent V_{TH} shift and the V_{TH} hysteresis are complex. At present, there is no quantitative expression that characterizes the degradation, which can only be statistically and extrapolated through experiments.

In order to realize the prediction application of the proposed model in actual operation, a longer-time of 168 h buck experiment under relatively gentle conditions of $f = 250$ kHz, $V_{GS} = +22/-12$ V, $R_G = 10\ \Omega$, $D = 0.3$, $V_{dc} = 270$ V ($T_j = 150\,^{\circ}$C) is carried out on a DT-MOSFET. The V_{TH} parameters are shown in Fig. 22(a).

It can be obtained from Fig. 22(a) that $\Delta V_{TH}^{HYST}(t)$ increases in the first 24 h and remains almost unchanged thereafter under this condition. Therefore, $V_{TH}^{UP}(t)$ is jointly affected by $V_{TH}^{SHIFT}(t)$ and $\Delta V_{TH}^{HYST}(t)$ within 24 h, and then it is only affected by $V_{TH}^{SHIFT}(t)$ and has consistent variation with $V_{TH}^{DOWN}(t)$. It is found that $V_{TH}^{SHIFT}(t)$ basically follows a power law with N_{cycles}, as shown in (10), for the tested trench gate devices and operating condition, therefore, $V_{TH}^{DOWN}(t)$ can be modeled as (10). Moreover, since $\Delta V_{TH}^{HYST}(t)$ is caused by the permanent $V_{TH}^{SHIFT}(t)$, and its change is relatively regular under this condition, $V_{TH}^{UP}(t)$ can also be modeled

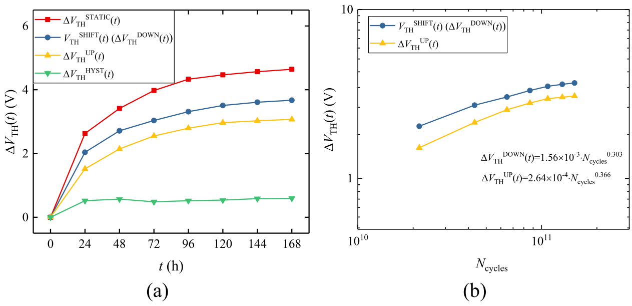

Fig. 22. V_{TH} instability parameters and modeling results. (a) V_{TH} instability parameters. (b) Modeling results.

TABLE VII
PREDICTION RESULTS OF THE PROPOSED MODEL

time	E_{ON}			E_{OFF}		
	test(μJ)	M3(μJ)	Err(%)	test(μJ)	M3(μJ)	Err(%)
0 h	341.01	332.56	-2.48	152.57	162.61	6.58
24 h	349.88	352.63	0.79	140.75	141.01	0.18
48 h	353.30	354.68	0.39	132.77	132.60	-0.13
72 h	357.30	359.92	0.73	127.23	129.76	1.99
96 h	360.34	362.54	0.61	123.31	126.24	2.38
120 h	362.87	365.86	0.82	120.67	125.01	3.60
144 h	364.55	368.14	0.98	118.51	125.16	5.61
168 h	365.50	372.20	1.83	117.68	125.41	6.57

approximately as (10). The modeling results of $V_{TH}{}^{UP}(t)$ and $V_{TH}{}^{DOWN}(t)$ are shown in Fig. 22(b). Furthermore, the V_{TH} variation during long-term operation can be obtained through modeling inversion, and then brought into the proposed model. The predicted switching losses are given in Table VII.

As can be found, the prediction error of the switching loss is also lower than 7% with V_{TH} obtained through experimental statistics, modeling, and inversion, which verifies the effectiveness of this model. Furthermore, this model can be applied to predict the dynamic switching losses of devices with the same process under the same operating conditions. It is, therefore, concluded that the accuracy of the proposed model depends on the accurate characterization of V_{TH} instability during long-term operation. For any device, it is first necessary to investigate the degradation mechanism of permanent V_{TH} shift and V_{TH} hysteresis under any operating condition, and second, an appropriate quantification of V_{TH} degradation should be given. In summary, the proposed model provides theoretical support for the dynamic prediction of switching losses during long-term operation, which is critical for evaluating and optimizing converter design.

VI. CONCLUSION

A dynamic analytical switching loss model considering V_{TH} instability is proposed in this article. The effects of permanent V_{TH} shift and recoverable V_{TH} hysteresis on the turn-ON and turn-OFF processes are revealed. Moreover, the deficiency of the existing analytical model is analyzed, and an improved model that can predict switching loss during continuous operation is presented. Furthermore, the model is validated through a buck converter under different operating conditions and on devices with different structures. The main conclusions are outlined as follows.

1) The V_{TH} instability caused by gate oxide degradation during long-term operation has different effects on switching loss during device turn-ON and turn-OFF. The variation in V_{TH} of the turn-OFF process $V_{TH}{}^{DOWN}$(t) is only affected by $V_{TH}{}^{SHIFT}$(t), and it increases with degradation, and consequently, E_{OFF} decreases. However, the change in V_{TH} of the turn-ON process $V_{TH}{}^{UP}$(t) depends on the values of $V_{TH}{}^{SHIFT}$(t) and $\Delta V_{TH}{}^{HYST}$(t), which have opposite effects. E_{ON} increases with the increase of $V_{TH}{}^{UP}$(t), and vice versa.
2) The "dynamic" analytical model considering V_{TH} instability is critical for predicting the switching loss during long-term operation. The existing analytical model is a "static" model suffering from evaluating switching loss during continuous operation, while the proposed model addresses this issue. $V_{TH}{}^{UP}(0)$ and $V_{TH}{}^{DOWN}(0)$ are corrected in the proposed model by decoupling the V_{TH} hysteresis and the DIBL effects. Moreover, the effect of $V_{TH}{}^{SHIFT}$(t) and $\Delta V_{TH}{}^{HYST}$(t) on $V_{TH}{}^{UP}$(t) and $V_{TH}{}^{DOWN}$(t) is considered.
3) The proposed analytical model can effectively track the change of switching loss during long-term operation under different operating conditions. The switching waveforms and switching losses of three analytical models and buck converter experiment are compared under different $V_{GS}{}^{OFF}$, R_G, V_{dc}, and I_{LOAD}. The comparison results show that the proposed analytical model can effectively predict the switching loss within 7% error under different long-term operating conditions.
4) The proposed analytical model is universally applicable to devices with different structures. For different degradation behaviors of devices with different gate structures, the proposed model can effectively characterize the evolution of switching losses. Moreover, accurate characterization of V_{TH} instability is of vital importance for the predication application of the model.

The proposed dynamic analytical switching loss model in this article lays a theoretical foundation for evaluating the switching loss and optimizing the converter design during continuous operation. The further improvement of model accuracy depends on more accurate quantification of V_{TH} instability.

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