DC Series Arc Fault Detection Method With Resonant Filter Design for PV Systems

Hwa-Pyeong Park, *Member, IEEE*, Seung-Jin Chang, *Member, IEEE*, Jae-Young Park, *Member, IEEE*, Mina Kim, *Member, IEEE*, Wan Kim, and Suyong Chae, *Senior Member, IEEE*

***Abstract*—Photovoltaic (PV) power generation has become widespread owing to the global need to achieve carbon neutrality. With the increase in the number of PV systems, a broken connector in the PV panel induces a dc series arc fault condition. Therefore, arc fault detection technology becomes significant to guarantee the safety and reliability of PV systems. However, the series arc fault condition is similar to that of the normal operation with a small current variation, which makes it difficult to classify the normal and arc fault conditions. In this article, the resonant filter is proposed to improve the dc series arc fault detection capability. The characteristics of arc fault current are analyzed with the considerations of PV and converter impedance. The operational principle and design methodology of the proposed resonant filter are analyzed to clarify the arc fault signal through decoupling with the converter impedance. In addition, the algorithm for arc fault detection is designed with the proposed resonant filter. The experiment setups are designed with a dc optimizer and two commercial inverters, which can verify the arc fault detection performance with the proposed resonant filter.**

***Index Terms*—Analog filter, arc fault, dc–ac inverter, dc–dc converter, fault diagnosis, photovoltaic (PV) systems.**

I. Introduction

THE power generation based on renewable energies, such as photovoltaic (PV) and wind turbines, is continuously increasing owing to the global need for carbon neutrality [1]. With an increase in the number of PV systems, reliability and safety are significant in preventing electrical and mechanical accidents. PV systems inevitably have the dc link voltage, which makes the possibility of a dc series arc fault condition, as shown in Fig. 1. Loose connectors, damaged cables, and cracked solder joints can induce the dc series arc fault condition. The series arc fault condition can occur in micro, string, and central inverters and junction boxes of PV arrays. In terms of industry, the Underwriters Laboratory (UL) introduced the UL 1699B standard for PV systems [2]. In addition, the National Electrical Codes (NEC) require arc fault detection devices (AFDDs) for dc systems over 80 V [3]. Therefore, arc fault detection with high precision is necessary to guarantee the safety of PV systems.

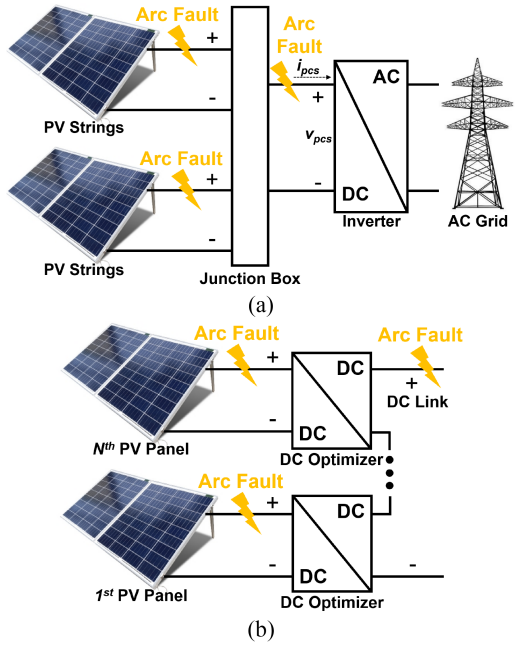

Fig. 1. Example of PV systems with dc series arc fault condition. (a) Array junction box with grid-connected inverter. (b) PV panels with DC optimizer.

Various dc series arc fault detection algorithms have been introduced for PV systems. DC arc faults can occur in both series and parallel fault conditions. A parallel arc fault is the same as a short circuit condition, which can be easily detected by a large change in current [4], [5]. However, a series arc fault has only a small current variation because it operates as a small series resistance in a power line or connector. Therefore, a series arc fault is more challenging than a parallel arc fault. DC series AFDDs require high precision and fast detection speeds because the energy losses in the arc fault are converted into heat energy. In [6], [7], [8], [9], and [10], a dc series arc fault detection method based on a time domain analysis was evaluated using voltage and current information. These

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Hwa-Pyeong Park and Wan Kim are with the School of Electronic Engineering, Kumoh National Institute of Technology, Gumi 39177, South Korea (e-mail: hppark@kumoh.ac.kr; a103203@kumoh.ac.kr).

Seung-Jin Chang and Mina Kim are with the Department of Electrical Engineering, Hanbat National University, Daejeon 34158, South Korea (e-mail: jpromo8@hanbat.ac.kr; minakim@hanbat.ac.kr).

Jae-Young Park is with the Energy ICT Research Department, Korea Institute of Energy Research, Daejeon 34129, South Korea (e-mail: jypark91@kier.re.kr).

Suyong Chae is with the Department of Electrical Engineering, Pohang University of Science and Technology, Pohang 37673, South Korea (e-mail: sychae@postech.ac.kr).

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methods have a simple implementation comprising the use of the characteristics according to the series arc fault conditions. However, it is difficult to distinguish the arc fault condition and normal operation with small magnitude variation. In addition, a number of sensors are required to improve the fault detection precision compared with normal conditions [6]. In [11], [12], and [13], a frequency domain analysis was used with the measured PV current to determine the arc fault characteristics. It considers the chaotic variation of arc impedance, which can distinguish between normal and fault conditions. However, the ac magnitude variation depends on the impedance design of the converter and inverter, which determines the precision of arc fault detection. In [14], [15], [16], [17], and [18], hybrid arc fault detection methods employing time and frequency domain analyses were introduced to improve the detection precision. It increases the available parameters with multidomain analysis, which can increase the series arc fault characteristics to classify the arc and normal conditions. In [14] and [15], statistical analyses in the time and frequency domains can distinguish the normal and arc fault conditions. However, it passively measures the PV current from the designed power systems, which is difficult to achieve consistent fault detection performance. In [19], [20], [21], [22], [23], and [24], arc fault detection methods using artificial intelligence are developed using normal and fault data. It can achieve high fault detection precision with several arc faults and normal characteristics according to machine learning (ML) and neural network (NN) models. AFDDs use a microprocessor to achieve cost-effectiveness, which makes it difficult to implement the online ML and NN. Therefore, a predefined model is normally applied to the microprocessor. It reduces the precision of arc fault detection since the arc fault characteristics are different according to the structure of the PV systems, PV inverters and converters, and line length. In [25], a dc series arc fault detection method was introduced with the modulation algorithm of a power converter. It is an active method for detecting fault conditions. However, it cannot be applied to existing PV systems. In [26], the passive component design was analyzed to detect the arc fault condition. It can maximize the arc fault characteristics to improve the fault detection capability. Those previous fault detection methods were focused on the signal and power processing technique to find the arc characteristics. In terms of signal processing, the previous methods passively measured the PV current to determine the dc series arc fault condition, which has different fault characteristics depending on the PV systems, such as the converter and inverter.

Since the series arc fault condition operates as a chaotic impedance variation, the large impedance of the inverter and converter reduces the magnitude of the frequency spectrum under the arc fault conditions. Therefore, the series arc fault detection in PV systems is tightly coupled with the power stage design of the grid-connected inverter and dc optimizer. This article analyzes the performance limitation of arc fault detection with the considerations of PV panel and converter impedance. In addition, a resonant filter is proposed to distinguish the dc series arc fault signal, which can be decoupled between the impedance of the PV systems and the fault detection capability. The operational principle and design methodology of the proposed resonant filter are analyzed to clarify the arc fault signal, which considers the minimization of grid and switching noises, and switching harmonics. Also, an arc fault detection algorithm is designed based on the voltage and current relationship of the resonant filter. The experimental results using the prototype dc optimizer can verify the performance of the dc series arc fault detection using the proposed resonant filter. In addition, the arc fault detection is verified with two commercial PV inverters.

II. Proposed Arc Fault Detection Method

The chaotic impedance variation of the arc fault condition can induce a change in the ac current magnitude in the frequency domain [14]. The arc impedance is analyzed with the arc voltage and current relationship using a voltage source, arc fault generator, and a load resistor. Fig. 2(a) shows the experimental results considering only the arc fault impedance. It verifies the chaotic impedance variation, which induces the wide frequency spectrum. Therefore, the load impedance is significant in the PV systems, which makes different arc fault characteristics. The conventional AFDD measures the PV current to calculate the fast Fourier transform (FFT). It compares the ac current magnitude variation for the arc fault detection. Fig. 2(b) and (c) shows the experimental results using two different commercial inverters under normal and arc fault conditions, which use the same PV panels and grid conditions. Fig. 2(b) shows the distinguished FFT magnitude variation between the normal and arc faults using Inverter 1 (DASSTECH, DSP-3325KSHK). However, using Inverter 2 (EKOS, EK-31), it is difficult to classify the arc fault condition with a very small magnitude change in the frequency domain, as shown in Fig. 2(c). Therefore, the conventional AFDDs have limited fault detection performance, because they passively measure the ac current from predesigned PV panels and converters. In this article, the effectiveness of the impedance of PV systems is analyzed for the arc fault detection capability. In addition, the proposed resonant filter is designed to obtain the desired ac current magnitude through impedance matching.

A. Analysis of Impedance for Fault Detection

With consideration of arc impedance variation, the ac current magnitude can be derived as follows:

$$i_{ac}(\omega) = v/z(\omega) \tag{1}$$

where $i_{ac}(\omega)$ is ac current according to impedance variation, v is the PV voltage, and $z(\omega)$ is the sum of the line impedance and input impedance of the converter. When the arc fault occurs, the chaotic arc impedance is added between the PV panel and converter. The impedance variation according to the arc fault increases the ac magnitude for a wide frequency bandwidth. Also, the current magnitude is determined with the PV and line impedances and the input impedance of the converter. Fig. 3(a) shows the equivalent dynamic model of the PV panel [27], where $I_{\rm ph}$ represents the electrons excited current by the solar irradiance, C_D ($V_{\rm pv}$, ω) and C_T ($V_{\rm pv}$) is the capacitance for diffusion and transition, R_d ($V_{\rm pv}$) and $R_{\rm sh}$ are the dynamic resistance of diode and shunt resistance, and R_s and L_s are series resistance and inductance. From the PV model, the dynamic PV

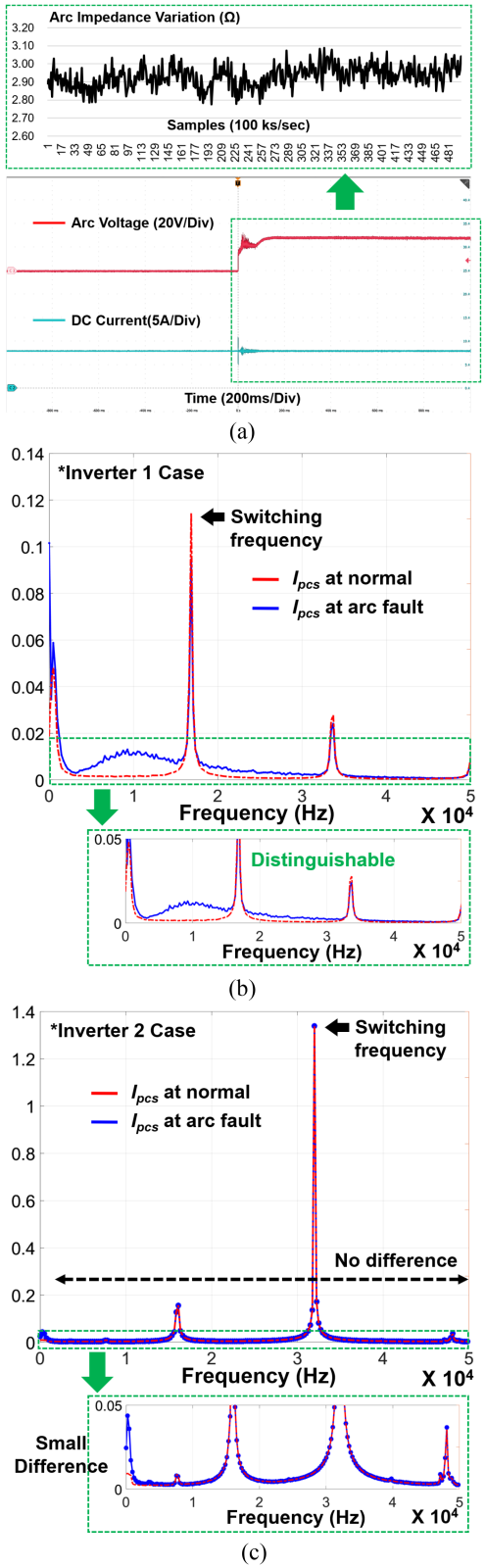

Fig. 2. Characteristics of arc fault condition. (a) Arc impedance analysis. (b) Current value using Inverter 1. (c) Current value using Inverter 2.

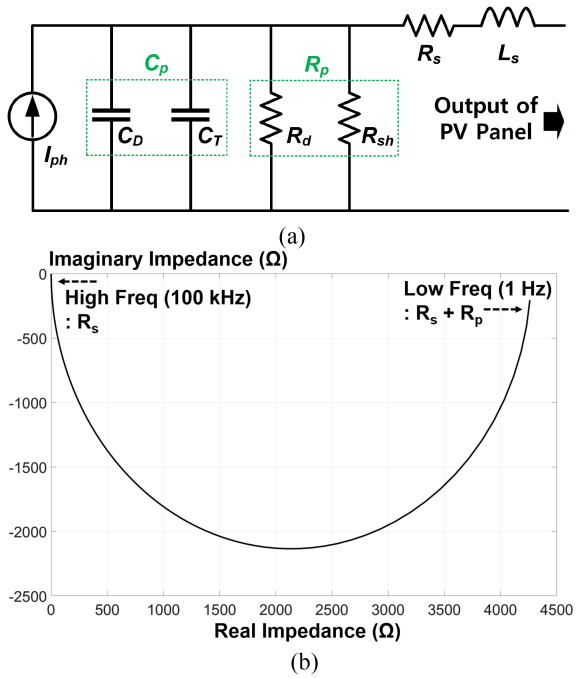

Fig. 3. Equivalent circuit models. (a) PV dynamic impedance model. (b) Impedance according to frequencies.

impedance can be derived as follows:

$$Z_{\text{pv}}(s) = R_s + sL_s + \frac{R_p}{1 + sC_pR_p}. \tag{2}$$

The impedance values are determined using the bias PV voltage and ac frequencies. From (2), the sum of R_s and R_p is dominant at the low frequency. In addition, L_s and R_s are dominant at a high frequency. Fig. 3(b) shows the impedance values according to the operating frequency.

The converters, such as dc optimizer, microinverter, and grid-connected inverter, have the input impedance, which can be derived as follows:

$$z_c(s) = v_i(s)/i_i(s) \tag{3}$$

where $v_i(s)$ and $i_i(s)$ are the input voltage and current of the power converter, respectively. This article employs the buck converter for the dc optimizer, which is used to analyze the input impedance. Fig. 4(a) shows the topology structure of the buck converter. The closed-loop input impedance includes the open-loop input impedance and loop gain, which can be derived as follows:

$$Z_{c,\text{cl}}(s) = \frac{Z_{c,\text{ol}}(1 + T_{\text{loop}})V_i}{V_i - DI_LT_{\text{loop}}Z_{c,\text{ol}}} \tag{4}$$

where T_{loop} is the loop gain, D is the duty ratio, $Z_{c,\text{ol}}$ is the input impedance of the open loop, V_i is the input voltage, and I_L is the inductor current. The open-loop input impedance can be derived with considerations of power stage design, duty ratio, and load

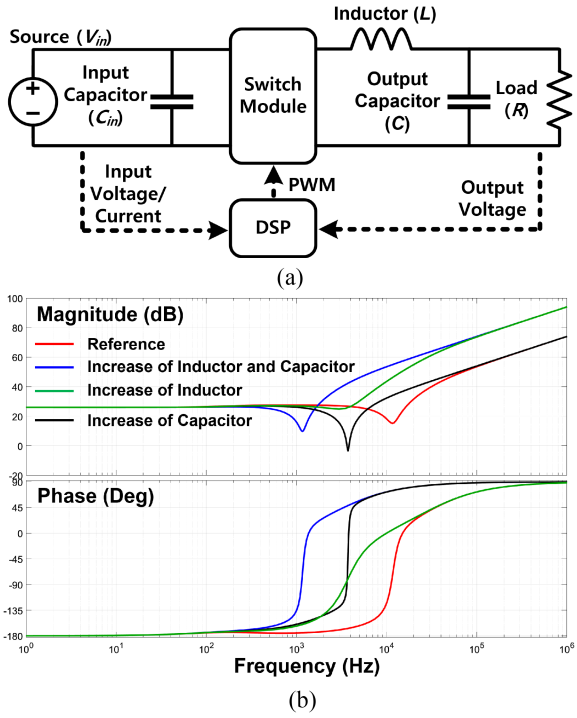

Fig. 4. Equivalent circuit model. (a) Buck converter structure. (b) Input impedance.

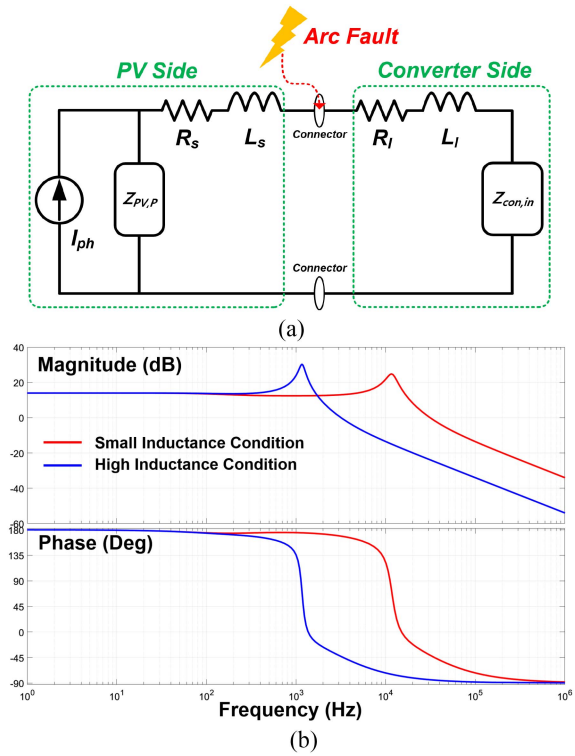

Fig. 5. Impedance between PV panel and converter. (a) Impedance structure. (b) Input current magnitude according to frequency.

resistance as follows:

$$Z_{c,\mathrm{ol}}(s) = \frac{R}{D^2} \cdot \frac{LCs^2 + \frac{L}{R}s + 1}{1 + RCs} \tag{5}$$

where R is the load resistance, L is the inductance, and C is the output capacitance. The loop gain can be derived with the transfer function of duty to the output voltage and feedback compensator as follows:

$$T_{\mathrm{loop}}(s) = \frac{K_p s + K_i}{s} \cdot \frac{V_i}{LCs^2 + \frac{L}{R}s + 1} \cdot \frac{\left(1 + \frac{Z_f}{Z_n}\right)}{\left(1 + \frac{Z_f}{Z_D}\right)} \tag{6}$$

where $H(s)$ is the feedback compensator, $G_{ud}(s)$ is the transfer function of duty to output voltage, K_p is the proportional gain, K_i is the integral gain, Z_f is the input capacitor impedance of the converter, and Z_n and Z_D are input impedance at zero output voltage and zero duty ratio, respectively. From (4)–(6), the input impedance of the power converter can be obtained according to the operating frequencies. Fig. 4(b) shows the input impedance magnitude of the buck converter according to frequencies. It has negative resistance characteristics in the low-frequency range. Also, the input impedance increases with the L–C filter design. The increase of inductance value can achieve a high input impedance as the increase of operating frequency.

The impedance structure between the PV panel and converter is described in Fig. 5(a), where $Z_{\mathrm{PV,P}}$ is the parallel impedance of the PV panel and $Z_{\mathrm{con,in}}$ is the input impedance of the converter. When the arc fault occurs in the connector, the arc impedance is added to the power line. The high input impedance of the converter induces the small ac current magnitude and vice versa. Fig. 5(b) shows the theoretical current magnitude according to frequencies. High line and buck inductances increase the input impedance. Therefore, the fault detection accuracy of conventional AFDDs is limited and different from passive current sensing and predesigned impedance.

B. Effectiveness of Switching Noise

The power converters have a switching operation for the power conversion, which induces the switching noise in the power line. The large noise magnitude cannot distinguish the fault and normal conditions, as shown in Fig. 2(a) and (b). The dc optimizers and inverters have over several kHz switching frequencies. Therefore, the frequency selection for the arc fault detection should avoid the switching frequency and its harmonics.

C. Proposed Resonant Filter

The high impedance between the PV panel and converter has a small current magnitude change at the arc fault condition. Therefore, the small impedance design can increase the arc signal magnitude at the fault condition. This article proposes the resonant filter for the dc series arc fault detection, which is shown in Fig. 6(a). The resonant filter is configured with R–L–C components, which is located within or close to the power converter. The impedance of the resonant filter can be derived as follows:

$$Z_a = 1/j\omega C_a + j\omega L_a + R_a, f_r = 1/\left(2\pi\sqrt{L_a C_a}\right) \tag{7}$$

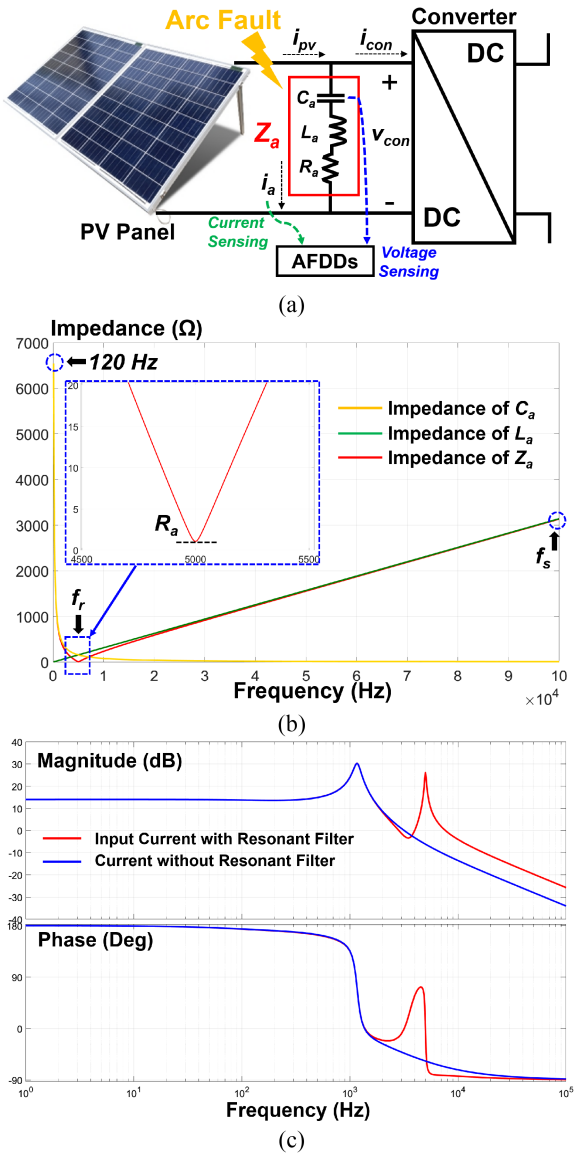

Fig. 6. Proposed resonant filter for arc fault detection. (a) Proposed arc fault detection structure. (b) Theoretical impedance analysis. (c) AC current magnitude with resonant filter according to frequency.

where L_a, C_a, and R_a are the passive components of the resonant module, Z_a is the impedance of the resonant module, and f_r is the resonant frequency. Z_a has impedance variation according to the frequency, as shown in Fig. 6(b). The minimum Z_a at f_r can increase the fault signal magnitude variation compared with the normal condition. Also, it can block the dc current with C_a. The current through Z_a can be derived as follows:

$$i_a(\omega) = v_z(\omega)/Z_a \tag{8}$$

where $v_z(\omega)$ is Z_a voltage according to frequencies, which can be described with power source and arc fault voltages ($v_z = v_{\text{in}} - v_{\text{arc}}(\omega)$). From (8), the dc series arc fault signal amplifying ratio (AR) can be derived as follows:

$$\text{AR} = i_{a,\text{arc}}(f_r)/i_{a,\text{nor}}(f_r) \tag{9}$$

where $i_{a,\text{arc}}$ and $i_{a,\text{nor}}$ are the resonant filter currents according to arc fault and normal conditions, respectively. Therefore, the designed Z_a value of the proposed resonant filter can increase the fault signal to distinguish the normal condition. It can be decoupled with the converter impedance, which is used for general-purpose AFDDs.

Fig. 6(b) shows the impedance of Z_a at the grid, resonant, and minimum switching frequencies, which considers the undesired periodic noises. The periodic noises of f_g have sinusoidal waveforms, which are dominant at the first harmonics. In addition, the periodic noises of f_{sw} have rectangular waveforms, which contain odd-order harmonics. Therefore, the resonant frequency of Z_a can be selected between f_g and f_{sw} to minimize the periodic noises, which can be derived as follows:

$$f_g < f_r < f_{\text{sw}}. \tag{10}$$

The power loss in Z_a is determined by the impedance at f_g and f_{sw}, which can be derived as follows:

$$P_{Ra} = i_a(\omega)^2 R_a. \tag{11}$$

Therefore, Z_a is higher than the desired minimum impedance at f_g and f_{sw}, which can be derived as follows:

$$Z_a(f_g),\ Z_a(f_{\text{sw}}) \geq Z_{\min} \tag{12}$$

where $Z_{\min}$ is the minimum impedance value, which is selected for the desired power loss at Z_a. $i_a(f_g)$ and $i_a(f_{\text{sw}})$ are designed with R_a and estimated ΔV_g and ΔV_{sw}. The desired $Z_{\min}$ can be derived as follows:

$$Z_{\min} = \sqrt{\frac{\Delta V^2 R_a}{P_{\text{loss}}}}. \tag{13}$$

The designed $Z_{\min}$ increases with an increase of estimated ΔV to obtain the desired power loss in Z_a and vice versa. In this article, the grid and minimum switching frequencies are designed as 60 Hz and 10 kHz, which induces the resonant frequency selection below 10 kHz. When the power loss in Z_a is below 100 μW at f_g and f_{sw}, the desired $i_a(f_g)$ and $i_a(f_{sw})$ are less than 10 mA with R_a of 1 Ω. In addition, the maximum ΔV_g and ΔV_{sw} are assumed as 2 V. Therefore, Z_a is over 200 Ω at f_g and f_{sw} and the designed 5 kHz resonant frequency should satisfy $Z_{\min}$ at f_g and f_{sw}, as shown in (12).

When f_r is designed with considerations of f_g and f_{sw}, L_a and C_a are designed to satisfy the desired minimum impedance ($Z_{\min}$) at f_g and f_{sw} to minimize the periodic noise and power loss in Z_a. The C_a value can be derived as follows:

$$C_a \leq \frac{1-(\omega_g/\omega_r)^2}{j\omega_g Z_{\min}},\ C_a \leq \frac{1-(\omega_{sw}/\omega_r)^2}{j\omega_{sw} Z_{\min}} \tag{14}$$

where ω_g, ω_{sw}, and ω_r are grid, switching, and resonant angular frequencies, respectively. From (14) and resonant frequency, L_a can be derived as follows:

$$L_a = \frac{1}{(2\pi f_r)^2 C_a}. \tag{15}$$

R_a is designed to obtain the fault signal amplifying. The small resistance is proper to measure the high fault current magnitude. However, parasitic resistance is inevitable at L_a and C_a, which determines R_a value in a practical manner.

TABLE I
DESIGN EXAMPLE OF RESONANT MODULE

Parameter	Value	
Resonant frequency	5 kHz	
L_a	4.7 mH, 0.538 Ω at f_r	
R_a	1.08 Ω at f_r	
C_a	0.2 μF, 0.47 Ω at f_r	
AR	9.3 at Inverter 1	11.7 at Inverter 2
Power loss	89 μW at f_r	27 μW at f_r

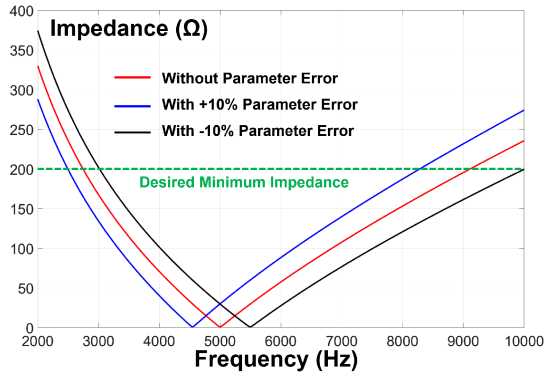

Fig. 7. Impedance sensitivity according to design margin.

This article has a 5 kHz resonant frequency, which is three times lower than the switching frequency of the inverter, i.e., 16 kHz and 32 kHz, respectively. Also, it is 83 times higher than the grid frequency, i.e., 120 Hz. The designed L_a has 4.7 mH with 0.538 Ω ac resistance at f_r. C_a is determined with f_r and L_a, which has 0.47 Ω ac resistance at f_r. R_a is the sum of ac resistance of L_a and C_a. Table I shows the designed specification of the resonant filter. From the designed resonant filter, Inverter 1 and Inverter 2 have 9.3 and 11.7 AR values from measured $v_z(\omega)$, respectively. The theoretical power loss on R_a is 87 μW and 27 μW at the resonant frequency, respectively.

The resonant filter is configured with an inductor and capacitor, which has parameter margins, such as 1%, 5%, and 10%. The worst condition is the 10% margin for L_a and C_a, which changes the resonant frequency and impedance at f_g and $f_{\rm sw}$. The change of resonant frequency is not effective in detecting the arc fault condition. However, in terms of power loss in Z_a, the impedance variation at grid and switching frequencies can increase the power loss. Fig. 7 shows the impedance with a 10% margin in L_a and C_a. Therefore, the design of L_a and C_a considers the parameter margin to obtain the desired loss in Z_a.

The advantage of the proposed method is the decoupling between the power conversion and series arc fault detection capability. When the fault signal can be measured with current sensors, digital active filters, such as bandpass and low-pass filters, can be applied to minimize the undesired noise. It is normally used as the preprocessing algorithm for the fault detection algorithm. However, it cannot amplify the fault signal in terms of the power level. The small fault signal in the power line

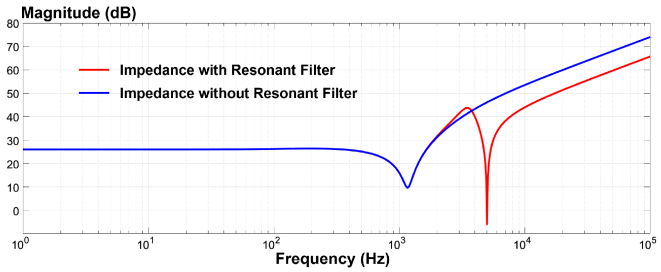

Fig. 8. Input impedance of boost converter with the proposed resonant filter.

according to the high impedance condition induces the small fault magnitude in the signal level, which makes it difficult to detect the fault condition. Therefore, the passive-type resonant filter is proposed to amplify the fault signal in the power level. In addition, it can be proper to already installed converter and inverter.

For the dc optimizer with a boost converter, the input impedance of the boost converter can be derived as follows:

$$Z_{\rm in}(s) = \frac{v_i(s)}{i_i(s)} \cong -(1-D)^2 R_o \left(1 - \frac{sL_b}{(1-D)^2 R_o}\right) \quad (16)$$

where D is the duty cycle, R_o is the load resistance, and L_b is the boost inductance. From (16), the boost inductor becomes dominant as the increase of operating frequency. Fig. 8 shows the input impedances with and without a resonant filter. The resonant filter can achieve arc fault signal amplifying with the differential type of converters.

D. Arc Fault Detection Algorithm

The proper resonant filter design can effectively amplify the magnitude of the arc fault signal compared with normal operation. Fig. 9(a) shows the proposed arc fault detection flowchart. The DSP calculates the discrete fourier transform (DFT) with measured i_a, which can be derived as follows:

$$I_a[u] = \frac{1}{N}\left|\sum_{n=0}^{N-1} i_a[n]\, e^{-\frac{2\pi u n}{N}}\right| \quad (17)$$

where N is the number of sampled data points for Fourier analysis. In this experiment, N is 512 and the sampling frequency is 250 kHz. The moving average (μ_{Ia}) and standard deviation (σ_{Ia}) are calculated to determine the threshold value for arc fault detection, which can be derived as follows:

$$I_{\rm th}[u] = \mu_{Ia}[u] + \alpha \cdot \sigma_{Ia}[u] \quad (18)$$

where α is the controllable value. When the calculated DFT magnitude is higher than the threshold value, the arc fault is detected in frequency domain analysis.

After the frequency analysis, the voltage relationship of Z_a is also considered to determine the arc fault condition in time domain analysis. The C_a voltage is the same as the source voltage in the normal condition. However, the C_a voltage at the arc fault condition can be described as $V_{\rm in}$–$V_{\rm arc}$. Fig. 9(b) shows the

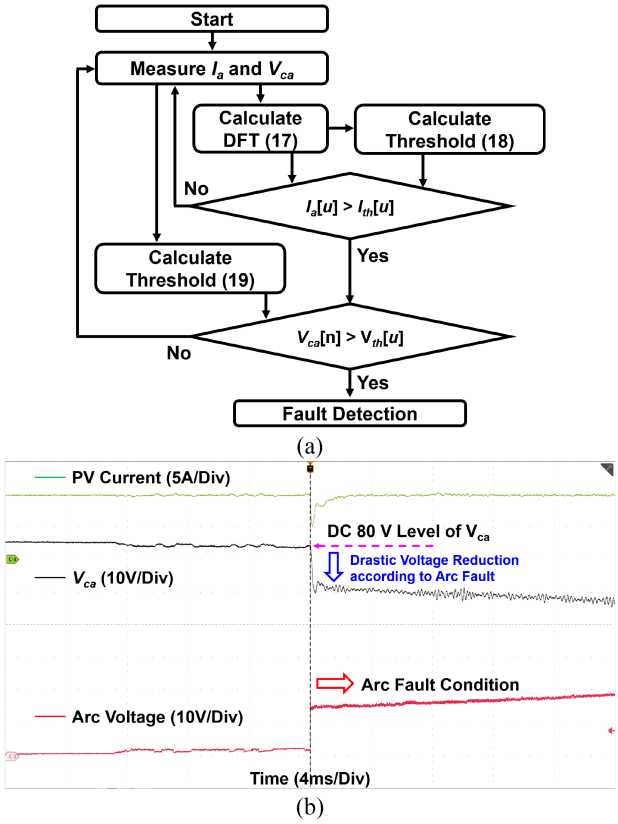

Fig. 9. Arc fault detection algorithm. (a) Fault detection flowchart. (b) DC voltage variation according to arc fault.

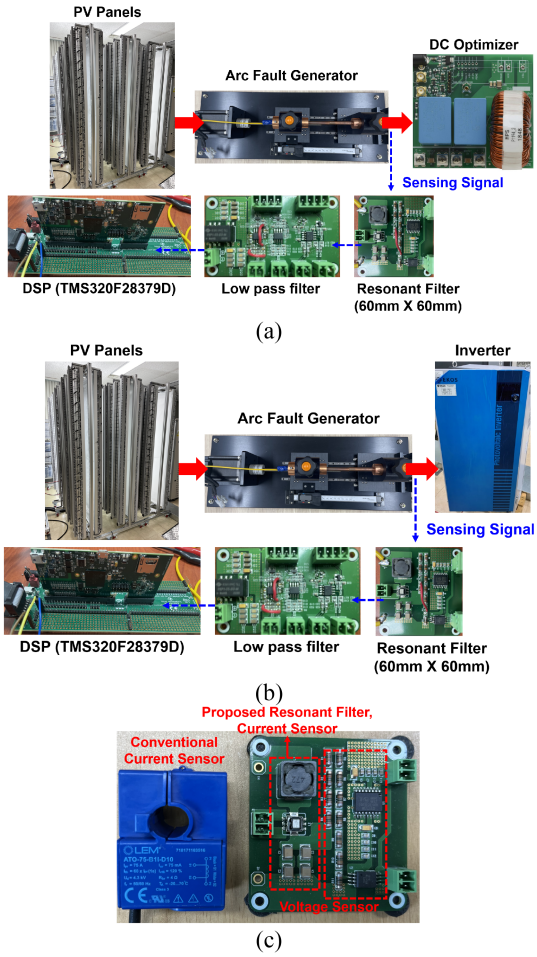

Fig. 10. Experimental setups. (a) Arc fault detection with converter. (b) Arc fault detection with commercial inverters. (c) Comparison with current sensor and resonant filter.

experimental results of V_{ca} variation at the arc fault condition. Therefore, the difference of V_{ca} can be utilized to detect the arc fault condition. The moving average and standard deviation of V_{ca} is calculated to determine the threshold value of fault detection, which can be derived as follows:

$$V_{\text{th}}[n] = \mu_{Vca}[n] + \beta \cdot \sigma_{Vca}[n] \tag{19}$$

where μ_{Vca} is the moving average value, β is the controllable value, and σ_{Vca} is the standard deviation. The measured V_{ca} is lower than the threshold value, the arc fault is detected in time domain analysis. Therefore, the proposed dc series arc fault detection method can be implemented with frequency and time domain analysis using the designed resonant filter.

The proposed resonant filter is designed to minimize the undesired periodic noises according to the grid and switching frequencies. The nonperiodic noises, such as soft-start and irradiance variation, are inevitable, which also injects the noises into the resonant filter. The large step response of voltage and current variation may induce the undesired signal amplifying. However, the dynamic response occurs within a short time, which can be classified with a fault detection algorithm. In a practical manner, the arc fault detection algorithm can check the magnitude difference for the *n*th number in terms of frequency spectrum after the drastic magnitude change in time domain analysis [15]. Therefore, the resonant filter considers the reduction of periodic noises to minimize the power loss in the resonant filter. In some cases, the resonant filter design should consider the periodic noises according to the power line communication signal.

III. Experimental Results

The performance of dc series arc fault detection is verified with the proposed resonant filter and designed fault detection algorithm. Fig. 10 shows the experimental setup for the arc fault detection with dc optimizer and commercial inverters, which includes PV modules, an arc fault generator, a proposed resonant filter, a preprocessing circuit, and DSP. The series arc fault detection methods based on signal processing normally use the current sensors, such as the current transformer and Rogowski coil. Also, the conventional methods have no power loss for an arc fault detection. However, the proposed method does not require the large size current sensors in the power line, since it requires only mA level signal sensing. The resonant filter only processes the small current, which can use L_a (SRR1208-472KL) and C_a (C1812X204KDRLCAUTO). Fig. 10(c) shows the power density comparison between the conventional current sensor

TABLE II
DESIGN EXAMPLE OF DC OPTIMIZER

Parameter	Value	
Rated power	1 kW (three PV panels)	
Input voltage range	50–150 V	
Switching frequency	150 kHz	
Switch	TPH3212PS (GaN FET)	
Controller	TMS320F28379D	
Buck inductance	1 mH (high impedance)	110 μH (small impedance)
Input and output capacitances	10 μF	

and the designed resonant filter. In terms of power density, the current sensor (ATO-75-B11-D10, LEM) and the proposed resonant filter have 48.01 cm^3 and 41 cm^3, respectively. Therefore, the resonant filter can achieve a higher density compared with current sensors. In terms of power loss, the resonant filter has the power loss in normal operation. In this article, the impedance in the grid and switching frequencies are designed to minimize the power losses below 200 μW.

A. *Arc Fault Detection With DC–DC Converter*

Fig. 11 shows the experimental results with the dc optimizer. The dc optimizer is designed for three series-connected PV panels. Table II shows the designed specification of the converter. Fig. 11(a) shows the steady state operation without the fault conditions. It includes the drain–source voltage, output voltage, and current. The FFT result is measured with the input current of dc optimizer, which is the base magnitude to compare the magnitude difference. It has a high noise signal at 21.6 kHz and 47.7 kHz from the auxiliary power supplies. Fig. 11(b) shows the arc fault condition with a small input impedance of the dc optimizer. It has a large current magnitude difference (21.6 dBm at 16 kHz) compared with normal conditions. It is proper to arc fault detection since the conventional AFDDs measure 10–100 kHz frequency ranges. Also, the input current magnitude increases for wide frequency bandwidth. Fig. 11(c) shows an arc fault condition with the large input impedance of dc optimizer. In this condition, the FFT magnitude is the same as in the normal condition. The noise signal according to auxiliary power is significant compared with the fault signal. Also, the FFT magnitude increases at a low frequency (2.1 kHz) near the resonant frequency of the *L–C* filter. It is difficult to utilize this characteristic since the peak current magnitude is different according to the converter design. Fig. 12(a) shows the normal condition with large input impedance and proposed resonant filter. The designed resonant filter has a current magnitude of 5 kHz from the switching operation. Fig. 12(b) shows the fault condition with large input impedance and proposed resonant filter. The current magnitude difference (25.6 dBm) can distinguish the arc fault condition. From Fig. 12, the proposed resonant filter can distinguish the arc fault and normal conditions.

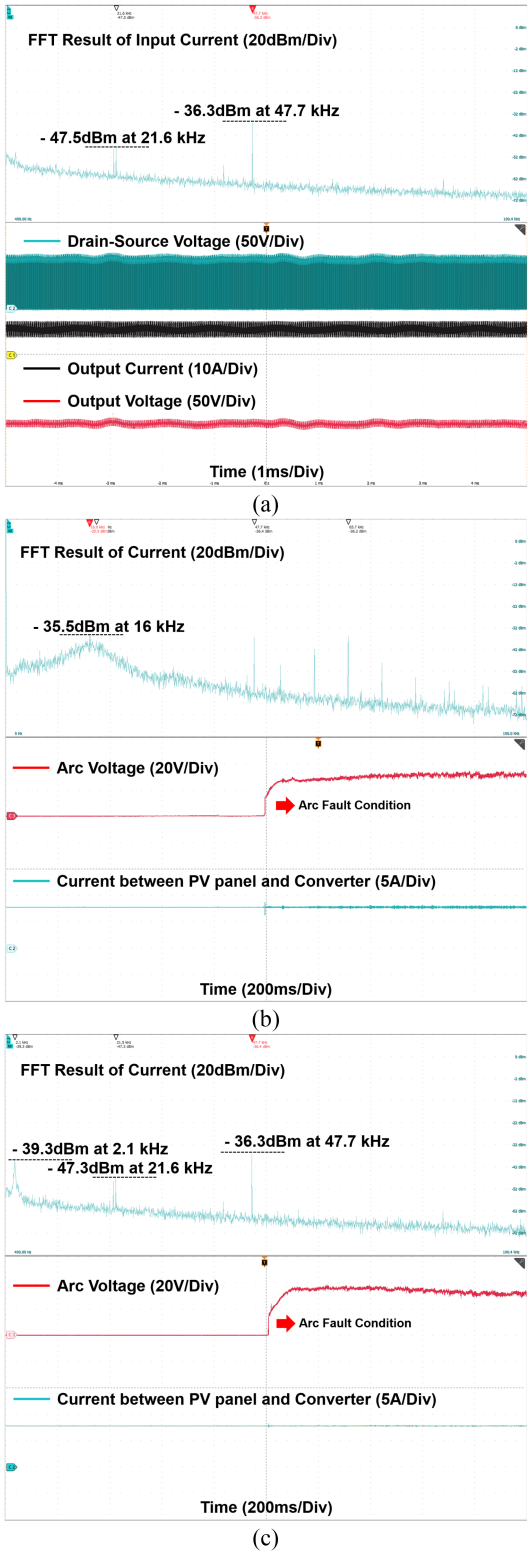

Fig. 11. Experimental verification without proposed resonant filter. (a) Normal operation of dc optimizer. (b) Arc fault and small impedance conditions with FFT magnitude. (c) Arc fault and high impedance conditions with FFT magnitude.

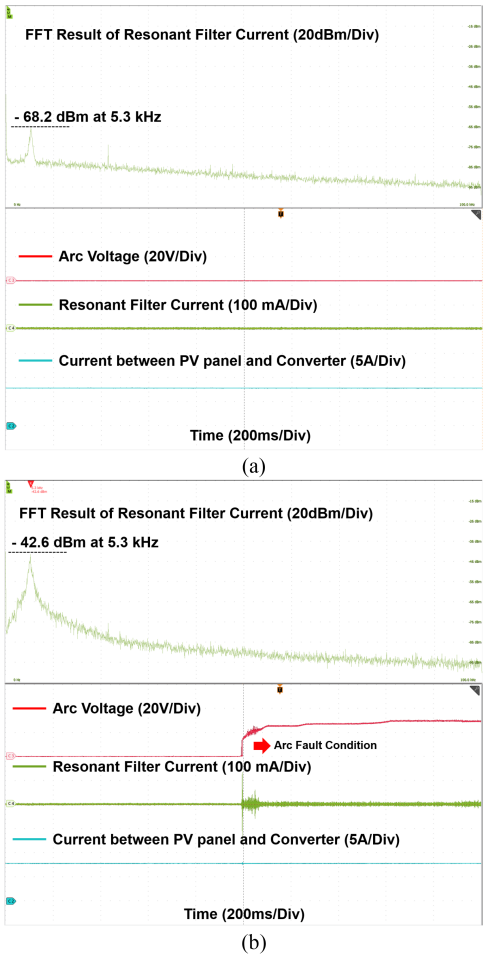

Fig. 12. Experimental verification with proposed resonant filter. (a) Normal operation with FFT magnitude. (b) Arc fault condition with FFT magnitude.

B. Arc Fault Detection With Commercial Inverters

Fig. 13(a) and (b) shows an arc fault detection of Inverter 1. Inverter 1 can distinguish the normal and arc fault conditions with PV current measuring. Fig. 2(b) shows the magnitude difference of Inverter 1 according to the normal and arc fault conditions. It has a 5.36 times magnitude difference according to an arc fault condition. With a resonant filter, the FFT magnitude difference between normal and arc fault is 9.1 times, which is a 1.6 times larger difference compared with conventional i_{pv} detection. In addition, it has 2.71 mA and 2.07 mA in grid and switching frequencies, respectively. The proposed resonant filter can achieve the series arc fault detection capability regardless of converter and inverter impedance. The conventional method using only a signal processing algorithm cannot classify the normal and fault conditions using the commercial Inverter 2. Using the resonant filter, Fig. 13(c) and (d) shows an arc fault detection performance of Inverter 2. The FFT magnitude difference between normal and arc fault is 10.3 times, which is a 5 times larger difference compared with conventional i_{pv} detection. It has 3.62 mA and 1.94 mA in grid and switching frequencies, respectively. In addition, the AFDDs with the proposed resonant filter can detect the arc fault condition within 100 ms.

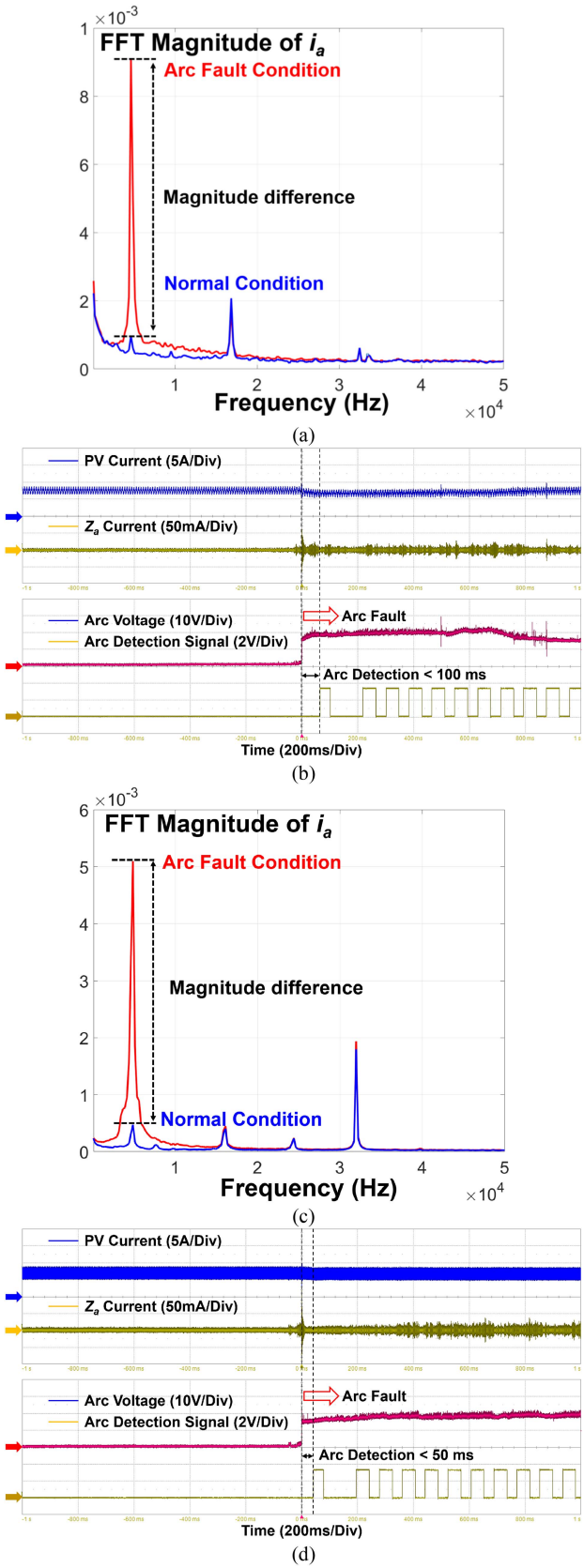

Fig. 13. Experimental verification. (a) FFT magnitude change of Inverter 1. (b) AFDD performance with Inverter 1. (c) FFT magnitude change of Inverter 2. (d) AFDD performance with Inverter 2.

IV. Conclusion

The large impedances of the inverter and converter reduce the magnitude of the frequency spectrum according to an arc fault condition. In this article, the resonant filter is proposed to clarify the arc fault condition. It can obtain a small impedance at the designed resonant frequency, which can amplify the arc fault signal. In addition, the design method of the resonant filter considers the undesired noise amplifying and power losses. The fault detection algorithm considers the signal processing technique using DFT and dc voltage variation of C_a. The experimental results using dc–dc converters and inverters verify the performance of the proposed arc fault detection method.

References

[1] A. K. Bhattacharjee, N. Kutkut, and I. Batarseh, "Review of multiport converters for solar and energy storage integration," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1431–1445, Feb. 2019.

[2] Underwriters Laboratories (UL) 1699B, "Outline of investigation for photovoltaic (PV) DC arc-fault circuit protection," *Issue 2*, Jan. 2013.

[3] National Electrical Code (NEC), NFPA70, National Fire Protection Association, Quincy, MA, 2011.

[4] C. He, L. Mu, and Y. Wang, "The detection of parallel arc fault in photovoltaic systems based on a mixed criterion," *IEEE J. Photovolt.*, vol. 7, no. 6, pp. 1717–1724, Nov. 2017.

[5] H. -L. Dang, S. Kwak, and S. Choi, "Identifying dc series and parallel arcs based on deep learning algorithms," *IEEE Access*, vol. 10, pp. 76386–76400, 2022.

[6] H.-P. Park, M. Kim, J.-H. Jung, and S. Chae, "Series dc arc fault detection method for PV systems employing differential power processing structure," *IEEE Trans. Power Electron.*, vol. 36, no. 9, pp. 9787–9795, Sep. 2021.

[7] N. L. Georgijevic, M. V. Jankovic, S. Srdic, and Z. Radakovic, "The detection of series arc fault in photovoltaic systems based on the arc current entropy," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5917–5930, Aug. 2016.

[8] X. Yao, V. Le, and I. Lee, "Unknown input observer-based series dc arc fault detection in dc microgrids," *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 4708–4718, Apr. 2022.

[9] A. Shekhar, L. Ramírez-Elizondo, S. Bandyopadhyay, L. Mackay, and P. Bauera, "Detection of series arcs using load side voltage drop for protection of low voltage dc systems," *IEEE Trans. Smart Grid*, vol. 9, no. 6, pp. 6288–6297, Nov. 2018.

[10] K. Gajula and L. Herrera, "Detection and localization of series arc faults in dc microgrids using Kalman filter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 3, pp. 2589–2596, Jun. 2021.

[11] W. Miao, Z. Wang, F. Wang, K. H. Lam, and P. W. T. Pong, "Multicharacteristics arc model and autocorrelation-algorithm based arc fault detector for dc microgrid," *IEEE Trans. Ind. Electron.*, vol. 70, no. 5, pp. 4875–4886, May 2023.

[12] H. Wang et al., "DC series arc fault detection method in photovoltaic system based on multiple frequency selections for common-mode conductive voltage," *IEEE Trans. Power Electron.*, vol. 37, no. 12, pp. 15538–15553, Dec. 2022.

[13] J.-C. Gu, D.-S. Lai, J.-M. Wang, J.-J. Huang, and M.-T. Yang, "Design of a dc series arc fault detector for photovoltaic system protection," *IEEE Trans. Ind. Appl.*, vol. 55, no. 3, pp. 2464–2471, May/Jun. 2019.

[14] H. -P. Park and S. Chae, "DC series arc fault detection algorithm for distributed energy resources using arc fault impedance modeling," *IEEE Access*, vol. 8, pp. 179039–179046, 2020.

[15] S. Chae, J. Park, and S. Oh, "Series dc arc fault detection algorithm for dc microgrids using relative magnitude comparison," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 4, pp. 1270–1278, Dec. 2016.

[16] S. Chen, X. Li, and J. Xiong, "Series arc fault identification for photovoltaic system based on time-domain and time-frequency-domain analysis," *IEEE J. Photovolt.*, vol. 7, no. 4, pp. 1105–1114, Jul. 2017.

[17] J. C. Kim, R. Ball, and B. Lehman, "Isolation and detection of arc fault noise in a real PV system using current demodulation and autocorrelation coefficients," *IEEE Trans. Power Electron.*, vol. 39, no. 8, pp. 10351–10367, Aug. 2024.

[18] S. Hwang, B. Kim, M. Kim, and H.-P. Park, "AC series arc fault detection for wind power systems based on phase lock loop with time and frequency domain analyses," *IEEE Trans. Power Electron.*, early access, doi: 10.1109/TPEL.2024.3410909.

[19] S. Lu, T. Sirojan, B. T. Phung, D. Zhang, and E. Ambikairajah, "DA-DCGAN: An effective methodology for DC series arc fault diagnosis in photovoltaic systems," *IEEE Access*, vol. 7, pp. 45831–45840, 2019.

[20] Y.-L. Shen and R.-J. Wai, "Wavelet-analysis-based singular-value-decomposition algorithm for weak arc fault detection via current amplitude normalization," *IEEE Access*, vol. 9, pp. 71535–71552, 2021.

[21] J. Yan, Q. Li, and S. Duan, "A simplified current feature extraction and deployment method for dc series arc fault detection," *IEEE Trans. Ind. Electron.*, vol. 71, no. 1, pp. 625–634, Jan. 2024.

[22] V. Le, C. Miller, B.-H. Tsao, and X. Yao, "Series arc fault identification in dc distribution based on random forest predicted probability," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 6, pp. 5636–5648, Dec. 2023.

[23] R. D. Telford, S. Galloway, B. Stephen, and I. Elders, "Diagnosis of series dc arc faults—A machine learning approach," *IEEE Trans. Ind. Inform.*, vol. 13, no. 4, pp. 1598–1609, Aug. 2017.

[24] H. Gao, K. Wang, Z. Wang, J. Cai, and Y. Lv, "Detection method of series arc fault in three-phase frequency converter load circuit under unknown working conditions," *IEEE Trans. Power Electron.*, vol. 39, no. 7, pp. 8744–8756, Jul. 2024.

[25] H.-P. Park, M. Kim, and S. Chae, "Smart dc optimizer for dc series arc fault detection and extinguishing," *IEEE Trans. Power Electron.*, vol. 37, no. 9, pp. 10117–10121, Sep. 2022.

[26] H.-P. Park, M. Kim, and S. Chae, "DC series arc fault detection and extinguishing method using input capacitor design," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2023, pp. 2446–2450.

[27] J. Johnson, D. Schoenwald, S. Kuszmaul, J. Strauch, and W. Bower, "Creating dynamic equivalent PV circuit models with impedance spectroscopy for arc fault modeling," in *Proc. IEEE 37th Photovolt. Spec. Conf.*, 2011, pp. 2328–2333.

Hwa-Pyeong Park (Member, IEEE) was born in Gimcheon, South Korea, in 1991. He received the Ph.D. degree in electrical engineering from the Ulsan National Institute of Science and Technology, Ulsan, South Korea, in 2019.

From 2019 to 2022, he was a Senior Researcher with the Korea Institute of Energy Research. He is currently with Kumoh National Institute of Technology, Gumi, South Korea. His research interests include high-power-density dc–dc converters, power control algorithms for power converters, and battery management systems.

Seung-Jin Chang (Member, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from the Department of Electrical and Electronic Engineering, Yonsei University, Seoul, South Korea, in 2010 and 2017, respectively.

In 2018, he joined the School of Electrical and Computer Engineering, Seoul National University, as a postdoctoral researcher. In 2018, he joined the Department of Electrical Engineering, Hanbat National University, Daejeon, South Korea, as an Assistant Professor, where he has been an Associate Professor since 2022. His research interests include condition monitoring based on machine/deep learning, diagnosis and prognostics of power facilities, including cables and batteries, applied signal processing techniques, and time–frequency analysis.

Jae-Young Park (Member, IEEE) received the B.S. (with highest Hons.) degree in electrical engineering from Konkuk University, Seoul, South Korea, in 2015, and the Ph.D. degree in convergence IT engineering from the Pohang University of Science and Technology, Pohang, South Korea, in 2022.

Since 2022, he has been a senior researcher with the Korea Institute of Energy Research, Daejeon, South Korea. His research interests include modeling, control, and operation of power electronic converter-based power grids.

Mina Kim (Member, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from Ulsan National Institute of Science and Technology, Ulsan, South Korea, in 2015 and 2021, respectively.

From 2021 to 2023, she was a senior researcher with the Korea Electronics Technology Institute. Since 2023, she has been an Assistant Professor of Electrical Engineering with Hanbat National University, Daejeon, South Korea. Her research interests include high-efficiency power conversion technology, control and power management algorithms, and reliability enhancement for next-generation low-voltage dc power systems and photovoltaic systems.

Wan Kim was born in Busan, South Korea, in 1999. He is currently working toward the undergraduate degree in electronic engineering from Kumoh National Institute of Technology, Gumi, South Korea.

His research interests include dc–dc converters, PV systems, arc fault detection, and quantum computing through field programmable gate array (FPGA).

Suyong Chae (Senior Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 1998 and 2000, respectively, and the Ph.D. degree in electrical engineering from the Seoul National University, Seoul, South Korea, in 2009.

From 2000 to 2010, he was a Research Engineer with Samsung SDI. From 2010 to 2022, he was a principal researcher with the Korea Institute of Energy Research. Since 2022, he has been a faculty member with the Department of Electrical Engineering, Pohang University of Science and Technology, Pohang, South Korea, where he is working as an Associate Professor. His research interests include power electronics, modeling, and control of distributed power systems.