Common-Mode EMI Noise Reduction With Improved Balance Technique for DC–AC Converters

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***Abstract*—Wide-bandgap semiconductor devices are widely used in power electronic systems for their high switching speed and frequency characteristics, which enhance power density and output fidelity, but also cause serious common-mode (CM) electromagnetic interference (EMI) issues. Balance technique is a promising method due to its significant CM noise suppression ability and high-power density. However, conventional balance techniques are typically constructed with additional inductors and front input grounding parasitic capacitors, which the high-frequency impedance of the former is affected by the equivalent parallel capacitances while the latter is sensitive to variations of front input circuits. To solve the aforementioned issues, an improved balance technique considering input parasitic inductor is proposed in this article. First, the CM EMI model and propagation paths of a dc–ac converter are analyzed. Second, a Wheatstone bridge is constructed with input parasitic inductor. Then, additional capacitors are introduced to achieve the balance condition. Furthermore, the effect of parasitic parameters of the additional CM current path on the CM reduction performance is investigated. Finally, the effectiveness of the proposed method is verified through simulation and experiments.**

***Index Terms*—Balance technique, common-mode (CM) current, electromagnetic interference (EMI) noise, parasitic parameters, wide-bandgap devices.**

I. Introduction

OVER the years, wide-bandgap (WBG) semiconductor devices have gradually replaced traditional silicon devices. The lower power loss characteristics of WBG devices allow for operation at higher switching frequencies compared to Si counterparts [1], [2], [3], [4]. High switching frequency is beneficial for filter design and can enhance power density, which is an important trend in the advancement of power electronics. However, high switching speed and high switching frequency also cause more serious electromagnetic interference (EMI) emission. At the same switching frequency, silicon carbide (SiC) MOSFETs can achieve higher switching speed than Si insulated gate bipolar transistor (IGBTs), which leads to 20 dB higher conducted EMI [5]. In the case of gallium nitride (GaN) high electron mobility transistors (HEMTs), faster switching speed and higher switching frequency can cause conductive EMI 30 dB higher than Si IGBTs [6]. These more severe EMI noise may cause abnormal operations and even system breakdown, such as motor bearing damage [7], [8] and photovoltaic (PV) leakage current [9], [10]. Therefore, how to eliminate the EMI noise caused by WBG semiconductor devices has gradually received widespread attention.

To solve the problem of EMI noise in power converters, various methods have been proposed. Adjusting the propagation path is an effective method to suppress EMI noise, which can be divided into two categories: 1) modifying the path impedance [11], [12], [13], [14], [15], [16] [17], [18], [19], [20], [21], [22] and 2) constructing a balanced propagation path [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34].

The method of modifying the propagation path impedance can be further classified into passive EMI filter (PEF) and active EMI filter (AEF). PEFs are one of the most wildly used solutions to suppress the EMI noise in power converters [11]. The design method of PEFs suppressing EMI noise at the converter input-side have been brought up and discussed thoroughly in [11], [12], and [13]. Meanwhile, the PEFs suppressing EMI noise at the converter output-side have been established to optimize the EMI behavior in [14], [15], and [16]. However, the common-mode (CM) current at the converter input-side and output-side is coupled in a dc–ac converter due to the existence of parasitic parameters. This means suppressing CM EMI noise at one side may worsen the CM EMI noise at the other side [17]. To suppress the EMI noise at the converter input-side and output-side at the same time, there are some researches featuring combination of PEFs at both sides [17], [18]. Although these PEFs can achieve decent CM reduction, the volume of filter inductors is large and could account for more than 30% of the entire system volume [21]. A modified LCL (MLCL) filter is applied in [19] for PV inverters to suppress the CM leakage current. The MLCL filter hardly increases the system volume, but a potential risk of resonance is introduced in the CM noise propagation path and a well-designed resonance suppression method is needed. As a matter of fact, PEFs can only suppress CM EMI noise but cannot cancel CM EMI noise theoretically, since the corner frequency of PEFs cannot be low enough with the limit of volume.

AEFs are proposed to suppress EMI, characterized with smaller volume of components than PEFs. An AEF is proposed

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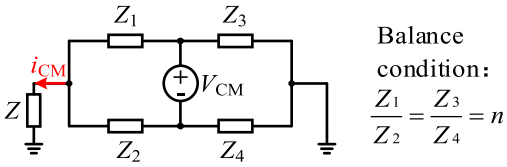


Fig. 1. Wheatstone bridge construction.

in [20]. It measures the CM current, and then generates and injects antiphase current to improve the EMI performance. In theory, AEFs can completely cancel CM EMI noise. Nevertheless, owing to the limited bandwidth of sensing and processing of the sensors and amplifiers, the effective attenuation range of an AEF is usually below few MHz [21]. Then, a hybrid EMI filter is investigated in [22] by installing a PEF with an AEF, so the effective attenuation range is promoted. Nonetheless, AEFs still face the challenges of the increased complexity of control systems and potential stability issues.

The balance technique is an attractive way to cancel the EMI noise with volume-friendly components. Balance technique can be further classified into symmetric topology and Wheatstone bridge. Symmetric three-level buck–boost converter are proposed in [23] and [24]. Since achieving symmetry requires circuit changes and synchronized driving signals, the complexity of system is increased. Wheatstone bridge is a technique implemented by adding a new CM current path for impedance balance to cancel CM EMI. The basic construction of Wheatstone bridge is depicted in Fig. 1. As long as the balance condition is achieved, the CM current flowing through the branch with resistance Z could be zero theoretically. Wheatstone bridges have been applied in some specific circuits. A Wheatstone bridge is formed by splitting the boost inductor at the converter input-side and combined with parasitic capacitors of the converter [25], as shown in Fig. 2(a). In a two-phase interleaved boost converter [26], the splitting boost inductors are made of integrated magnetics, which can not only form a Wheatstone bridge to reduce CM noise but also contribute to power density. Then, a Wheatstone bridge is introduced in a multichannel PFC converter [27], and coupled-inductors are used to reduce the parasitic effects. Moreover, in a two-switch forward converter [28], Wheatstone bridge is introduced, and the balance condition can be achieved by proper designing of the windings terminals. In [29], an additional CM current path with an extra inductor in series is inserted to form a Wheatstone bridge, as shown in Fig. 2(b). The other branches include input-side EMI filter inductor, input-side parasitic capacitor, and grounding parasitic capacitor of motor. When these parameters satisfy the balance condition, the CM noise at the converter input-side is reduced. In a three-phase neutral point clamped inverter [30], the additional balance inductors are coupled with converter output-side differential mode (DM) filter inductors to mitigate the impact of parasitic parameters of inductors on CM noise reduction performance. Another two branches of the Wheatstone bridge include grounding parasitic capacitors of converter input-side and phase leg midpoint, as shown in Fig. 2(c). Similar processes have been used in an interleaved three-phase ac–dc converter [31], and six additional inductors are coupled with the DM inductors. A Wheatstone bridge is achieved with an extra capacitor in a

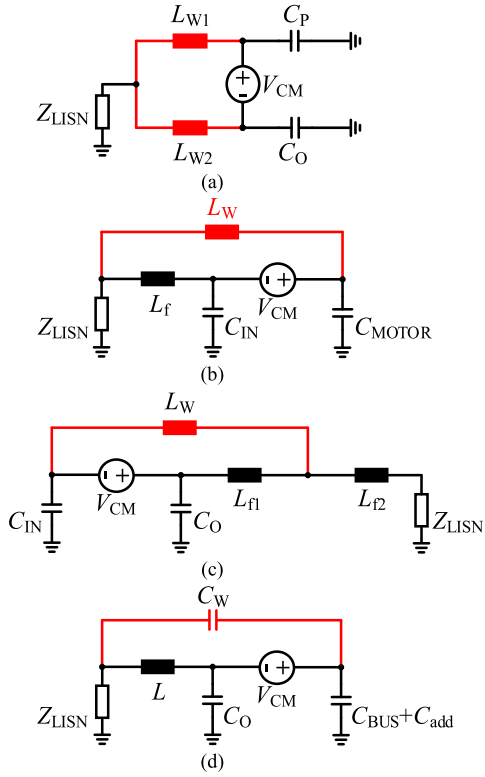


Fig. 2. Wheatstone bridge circuit of various topologies. (a) Boost converter [25]. (b) Three-phase DC–AC converter [29]. (c) Three-level neutral point clamped converter [30]. (d) Boost AC–DC rectifier and DC–AC inverter [32].

rectifier system, and the CM noise of the inverter to rectifier is reduced with a decoupling inductor in [32], as shown in Fig. 2(d). On the one hand, the balance technique achieved by adding an inductance path usually has limited CM reduction performance in high frequency range, since the inductor design with controllable high-frequency parasitic parameters is still challenging [33], [34]. On the other hand, the performance of CM EMI reduction could be deteriorated with the different front input circuits due to the grounding parasitic capacitor of dc bus forming part of the Wheatstone bridges. Therefore, a solution that can achieve balance conditions by adding capacitors and decoupling the influence of the grounding parasitic capacitor of dc bus is desired.

In this article, an improved balance technique is proposed for CM EMI reduction. The contributions of this article include the following.

1) Decouple the Wheatstone bridge circuit from the grounding parasitic capacitors of dc bus, and eliminate the influence of the front input circuit on CM reduction performance.
2) Introduce additional capacitor branches and avoid the complex design of high-frequency parasitic parameters for the inductor, thereby enhancing the performance of high-frequency CM reduction.
3) Analyze the effect of parasitic inductor of additional CM current path on CM reduction performance, and derive the revised expression for the balance condition.

The rest of this article is organized as follows. In Section II, the CM EMI model of a dc–ac converter is developed, and the

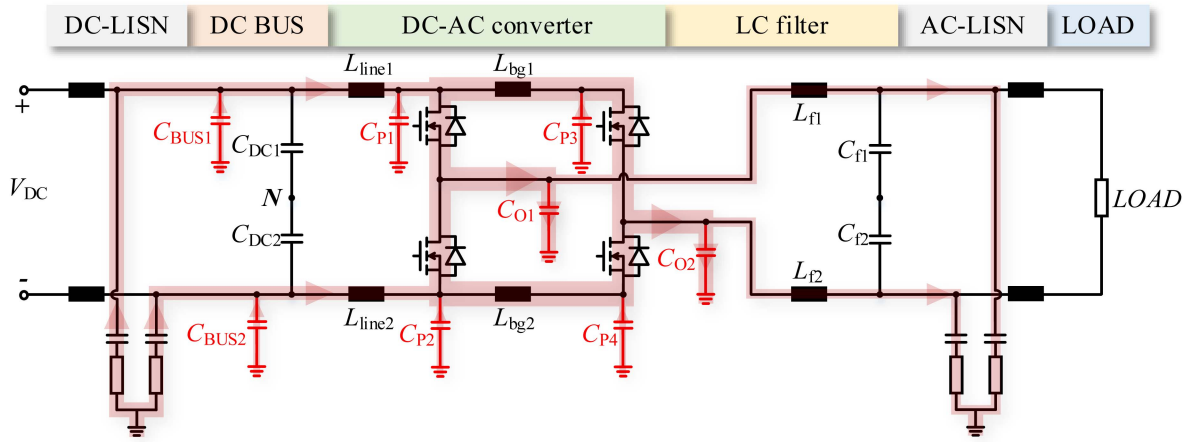


Fig. 3. Topology of a DC–AC converter and the CM current propagation path.

CM noise propagation path is analyzed. Based on the analysis, an improved balance technique is applied to the converter in Section III. Then, the effect of the parasitic parameters of additional CM current path on CM reduction performance is analyzed, and the principle of designing the additional capacitor is presented. The effectiveness of the proposed method is demonstrated in Section IV. Finally, Section V concludes this article.

II. CM EMI Model of the DC–AC Converter

In this article, a dc–ac converter is taken as an example. The topology of a dc–ac converter is shown in Fig. 3. It contains two line impedance stabilization networks (LISN), input dc bus, converter, output *LC* filter, and load. LISNs are used to measure the CM current flowing through converter input-side and output-side. C_{BUS1} and C_{BUS2} represent the grounding parasitic capacitors of the positive or negative dc bus. $C_{\mathrm{P}i}$ represents the grounding parasitic capacitors of power devices, $C_{\mathrm{O}i}$ denotes the grounding parasitic capacitors of midpoint of the phase legs. i represents the phase leg number. L_{line1} and L_{line2} represent the parasitic inductors between the input positive or negative port and the phase leg. When considering input parasitic inductors, the input-side capacitors can be divided into two parts, including grounding parasitic capacitors of power devices and grounding parasitic capacitors of dc bus. The parasitic inductors between the two phase legs are denoted as L_{bg1} and L_{bg2}. These parameters are presented in Section IV.

A. CM EMI Model

Due to the symmetrical structure of the dc–ac converter, the modeling of the CM noise source is first analyzed based on phase leg 1, as shown on the left side of Fig. 4(a), which is connected to the dc bus capacitor. First, the CM voltage sources are used to replace the switching devices according to the substitution theorem. Meanwhile, the value of the dc bus capacitor tends to be large, so it could be treated as a short circuit in the CM EMI model, as illustrated on the right side of Fig. 4(a). Second, in such a dual-source circuit, the superposition theorem is used to calculate the equivalent CM noise by analyzing the

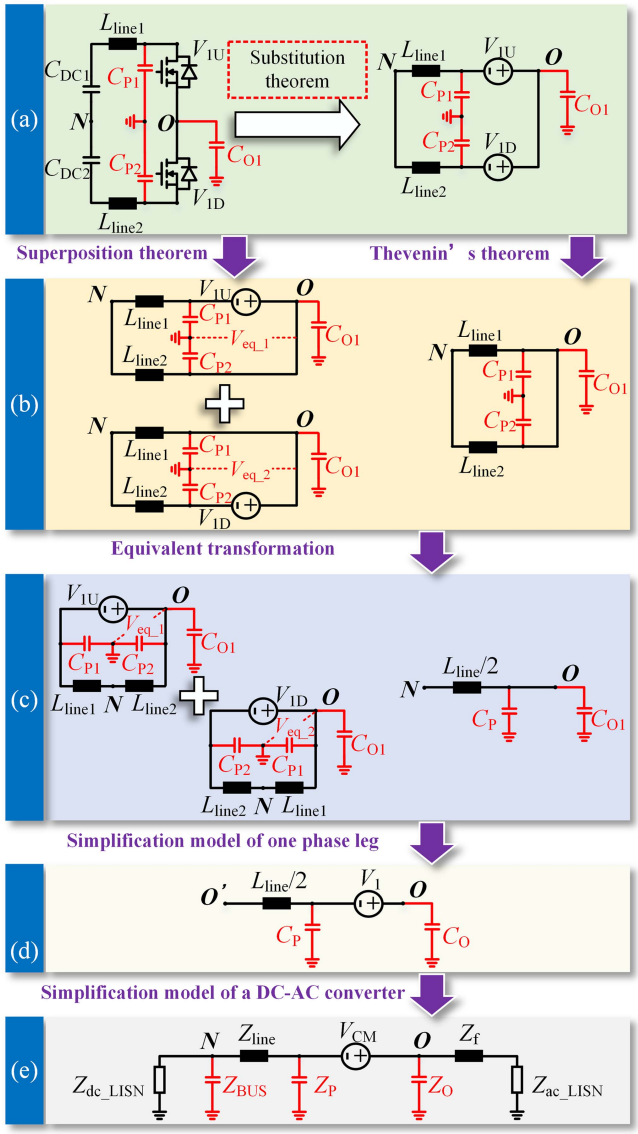


Fig. 4. Simplification of CM EMI model. (a) Replace the switching devices with CM voltage sources. (b) Derive equivalent CM impedance and noise source. (c) Equivalent transformation. (d) Simplified model of one phase leg. (e) Simplified model of a DC–AC converter.

voltage sources separately, as shown on the left side of Fig. 4(b). Furthermore, based on Thevenin's theorem, the voltage sources are set as short circuit to calculate the equivalent impedance between the port O and ground port, as shown on the right side of Fig. 4(b). For simplicity, we assume that C_{P1} is equal to C_{P2}. Third, by converting the CM noise circuit into the left side of Fig. 4(c), equivalent CM noise can be easily derived as

$$V_{\mathrm{eq\_1}} = \frac{V_{\mathrm{1U}}}{2} \tag{1}$$

$$V_{\mathrm{eq\_2}} = \frac{V_{\mathrm{1D}}}{2}. \tag{2}$$

The grounding parasitic capacitors of power devices C_{P1} and C_{P2} can be considered to be connected in parallel and the equivalent capacitance is denoted as sum of C_{P1} and C_{P2}. Considering that the circuit structure is symmetrical, the equivalent impedance circuit can be expressed on the right side of Fig. 4(c)

$$L_{\mathrm{line1}} = L_{\mathrm{line2}} = L_{\mathrm{line}} \tag{3}$$

$$C_{\mathrm{P}} = C_{\mathrm{P1}} + C_{\mathrm{P2}} \tag{4}$$

$$L_{\mathrm{eq}} = L_{\mathrm{line}}/2. \tag{5}$$

The simplified CM EMI of phase leg 1 is shown in Fig. 4(d)

$$V_1 = V_{\mathrm{eq}} = V_{\mathrm{eq\_1}} + V_{\mathrm{eq\_2}} = \frac{V_{\mathrm{1U}} + V_{\mathrm{1D}}}{2}. \tag{6}$$

Furthermore, $L_{\mathrm{bg}i}$ can be disregarded since the distance between two phase legs is short enough compared to the distance between the input positive or negative port and the phase legs. The phase leg 2 can then be simplified to the same diagram as phase leg 1 according to the symmetrical structure of two phase legs.

Finally, after modeling the switching devices circuit, the equivalent CM impedance circuits at the converter input-side and converter output-side need to be modeled. At the converter input-side, the grounding parasitic capacitors of the positive or negative dc bus C_{BUS1} and C_{BUS2} can be simplified as parallel in the CM EMI model. And the same can be done for dc-LISN, which is regarded as two 50-Ω resistors in parallel. Similarly, for the converter output-side, the two phases are connected in parallel in the CM EMI model. Therefore, the filter inductors and ac-LISN are simplified in the same manner as the converter input-side, as presented in Fig. 4(d), with each component represented by its impedance

$$V_{\mathrm{CM}} = (V_1 + V_2)/2 \tag{7}$$

$$Z_{\mathrm{BUS}} = Z_{\mathrm{BUS1}} // Z_{\mathrm{BUS2}} \tag{8}$$

$$Z_{\mathrm{P}} = Z_{\mathrm{C_{P1}}} // Z_{\mathrm{C_{P2}}} // Z_{\mathrm{C_{P3}}} // Z_{\mathrm{C_{P4}}} \tag{9}$$

$$Z_{\mathrm{O}} = Z_{\mathrm{C_{O1}}} // Z_{\mathrm{C_{O2}}} \tag{10}$$

$$Z_{\mathrm{line}} = Z_{\mathrm{L_{line}}}/2 \tag{11}$$

$$Z_{\mathrm{f}} = Z_{\mathrm{L_{f1}}} // Z_{\mathrm{L_{f2}}}. \tag{12}$$

B. CM Current Propagation Path

From the CM current direction shown in Fig. 3, it is evident that the CM current is generated by the CM noise source (switching actions) and passes through grounding parasitic capacitors of power devices, filter inductances, and the ac-LISN. The CM current at this side of propagation path may cause abnormal operation of the load. The filter capacitors would not contribute to CM current due to their floating midpoint. Because of the CM current coupling at the converter input-side and output-side, the CM current returns to the CM noise source through the common ground, passing through the grounding parasitic capacitors, input parasitic inductors, and the dc-LISN. The CM current at this side of propagation path may cause pollution to the input source of the converter.

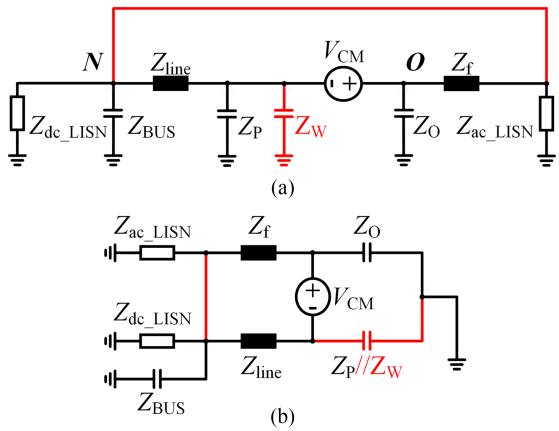


Fig. 5. Construction of Wheatstone bridge. (a) Adding an ideal CM current path and an additional capacitor. (b) Adjustment of the circuit to a Wheatstone bridge representation.

III. CM EMI Elimination of Balance Technique

A. Balance Technique With Input Parasitic Inductor

To suppress the CM noise, the balance technique is applied, as shown in Fig. 5(a). A new CM current path is added between the converter input-side and output-side. Due to the significant impedance ratio between filter inductors (in the uH range) and the input parasitic inductors (in the nH range), an additional capacitor C_{W} is connected in parallel with C_{P} to achieve the balance condition. The Wheatstone bridge is developed, as shown in Fig. 5(b), and the balance condition is

$$\frac{Z_{\mathrm{f}}}{Z_{\mathrm{line}}} = \frac{Z_{\mathrm{O}}}{Z_{\mathrm{P}} // Z_{\mathrm{W}}} \tag{13}$$

where Z_{W} represents the impedance of the additional capacitor C_{W}. As long as the balance condition is met, the CM current flowing through the dc-LISN and ac-LISN is theoretically zero, so the CM noise is effectively canceled. Moreover, the grounding parasitic capacitors of dc bus are excluded from the Wheatstone bridge, and variations in grounding parasitic capacitors of dc bus are decoupled from the CM reduction performance.

Two extra circuits are utilized for the physical attachment of the additional CM current path to prevent the fundamental current from flowing into the additional CM current path. Because of the parallel connection of dc bus capacitors and filter capacitors in the dc–ac converter, only high-frequency current harmonics will flow through these capacitors. Therefore, the midpoint of the dc bus can serve as the CM connection point at the converter input-side, while the midpoint of the filter capacitor

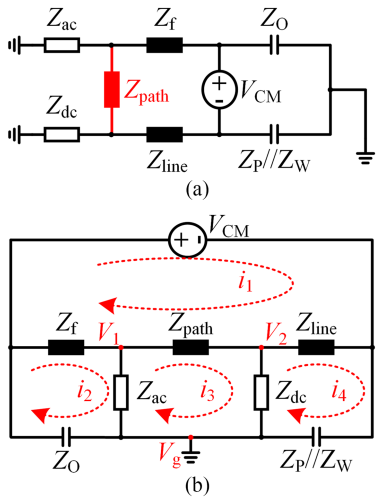


Fig. 6. Rearrangement of Wheatstone bridge.

can function as the CM connection point at the converter output-side. The impedances of dc bus capacitors, filter capacitors, and additional CM current path are lumped as $Z_{\rm path}$, as shown in Fig. 6. The dc bus capacitors and filter capacitors are large enough, so $Z_{\rm path}$ is dominated by the additional CM current path in high frequency range. Furthermore, the additional CM current path is modeled as a series connection of parasitic resistor and parasitic inductor. A wire with relatively low resistance is used in experiment, so $Z_{\rm path}$ is further dominated by the parasitic inductor in high frequency range. The influences of the parasitic inductor of the additional CM current path on CM reduction performances will be discussed in the following section.

B. Effect of Additional CM Current Path Parasitic Parameters on CM Reduction Performance

In practice, there are unwanted parameters in the additional CM current path, as shown in Fig. 6(a), which can disrupt the balance condition, making it impossible to completely cancel the CM noise. Rearrange the Wheatstone bridge in Fig. 6(b) to calculate the CM current. For brevity, $Z_{\rm dc}$ represents the $Z_{\rm dc\_LISN}$ in parallel with $Z_{\rm BUS}$, $Z_{\rm ac}$ represents the $Z_{\rm ac\_LISN}$. In the ideal scenario, based on (13), the CM current flowing through $Z_{\rm dc}$ and $Z_{\rm ac}$ is zero, which implies

$$\begin{cases} i_2 = i_3 = i_4 \\ V_1 = V_2 = V_g. \end{cases} \tag{14}$$

Based on Fig. 6(b), first list the current expressions for each grid based on Kirchhoff's law

$$\begin{cases} (\mathrm{Z_f}+\mathrm{Z_{path}}+\mathrm{Z_{line}})\, i_1 - \mathrm{Z_f} i_2 - \mathrm{Z_{path}} i_3 - \mathrm{Z_{line}} i_4 = V_{\rm CM} \\ (\mathrm{Z_f} + \mathrm{Z_{ac}} + \mathrm{Z_O})\, i_2 - \mathrm{Z_f} i_1 - \mathrm{Z_{ac}} i_3 = 0 \\ (\mathrm{Z_{path}} + \mathrm{Z_{ac}} + \mathrm{Z_{dc}})\, i_3 - \mathrm{Z_{ac}} i_2 - \mathrm{Z_{path}} i_1 - \mathrm{Z_{dc}} i_4 = 0 \\ (\mathrm{Z_{line}} + \mathrm{Z_{dc}} + \mathrm{Z_P}//\mathrm{Z_W})\, i_4 - \mathrm{Z_{dc}} i_3 - \mathrm{Z_{line}} i_1 = 0. \end{cases} \tag{15}$$

Based on Fig. 6(b) and (15), the CM current on the dc-LISN and ac-LISN can be derived as

$$\begin{cases} i_{\rm CMIN} = i_3 - i_4 \\ i_{\rm CMOUT} = i_2 - i_3 \end{cases}. \tag{16}$$

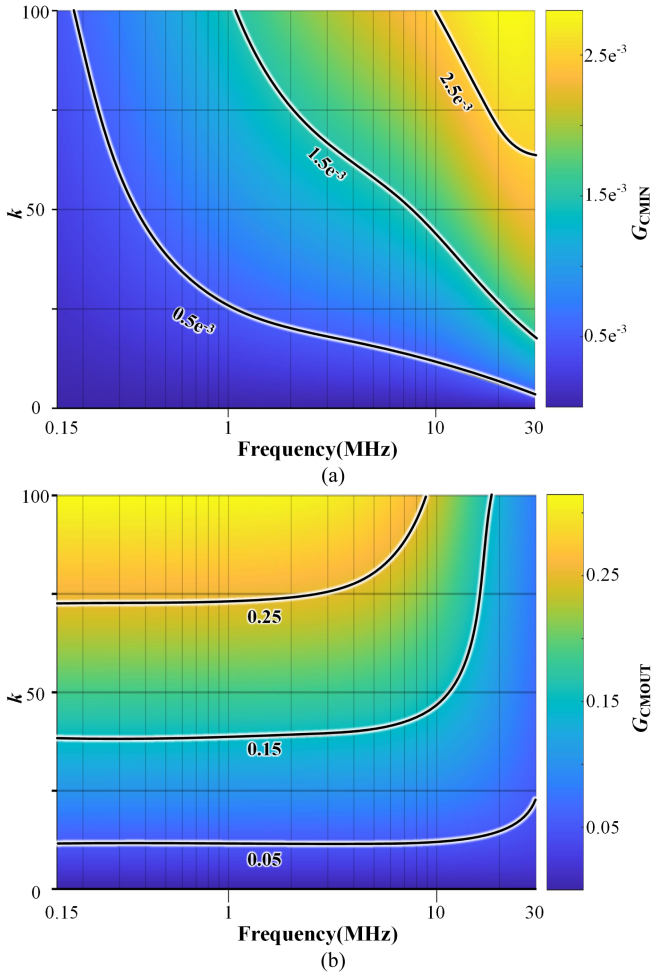


Fig. 7. Effect of additional CM current path parasitic inductor on CM noise gain at the: (a) converter input-side; (b) converter output-side.

As a matter of fact, $i_{\rm CMIN}$ and $i_{\rm CMOUT}$ are positively correlated with the voltage measured by LISNs, $V_{\rm CMIN}$ and $V_{\rm CMOUT}$, which are functions of $Z_{\rm path}$. Define the input-side CM noise gain $G_{\rm CMIN}$ and the output-side CM noise gain $G_{\rm CMOUT}$, respectively, as follows:

$$G_{\rm CMIN} = \frac{|V_{\rm CMIN}|}{|V_{\rm CM}|} \tag{17}$$

$$G_{\rm CMOUT} = \frac{|V_{\rm CMOUT}|}{|V_{\rm CM}|}. \tag{18}$$

Assuming $Z_{\rm path}/Z_{\rm line}$ as a function of k, the relationship among $G_{\rm CMIN}$, $G_{\rm CMOUT}$, k and frequency is shown in Fig. 7. As k increases, $G_{\rm CMIN}$ and $G_{\rm CMOUT}$ gradually increase throughout the frequency range. This is reasonable since the larger parasitic inductors lead to greater imbalance. $G_{\rm CMIN}$ has a larger increment in the high frequency range than that in the low frequency range, while $G_{\rm CMOUT}$ presents larger increment in the low frequency range. Overall, the larger the $Z_{\rm path}$, the poorer the CM reduction performance. Therefore, when considering the parasitic inductor of the additional CM current path, the original balance condition is no longer met. The balance condition should be revised.

TABLE I
SIMULATION AND EXPERIMENTAL PARAMETERS

Parameter	Value
Dc voltage V_{dc}/V	200
Filter inductor L_f/μH	39
Input parasitic inductor L_{line}/nH	90.3
Additional CM path parasitic inductor L_{path}/nH	500
Additional capacitor C_W/nF	9.05
Power device parasitic capacitor C_P/pF	37.6
Phase leg midpoint parasitic capacitor C_O/pF	21
Dc bus parasitic capacitor C_{BUS}/pF	93.8
Switching Frequency f_{sw}/kHz	160
Output Frequency f_{out}/kHz	1

Based on (15) and (16), we first assume that i_{CMIN} equals zero, i.e., the CM noise measured at the dc-LISN is zero. In this case, the balance condition becomes

$$\frac{Z_{ac}Z_f + Z_{path}(Z_{ac}+Z_f+Z_O)}{Z_{line}Z_{ac}} = \frac{Z_O}{Z_P//Z_W}. \quad (19)$$

Moreover, assuming i_{CMOUT} equals zero, i.e., the CM noise measured at the ac-LISN is zero. In this case, the balance condition becomes

$$\frac{Z_f}{Z_{line}+\frac{Z_{path}}{Z_{dc}}(Z_{dc}+Z_P//Z_W+Z_{line})} = \frac{Z_O}{Z_P//Z_W}. \quad (20)$$

Balance conditions (13), (19), and (20) can be transformed as follows:

$$Z_P//Z_W = \frac{Z_O Z_{line}}{Z_f} \quad (21)$$

$$Z_P//Z_W = \frac{Z_O Z_{line}}{Z_f+\frac{Z_{path}}{Z_{ac}}(Z_{ac}+Z_f+Z_O)} \quad (22)$$

$$Z_P//Z_W = \frac{Z_O Z_{line}+Z_O Z_{path}+\frac{Z_O Z_{line} Z_{path}}{Z_{dc}}}{Z_f-\frac{Z_{path}Z_O}{Z_{dc}}}. \quad (23)$$

In (23), Z_{dc} represents the grounding parasitic capacitor of dc bus (in the tens of pF levels). In addition, Z_{path} is often in the hundreds of nH making the ratio of Z_{path}/Z_{dc} small enough in the concerned frequency range. Therefore, it can still be considered that the impact of variations in the front input circuit is decoupled from the balance technique. For a specific analysis, by substituting the parameters from Table I into (17) and (18), the changing trends of G_{CMIN} and G_{CMOUT} under different frequencies and different C_W are given in Fig. 8. The solid lines represent G_{CMIN}, and the dashed lines represent G_{CMOUT}. With the increase of C_W, both G_{CMIN} and G_{CMOUT} gradually decrease, and the rates of change also gradually decrease, as shown in Fig. 8(a). Taking the noise gain at 5 MHz as an example for analysis, G_{CMOUT} reaches an inflection point when $C_W = 5.6$ nF and gradually increases thereafter, while G_{CMIN}

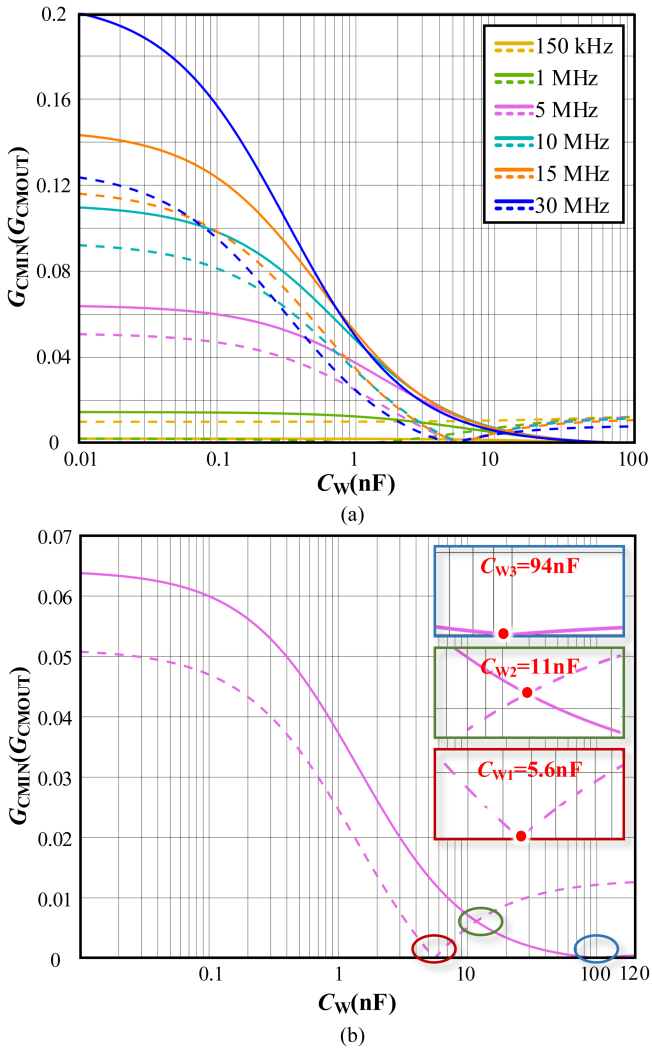
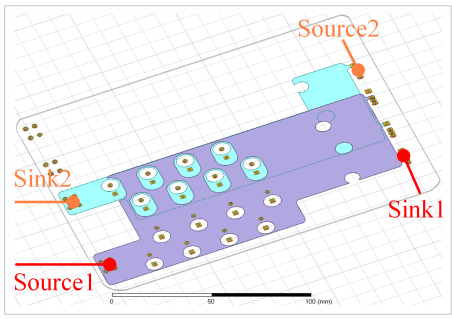


Fig. 8. CM noise gains changing trends: (a) at different frequency points; (b) taking 5 MHz as an example. The solid lines represent G_{CMIN}, and the dashed lines represent G_{CMOUT}.

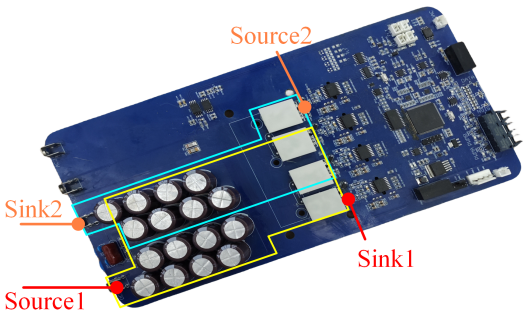
continues to decrease until C_W is around 94 nF. G_{CMIN} reaches the inflection point and then increases thereafter, as shown in Fig. 8(b). It is obvious that a relatively smaller C_W needs to be selected to achieve the best CM reduction performance at the converter output-side, while a relatively larger C_W needs to be selected to achieve the best CM reduction performance at the converter input-side. Due to the conflicting requirements for C_W, it is necessary to take into account the CM reduction performance at both sides, and a tradeoff design needs to be made. As a matter of fact, both the input and output sides of the converter have relatively low noise gain characteristics when $C_W = 11$ nF, as shown in Fig. 8(b).

IV. SIMULATION AND EXPERIMENT

To carry out the proposed method, the parasitic parameters of the main circuit should be obtained. The input parasitic inductors $L_{line\,i}$ could be simulated using ANSYS Q3D extractor, in which the power PCB file of dc–ac converter is imported and voltage nets are assigned, as shown in Fig. 9. After a frequency sweep



(a)



(b)

Fig. 9. Extraction of input parasitic inductors. (a) Simulation model in ANSYS Q3D. (b) Power board of DC–AC converter.

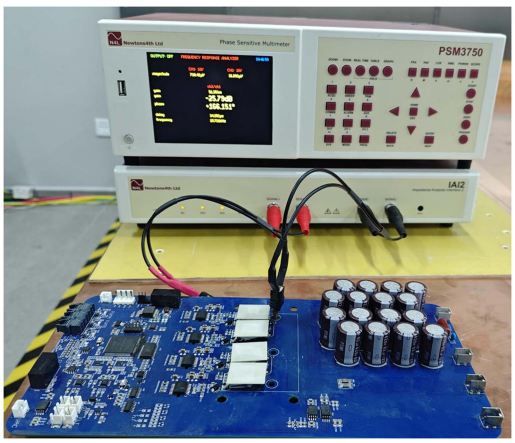
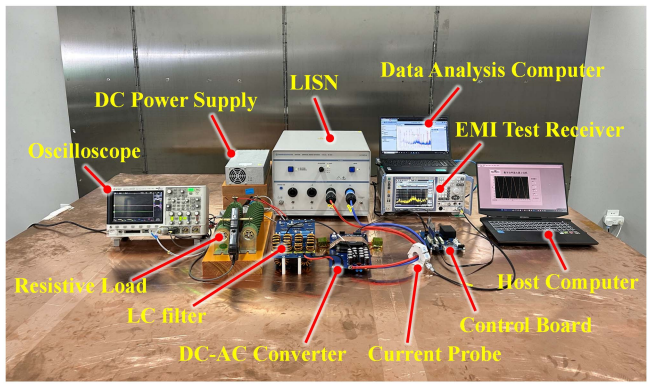


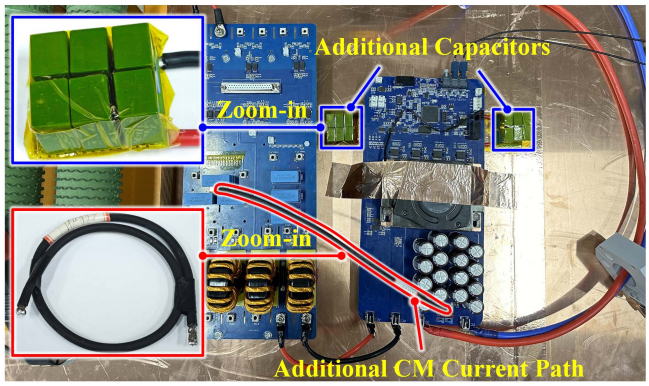
Fig. 10. Impedance measurement setup.

operation, the parasitic inductances are extracted and $L_{\text{line}i}$ is chosen to be the average value of 90.3 nH.

Other parasitic parameters of the dc–ac converter could be obtained by using an impedance analyzer Newtons4th Ltd PSM3750, as shown in Fig. 10. The experimental platform is shown in Fig. 11. The improved balance technique is composed of additional capacitors and an additional CM current path, as shown in Fig. 11(b). The additional capacitors are divided into two identical groups to ensure the symmetry of the CM circuit and connected between the positive or negative terminals of the phase leg and ground. A wire with relatively low parasitic parameters is used as the additional CM current path in the experiment. The main circuit parameters are given in Table I.



(a)



(b)

Fig. 11. Experimental platform. (a) Experimental setups. (b) Additional branches.

A. Simulation Verification of the Improved Balance Technique

To verify the effectiveness of the proposed method, the simulated comparisons of the method in [30] and the improved balance technique are shown in Fig. 12. For the input-side of the converter, it can be observed that the improved balance technique effectively suppresses CM noise across the concerned frequency range, with a maximum suppression of 55 dB at around 5.6 MHz, as shown in Fig. 12(a). For the output-side of the converter, the CM reduction performance with the improved balance technique achieves significant suppression within the concerned frequency range, with a maximum suppression of 45 dB at around 5.6 MHz, as shown in Fig.12(b). In both simulations, the improved balance technique can achieve performances similar to the method in [30] in low frequency range. Moreover, the improved balance technique demonstrates superior CM reduction performance in the frequency range of several MHz, where the equivalent parallel capacitances of the additional inductor could cause noise peaks in [30].

To explore the influence of the proposed method on system efficiency, a platform with the same parameters as the actual system is constructed to conduct loss simulations. The loss of a dc–ac converter is mainly composed of switching devices loss and magnetic components loss. The comparison of power loss distribution is shown in Fig. 13. It can be observed that the switching loss of the power devices decreases with the integration of the improved balance technique, while the

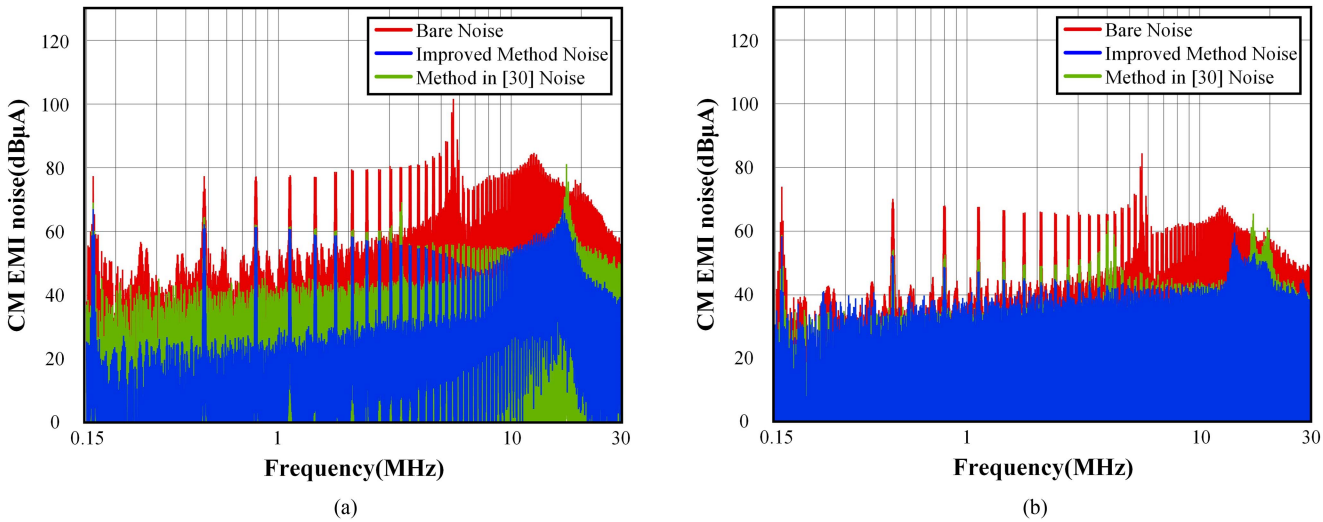


Fig. 12. Comparison of the simulated CM EMI spectra. (a) Converter input-side. (b) Converter output-side.

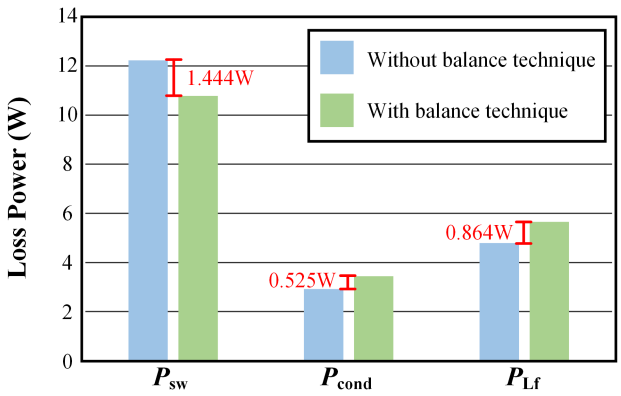


Fig. 13. Comparison of the system power loss.

conduction loss and the loss of the output filter inductor increase. The main reason of such phenomenon is that an appropriate resonance introduced by the additional branches leads to an increase in current ripple, thereby increasing conduction losses and magnetic component losses. It should be pointed out that because the current ripple increases, the direction of the inductor current changes near the zero crossing point of the fundamental frequency current. This creates conditions for zero voltage switching (ZVS) and reduces switching losses. For quantitative analysis, the reduction in switching loss outweighs the increase in conduction loss and the loss of the output filter inductor, resulting in a system efficiency improvement from 97.324% to 97.331% with integrating the improved balance technique. A slight improvement in system efficiency is achieved with the improved balance technique.

B. Experiment Verification of the Improved Balance Technique

The experiment of CM noise is measured with or without the improved balance technique. The experimental results are shown in Fig. 14 and the dotted lines are envelopes of the simulation results. Fig. 14(a) shows that the converter input-side CM noise

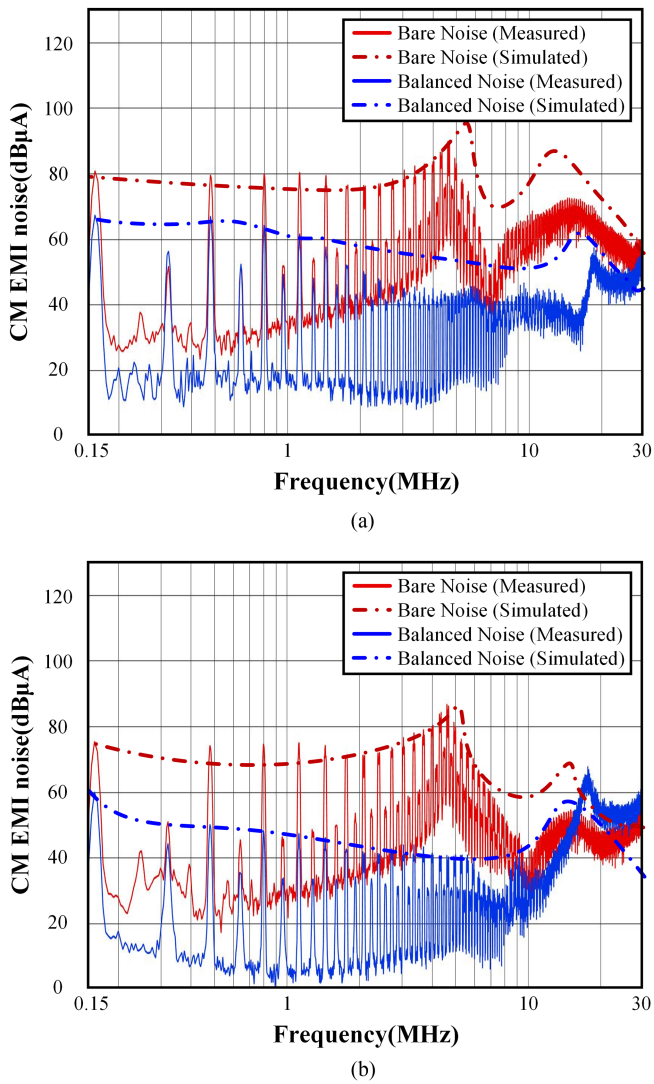


Fig. 14. Comparison of the experimental CM EMI spectra with and without balance technique. (a) Converter input-side. (b) Converter output-side.

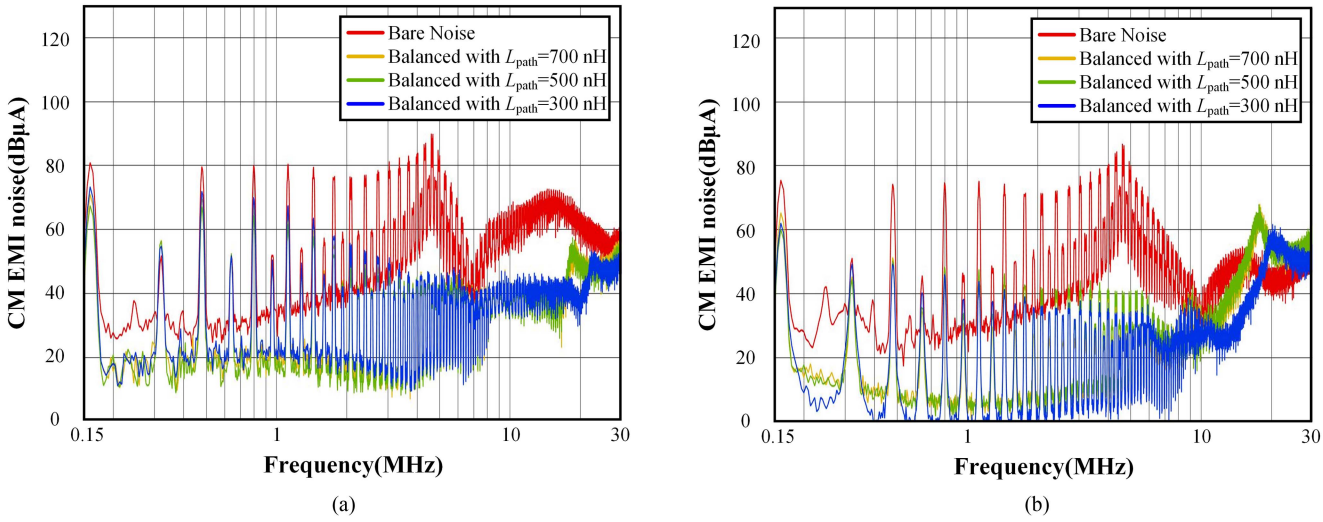


Fig. 15. Comparison of the experimental CM EMI spectra under different values of L_{path}. (a) Converter input-side. (b) Converter output-side.

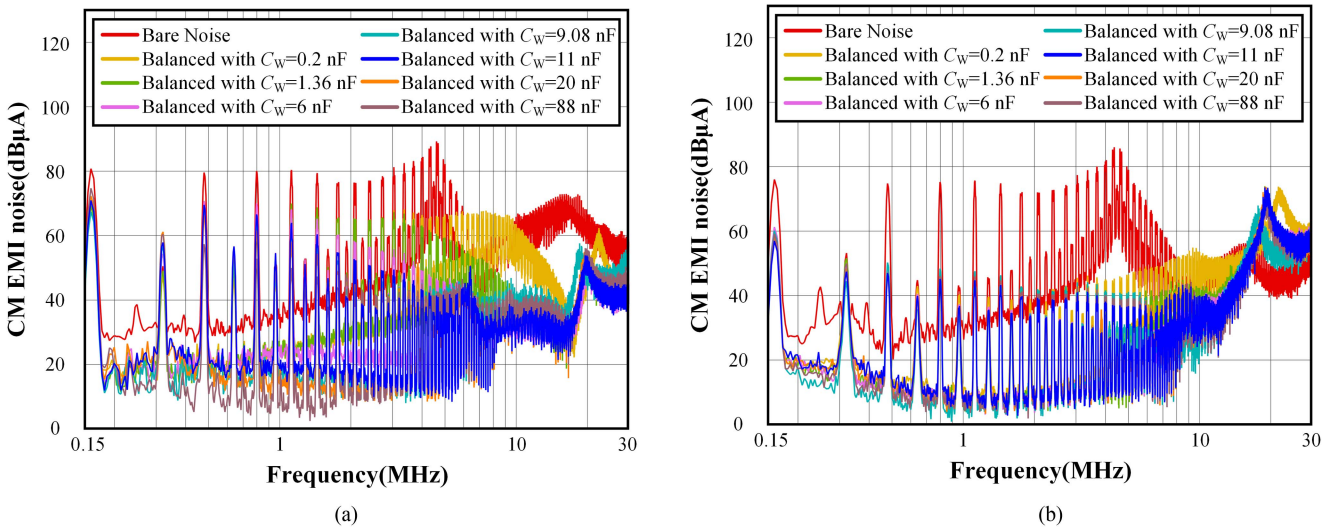


Fig. 16. Comparison of the experimental CM EMI spectra with different values of the C_{W}. (a) Converter input-side. (b) Converter output-side.

is greatly reduced across the concerned frequency range by up to 50 dB. Fig. 14(b) shows that the converter output-side CM noise is greatly reduced across the concerned frequency range by up to 45 dB. The simulation and experimental results are in good agreement.

To evaluate the influence of the parasitic inductance of the additional CM current path on the CM reduction performance, the experiment of CM noise is measured with different parasitic inductances. The results are given in Fig. 15 when the parasitic inductances are set as 300, 500, and 700 nH, respectively. From Fig. 15(a), the converter input-side CM reduction performances are degraded above 16 MHz under large parasitic inductance. From Fig. 15(b), the converter output-side CM reduction performances are seriously degraded under large parasitic inductance and have already degraded significantly at low frequencies. These results are consistent with the theoretical calculations shown in Fig. 7.

In order to verify the effectiveness of the principle of designing the additional capacitor C_{W}, the experiment of CM noise is measured with different C_{W}, as shown in Fig. 16. The CM reduction performance at the converter input-side gradually improved as the capacitance value of C_{W} increased to 11 nF, as shown in Fig. 16(a). Compared with the ideal scenario where the calculated C_{W} is 9.05 nF, the CM reduction performance has significantly improved from 700 kHz to 7 MHz, with a maximum improvement of 6 dB. Continuing to increase C_{W} can still slightly improve the CM reduction performance, but the benefits are minimal. This is consistent with the analysis results in Fig. 8. The CM reduction performance at the converter output-side gradually improved as the capacitance value increased to 6 nF, as shown in Fig. 16(b). Compared with the ideal scenario, the CM reduction performance has significantly improved from 500 kHz to 7 MHz, with a maximum increment of 4 dB. Continuing to increase C_{W} could slightly degrade the CM reduction

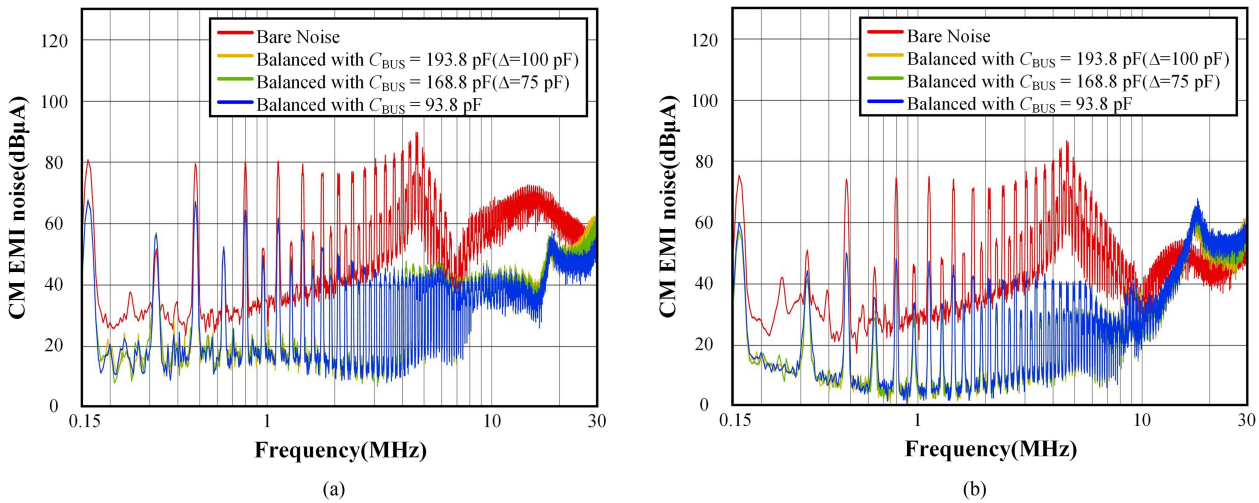


Fig. 17. Comparison of the experimental CM EMI spectra with different grounding parasitic capacitors of DC bus. (a) Converter input-side. (b) Converter output-side.

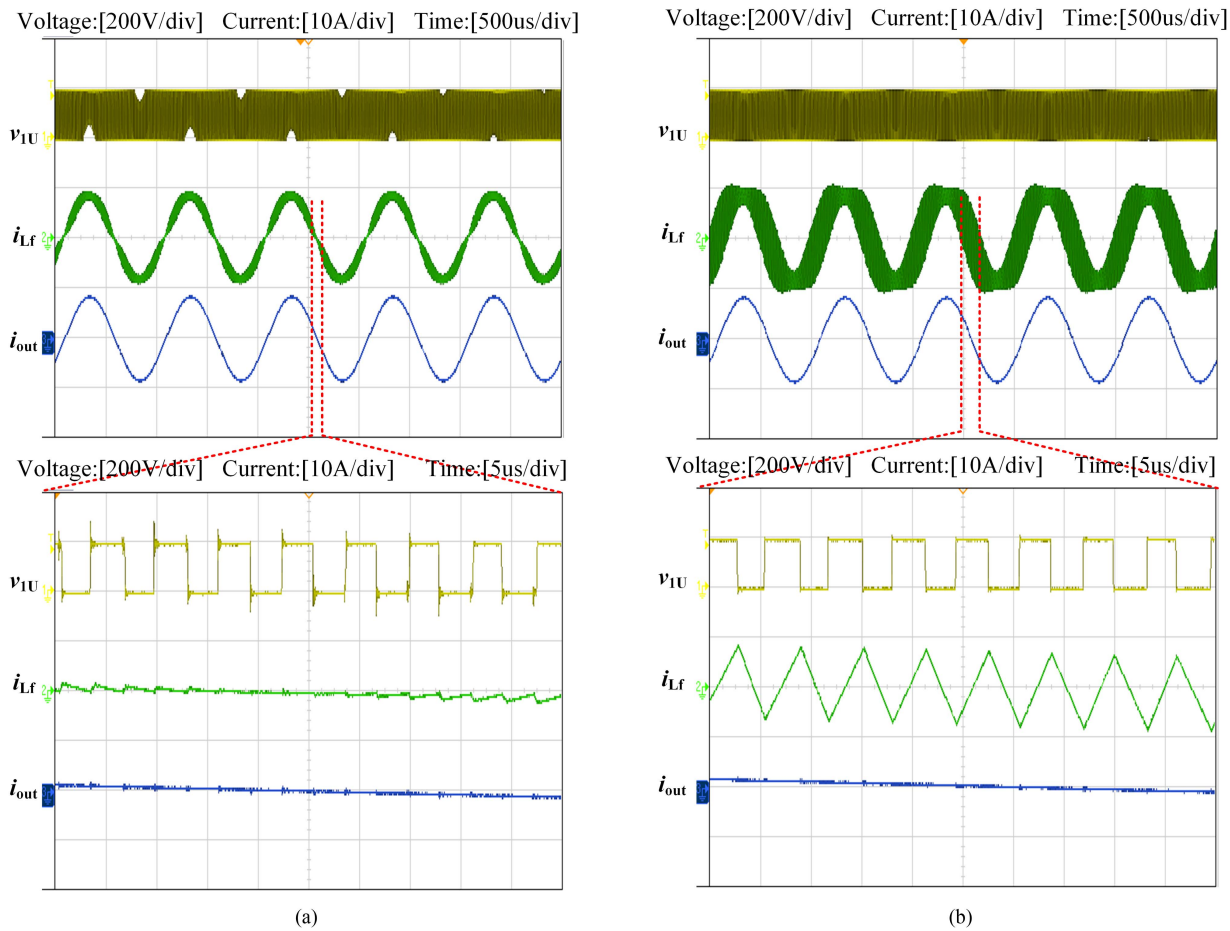


Fig. 18. Experimental testing system efficiency. (a) Without balance technique. (b) With balance technique.

performance. As discussed in Section III-B, selecting a tradeoff of 11 nF can achieve a CM reduction performance similar to that of C_W being 6 nF. The degraded reduction performances can be optimized by adjusting the capacitor value of C_W, as discussed previously.

To evaluate the effectiveness of decoupling the front input circuits variations, the experiment of CM noise is measured with different grounding parasitic capacitors. The grounding parasitic capacitors are varied by implemented capacitors in parallel between dc bus and ground, and the results are shown in

Fig. 17. The fluctuations of converter input-side CM reduction performance are within 5 dB when C_{BUS} increases 100 pF, and at converter output-side are less than 2 dB. The improved balance technique can achieve almost consistent reduction performances under different values of grounding parasitic capacitor of dc bus.

To explore the impact of the improved balance technique on system efficiency, the experiment of system efficiency is measured with and without the improved balance technique. The experimental waveforms are shown in Fig. 18. It can be observed that the improved balance technique introduces appropriate resonance, which results in an increase in the ripple of inductor current, further increasing the conduction loss of switching devices and the losses of magnetic components. In the meantime, at the zero crossing point of the fundamental frequency current, the direction of the inductor current changes, as shown in Fig. 18(b), creating conditions for ZVS and reducing switching losses. It is revealed in simulation that the reduction in switching loss could exceed the increase in conduction loss and the loss of the output filter inductor. Through a HIOKI PW8001 power analyzer measurement, it is found that there is a slight improvement from 97.436% to 97.449% when integrating the improved balance technique.

V. Conclusion

This article investigates an improved balance technique for a dc–ac converter. It does not require additional inductors, reducing the difficulty of designing the high-frequency parasitic parameters of inductors that could induce noise peaks. Moreover, it decouples the effect of grounding parasitic capacitor of the dc bus, eliminating the impact of front input circuits variations on CM reduction performance. First, CM noise source and propagation paths are analyzed. Based on circuit theorems, the converter model is then simplified, and the CM current at the converter input-side and output-side is derived. An improved balance technique considering input parasitic inductor has been proposed. Furthermore, the impact of parasitic parameters on the CM reduction performance is discussed. The revised expressions for the balance condition are derived. Finally, the effectiveness of the improved balance technique is validated by simulations and experiments.

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