Analysis and Design of an Isolated Current Source Class-E Inverter With Significant Harmonics

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***Abstract*—This article presents an isolated current source class-E inverter topology with load-independent zero-voltage switching. If harmonics were neglected (thanks to high quality factor), the current source behavior would be maintained at any load as reported in the literature. When harmonics are significant, the load current starts to vary with the load. This article aims to predict the load range with a soft current source defined by a small load current variation (5% in the example), considering the impact of harmonics. To obtain the accurate load current variation with the load resistance, the time-invariant multifrequency modeling (TIMF) method is utilized to solve the steady-state solution without numerical iteration. The switch and its paralleled shunt capacitor are modeled as a single component to treat the discontinuous state of the capacitor. The modified TIMF modeling provides a direct solution of the RMS load current and resonant capacitor's voltage stress, enabling general guidance of the coupled inductors design considering the tradeoff between load range and voltage stress. Three 10 V input, 0.6 Arms output, and 16.4 W maximum power prototypes were built with different load ranges. A maximum 47:1/30:1 load range for 10%/5% output current variation was achieved.**

***Index Terms*—Coupled inductors, current source, resonant inverters, zero-voltage switching (ZVS).**

I. Introduction

With the widely applied wide bandgap devices, the switching frequency of power converters has entered megahertz (MHz) region to help with miniaturization. Load-independent (LI) class-E inverters are promising topologies as they provide intrinsic constant voltage (CV) [1], [2], [3] or constant current (CC) [4], [5] output, eliminating the need for a very high bandwidth control loop and current sensing [6].

As mentioned in [6], there are some applications where a constant ac output current is beneficial. Possible applications include auxiliary power supplies (APS) [7], wireless chargers [8], and LED drivers [9], [10]. An LI class-EF inverter with infinite input inductor (L_{in}) has been proposed [6]. For class-E inverter, LI CC output can be realized either by adding impedance matching networks [4], [11] or using parallel resonant class-E topology [5].

For applications either isolation is required, e.g., APS, or isolation naturally exists, e.g., wireless power transfer (WPT), an isolated topology is needed. An improved isolated parallel resonant class-E inverter is proposed with all resonant inductors integrated with the isolation stage, resulting in the same number of passive components but with an improved load range [12]. However, the parallel resonant network has a high circulating current, leading to higher conduction losses. Besides, the resonant inductors are either leakage or magnetizing inductors, making it not suitable for applications like WPT, where the coupling varies with small distance change or misalignment [13]. WPT with series-series (S-S) compensation for class-E inverter has been analyzed to achieve a CC output [24]. In this article, the trans-susceptance network proposed in [4] is integrated with the isolation stage as shown in Fig. 1, which is similar to the WPT with S-S compensation in [24]. Only self-inductances will be used for resonance thus the tolerance can be improved. An equivalent circuit is used to explain the CC behavior and basic design steps are provided when the harmonics are not significant.

The design and analysis of the class-E inverters are usually based on a high loaded Q assumption that the harmonics are well mitigated so only the fundamental component exists in the output resonant network [4], [5], [6]. However, a high-Q design imposes increased voltage stress on resonant components for series resonant networks or increased current stress for parallel resonant networks. Furthermore, even a high loaded Q

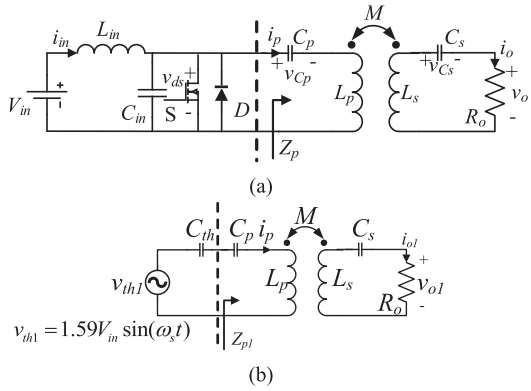

Fig. 1. Topology and equivalent circuit of the isolated CC class-E inverter. (a) Topology of the isolated CC Class-E inverter. (b) Equivalent circuit at switching frequency.

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is designed at heavy load, a high Q can still not be guaranteed at light load condition, leading to a larger than expected variation on the load voltage/current [4], [5]. Inductors are the major contributors of harmonic mitigation in series resonant network, but large inductance also leads to increased volume, loss and voltage stress. Therefore, the variation of load voltage/current variation under different inductances needs to be quantified to provide guidance for inductance selection based on desired load range.

To investigate the impact of harmonics on the load voltage/current variation for LI class-E inverters, the circuit analysis needs to include harmonics. State-Space Modeling has been used for class-E inverters for high-Q cases. To solve such circuits considering the harmonics, state space analysis (SSA) [14], [15], [16], [17] has been used for class-E inverter with infinite L_{in}. However, this method requires a few numerical iterations. Also, the ON and OFF periods need to be solved separately as the circuit topology varies in these two periods. This makes SSA very time-consuming. Besides, there has not been the SSA of class-E with finite L_{in} without assuming high Q, even though theoretically this is doable.

Frequency domain analysis like the extended impedance method (EIM) [18], [19] has been used to solve the steady state solution. The switch S is modeled by a time-dependent resistor and linearized by its Fourier series. The circuit is then solved with the impedance matrix form. However, a high harmonic level is needed for EIM as indicated in [18], which increases the matrix size and time to obtain the results.

An alternative analysis method to linearize the switch is time-invariant multifrequency (TIMF) modeling [20]. It has been used in the steady-state and dynamic modeling of PWM converters with the quasi-Fourier series (QFS) representation of state variables and the switching function [21]. The circuit's steady state can be solved with a simple matrix without numerical iteration. For resonant converters where the switch is paralleled with a shunt capacitor like class-E inverters, the TIMF has not been used yet.

This article extends the TIMF modeling to the isolated CC class-E resonant inverter by suggesting a way to model the switched shunt capacitor C_s to treat its interrupted state. The harmonic order of up to 3 is considered, which provides a balance between accuracy and matrix size. The RMS variation of the load current as load resistance varies can be quantified directly from the TIMF model so that the load range for different inductance selections and the resulting voltage stress on the primary compensation capacitor can be obtained. The tradeoff between load range and voltage stress is displayed with normalized inductances to provide general guidance of the isolation stage design for the desired load range. Additional load current variation from component ESRs is also analyzed.

The rest of this article as organized as follows. The topology and basic design equations will be described in Section II. Although the theory is applicable for arbitrary duty ratio, D will be kept at 0.5 herein for maximum power output capability [5]. Section III will demonstrate the impact of poor harmonic mitigation on the circuit operation under light load conditions. The TIMF model and how it can be utilized in the class-E inverter will be introduced in Section IV. With the help of the TIMF model, Section V will introduce revised design steps considering the impact of inductance selection on the load range and voltage stress, providing general guidance for the coupled inductors design. Section VI will show the experimental validation of three prototypes with different load ranges. Finally, Section VII concludes this article.

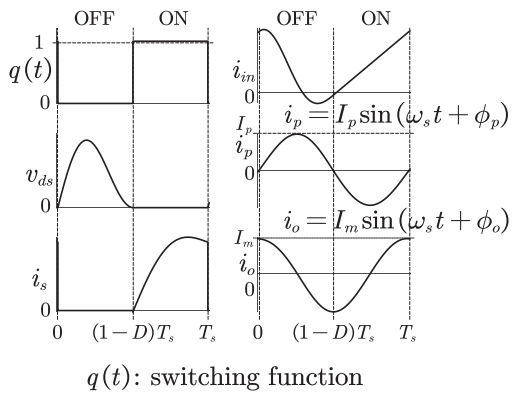

Fig. 2. Operation Waveforms of the circuit in Fig. 1(a) without harmonics.

II. Current Source Realization Based on Thevenin's Equivalent Circuit

A. Topology and Operation

Fig. 1 shows the topology and its equivalent circuit at the switching frequency of the isolated CC class-E inverter. Fig. 2 shows the operation waveforms. When the switch S is ON, the L_{in} is charged. When the switch S is OFF, the L_{in} resonates with C_{in}, and ZVS can be achieved if the switch is turned ON when v_{ds} resonates back to zero; the ratio between this resonant frequency and the switching frequency is denoted as q here. The v_{ds} driving the properly designed load network generates a constant output current at the switching frequency. Under the assumption that the harmonic component of i_p is low enough, the expression of the fundamental component of v_{ds} has revealed that the subcircuit to the left of the dashed line of Fig. 1(a) can be represented by an equivalent voltage source in series with a capacitor at switching frequency, as shown in Fig. 1(b), if the following conditions are satisfied for $D = 0.5$ [4]:

$$1/\sqrt{L_{\text{in}}C_{\text{in}}} = q\omega_s = 1.2915\omega_s \text{ for ZVS} \tag{1}$$

$$\phi_p = 0 \text{ for load} - \text{independence}. \tag{2}$$

Detailed derivation of (1) and (2) can be found in [3]. The realization of (2) can be derived from Fig. 1(b) with Z_{p1} matching the impedance of C_{th}

$$Z_{p1} = j/(\omega_s C_{th}). \tag{3}$$

Since

$$Z_{p1} = j\omega_s L_p - j\frac{1}{\omega_s C_p} + \frac{{\omega_s}^2 M^2}{R_o + j\omega_s L_s - j\frac{1}{\omega_s C_s}}. \tag{4}$$

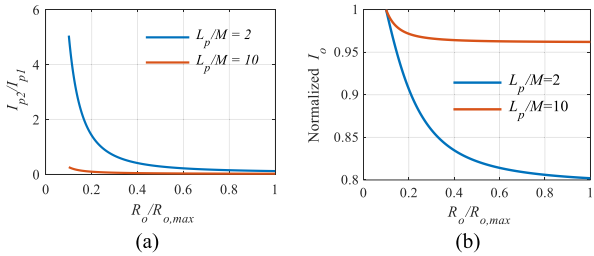

Fig. 3. Impact of L_p on circuit performance. (a) Increased harmonic components at light load when L_p is low. (b) Increased output current variation when L_p is low.

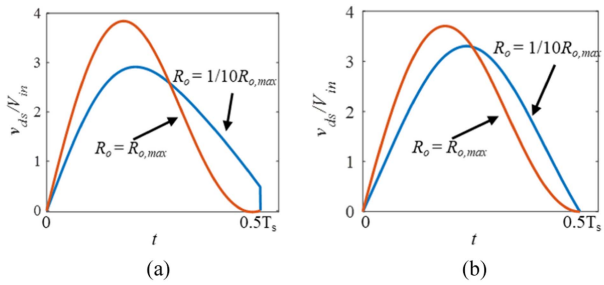

Fig. 4. Impact of L_p on the v_{ds} waveforms during OFF period. (a) Non-ZVS at light load for $L_p/M = 2$. (b) ZVS kept for $L_p/M = 10$.

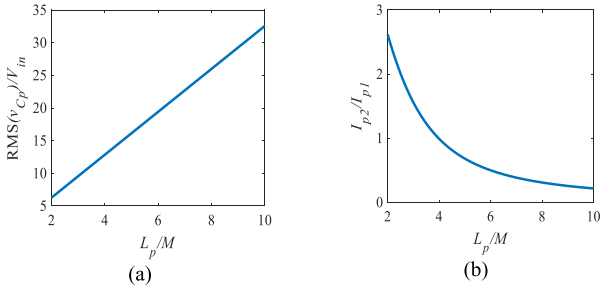

Fig. 5. Tradeoff between voltage stress and harmonic mitigation with L_p selection at 0.8 coupling. (a) Voltage stress increases with L_p. (b) Second Harmonic at 1/10 of full load is mitigated with increased L_P.

Condition (2) can be solved by combining (3) and (4)

$$\omega_s L_s = 1/(\omega_s C_s) \tag{5}$$

$$\omega_s L_p = \frac{1}{\omega_s C_p} + \frac{1}{\omega_s C_{th}}. \tag{6}$$

With the above conditions satisfied, the output current can be calculated as

$$i_{o1} = 1.59 V_{\text{in}} \cos(\omega_s t)/(\omega_s M). \tag{7}$$

Therefore, M can be designed as

$$M = 1.59 V_{\text{in}}/(\omega_s I_m). \tag{8}$$

B. Design of L_{in} for Maximum Load

The design of L_{in} follows the same rule for CV class-E to maintain a constant v_{th1} [4]

$$\sqrt{L_{\text{in}}/C_{\text{in}}} = 0.75 \min[\text{Re}(Z_{p1})]. \tag{9}$$

The required L_{in} can be derived by Combining (1), (4), and (9)

$$L_{\text{in}} = \frac{\omega_s M^2}{0.97 R_{o,\max}} \tag{10}$$

where $R_{o,\max}$ is the load resistance for full load condition.

III. Impact of Harmonics

Similar to CV class-E, the self-inductance L_p needs to be designed to mitigate the harmonics. The working principle of the proposed inverter was explained in Section II based on the assumption that the harmonic components are low enough so only the fundamental component is considered. However, in reality, the harmonics always exist unless L_p is sufficiently large. Therefore, it is important to study the impact of harmonics on the circuit operation and the price it takes for harmonic mitigation.

A. Harmonic Component versus L_p

To address the impact of L_p on the harmonic component, two L_p values are used in the simulation with the same M and 0.8 coupling coefficient. The second harmonic component is then extracted for different load conditions and compared with the fundamental component. Fig. 3 shows the harmonic component variation at different load conditions and L_ps. For $L_p/M = 10$, the second harmonic component is higher than the fundamental for 1/5 of the rated load or lower, making the assumption in Section I no long exist. This also leads to a much larger RMS(I_o) variation at light load as shown in Fig. 3(b).

B. Impact on ZVS

Fig. 4 shows the v_{ds} waveforms at rated load and 1/10 of rated load conditions. With the high harmonic component when $L_p/M = 2$, ZVS on the switch S is also lost at light load.

C. Voltage Stress of C_p

Larger L_p helps mitigate the harmonics to ensure proper operation as discussed in Section III-A and B. However, this also leads to increased impedance thus higher voltage stress. The voltage stress of C_p also increases with L_p as can be seen from the impedance relationship in (6). Fig. 5 illustrates the tradeoff at 0.8 coupling coefficient.

IV. Time-Invariant Multifrequency Analysis

As has been discussed in Section III, there are tradeoffs in the selection of L_p. Larger L_p can help mitigate the harmonics, leading to smaller output current variation over a wider range. However, this leads to higher inductor volume, weight, and loss. The voltage stress on C_p also becomes significantly larger, increasing the capacitor volume and loss. As the value of L_p is directly related to the output current variation over a certain load range, a perfect selection of L_p is the minimum one that results in a desired I_o variation within the required load range, therefore minimizing the voltage stress. In this case, the harmonics cannot be ignored and the equivalent circuit in Fig. 1 cannot be applied.

Time-invariant multifrequency analysis has been used in PWM converters to solve the circuits' steady state. With the QFS representation of state variables and the switching function, the circuit's steady state can be solved with a simple matrix without numerical iteration. Here, in this article, the state-space model is first established. The TIMF model is then derived. Note that circuits with interrupted state variables like the voltage of C_{in} here have not been analyzed with TIMF before. Here, we suggest a way to deal with this interrupted state in the state space model.

A. State-Space Model

The state-space model usually requires solving the ON and OFF intervals separately. To have a continuous and unified state-space mode, the switch S and C_{in} are treated as a single component with its description equations as

$$\begin{cases} v_{ds} = q'(t) v_{C\text{in}} \\ C_{\text{in}} \frac{dv_{C\text{in}}}{dt} = q'(t)(i_{\text{in}} - i_p) \end{cases} \tag{11}$$

where $q'(t) = 1\text{-}q(t)$, so $q'(t) = 1$ when the switch is OFF. A complete state-space model can then be derived as

$$\begin{cases} L_{\text{in}} \frac{di_{\text{in}}}{dt} = V_{\text{in}} - q'(t) v_{C\text{in}} \\ L_p \frac{di_p}{dt} - M \frac{di_o}{dt} = q'(t) v_{C\text{in}} - v_{Cp} \\ M \frac{di_p}{dt} - L_s \frac{di_o}{dt} = v_{Cs} + i_o R_o \\ C_{\text{in}} \frac{dv_{C\text{in}}}{dt} = q'(t)(i_{\text{in}} - i_p) \\ C_p \frac{dv_{Cp}}{dt} = i_p \\ C_s \frac{dv_{Cs}}{dt} = i_o \end{cases}. \tag{12}$$

B. TIMF Model

The key concept of TIMF is to have the QFS representation of state variables as

$$x(t) = x_0(t) + \sum_{n=1}^{N} x_{\alpha n}(t) \cos(n\omega_s t) + x_{\beta n}(t) \sin(n\omega_s t) \tag{13}$$

where ω_s is the angular switching frequency; $x_0(t)$, $x_{\alpha n}(t)$, and $x_{\beta n}(t)$ are the time-dependent QFS coefficients; n is the index term; N is the number of harmonics considered. The QFS representation of the switching function $q'(t)$ is

$$q'(t) = q'_0 + \sum_{n=1}^{N} q'_{\alpha n} \cos(n\omega_s t) + q'_{\beta n} \sin(n\omega_s t). \tag{14}$$

Before applying TIMF to the state-space model, the number of harmonics N needs to be determined first. Here, N is selected to be 3.

By applying the properties derived in [20] to (12), the TIMF model for switching stage is derived as

$$\begin{cases} L_{\text{in}}(-\mathbf{\Omega i_{in}} + \frac{d\mathbf{i_{in}}}{dt}) = \mathbf{V_{in}} - \mathbf{Q'v_{Cin}} \\ L_p(-\mathbf{\Omega i_p} + \frac{d\mathbf{i_p}}{dt}) - M(-\mathbf{\Omega i_o} + \frac{d\mathbf{i_o}}{dt}) = \mathbf{Q'v_{Cin}} - \mathbf{v_{Cp}} \\ M(-\mathbf{\Omega i_p} + \frac{d\mathbf{i_p}}{dt}) - L_s(-\mathbf{\Omega i_o} + \frac{d\mathbf{i_o}}{dt}) = \mathbf{v_{Cs}} + \mathbf{i_o} R_o \\ C_{\text{in}}(-\mathbf{\Omega v_{Cin}} + \frac{d\mathbf{v_{Cin}}}{dt}) = \mathbf{Q'}(\mathbf{i_{in}} - \mathbf{i_p}) \\ C_p(-\mathbf{\Omega v_{Cp}} + \frac{d\mathbf{v_{Cp}}}{dt}) = \mathbf{i_p} \\ C_s(-\mathbf{\Omega v_{Cs}} + \frac{d\mathbf{v_{Cs}}}{dt}) = \mathbf{i_o} \end{cases} \tag{15}$$

TABLE I
ERROR PERCENTAGE OF THE HARMONIC COMPONENTS SOLVED FROM TIMF MODEL COMPARED WITH SIMULATION. THE CIRCUIT PARAMETERS ARE: $V_{\text{IN}} = 10$ V; $L_{\text{IN}} = 185$ NH; $C_{\text{IN}} = 1.78$ NF; $C_{\text{p}} = 792$ PF; $C_{\text{s}} = 2.2$ NF; $L_{\text{p}} = 764$ NH; $L_{\text{s}} = 292$ NH; M = 373 NH; $R_{\text{o}} = 3\ \Omega$ (LIGHT LOAD); AND 30 Ω (FULL LOAD)

	1/10 of full load				Full Load			
Variable	DC	First	Second	Third	DC	First	Second	Third
i_{in}(%)	17.7	1.8	4.3	15.6	0.9	0.3	1.0	17.2
v_{ds}(%)	0	1.9	4.2	15.3	0	0.3	1.1	17.1
i_p(%)	0	2	4.1	15.0	0	1.2	0.9	17.3
i_o(%)	0	1.8	4.2	14.9	0	0	1.0	16.7
$RMS(i_o)$(%)	3.3				0.3			

where bold terms denote vector or matrix. For $N = 3$, $\mathbf{V_{in}}$, $\mathbf{i_{in}}$, $\mathbf{i_p}$, $\mathbf{i_o}$, $\mathbf{v_{Cin}}$, $\mathbf{v_{Cp}}$, and $\mathbf{v_{Cs}}$ are 7×1 column vectors, which consist of time-dependent QFS coefficient (i.e., $\mathbf{x} = [x_0\ x_{\alpha 1}\ x_{\beta 1}\ x_{\alpha 2}\ x_{\beta 2}\ x_{\alpha 3}\ x_{\beta 3}]^T$); Note that $\mathbf{V_{in}}$ only contains dc component as V_{in}. $\mathbf{Q'}$ and Ω are 7×7 matrices:

$$\mathbf{\Omega} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -\omega_s & 0 & 0 & 0 & 0 \\ 0 & \omega_s & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -2\omega_s & 0 & 0 \\ 0 & 0 & 0 & 2\omega_s & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -3\omega_s \\ 0 & 0 & 0 & 0 & 0 & 3\omega_s & 0 \end{bmatrix} \tag{16}$$

$$\mathbf{Q'} = \begin{bmatrix} q'_0 & \mathbf{Q_1}' \\ \mathbf{Q_1}'^T & \mathbf{Q_2}' + \mathbf{Q_2}'^{\boldsymbol{T}} \end{bmatrix} \tag{17}$$

where

$$\mathbf{Q_1}' = \begin{bmatrix} q'_{\alpha 1} & q'_{\beta 1} & q'_{\alpha 2} & q'_{\beta 2} & q'_{\alpha 3} & q'_{\beta 3} \end{bmatrix}$$

$$\mathbf{Q_2}' = \begin{bmatrix} \frac{q'_0}{2} + \frac{q'_{\alpha 2}}{4} & 0 & 0 & 0 & 0 & 0 \\ \frac{q'_{\beta 2}}{2} & \frac{q'_0}{2} - \frac{q'_{\alpha 2}}{4} & 0 & 0 & 0 & 0 \\ \frac{q'_{\alpha 1} + q'_{\alpha 3}}{2} & \frac{q'_{\beta 3} - q'_{\beta 1}}{2} & \frac{q'_0}{2} & 0 & 0 & 0 \\ \frac{q'_{\beta 1} + q'_{\beta 3}}{2} & \frac{q'_{\alpha 1} - q'_{\alpha 3}}{2} & 0 & \frac{q'_0}{2} & 0 & 0 \\ \frac{q'_{\alpha 2}}{2} & -\frac{q'_{\beta 2}}{2} & \frac{q'_{\alpha 1}}{2} & -\frac{q'_{\beta 1}}{2} & \frac{q'_0}{2} & 0 \\ \frac{q'_{\beta 2}}{2} & \frac{q'_{\alpha 2}}{2} & \frac{q'_{\beta 1}}{2} & \frac{q'_{\alpha 1}}{2} & 0 & \frac{q'_0}{2} \end{bmatrix}. \tag{18}$$

C. Steady-State Circuit Model

The TIMF model provides both dynamic and steady-state analysis. The steady-state model can be obtained by letting all derivative terms in (15) be zero. Time-domain waveforms can be recovered via (13) with the solved unknowns from (15). The RMS value of the state variables can be obtained without getting the time-domain waveforms

$$\text{RMS}(x(t)) = \sqrt{\mathbf{x}^T \mathbf{x}/2}. \tag{19}$$

To validate the TIMF mode, an example circuit is analyzed and compared with the simulation. Table I compares the solved harmonic components of the key variables from TIMF with the simulation at full load and light load conditions. The error for harmonic components below third order is within 2% at full load. At light load, the error is within 2% for the fundamental and 5% for the second harmonics. Both cases show higher errors in the third harmonics, which is normal for $N = 3$ [20]. Note that even

TABLE II
PHASE ERROR OF HARMONIC COMPONENTS SOLVED FROM TIMF MODEL COMPARED WITH SIMULATION WITH THE SAME CIRCUIT PARAMETERS

	1/10 of full load			Full Load		
Variable	First	Second	Third	First	Second	Third
i_{in} (degree)	6.8	18.3	13.6	–0.2	0.3	1.4
v_{ds} (degree)	6.8	18.3	13.6	–0.2	0.3	1.4
i_p (degree)	6.8	18.4	13.7	–0.2	0.3	1.4
i_o (degree)	6.8	18.4	13.7	–0.2	0.3	1.4

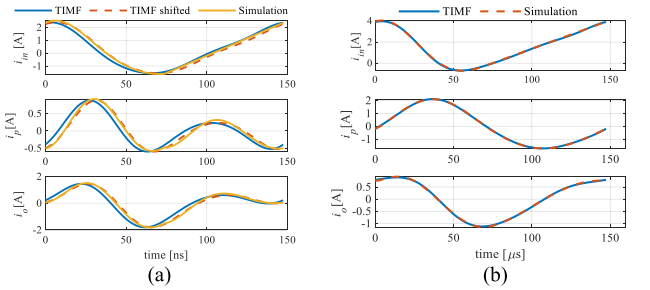

Fig. 6. Reconstructed current waveforms via (13) versus simulation. (a) With significant harmonics at light load. (b) At full load.

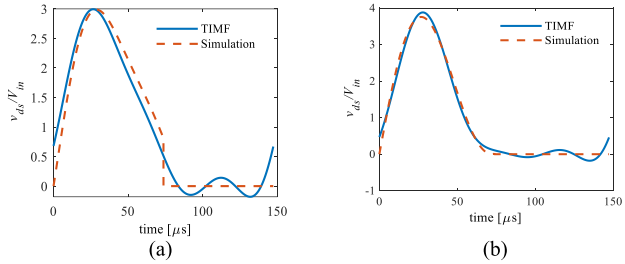

Fig. 7. Reconstructed v_{ds} waveforms via (13). (a) At 1/10 of full load. (b) At full load.

though the errors for the dc component in light load condition and third harmonic components seem to be high, the errors are still within 4% of the total RMS for each state variable. That's because these components are not dominant in the spectrum. Therefore, the calculated RMS of the output current shows less than 3.5% error for both cases. Therefore, $N = 3$ is enough for the analysis of the circuit topology analyzed in this article. Table II gives phase errors of the key state variables. The phase error increases with lighter load conditions. The phase error is the same for all variables listed, suggesting there's a time lead for the TIMF solution at light load.

D. Time Offset at Light Load

Fig. 6 shows the comparison of the reconstructed waveforms via (13). The reconstructed waveforms agree well with the simulation at full load. At light load, all the waveforms lead the simulation by the same amount of time, which has been suggested in Table I. The v_{ds} waveforms cannot be reconstructed with the solution of only up to the third harmonics as indicated in Fig. 7. This has also been described in the analysis of class-E power amplifiers when a limited number of harmonic orders are considered [22]. To avoid making the **Q** matrix size too large, a new way to reconstruct v_{ds} is proposed in this article. Since the

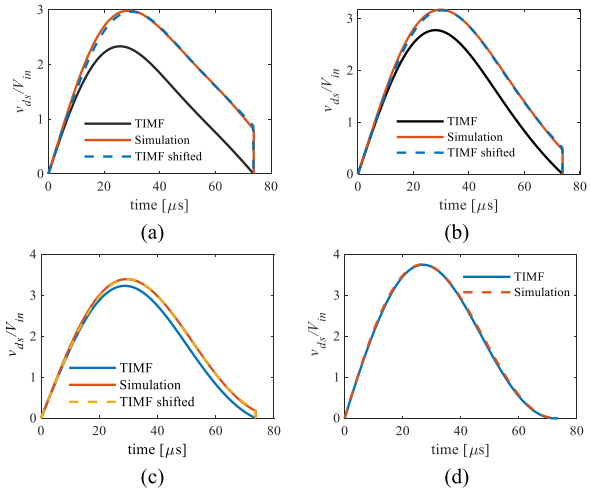

Fig. 8. Reconstructed v_{ds} waveforms via (20). (a) $R_o = 3\ \Omega$. (b) $R_o = 6\ \Omega$. (c) $R_o = 15\ \Omega$. (d) $R_o = 30\ \Omega$.

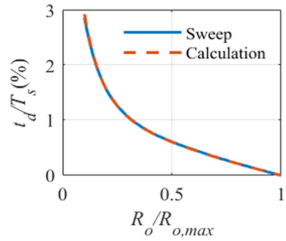

Fig. 9. Required time offset to reconstruct v_{ds} for different load conditions with the same parameters with Table I.

currents i_{in} and i_p agree with the simulation, the v_{ds} during OFF period can be reconstructed as

$$v_{ds} = \int_0^t 1/C_{\text{in}}(i_{\text{in}} - i_p)dt \qquad (0 < t < (1-D)T_s). \quad (20)$$

Fig. 8 shows the reconstructed v_{ds} waveforms via (20) at different load conditions. It agrees well with the simulation results at full load, but shows higher errors as the load becomes lighter. This is because the time lead of i_{in} and i_p as indicated in Fig. 6(a). As this lead varies for different load conditions and different inductances, a function is needed to calculate the right time to delay the solved variables. The criteria used in this article is the volt-second balance of L_{in} as

$$\int_0^{(1-D)T_s} v_{ds}(t - t_d)dt = V_{\text{in}}T_s \quad (21)$$

where t_d is the time offset, which can be obtained by sweeping t_d to satisfy (21). As indicated in Fig. 8(a)–(c), the v_{ds} directly calculated from (20) ($t_d = 0$) does not satisfy (21). Fig. 9 shows the t_d at different load conditions. After applying the currents with t_d time delay to (20), the v_{ds} and the currents all agree well with the simulation as shown in the dashed waveforms in Figs. 6 and 8. With accurate v_{ds} waveforms, the ZVS condition can be predicted without simulation.

To reduce the extra sweeping time required to obtain t_d, a simplified equation is derived for $D = 0.5$. Equation (21) for the

case without time offset is

$$\int_0^{0.5T_s} v_{ds}(t)dt = \frac{i_{\text{in}0}}{2C_{\text{in}}}(0.5T_s)^2 + \frac{0.5T_s}{\omega_s C_{\text{in}}} \times \left[(i_{\text{in}\beta 1} - i_{p\beta 1}) + \frac{(i_{\text{in}\beta 2} - i_{p\beta 2})}{2} + \frac{(i_{\text{in}\beta 3} - i_{p\beta 3})}{3}\right] + \frac{1}{{\omega_s}^2 C_{\text{in}}}\left[2(i_{\text{in}\alpha 1} - i_{p\alpha 1}) + \frac{2(i_{\text{in}\alpha 3} - i_{p\alpha 3})}{9}\right]. \quad (22)$$

When there is a time offset, considering t_d is usually small so $\sin(\omega_s t_d) \approx \omega_s t_d$ and $\cos(\omega_s t_d) \approx 1$, (22) can be written as (with third harmonic ignored)

$$\int_0^{0.5T_s} v_{ds}(t - t_d)dt \approx \int_0^{0.5T_s} v_{ds}(t)dt + \frac{0.5T_s t_d}{C_{\text{in}}} (i_{\text{in}\alpha 1} - i_{p\alpha 1} + i_{\text{in}\alpha 2} - i_{p\alpha 2}) + \frac{t_d}{\omega_s C_{\text{in}}}(2i_{\text{in}p1} - 2i_{\text{in}\beta 1}). \quad (23)$$

The difference between (22) and (23) is used to calculate t_d

$$t_d = \frac{\left(V_{\text{in}}T_s - \int_0^{0.5T_s} v_{ds}(t)dt\right) C_{\text{in}}}{0.5T_s(i_{\text{in}\alpha 1} - i_{p\alpha 1} + i_{\text{in}\alpha 2} - i_{p\alpha 2}) + 2(i_{\text{in}p1} - i_{\text{in}\beta 1})/\omega_s}. \quad (24)$$

Note that the integral term in (24) is obtained through (22) instead of using numerical method. The calculated t_d using (24) is shown with the dashed curve in Fig. 9. A good agreement can be observed when compared to the results from sweeping t_d.

Further study has revealed that such time offset can occur at full load (high-Q) conditions as well if ZVS is not realized due to improper parameter design. This is because TIMF is a continuous model so it cannot deal with the step change of voltage when there's non-ZVS. Therefore, the calculated t_d is a possible indication of non-ZVS and how high the turn-ON voltage is.

E. Summary of TIMF Modeling for Class-E Inverters

The proposed TIMF modeling can be summarized with a multi-variable function as

$$\mathbf{AX} = \mathbf{C} \quad (25)$$

where

$$\mathbf{A} = \begin{bmatrix} -L_{in}\boldsymbol{\Omega} & \mathbf{0} & \mathbf{0} & \mathbf{Q}' & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & -L_p\boldsymbol{\Omega} & M\boldsymbol{\Omega} & -\mathbf{Q}' & \mathbf{I} & 0 \\ \mathbf{0} & -M\boldsymbol{\Omega} & L_s\boldsymbol{\Omega} - \mathbf{I}R_o & \mathbf{0} & \mathbf{0} & -\mathbf{I} \\ -\mathbf{Q}' & \mathbf{Q}' & \mathbf{0} & -C_{in}\boldsymbol{\Omega} & \mathbf{0} & 0 \\ \mathbf{0} & -\mathbf{I} & \mathbf{0} & \mathbf{0} & -C_p\boldsymbol{\Omega} & 0 \\ \mathbf{0} & \mathbf{0} & -\mathbf{I} & \mathbf{0} & \mathbf{0} & -C_s\Omega \end{bmatrix} \quad (26)$$

$$\mathbf{X} = \begin{bmatrix} \mathbf{i_{in}} & \mathbf{i_p} & \mathbf{i_o} & \mathbf{v_{C_{in}}} & \mathbf{v_{Cp}} & \mathbf{v_{Cs}} \end{bmatrix}^T \quad (27)$$

$$\mathbf{C} = \begin{bmatrix} \mathbf{V_{in}} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \end{bmatrix}^T. \quad (28)$$

Note that $\mathbf{I}$ and $\mathbf{0}$ represent unit and zero matrices. $\mathbf{C}$ is a column vector where only the first element is non-zero as V_{in}.

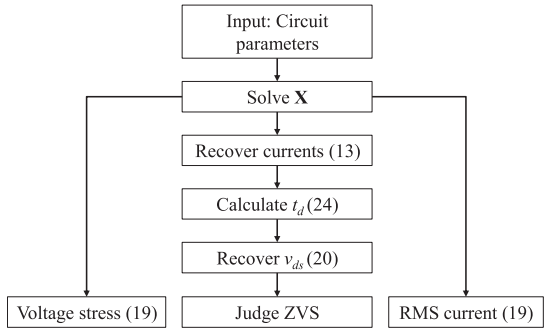

Fig. 10. Flow chart to use TIMF to assist with circuit design.

$\mathbf{X}$ is the column vector combining the harmonic components of all state variables. It can be solved as

$$\mathbf{X} = V_{in}\mathbf{A}_1 \quad (29)$$

where $\mathbf{A_1}$ is the first column of $\mathbf{A}^{-1}$. The TIMF modeling for the CC class-E inverter can be summarized as (29). Further steps can be applied to assist with the design as shown in the flow chart in Fig. 10. After solving the harmonic components, the RMS current and voltage stress can be further calculated. If ZVS needs to be confirmed, the v_{ds} can also be recovered via (20) after applying the calculated t_d offset from (20) to i_{in} and i_p. Note that even though the time offset is not needed when ZVS is achieved, the t_d will be naturally calculated as zero then, so no extra effort is needed.

V. Design of Inductances for Desired Load Range

As a current source ZVS inverter, the performance is evaluated by its working load range to keep a constant output current and minimal switching loss. However, an output current with zero variation and zero voltage at turn-ON for all load conditions only exists theoretically with the first harmonic analysis. In [19], the CV class-E inverter is proposed to be designed for quasi-ZVS to give more freedom for the circuit design while maintaining a low switching loss. For example, the lack of ZVS in Fig. 8(a) incurs an additional loss of 5% of full power. The goal of the design methodology discussed now is to reduce the 5% to below 0.1% enjoyed by the quasi-ZVS waveform in Fig. 8(c). Similarly in this article, inequality instead of equality is used as the design criteria for constant output current and minimal switching loss

$$\begin{cases} |\text{RMS}[i_o(R_{o,\min})]/\text{RMS}[i_o(R_{o,\max})] - 1| < \sigma_1 \\ v_{ds}(0.5T_s)/V_{\text{in}} < \sigma_2 \end{cases} \quad (30)$$

where σ_1 and σ_2 are based on the application requirements. The load range is then defined as $R_{o,\max}/R_{o,\min}$.

As stated at the beginning of Section IV, the purpose of this article is to quantify the inductances needed for a desired load range while satisfying (30), which may vary for different applications, from 15:1 [10] to 2:1 [23]. The required inductances at different coupling coefficients and the resulting voltage stress will be quantified.

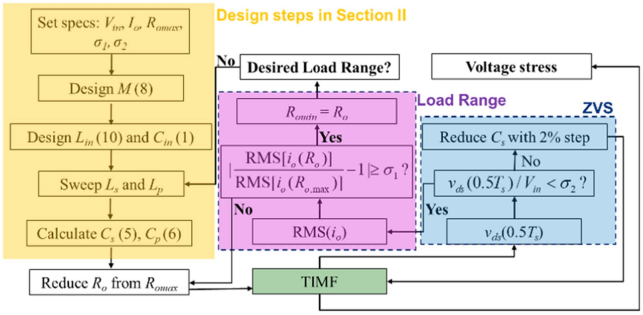

Fig. 11. Parameter sweeping process with proposed design criteria in (30).

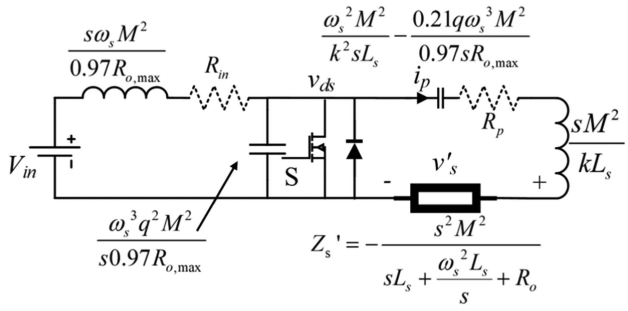

Fig. 12. Laplace transformation of circuits in Fig. 1(a) by applying (1)–(10).

TABLE III
TWO DESIGN EXAMPLES WITH THE DESIGN PROCESS IN FIG. 11

	Case 1	Case 2
L_p (nH)	764	2000
L_s (nH)	292	193
C_p (pF)	772	283
C_s (nF)	1.94 (calculation)→1.75	2.85 (calculation)
$R_{o,\min}$ (Ω)	11.9	4.5
RMS(v_{C1})/V_{in}	4.6	12.3
Load Range	2.8:1	7.3:1

A. Design Process for Desired Load Range

Different from the design steps proposed in Section II where only the fundamental component is considered, the criteria in (30) requires a new design procedure to obtain a specific load range. Fig. 11 shows the proposed design procedure to obtain the design for the desired load range. The design of M, L_{in}, and C_{in} still follows the equations in Section II. The L_p and L_s are then swept to quantify the load range and voltage stress of C_p. For each L_p and L_s value set, the C_p is still calculated with (6). The secondary resonant capacitor C_s is first calculated via (5), but may need to be reduced to make Z_{p1} more inductive if the original value cannot guarantee quasi-ZVS within the load range, especially for small load range cases where there are higher harmonic components. The load range for each set of L_p and L_s is obtained by reducing R_o from $R_{o,\max}$, and calculating the difference of RMS(I_o) from $R_{o,\max}$ with the help of the TIMF analysis until the σ_1 threshold is reached. By sweeping L_p and L_s values and repeating the process in the load range box, the required inductances for the desired load range can be obtained.

A MATLAB code was developed with the logic in Fig. 11. Table III gives two cases with different load ranges. The V_{in}, L_{in}, C_{in}, and M are the same as Table I, which provides 0.707 Arms output current for $R_{o,\max} = 33\ \Omega$. Here, σ_1 and σ_2 are set as 5%. For case 1 with a relatively smaller L_p, the load range is only to 2.8:1. The calculated C_s from (6) cannot guarantee quasi-ZVS from the TIMF result. Instead, it was reduced to the value shown in the table. For case 2 where the L_p is increased, the load range is increased to 7.3:1. All the equations in Section I can be utilized for the circuit design. There's no need to revise C_s to achieve quasi-ZVS. With the increased load range from case 1 to case 2, a significant increase in the voltage stress of C_p is displayed, which leads to increased volume and loss. Therefore, the circuit needs to be designed with the exact desired load range to minimize such voltage stress.

B. Design of the Coupled Inductors

To guide the coupled inductors design, load range is obtained for different L_p and L_s values with the sweeping process in Fig. 12. Normalization of the inductances is proposed for the results to be utilized generally.

Fig. 12 shows the circuits in Fig. 1(a) in Laplace domain by applying (1)–(10). Here, k is the coupling coefficient

$$k = M/\sqrt{L_p L_s}. \tag{31}$$

The secondary side is reflected to the primary side as the impedance Z_s'. The relationship between v_s' and i_o is

$$I_o(s) = -V'_s(s)/(sM). \tag{32}$$

Note that for steady-state analysis using TIMF, s = $nj\omega_s$ (n = 12,3,…). Observation of all the impedances reveals a common term as $\omega_s{}^2M^2$, which is determined by the required current gain according to (8). It can also be found that when $\omega_s L_s/R_{o,\max}$, and k are fixed, the change of the other variables leads to the same proportion of variation across all the impedances in Fig. 11, which results in the same voltage solution on each impedance. Therefore, a conclusion can be made that specific $\omega_s L_s/R_{o,\max}$, and k will cause the same I_o variation for the same $R_o/R_{o,\max}$, hence the same load range. In this case, $\omega_s L_s/R_{o,\max}$ and k are used here as the two characteristic variables for the load range design. L_p is not used here since its dependent on M, L_s, and k as shown in (31).

Fig. 13 shows a load range contour and RMS(v_{C1})/V_{in} contour as a function a $\omega_s L_s/R_{o,\max}$ and k when $\sigma_1 = \sigma_2 = 5\%$. Load range is increased by reducing L_s or k. As discussed in previous subsection, C_s needs to be reduced from the calculation result for ZVS at certain inductances. The boundary is drawn as the red dotted line to the right of which C_s needs to be reduced at a small load range. From RMS(v_{C1})/V_{in} contour, the voltage stress of C_p is seen increasing with the load range. Note that the load range is greatly increased when k is below 0.5 even when L_s is relatively large, which leads to smaller voltage stress. Therefore, reducing k is a preferable way from the aspect of voltage stress. However, reducing L_s or k leads to increased L_p, which always results in the loss and size increase. Here the load range contour is plotted only to 30:1 because it's difficult to realize a wider

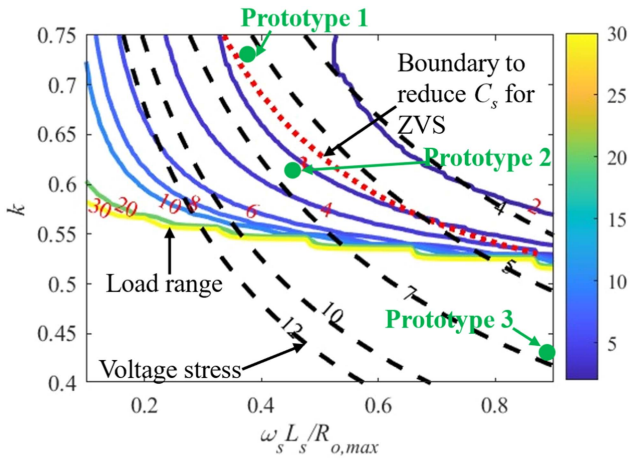

Fig. 13. Load range and voltage stress contour as a function of k and L_s. The solid lines are the load range contour. The dashed lines are the voltage stress contour. The dotted line is the boundary to the right of which C_s needs to be reduced to realize ZVS.

range in real cases considering the impact of ESRs, which will be discussed right after.

C. Design Process for $\sigma_1 = \sigma_2 = 5\%$

The design procedure in Fig. 11 provides a general approach to obtain the circuit parameter for specific load range and voltage stress. When $\sigma_1 = \sigma_2 = 5\%$, the design process can be simplified with the help of Fig. 13, which provides the selection for k and L_s based on the intersection of the desired load range contour and voltage stress contour. Therefore, now the design process for this special case can be simplified to the yellow box in Fig. 11, the only difference is that L_s and k are selected as the intersection of the two contours from Fig. 13, which then also determines L_p based on (31).

D. Impact of ESRs

As shown in Fig. 12, ESRs on the primary side, i.e., R_p can lead to voltage divider effect and reduce v_s', which then reduces the output current at heavy load. The secondary ESR can be absorbed into R_o so the impact on the output current is relatively small. The conduction loss of the switch and capacitor is smaller compared to the magnetic losses, especially at multi-MHz switching [5], [24], [25]. Therefore, the impact of the switch's ON-resistance and ESR of C_{in} is not studied here.

The impact of the ESRs is studied by adding R_{in} (ESR of L_{in}) and R_p (combined ESR of L_p and C_p) to the TIMF model and analyzing the extra variation percentage of RMS(I_o) at $R_{o,\min}$, on top of the 5% variation defined by σ_2. Fig. 14 shows the extra percentage at $R_{o,\min}$ for load range as 2:1 and 10:1. The ESRs are divided by the reflected secondary impedance at switching frequency, $\omega_s{}^2M^2/R_{o,\max}$, for normalization purposes. A larger variation of RMS(I_o) can be observed at wider load range.

VI. Experimental Verification

To verify the results in the previous section, three prototypes were built with different load ranges. The switching frequency

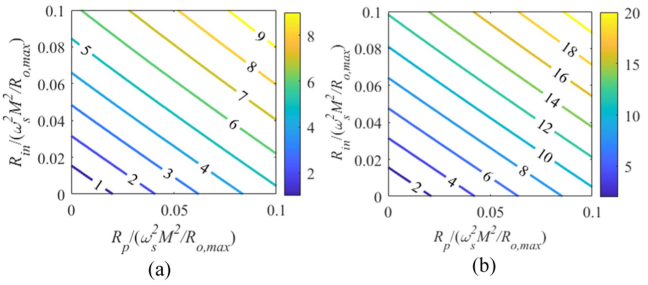

Fig. 14. Extra variation percentage of RMS(I_o) at $R_{o,\min}$ defined by the load range as (a) 2:1 and (b) 10:1 for $\sigma_2 = 5\%$.

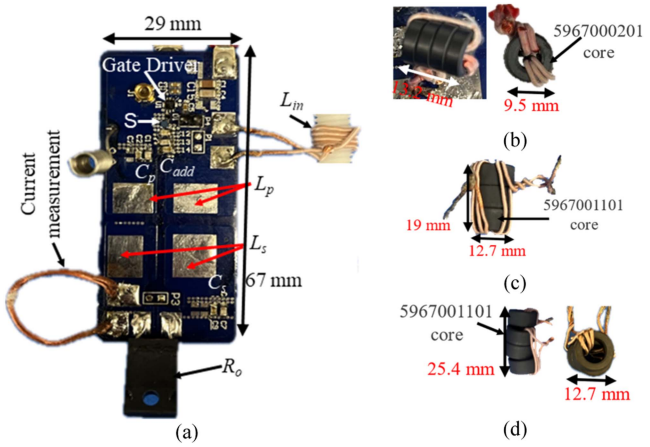

Fig. 15. Prototyped hardware. (a) PCB with the same L_{in} and C_{in}. (b)–(d) Coupled inductors for prototypes 1–3.

TABLE IV
Parameters of the Three Prototypes for Experimental Verification

	Prototype 1	Prototype 2	Prototype 3
V_{in} (V)	10		
f_s (MHz)	6.78		
L_{in} (nH)	170		
C_{in} (nF)	1.79		
C_{add} (nF)	1.59		
L_p (nH)	795 (3 turns)	936 (3 turns)	938 (3 turns)
L_s (nH)	413 (2 turns)	493 (2 turns)	1013 (3 turns)
k	0.73	0.62	0.43
C_p (pF)	740	625	625
C_s (nF)	1.2	1.1	0.54
$R_{o,\max}$ (Ω)	47	47	47

is 6.78 MHz and the duty ratio is 0.5. Table IV gives the parameters of the tested circuits. Although the switch's output capacitance C_{oss} was not discussed in Section IV and V owing to the linearity assumption underlying TIMF, it was accounted for in the hardware by subtracting the 200 pF of C_{oss} from C_{in} to arrive at C_{add} in Table IV. This proves to be effective when C_{in} is much larger than C_{oss} in [5] and [19], and in the v_{ds} waveforms in Fig. 17. When such assumption is not satisfied, [26] is available to consider the nonlinearity of C_{oss} in the design by introducing the C-V relationship in the state equations. The RMS(I_o) is designed at 0.6 A. The $R_{o,\max}$ is 47 Ω for a 16 W maximum output power. Fig. 15 shows the hardware and the three sets of coupled inductors. Ferrite 67 cores from Fair-rite are used. Litz 22/450/48 (equivalent AWG 22 wire constructed

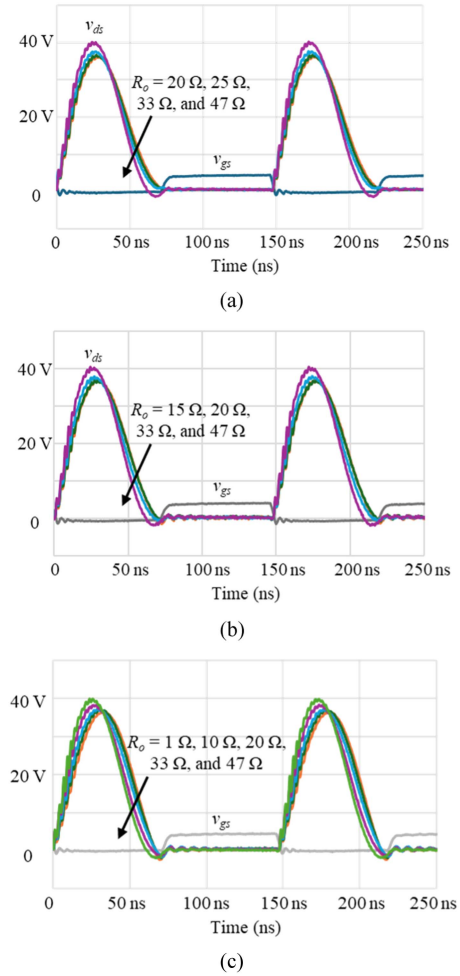

Fig. 16. ZVS achieved as shown in all measured v_{ds} waveforms of the three prototypes in Table IV. (a) Prototype 1. (b) Prototype 2. (c) Prototype 3.

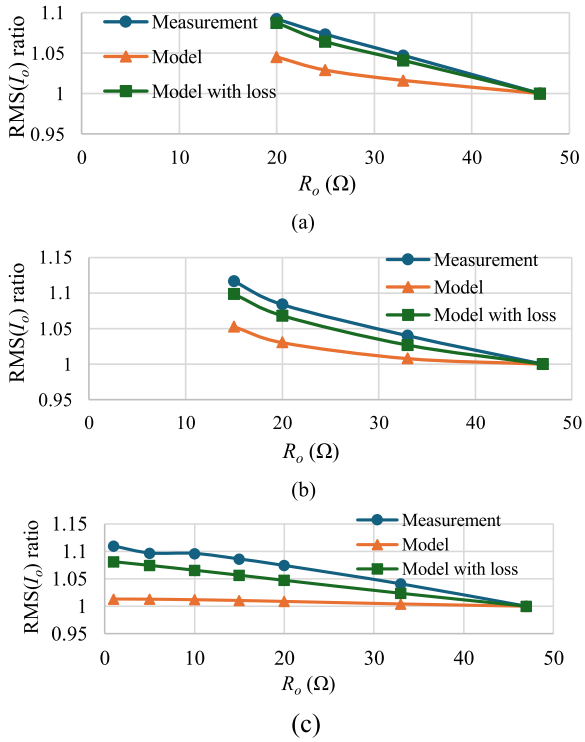

Fig. 17. RMS(I_o) variation with load resistance for the three prototypes. (a) Prototype 1. (b) Prototype 2. (c) Prototype 3.

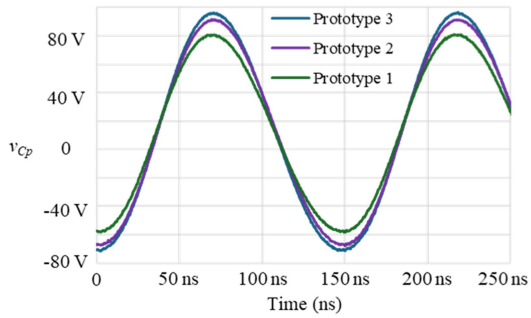

Fig. 18. Measured voltage waveforms of C_p.

by 450 strands of AWG 48 wire) from New England wire is used for the windings. Prototype 1 utilized 4 paralleled smaller cores compared to prototypes 2 and 3. For prototype 3, each of the primary and secondary windings are wrapped on three paralleled cores among which two cores are shared by L_p and L_s to realize a coupling coefficient as low as 0.43. The same PCB board is used in the three prototypes, with the same L_{in}, C_{in}, and $R_{o,\max}$. A Litz wire loop is formed at the secondary side for the measurement of i_o with the current probe TCP0030A. A 30 nH inductance introduced by this loop is counted towards L_s. To measure the efficiency, the Agilent 34405A multimeter (51/2 digits) is used to measure the input voltage and current. The output power is calculated as RMS$(i_o)^2 R_o$.

Fig. 16 shows the measured v_{ds} waveforms of the three prototypes. ZVS is achieved for all load conditions within the tested load range. Fig. 17 shows the RMS(I_o) variation with the varying load resistance for the three prototypes. The RMS(I_o) is normalized based on the value at full load. The load range increases from protypes 1–3 as predicted in Fig. 13. For prototypes 1 and 2, the load resistance is varied within the range that's defined by the 5% RMS(I_o) variation theoretically. However, a 10% variation is observed from the measurement. To justify the impact from ESRs, another curve is plotted by adding the R_{in} and R_p to the model. For the three prototypes, the same air-core inductor L_{in} is used with the measured ESR (R_{in}) as 80 mΩ. The calculation of R_p includes the winding and core loss of L_p, and the ESR of C_p. The estimated R_p for the three prototypes are 0.3, 0.4, and 0.45 Ω, respectively. By considering the ESRs, the output current variation provided by the model is similar to the measurement. Specifically for prototype 3, even though the RMS(I_o) only varies about 1% within 47:1 load range theoretically due to the low coupling, the variation is about 10% in the measurement, which implies that the load range is mainly determined by the ESR instead of the inductance in this case. With the ESR considered, a 5% variation is still observed from 1–30 Ω load resistance, delivering a 30:1 load range.

Fig. 18 shows the voltage stress of C_p. The voltage stress increases slightly from prototype 1 to prototype 3, which agrees

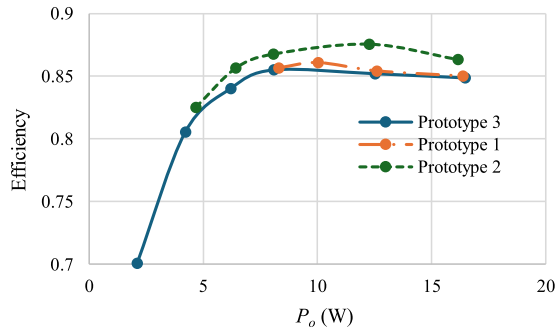

Fig. 19. Measured efficiency of the three prototypes.

with the prediction in Fig. 12. The RMS(v_{Cp}) for the three prototypes are $5V_{\text{in}}$, $5.7V_{\text{in}}$, and $6V_{\text{in}}$, respectively.

The efficiency of the three prototypes is measured as shown in Fig. 19. Gate driving loss at 6.78 MHz is measured as 0.3 W, which is included in the efficiency measurement. The efficiencies of prototypes 1 and 2 are slightly higher than prototype 3 due to their relatively lower inductances and smaller number or size of cores. A peak 87% efficiency is achieved on prototype 2.

VII. Conclusion

The analyzed isolated CC class-E inverter achieves a constant load current when harmonics are neglected. However, harmonic mitigation via increasing L_p leads to increased voltage stress. The TIMF model is used to solve the steady-state solutions considering the harmonics. The switch and its paralleled shunt capacitor are modeled as a single component to treat the discontinuous state of the capacitor. The proposed model provides accurate fundamental and second harmonic solutions, leading to a precise RMS calculation of the load current and voltage stress. In addition, the recovery of time-domain v_{ds} waveform is achieved with the proposed equation to calculate the time offset of TIMF solution at light load. The proposed TIMF-assisted design methodology provides a guideline of the coupled inductors design for the desired load range and voltage stress with two normalized characteristic parameters for generalization. For designs with theoretically wide load ranges, the ESRs may become the determining factor in the real case. The theory was validated with three prototypes with different load ranges. The measured load current variation within the predicted load ranges agrees well with the theory when ESRs are considered. A maximum 47:1/30:1 load range for 10%/5% output current variation was achieved.

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