An Online-Optimized ZVS-Current Tracked Soft-Switching Modulation for Triple Active Bridge Converter

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***Abstract*—This article presents the synthesis and implementation of a switching-network loss-reduced, soft-switching-enabled PWM modulation scheme for an isolated bidirectional triple-active bridge (TAB) dc–dc converter that dynamically varies the five phase-duty control variables. Due to the power coupling among each TAB port, circuit analysis of TAB's operational modes becomes complex, posing a challenge to implementing a computationally intensive PWM strategy derived from the established frequency domain-based circuit analysis approach. In this work, we first develop the time-domain analytical model of the TAB converter, drawing on the working principles of the dual active bridge (DAB) converter and the linear superposition theorem. This model simplifies the calculation of switching transient currents in a TAB converter, which significantly influences soft-switching operation and overall switching loss in the high-frequency H-bridges. Second, a rigorous effort is made to decipher the zero-voltage-switching (ZVS) process of the TAB converter considering the influence of voltage-dependent junction capacitances, and the critical ZVS current requirements are correctly identified. Using the proposed TAB circuit model, associated loss models, and identified ZVS criteria, the design optimization of the TAB port inductances is further carried out. Subsequently, we propose a simplified penta-phase shift modulation scheme for the TAB converter, ensuring the soft-switching of the H-bridges. This proposed modulation solution is easier to implement, computationally stress-free, features all-ZVS, and exhibits low switching and conduction loss characteristics. The proposed modulation solution is also implemented, validated, and benchmarked in a 2.4-kW/100-kHz GaN-based TAB converter proof-of-concept, tailored for space power supply applications. The converter achieves a peak efficiency of 96.8%, and its average efficiency at 20% loading condition is benchmarked at 94.82%, representing a ∼4% improvement over the traditional phase-shift modulation-operated TAB.**

***Index Terms*—Efficiency optimization, soft-switching modulation, triple-active bridge (TAB), zero-voltage-switching (ZVS) strategy.**

I. Introduction

TO address the adverse environmental impact of fossil fuel consumption, the urgent imperative is to advance renewable energy usage. Within renewable energy systems, the essential requirement for energy storage equipment arises to meet load demands with more stable, reliable, and swift response [1], [2]. Traditional solutions, employing numerous independent two-port converters, are encumbered by inherent limitations of bulky, costly, inefficient multistage power conversion systems diminishing the lifespan of energy storage elements.

In contrast to various two-port converters, multiport converters (MPCs) have emerged as promising solutions in versatile energy management systems, offering a straightforward converter architecture with fewer power switches and passive components, facilitating miniaturization, integration, and higher power density [2]. Among various MPC architectures, the triple-active bridge (TAB) converter [3], illustrated in Fig. 1, stands out as a representative design that is a multiport network with three H-bridges connected via a high-frequency (HF) multiwinding transformer. This converter finds broad applications in electric vehicles (EVs) [4], [5], [6], fuel cell vehicles [7], and dc microgrids [8], among other domains.

Derived from the dual-active bridge (DAB) converter family [9], [10], [11], the TAB converter exchanges power between its ports by varying their relative phase shifts, resulting in different control strategies for various phase shift dimensions. The basic

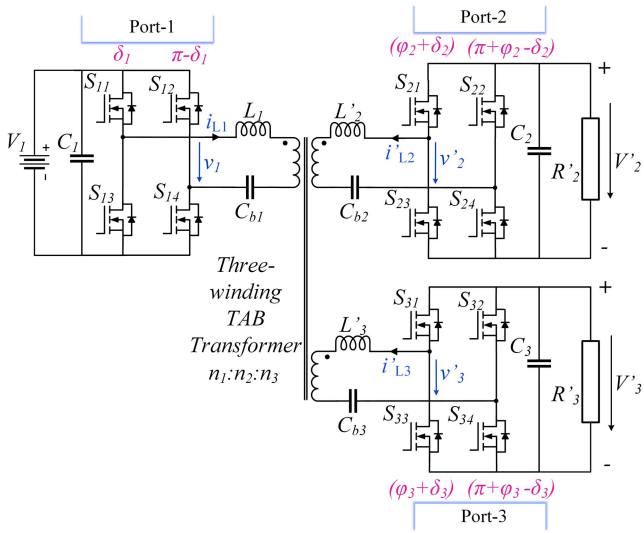

Fig. 1. TAB converter topology and phase shifts of the individual half-bridge gating signals.

Manuscript received 9 February 2024; revised 6 May 2024; accepted 13 July 2024. Date of publication 16 July 2024; date of current version 11 September 2024. Recommended for publication by Associate Editor M. Chen. *(Corresponding author: Ayan Mallik.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3429278.

Digital Object Identifier 10.1109/TPEL.2024.3429278

TAB modulation that uses 50% duty cycles on all three H-bridge voltages and simply modulates the phase-shifts between the bridge voltages to transfer power between the ports, is called dual-phase-shift (DPS) [12], [13] or phase-shift-modulation [4], [5]. However, when operating in light load or/and nonunity voltage gain conditions with mismatched port voltages, the TAB converter under the DPS scheme suffers from high conduction and switching losses due to higher circulating currents and switching peak currents with loss of soft-switching, respectively. In order to cater to the above-mentioned drawbacks, some higher dimension modulation schemes where the duty cycles of the bridge voltages are actively controlled alongside the inter-port phase shifts, are studied and presented in some recent research works [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25]. Works presented in [12], [13], [14], [15], [16], [17], [18], [20], [21], [22], [23], [24], and [25] adopt a five variable-based TAB control system that includes all the inner and intra phase-shift angles of the individual TAB ports, which is named as penta-phase-shift (PPS) modulation in [12] and [13]. Such a modulation scheme possesses the highest control dimension and the other control strategies with fewer dimensions can be regarded as its special form. Although the PPS modulation provides the maximum control flexibility, it comes at the cost of additional computational complexity and difficulty in implementation in the digital controller environment. With a target to minimize the circulating current, the PPS modulation introduced in [14] computes the inter-port phase-shift values on the basis of a fundamental harmonic approximation (FHA) oriented analysis of the TAB converter. FHA misses out on most of the insights into the shape of the switching current waveshape that is critical to accurately correlate the switching and conduction losses in the bridges with the phase/duty control variables and thus results in a nonoptimal point converter operation. To address this issue, a few works in [12], [13], [15], [18], and [21] adopt a generalized harmonic approximation (GHA) based frequency domain analysis of the TAB's port voltage and current waveshapes that results in accurate formulation of the winding current RMSs and switching current peaks, required to quantify the conduction and switching losses in the bridges. Using this GHA-based TAB model, a conduction loss optimized PPS modulation is presented in [12]. However, it does not take into account switching losses, a dominant component, especially at lighter loads, attributed to the absence of soft-switching.

The investigation of the zero-voltage-switching (ZVS) process in TAB converters has been explored in some recent studies [13], [15], [18], [19], [26] that emphasize the significance of achieving soft-switching across a broad range of gain and load conditions to enhance converter efficiency. Existing works often simplify the TAB converter to a two-port topology using Thevenin theorem. They categorize the ZVS process into three [13] or four [15] types, aiming to identify ZVS conditions based on factors such as the switching device's junction capacitance C_{oss}, switching instant current, and TAB port voltages. However, the studies in [13] and [15] overlook the nonlinear behavior of C_{oss}, leading to potential inaccuracies in identified ZVS current requirements and suboptimal compensation of the phase-shift angles. Another attempt to consolidate ZVS conditions for a TAB is presented in [18], where C_{oss} is modeled as a nonlinear function of the drain-source voltage v_{DS}. Nevertheless, none of the ZVS-related studies on the TAB converter compute the critical deadtime required for ZVS events. Furthermore, despite the proven superiority of charge-based ZVS analysis over energy and current-based approaches for DAB converters, especially under light load conditions [27], [28], [29], such an approach has not been adopted for the ZVS analysis of TAB converters.

Furthermore, while the existing research works aim to offer an optimized TAB modulation scheme for minimizing conduction and switching losses in the power devices, the design-level optimization of the HF switching network, including the HF TAB Port inductors, is notably absent in the current literature. It is important to highlight that, in addition to optimizing the modulation scheme, the judicious selection of line inductors is crucial for achieving globally optimal power conversion efficiency with wide ZVS range.

Another challenging issue in the state-of-the-art TAB converter research [19], [24] is the difficulty of digital microcontroller-based implementation of the loss optimal PPS modulation scheme. The existing approaches for modulating the TAB control variables in a hardware setup are categorized and described below.

1) *Look-up table (LUT)-based calculation:* The works outlined in [13], [14], [17], and [18] initially identify the optimal TAB modulation variables offline through a multivariable loss optimization framework developed using either GHA [13], [18] or FHA [14], [17]-based TAB converter models. Subsequently, these values are stored for each load and gain condition in a LUT within the controller. However, this process introduces challenges related to memory allocation on the microcontroller based on the size of the LUT.
2) *Polynomial regression fitted control variable model derived calculation:* Another way of attaining the optimal PPS control variables is to derive mathematical models of the TAB duty variables as polynomial functions of the port voltages and operating loads [31], [32] (from GHA-based TAB model) and input that expression into the digital controller. However, such expressions are often computationally intensive, and their outcomes may not precisely match the optimal control variable values in practice. This discrepancy can result in a loss of soft-switching or higher loss operation.
3) *Artificial neural network (ANN) model-based calculation:* Some recent studies [20], [24], [37], [38] have adopted this approach, training an ANN model using extensive datasets derived from hardware or software simulation tools in order to attain optimized phase compensations for specific converter operating conditions. Although such control methods can incorporate the effects of circuit nonidealities in optimal operating point synthesis, this process is time-intensive, requiring a specialized and cost-intensive hardware interface for executing the ANN, and it focuses solely on RMS current optimization.
4) *On-line Calculation:* Dey and Mallik [12] targeted minimal conduction loss operation in the TAB converter,

deriving optimal real-time solutions through a gradient descent search algorithm. Similarly, Ibrahim et al. [23] proposed a multidimensional ripple correlation methodology to iteratively identify the winding RMS current-optimized operating point. Although on-line calculation was achieved in [12] and [23], the iterative algorithm presented computational challenges, limiting its broader applicability. In addition, Gong et al. [19] introduced a simplified four-variable-based soft-switched modulation scheme that is easily implementable in a digital environment. However, this work involves reducing the magnetizing inductance of the transformer to achieve soft-switching at the expense of higher conduction loss.

It is clear from the above-mentioned drawbacks that a simplified, online computable, and efficient multivariable control strategy is needed that can minimize the overall system loss in a TAB dc–dc converter while maintaining soft-switching under all output voltage gain and loading conditions. Keeping the identified research gaps in mind, in this article, the authors intend to develop and employ a PPS modulation technique that can compute the control variables online based on the converter's operating conditions while ensuring a switching loss minimized all-ZVS converter operation. Such a modulation scheme is derived from a mathematically synthesized time-domain oriented model of a TAB converter model and its identified ZVS criteria. The TAB converter in this study is designed with power ratings of 2400, 1600, and 800 W at port-1, port-2, and port-3, respectively. Port-1, designated as the input port, operates at a dc voltage level of 160 V. On the other hand, the output ports, namely port-2 and port-3, have varied dc bus voltage levels, ranging from 100 to 130 V and 16 to 28 V, respectively. These voltage specifications align with the standard voltage levels employed in NASA space shuttles [30].

The key contributions of this work can be summarized as follows.

a) A time-domain analysis of the TAB converter is carried out from the proposed modeling approach that utilizes the superposition theorem applied on three fundamental DAB cells constructing the complete TAB converter. This novel approach enables the precise quantification of peak switching transient currents, a pivotal factor in determining ZVS. Notably, this method obviates the need for computationally intensive higher order harmonic inclusive GHA-oriented analysis [13], [18].

b) The ZVS process in a TAB converter is revisited, utilizing a current-commutated stored charge-based methodology for accurately identifying the critical ZVS conditions, considering the nonlinear characteristics of the output capacitances of power devices.

c) A ZVS transition-informed switching loss model for the TAB converter is synthesized using the time-domain TAB model. In addition, a mathematical framework for switching loss optimization is developed, resulting in the optimal selection of TAB port inductances for rated converter voltages and loads. This marks a significant advancement in the design optimization of a TAB converter for a specific rating, by enhancing its ZVS range and overall efficiency under any control scheme.

d) Leveraging the developed time-domain TAB model and charge-based ZVS conditions, an online computable five-variable PPS control scheme is proposed. This scheme ensures all-ZVS operation of the TAB converter under varying load and gain conditions, while mitigating challenges associated with memory allocation and computational demands on the digital controller.

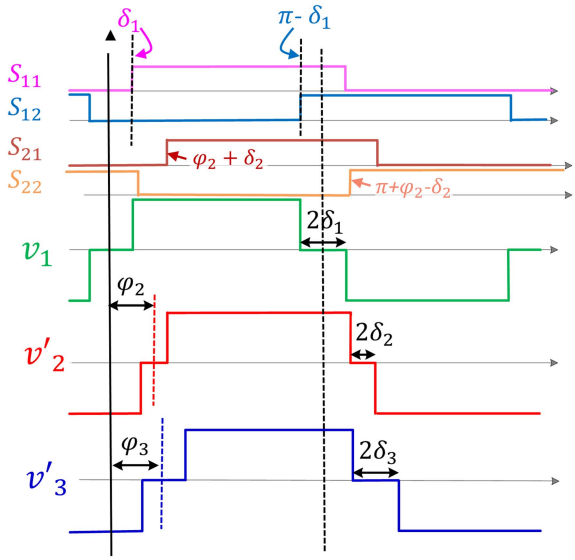

Fig. 2. Full-bridge output voltages in relation to the gate signal phase displacements of the individual half-bridges.

II. Triple Active Bridge Converter Operation and Time-Domain Circuit Modeling

Fig. 1 illustrates the schematic of the TAB converter, featuring three dc voltage sources or loads denoted as V_1, V_2', and V_3' , connected to a three-terminal transformer through three full-bridge cells. The transformer serves as an ac-link, coupling these ports at distinct voltage levels determined by corresponding turn ratios ($n_1 : n_2 : n_3$). The inductors L_1, L'_2, and L'_3 can be standalone components or formed using the transformer leakage inductances. The phase shifts of the gate driving signals of all the HF switching legs highlighted in Fig. 1 result in the full-bridge port output voltages v'_2 and v'_3 (depicted in Fig. 2), phase-displaced by φ_2 and $\varphi_3$with respect to v_1. Although these inter-bridge phase-shifts traditionally acted as the major power flow control parameters for a TAB, the intra-bridge phase shifts of $2\delta_1$, $2\delta_2$, and $2\delta_3$ are also introduced in this work in order to have a superior control (PPS modulation) over the power flow with a target of lower loss operation. The range of these TAB control variables are: $\varphi_k \in [-\pi/2,\ \pi/2]$ and $\delta_k \in [0,\ \pi/2]$, where $k = 1, 2\ or\ 3$ and $\varphi_1 = 0$. The average power sourced by each of the dc TAB ports are denoted as P_1, P_2, and P_3. Fig. 3 presents the simplified schematic of the TAB network, transformed into primary-referred Y and Δ-equivalent circuit

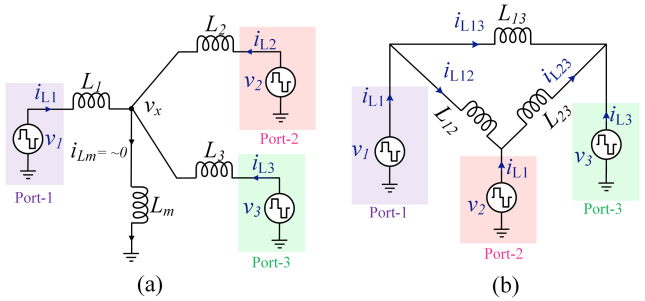

Fig. 3. Equivalent circuits of the TAB converter. (a) Y- equivalent. (b) Δ-equivalent circuit.

models. The electrical quantities depicted in Fig. 3 can be expressed as follows:

$$\begin{cases} L_2 = L_2'\left(\frac{n_1}{n_2}\right)^2;\ v_2 = v_2'\left(\frac{n_1}{n_2}\right);i_2 = i_2'\left(\frac{n_2}{n_1}\right) \\ L_3 = L_3'\left(\frac{n_1}{n_3}\right)^2;\ v_3 = v_3'\left(\frac{n_1}{n_3}\right);i_3 = i_3'\left(\frac{n_3}{n_1}\right) \\ L_{12} = L_1 + L_2 + L_1L_2/L_3 \\ L_{13} = L_1 + L_3 + L_1L_3/L_2 \\ L_{23} = L_2 + L_3 + L_2L_3/L_1 \end{cases}. \quad (1)$$

In accordance with the Δ-equivalent circuit model, the total instantaneous current in and average power sourced by each TAB port can be divided into two parts based on the following relationships:

$$\begin{cases} i_{L1}\ (t) = i_{L12}\ (t) + i_{L13}\,(t) \\ i_{L2}\ (t) = i_{L23}\ (t) - i_{L12}\,(t) \\ i_{L3}\,(t) = -i_{L23}\,(t) - i_{L13}\,(t) \end{cases} \quad (2)$$

$$\begin{cases} P_1 = P_{L12} + P_{L13} \\ P_2 = P_{L23} - P_{L12} \\ P_3 = -P_{L23} - P_{L13} \end{cases}. \quad (3)$$

Here, i_{Lab} and P_{Lab} denote the current and average power flowing through the Δ-model L_{ab} HF inductor, from port- a to b.

In the context of Δ-model inductors connected to each TAB port, the current flowing through each TAB port's inductor can be interpreted as a composition of two branch currents, influenced exclusively by the voltage sources connected to the respective ends of the inductor. The resulting current i_{Lxy} and power P_{Lxy} flowing from port x to y through L_{xy} depend solely on the intra-bridge phase-shifts of port x and y (δ_x and δ_y) and the relative phase difference between the two corresponding ports ($\varphi_y - \varphi_x$). Consequently, the TAB converter can be decomposed into three separate DAB converters, as illustrated in Fig. 4. Now, in order to synthesize the TAB bridge currents, voltages, and power flow among the ports, the operation and time domain circuit analysis of a standalone DAB cell needs to be studied first, which is outlined below.

A. Analysis of a DAB Cell Under Different Operating Modes

Fig. 5(a) depicts a primary side-referred dc–dc DAB converter circuit transferring power P_{Lxy} between dc voltage sources V_x

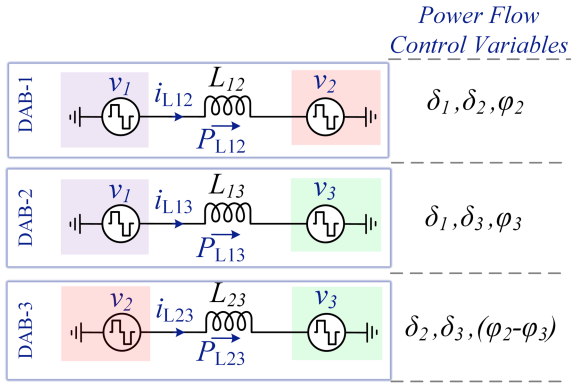

Fig. 4. DAB-based equivalent circuit representation of the Δ-TAB circuit.

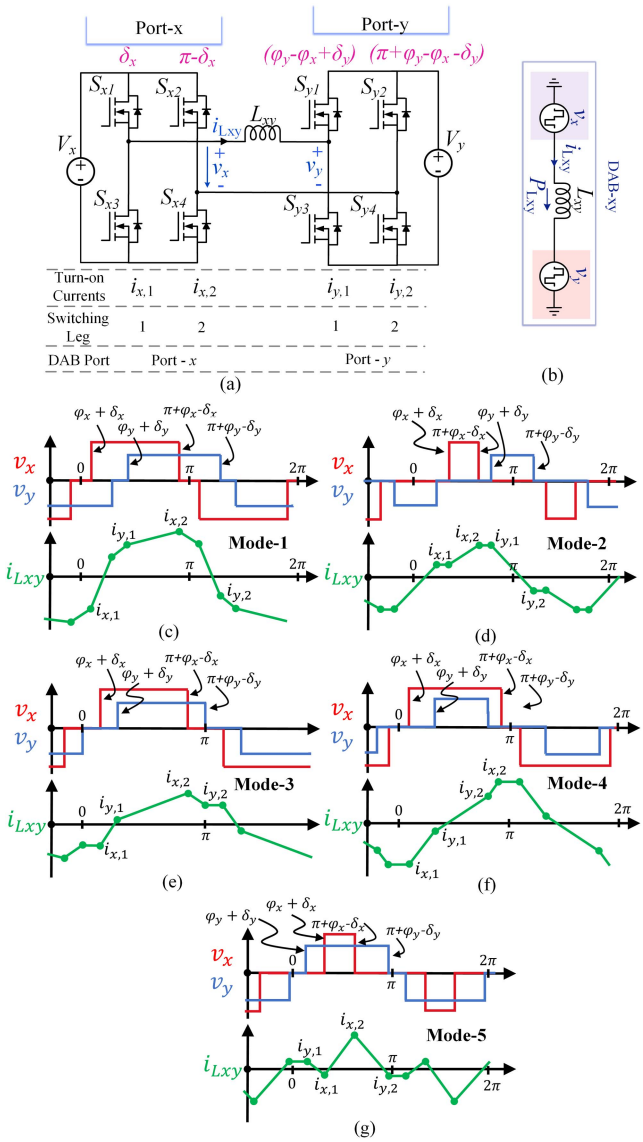

Fig. 5. (a) Primary referred DAB converter circuit. (b) Equivalent model of a DAB. (c)–(g) Switching bridge voltage and inductor current waveforms for a DAB under different operating modes.

TABLE I
SWITCHING CURRENTS, ZVS POSSIBILITIES, AND POWER FLOW ANALYSIS IN A DAB UNDER DIFFÈRENT OPERATING MODES

Operating Modes	*Condition*	*Turn-on Switching Currents of Leading (1) and Lagging Leg (2) of the DAB Ports (Power Flowing from Port x to y) [$pu_{xy} = V_x/2\pi f_{sw}L_{xy}$]*		*Minimum ZVS Condition*	*All-ZVS Possibilities*	*Transferred average Power P_{Lxy}(p.u.); $P_{base} = V_x^2/2\pi f_{sw}L_{xy}$*
Mode-1	$(\varphi_y-\varphi_x)\geq(\delta_x+\delta_y)$; $(\delta_x+\delta_y)\leq\frac{\pi}{2}$	$i_{x,1}$	$-pu_{xy}[m_{xy}(\varphi_y-\varphi_x)-(1+m_{xy})\delta_x+(1-m_{xy})\pi/2]$	$i_{x1}<0$; $i_{x2}>0$; $i_{y1}>0$; $i_{y2}<0$	Possible	$m_{xy}\left[(\varphi_y-\varphi_x)\left\{1-\frac{(\varphi_y-\varphi_x)}{\pi}\right\}-\frac{\delta_x^2+\delta_y^2}{\pi}\right]$
		$i_{x,2}$	$pu_{xy}[m_{xy}(\varphi_y-\varphi_x)-(1-m_{xy})\delta_x+(1-m_{xy})\pi/2]$			
		$i_{y,1}$	$pu_{xy}[(\varphi_y-\varphi_x)+(1-m_{xy})\delta_y-(1-m_{xy})\pi/2]$			
		$i_{y,2}$	$-pu_{xy}[(\varphi_y-\varphi_x)-(1+m_{xy})\delta_y-(1-m_{xy})\pi/2]$			
Mode-2	$\frac{\pi}{2}\geq(\varphi_y-\varphi_x)$; $(\varphi_y-\varphi_x)\geq\pi-(\delta_x+\delta_y)$	$i_{x,1}$	$-pu_{xy}[m_{xy}\delta_y-\delta_x+(1-m_{xy})\pi/2]$		Not Possible	$\frac{2m_{xy}}{\pi}\left(\frac{\pi}{2}-\delta_x\right)\left(\frac{\pi}{2}-\delta_y\right)$
		$i_{x,2}$	$pu_{xy}[-m_{xy}\delta_y-\delta_x+(1+m_{xy})\pi/2]$			
		$i_{y,1}$	$pu_{xy}[-m_{xy}\delta_y-\delta_x+(1+m_{xy})\pi/2]$			
		$i_{y,2}$	$pu_{xy}[m_{xy}\delta_y-\delta_x+(1-m_{xy})\pi/2]$			
Mode-3	$\lvert\delta_x-\delta_y\rvert\leq(\varphi_y-\varphi_x)$; $(\varphi_y-\varphi_x)<\min\begin{bmatrix}(\delta_x+\delta_y),\\(\pi-\delta_x-\delta_y)\end{bmatrix}$	$i_{x,1}$	$-pu_{xy}[m_{xy}\delta_y-\delta_x+(1-m_{xy})\pi/2]$		Not Possible	$m_{xy}\left[(\varphi_y-\varphi_x)\left(1-\frac{\varphi_y-\varphi_x}{2\pi}\right)-\frac{(\varphi_y-\varphi_x)(\delta_x+\delta_y)}{\pi}-\frac{(\delta_x-\delta_y)^2}{2\pi}\right]$
		$i_{x,2}$	$pu_{xy}[m_{xy}(\varphi_y-\varphi_x)-(1-m_{xy})\delta_x+(1-m_{xy})\pi/2]$			
		$i_{y,1}$	$pu_{xy}[(\varphi_y-\varphi_x)+(1-m_{xy})\delta_y-(1-m_{xy})\pi/2]$			
		$i_{y,2}$	$pu_{xy}[m_{xy}\delta_y-\delta_x+(1-m_{xy})\pi/2]$			
Mode-4	$(\varphi_y-\varphi_x)<\lvert\delta_x-\delta_y\rvert$; $\delta_y>\delta_x$	$i_{x,1}$	$-pu_{xy}[m_{xy}\delta_y-\delta_x+(1-m_{xy})\pi/2]$		Possible for $m_{xy}>1$	$m_{xy}(\varphi_y-\varphi_x)\left(1-\frac{2\delta_y}{\pi}\right)$
		$i_{x,2}$	$pu_{xy}[m_{xy}\delta_y-\delta_x+(1-m_{xy})\pi/2]$			
		$i_{y,1}$	$pu_{xy}[(\varphi_y-\varphi_x)+(1-m_{xy})\delta_y-(1-m_{xy})\pi/2]$			
		$i_{y,2}$	$pu_{xy}[(\varphi_y-\varphi_x)-(1-m_{xy})\delta_y+(1-m_{xy})\pi/2]$			
Mode-5	$(\varphi_y-\varphi_x)<\lvert\delta_x-\delta_y\rvert$; $\delta_x>\delta_y$	$i_{x,1}$	$-pu_{xy}[-m_{xy}(\varphi_y-\varphi_x)-(1-m_{xy})\delta_x+(1-m_{xy})\pi/2]$		Possible for $m_{xy}<1$	$m_{xy}(\varphi_y-\varphi_x)\left(1-\frac{2\delta_x}{\pi}\right)$
		$i_{x,2}$	$pu_{xy}[m_{xy}(\varphi_y-\varphi_x)-(1-m_{xy})\delta_x+(1-m_{xy})\pi/2]$			
		$i_{y,1}$	$pu_{xy}[\delta_x-m_{xy}\delta_y-(1-m_{xy})\pi/2]$			
		$i_{y,2}$	$-pu_{xy}[\delta_x-m_{xy}\delta_y-(1-m_{xy})\pi/2]$			

and V_y, switching at frequency f_{sw} . The shapes of the H-bridge voltages v_x and v_y are controlled by modulating the phase-shift and duty cycle variables, i.e., $(\varphi_y-\varphi_x)$, δ_x, and δ_y, achieving a particular inductor current i_{Lxy} shape and desired power flow. The equivalent model of the DAB circuit is depicted in Fig. 5(b). Depending on the relative values of the three control variables that generate non-negative power transfer from port-x to port-y, i.e, $P_{Lxy}>0$, or, $0\leq\delta_x,\ \delta_y,\ (\varphi_y-\varphi_x)\leq\frac{\pi}{2}$, the operation of the converter can be categorized into five operating zones [see Fig. 5(c)–(g)], where the voltage across the line inductor v_{Lxy} ($=v_x\ -v_y$) and i_{Lxy} take different profiles [9], [10]. By integrating the $i_{Lxy}v_{Lxy}$ product over a half switching cycle the average transferred power P_{Lxy} in a DAB is determined: $P_{Lxy}=\int_0^{T_s/2} i_{Lxy}v_{Lxy}dt$. Each of the identified operating modes showcases different expressions for P_{Lxy} (normalized with respect to base power, $P_{\text{base}}=\frac{V_x^2}{X_L}=\frac{V_x^2}{2\pi f_{sw}L_{xy}}$), as well as for instantaneous values of $i_{Lxy}(t)$ (per unit or base current, $p\,u_{xy}=\frac{V_x}{X_L}=\frac{V_x}{2\pi f_{sw}L_{xy}}$) during the turn-ON switching instants for the leading and lagging switching legs of both the DAB ports, i.e., $i_{x,1},\ i_{x,2},\ i_{y,1},\ i_{y,2}$, as outlined in Table I. In the derived expressions, the output dc voltage gain of the power receiving port (port-y) is denoted as m_{xy} $(=V_y\ /V_x)$.

The fundamental basis of the ZVS conditions for each of the HF switching legs in a DAB is primarily established by analyzing the direction of the current flow in the inductor at the switching instants. From the circuit waveforms, given in Fig. 5(c)–(g), it can be inferred that the rising edge of v_x marks the turn-on instant ($\theta=\varphi_x+\delta_x$) of leg-1 high side switch of port-x, i.e., S_{x1}, whereas the falling edge of v_x identifies the turn-ON instant ($\theta=\pi-\varphi_x-\delta_x$) of leg-2 high side switch of same port, i.e., S_{x2}. The inductor current i_{Lxy} at $\theta=\varphi_x+\delta_x$ ($i_{Lxy}|_{\theta=\varphi_x+\delta_x}=i_{x,1}$) should be directed towards port-x (or, $i_{x,1}<0$) in order for S_{x1} to undergo soft-turn ON. In that way, the body capacitor of S_{x1}, $C_{\text{oss, }S_{x1}}$ will discharge and the body capacitor of S_{x3} will charge with i_{Lxy} current during the dead-time before S_{x1} turns on and hence, it creates the opportunity for S_{x1} to turn-ON with a zero voltage across the device ($v_{\text{DS, }S_{x1}}$). Similarly, the other three crucial ZVS conditions corresponding to the rest of the three HF switching legs in the DAB are summarised as

$$i_{x,2}>0;\ i_{y,1}>0;\ i_{y,2}<0. \tag{4}$$

From the expressions of $i_{x,1},\ i_{x,2},\ i_{y,1}$, and $i_{y,2}$ under the five modes of DAB operation highlighted in Table I, it can be concluded that ZVS conditions can be simultaneously satisfied for mode-1, mode-4, and mode-5 only. For any DAB operating in mode-2 and mode-3, the leading leg of the primary H-bridge and lagging leg of the secondary H-bridge, cannot achieve soft-switching simultaneously because in both the modes, $i_{x,1}=-i_{y,2}$, which does not satisfy the conditions outlined in (4) together. Moreover, mode-2 and mode-3 operation incurs higher conduction loss in the system for a specific power flow compared to other modes due to higher inductor current RMS [9], [33]. Keeping these conditions in mind, a soft-switching enabled DAB modulation scheme (for buck action, i.e., $m_{xy}=V_y\ /V_x<1$) is proposed in [9], where the DAB operates in mode-5 until $(\varphi_y-\varphi_x)\leq(1-m_{xy})\pi/2$ and moves to mode-1 when $(\varphi_y-\varphi_x)>(1-m_{xy})\pi/2$. Similarly, for the boost mode operation, i.e., $m_{xy}>1$, it can be deduced that the DAB should operate in mode-4 when $(\varphi_y-\varphi_x)\leq(1-\frac{1}{m_{xy}})\pi/2$ and in mode-1 while $(\varphi_y-\varphi_x)>(1-\frac{1}{m_{xy}})\pi/2$ so that ZVS can be attained at all legs based on direction of current flow.

B. Synthesis of TAB Switching Currents and Power Flow Using Time-Domain Modelling

Once the standalone DAB converter's analytical modeling is complete, the winding currents and power flow of the TAB converter can be accurately quantified by employing the superposition theorem, stated in (2)–(3). It needs to be mentioned that for the TAB converter under study, port-1 is considered as the power input port and port-2 and port-3 are used as output ports (i.e., $P_1 > 0$; $P_2 < 0$; $P_3 < 0$ and $P_1 + P_2 + P_3 = 0$). Thus, two possibilities of power transfer arrive in the Δ-TAB model: 1) $P_{L12} > 0$, $P_{L13} > 0$, $P_{L23} < 0$; or, $\varphi_2 > \varphi_3$; 2) $P_{L12} > 0$, $P_{L13} > 0$, $P_{L23} > 0$; or, or, $\varphi_2 < \varphi_3$. Keeping these two power transfer scenarios in mind, the Y-TAB inductor currents or the transformer winding currents during the switching transients are deduced using Table I and the relations given in (2).

The TAB port-1 bridge current $i_{L1}(t)$ at the turn-ON transient of leading (leg 1) and lagging (leg 2) switching legs are deduced as

$$\begin{cases} i_{L1,1} = i_{1,1}|_{P_{L12},\ x=1,\ y=2} + i_{1,1}|_{P_{L13},\ x=1,\ y=3} \\ i_{L1,2} = i_{1,2}|_{P_{L12},\ x=1,\ y=2} + i_{1,2}|_{P_{L13},\ x=1,\ y=3} \end{cases} \tag{5}$$

where $i_{1,1}|_{P_{L12},\ x=1,\ y=2}$ and $i_{1,2}|_{P_{L12},\ x=1,\ y=2}$are the L_{12} inductor current (i_{L12}) during turn-ON instants of the leading and lagging legs of port-1 H-bridge inside DAB-1 module (as given in Fig. 4), respectively, and the active power is being transferred from port-1 to port-2 or $P_{L12} > 0$. Similarly, $i_{1,1}|_{P_{L13},\ x=1,\ y=3}$ and $i_{1,2}|_{P_{L13},\ x=1,\ y=3}$ are represented as the instantaneous values of i_{L13} during turn-ON instants of port-1 H-bridge leading and lagging switching legs (DAB-2), respectively, while $P_{L13} > 0$. The values of $i_{1,1}|_{P_{L12}}$, $i_{1,1}|_{P_{L13}}$, $i_{1,2}|_{P_{L12}}$, and $i_{1,2}|_{P_{L13}}$ can be calculated based on the operating modes of the corresponding DAB cells from Table I.

In a similar manner the rest two winding currents of the TAB ($i_{L2}(t)$ and $i_{L3}(t)$) during the turn-ON instants of port-2 and port-3 switching legs can be synthesized using the superposition theorem of (2) and are highlighted as $i_{L2,1}$, $i_{L2,2}$ and $i_{L3,1}$, $i_{L3,2}$, respectively, in the following equations:

$$\begin{cases} i_{L2,1} = \begin{cases} -i_{2,1}|_{P_{L12},\ x=1,\ y=2} \\ \quad +i_{2,1}|_{P_{L23},\ x=2,y=3}, & \text{if } \varphi_3 > \varphi_2 \\ -i_{2,1}|_{P_{L12},\ x=1,\ y=2} \\ \quad -i_{2,1}|_{P_{L32},\ x=3,y=2}, & \text{if } \varphi_3 < \varphi_2 \end{cases} \\ i_{L2,2} = \begin{cases} -i_{2,2}|_{P_{L12},\ x=1,\ y=2} \\ \quad +i_{2,2}|_{P_{L23},\ x=2,y=3}, & \text{if } \varphi_3 > \varphi_2 \\ -i_{2,2}|_{P_{L12},\ x=1,\ y=2} \\ \quad -i_{2,2}|_{P_{L32},\ x=3,y=2}, & \text{if } \varphi_3 < \varphi_2 \end{cases} \end{cases} \tag{6}$$

$$\begin{cases} i_{L3,1} = \begin{cases} -i_{3,1}|_{P_{L13},\ x=1,\ y=3} \\ \quad -i_{3,1}|_{P_{L23},\ x=2,y=3}, & \text{if } \varphi_3 > \varphi_2 \\ -i_{3,1}|_{P_{L13},\ x=1,\ y=3} \\ \quad +i_{3,1}|_{P_{L32},\ x=3,y=2}, & \text{if } \varphi_3 < \varphi_2 \end{cases} \\ i_{L3,2} = \begin{cases} -i_{3,2}|_{P_{L13},\ x=1,\ y=3} \\ \quad -i_{3,2}|_{P_{L23},\ x=2,y=3}, & \text{if } \varphi_3 > \varphi_2 \\ -i_{3,2}|_{P_{L13},\ x=1,\ y=3} \\ \quad +i_{3,2}|_{P_{L32},\ x=3,y=2}, & \text{if } \varphi_3 < \varphi_2 \end{cases} \end{cases} . \tag{7}$$

Here, two sets of equations for each turn-ON current arise due to the two different power flow possibilities ($P_{L23} > 0$ and $P_{L23} < 0$), as stated earlier. Consolidating the expressions given in (5)–(7), the HF inductor current corresponding to any port-x (of Y-model) of a n-port multiactive-bridge (MAB) converter during its leading and lagging switching leg turn-ON instants can be identified using the unified expression shown in the following equation:

$$i_{Lx,j} = \sum_{\substack{y=1 \\ y \neq x}}^{n} \begin{cases} i_{x,j}|_{P_{xy}}, & \text{if } \varphi_y > \varphi_x \\ -i_{x,j}|_{P_{yx}}, & \text{if } \varphi_y < \varphi_x \end{cases} . \tag{8}$$

Here, leading and lagging HF legs are identified as $j = 1$ and 2, respectively. $i_{x,j}|_{P_{xy}}$ represents the jth leg turn-ON current of port-x corresponding to the DAB cell comprising port-x and y bridge voltage sources (v_x and v_y) and the Δ-model inter-port inductor L_{xy} connected in between and the power is flowing from port-x to port-y ($\varphi_y > \varphi_x$). On the other hand, $i_{x,j}|_{P_{yx}}$ showcases the same turn-ON current of that DAB cell if the power flow is in the reverse direction ($\varphi_x > \varphi_y$). Both of these current quantities can be derived from their expressions given in Table I based on the relative values of phase-duty control variables. Thus, the peak switching currents in a TAB or MAB converter can be calculated from the developed time-domain model of the converter fundamentally constructed using multiple DAB building blocks without engaging any frequency domain oriented higher order harmonic-based complex and approximated calculations. These identified current vertices are major points of interest while computing the switching loss in the system as well as evaluating the soft-switching ability of the converter. Furthermore, it is noteworthy to mention that, regardless of the power flow directions in a Δ-TAB model, if the fundamental DAB cells operate in ZVS-favorable modes (mode-1, 4, or 5) while satisfying the ZVS conditions of (4), the superposition of the port currents creates a favorable condition for the TAB port switches to undergo soft-switching.

Furthermore, using the same modeling technique, the average normalized power sourced by any of the MAB port (port-x) can be precisely quantified as

$$P_x = \sum_{\substack{y=1 \\ y \neq x}}^{n} P_{Lxy} \tag{9}$$

where the power transfer in the DAB cell, P_{Lxy}, is deduced from Table I based on its mode of operation.

III. Charge-Based ZVS Analysis of the TAB Converter

In order to attain better system efficiency and improved EMI performance for a wide load operation, the achievement of ZVS operation in the TAB converter is of paramount importance. To realize effective ZVS operation, it is crucial to consider the charge stored in the nonlinear parasitic capacitors (C_{OSS}) of the switching power devices during the commutation process. This necessitates a minimal inductor current ($I_{\text{Lx,crit}}$) to successfully

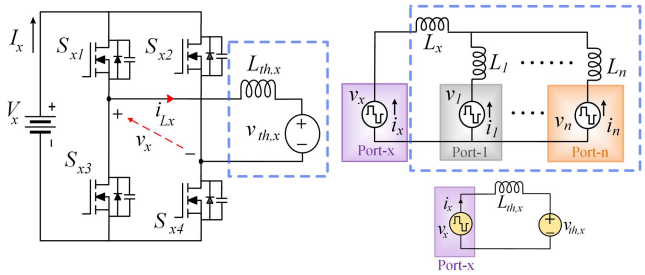

Fig. 6. Derivation of the port-equivalent TAB circuit model to analyze ZVS criteria. (a) Identified Thevenin equivalent line inductance and port voltage to be derived from the perspective of port-x. (b) Steps to derive Thevenin-equivalent circuit elements from Y-model.

complete the commutation process during the dead-band, a parameter that will be comprehensively derived in this section.

A. Thevenin Equivalent Circuit Formulation

To facilitate a simplified analysis of the commutation process, a Thevenin equivalent circuit model of the TAB converter is introduced. The equivalent circuit related to Port-x (where x signifies the commutating port) is depicted in Fig. 6(a). In this representation, V_x represents the dc voltage source on the commutating side, while v_x and i_{Lx} denote the voltage across the half-bridges and the port-x inductor current on the commutating side, respectively. $L_{th,x}$ and $v_{th,x}$ represent the Thevenin equivalent impedance and voltage of the noncommutating side. The expressions for $L_{th,x}$ and $v_{th,x}$ are derived from the Y-type TAB configuration based on the Thevenin theorem [see Fig. 6(b)] and are presented in the following equations:

$$L_{th,x} = \left(\sum_{\substack{y=1 \\ y \neq x}}^{3} \frac{1}{L_y} \right)^{-1} + L_x \tag{10}$$

$$v_{th,x}\ (t) = \left(\sum_{\substack{y=1 \\ y \neq x}}^{3} \frac{v_y\,(t)}{L_y} \right) \cdot \left(\sum_{\substack{y=1 \\ y \neq x}}^{3} \frac{1}{L_y} \right)^{-1}. \tag{11}$$

Here, $v_{th,x}(t)$ contains the information regarding phase-duty control parameters of the noncommutating TAB ports and can be utilized in order to find the ZVS conditions of the port-x MOSFETs. At any switching time instant, $v_{th,x}(t)$ can be derived from TAB port voltages $v_y(t)$ as given in the following equation:

$$v_y\,(t) = \begin{cases} 0,\ (\varphi_y - \delta_y) < \omega t < (\varphi_y + \delta_y) \\ V_y, (\varphi_y + \delta_y) < \omega t < (\pi + \varphi_y - \delta_y) \\ 0,\ (\pi + \varphi_y - \delta_y) < \omega t < (\pi + \varphi_y + \delta_y) \\ -V_y, (\pi + \varphi_y + \delta_y) < \omega t < (2\pi + \varphi_y - \delta_y) \end{cases}. \tag{12}$$

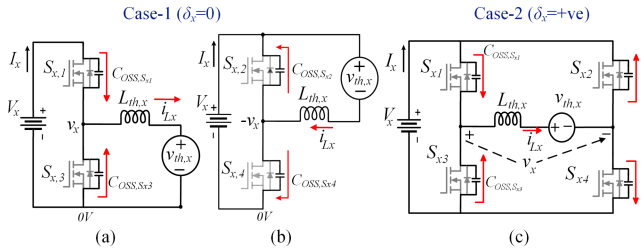

Fig. 7. Different switching commutation scenarios in a TAB H-bridge. (a) S_{x1} turns ON alone. (b) S_{x2} turns ON alone. (c) S_{x1} and S_{x4} turn ON simultaneously.

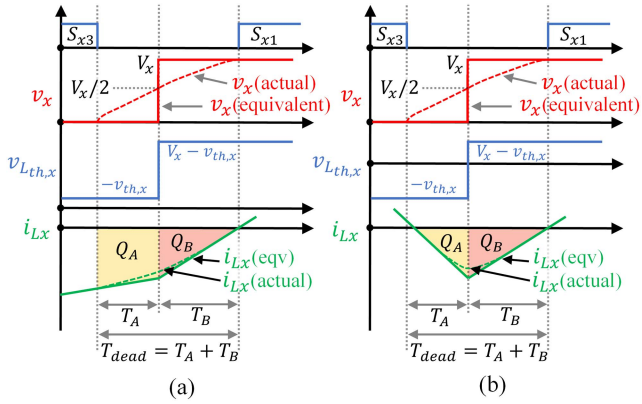

Fig. 8. Actual and approximated ZVS transient waveforms of the TAB port voltage and current when (a) $v_{th,x} < 0$ and (b) $V_x > v_{th,x}(t) > 0$.

B. Solutions for Charge-Based ZVS Conditions

As the high side and low side MOSFETs placed on the same switching leg exhibit complementary switching, achieving ZVS in one of them confirms the same for the other. Consequently, the analysis here focuses on the commutation process and ZVS characteristics of S_{x1} and S_{x2}. Theoretically, three following switching conditions are considered: S_{x1} turns ON alone, S_{x2} turns ON alone, (case-1: when $\delta_x > 0$) and S_{x1} and S_{x4} turn ON simultaneously (case-2: when $\delta_x = 0$). The corresponding commutation process during the dead-band is illustrated in Fig. 7.

Analyzing ZVS operation under case-1, we focus on the transient process during the turn-ON of S_{x1}. Fig. 7(a) illustrates the current path during dead time. Following the turn-OFF of S_{x3}, inductor $L_{th,x}$ resonates with junction capacitances $C_{\text{OSS},S_{x1}}$ and $C_{\text{OSS},S_{x3}}$. Inductor current (i_{Lx}) charges $C_{\text{OSS},S_{x3}}$ and discharges $C_{\text{OSS},S_{x1}}$. The voltage across $C_{\text{OSS},S_{x3}}$ begins to rise, while the voltage across $C_{\text{OSS},S_{x1}}$ decreases that leads v_x to rise from 0 V to dc link voltage V_x, as depicted in Fig. 8. As $C_{\text{OSS},S_{x1}}$ voltage reaches 0, a small negative i_{Lx} flows through the body diode of S_{x1}, before its channel turns ON, signifying the achievement of ZVS. The critical ZVS current ($I_{Lx,1,\text{crit}}$) is defined as the current that results in i_{Lx} being exactly 0 at the end of dead time (T_{dead}), representing the minimum i_{Lx} value necessary for achieving ZVS in the corresponding switch.

Due to the strong nonlinearity of the junction capacitance, accurately describing the v_x waveform during dead time is

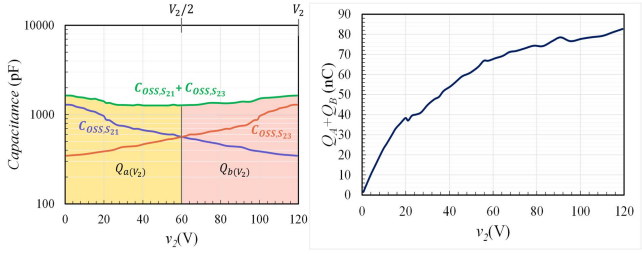

Fig. 9. Variation of C_{oss} and its stored charge with varying v_{DS} for EPC 2215 GaN MOSFET.

challenging. A linear approximation proposed in [27] and [28] that piecewise linearizes v_x, assuming it changes instantly from 0 to V_x when actual v_x equals $V_x/2$. T_A represents the time when $v_x = V_x\ /2$, and the equivalent i_{Lx} is linearized into two pieces with T_A as the middle point, as depicted in Fig. 8. This linearized i_{Lx} during the dead time is mathematically expressed as follows:

$$i_{Lx}(t) = \begin{cases} i_{Lx}(T_A) - \frac{v_{th,x}}{L_{th,x}}\ (t - T_A), t \in [0, T_A) \\ i_{Lx}(T_A) + \frac{(V_x - v_{th,x})}{L_{th,x}}\ (t - T_A), t \in [T_A, T_{\text{dead}}) \end{cases}. \tag{13}$$

Further, considering $i_{Lx}\ (T_{\text{dead}}) = 0$ in Fig. 8(a), $T_B\ (= T_{\text{dead}}\ - T_A)$ can be derived as, $\frac{-i_{Lx}(T_A)L_x}{V_x - V_{th,x}}$.

To achieve ZVS, it is imperative to completely discharge the stored charges $C_{\text{OSS},S_{x1}}$ and charge $C_{\text{OSS},S_{x3}}$ through the inductor current, i_{Lx}. The shaded region in Fig. 8 represents the total charges liberated by i_{Lx}. This region is partitioned into Q_A and Q_B, signifying the conveyed charges during the v_x transition from 0 to $V_x/2$ and $V_x/2$ to 0, respectively, which are calculated using the following equation:

$$\begin{cases} Q_A = \int_0^{T_A} i_{Lx}(t)\,.dt = |i_{Lx}(T_A)|\,T_A - \frac{v_{th,x}T_A^2}{2L_{th,x}} \\ Q_B = \int_{T_A}^{T_{dead}} i_{Lx}(t)\,.dt = \frac{|i_{Lx}(T_A)|^2 L_{th,x}}{2(V_x - v_{th,x})} \end{cases}. \tag{14}$$

Simultaneously, the C_{oss} of the MOSFETs experiences nonlinear changes concerning changes in drain-source voltage v_{DS}. The stored charges in the C_{oss} necessitate calculation and can be derived by integrating the nonlinear C_{oss}-v_{DS} plot available in the MOSFET's datasheet, as shown in Fig. 9. The shaded area in Fig. 9 represents the total charge stored in the $C_{\text{OSS},S_{x1}}$ and $C_{\text{OSS},S_{x3}}$ pair that can be divided into two parts: $Q_{a(V_x)}$ and $Q_{b(V_x)}$, depending on v_x transition from 0 to $V_x/2$ and $V_x/2$ to V_x. Due to $C_{\text{OSS},S_{x1}}(v_x) = C_{\text{OSS},S_{x3}}(V_x - v_x)$, the relation between Q_a and Q_b is formed as

$$\begin{aligned} Q_{a(V_x)} &= \int_0^{\frac{V_x}{2}} C_{\text{OSS},S_{x1}}(v_x)\,.dv_x \\ &\quad + \int_{V_x}^{\frac{V_x}{2}} C_{\text{OSS},S_{x3}}(V_x - v_x)\,.dv_x \\ &= \int_{\frac{V_x}{2}}^{V_x} C_{\text{OSS},S_{x1}}(v_x)\,.dv_x \\ &\quad + \int_{\frac{V_x}{2}}^{0} C_{\text{OSS},S_{x3}}(V_x - v_x)\,.dv_x = Q_{b(V_x)}. \end{aligned} \tag{15}$$

The prerequisite for achieving ZVS is that the conveyed charges in i_{Lx} must surpass the capacitance stored charges. This results in the constraint

$$Q_A = Q_B\ \geq\ Q_{a(V_x)} = Q_{b(V_x)}. \tag{16}$$

Consequently, based on (14)–(16), the critical ZVS current $I_{Lx,1,\text{crit}}$ of S_{x1} [under condition of Fig. 8(a)] is derived as

$$I_{Lx,1,\text{crit}} = -\sqrt{2Q_{B(V_x)}\left[V_x - v_{th,x}(t)\right]/L_{th,x}}. \tag{17}$$

For any switching current i_{Lx} lower than $I_{Lx,1,\text{crit}}$, S_{x1} will undergo soft-switching.

In a similar way as stated above, the critical ZVS currents for other switching transitions (as depicted in Fig. 7) are formulated and highlighted in Table II. Therefore, depending on the operating state of the TAB defined by the status of the control variables $(\varphi_2, \varphi_3, \delta_1, \delta_2, \delta_3)$ and its circuit parameters such as dc link port voltages, port inductances, and switching device parameters, the required ZVS currents can be identified online.

IV. Optimized Selection of the HF TAB Inductors for Reduced Switching Loss

Before synthesizing the TAB modulation scheme that enables the soft-switching by tracking the critical ZVS currents identified in the previous section, optimally selecting the TAB port inductances is a crucial intermediate design step. It helps to broaden the ZVS range of the converter to an extremely light load for a wide voltage range operation. With this aim, this section presents a formulated mathematical optimization framework that tries to identify the optimal choice of the HF port inductors (L_x) that minimizes the total switching loss (the major loss element at a lighter operating load) in the converter.

The objective function for minimization is formulated in (18), which correlates to the total switching loss incurred during the hard turn-ON and hard turn-OFF switching transients for each HF TAB switching leg

$$F_{\text{sw\_loss}}(\delta_x, \varphi_x) = \begin{cases} \sum_{x=1}^{3} \left[2V_x\,|i_{Lx}(\varphi_x)|\,f_{\text{sw}}t_{\text{off},x} \right. \\ \quad \left. +2V_x\,|i_{Lx}(\varphi_x)|\,f_{\text{sw}}t_{\text{on},x}\cdot(1 - \text{ZVS}(x))\right]\ ;\ \delta_x = 0 \\ \sum_{x=1}^{3}\sum_{j=1}^{2} \left[2V_x\,|i_{Lx,j}(\tau_{x,j})|\,f_{\text{sw}}t_{\text{off},x,j} \right. \\ \quad \left. +2V_x\,|i_{j,k}(\tau_{x,j})|\,f_{\text{sw}}t_{\text{on},x,j}\cdot(1 - \text{ZVS}(x,j))\right]\ ;\ \delta_x > 0 \end{cases}. \tag{18}$$

where $\text{ZVS}(x, j)$ can be 1 or 0, depending on if the jth (j = 1, 2) half-bridge of the TAB port-x (x = 12,3) is achieving ZVS, or not. The ZVS conditions used in the objective function calculation algorithm are determined from Table II as described before. The turn-OFF current of jth half-bridge of port-x is shown as $|i_{Lx,j}(\tau_{x,j})|$ and can be calculated using (8), which is a function of the TAB port inductances (L_x). Further, $f_{\text{sw}}, t_{\text{on},x,j}$ and $t_{\text{off},x,j}$ denote the converter switching frequency, device turn-ON, and OFF time of jth leg of TAB port-x, respectively.

TABLE II
SUMMARIZED ZVS CURRENT REQUIREMENTS FOR PORT-X IN A TAB

Case	δ_x	Leg undergoing turn-on event	Min required Switch Currents for ZVS	Switching time (ωt)
1	+ve	*Leg-1*	$I_{Lx,1,crit} = \begin{cases} -\sqrt{2Q_{B(V_x)}[V_x - v_{th,x}(t)]/L_{th,x}}\ ; if\ V_x > 0 > v_{th,x}(t) \\ -max\left[\sqrt{2Q_{B(V_x)}[V_x - v_{th,x}(t)]/L_{th,x}}, \sqrt{2Q_{A(V_x)}v_{th,x}(t)/L_{th,x}}\right]; if\ V_x > v_{th,x}(t) > 0 \\ 0\ ;\ if\ v_{th,x}(t) > V_x > 0 \end{cases}$	$\varphi_x + \delta_x$
		Leg-2	$I_{Lx,2,crit} = \begin{cases} 0\ ;\ if\ V_x > 0 > v_{th,x}(t) \\ max\left[\sqrt{2Q_{A(V_x)}[V_x - v_{th,x}(t)]/L_{th,x}}, \sqrt{2Q_{B(V_x)}v_{th,x}(t)/L_{th,x}}\right]; if\ V_x > v_{th,x}(t) > 0 \\ \sqrt{2Q_{B(V_x)}v_{th,x}(t)/L_{th,x}}\ ; if\ v_{th,x}(t) > V_x > 0 \end{cases}$	$\pi + \varphi_x - \delta_x$
2	0	*any*	$I_{Lx,1,crit} = -I_{Lx,2,crit} = \begin{cases} -\sqrt{4Q_{B(V_x)}[V_x - v_{th,x}(t)]/L_{th,x}}\ ; if\ V_x > 0 > v_{th,x}(t) \\ -\sqrt{4Q_{B(V_x)}[V_x + v_{th,x}(t)]/L_{th,x}}; if\ V_x > v_{th,x}(t) > 0 \\ 0\ ;\ if\ v_{th,x}(t) > V_x > 0 \end{cases}$	φ_i

Here, $t_{\text{on},x,j}$ and $t_{\text{off},x,j}$ depends on the device parameters and can be determined from the device datasheet depending on the operating conditions. In addition, $F_{\text{sw\_loss}}(\delta_x,\ \varphi_x)$ is quantified in such a way that minimization of the function tries to minimize the overall switching loss in the power devices by increasing the number of the ZVS events.

Now, the switching loss optimization problem in the TAB converter can be generalized for a five-variable control system defined by the PPS modulation logic, where the objective function $F_{\text{sw\_loss}}$ is minimized for a specific (L_1, L'_2, L'_3) combination. The constraints in this problem are defined by the output power demand P_2 and P_3 formulated using (9). Thus, for a specific converter operating condition, defined by the ports' voltages and load conditions ($V_1, V'_2, V'_3, P_2, P_3$), the multi-dimensional optimization problem is depicted in the flowchart given in Fig. 10. Solving this problem while looking for globally minimum normalized average (over n discrete data points represented by different P_2, P_3 combinations), switching loss over a wide load range, $\overline{f_m} = 1/n \sum_{i=1}^{n} F_{\text{sw}_{\text{loss},i}}/(-P_{2,i} - P_{3,i})$ by iterating (L_1, L'_2, L'_3) combinations leads to the optimal ($L_{1,\text{opt}}$, $L'_{2,\text{opt}}$, $L'_{3,\text{opt}}$) set. The result from the optimization process is depicted in Fig. 11, where the optimal $L'_{2,\text{opt}}$ and $L'_{3,\text{opt}}$ are identified as 3 μH and 0.35 μH for two different TAB port voltage combinations (based on the specifications of the converter under study) that lead to the minimum average switching loss over the complete load range.

V. SYNTHESIS AND COMPARATIVE ANALYSIS OF THE PROPOSED ZVS CURRENT TRACKED SOFT-SWITCHING MODULATION

In order to reduce the losses in the TAB converter's switching network, the bridge voltage duty variables need to be intelligently optimized alongside the two essential phase-shift variables using a PPS modulation technique. With an aim of achieving soft-switching across all the six TAB switching legs, a ZVS current tracked soft-switching modulation (ZCTSM) strategy is formulated and presented in this section that observes the switching peak currents and maintains them at or above the critical ZVS currents by compensating the duty control variables ($\delta_1,\ \delta_2, \delta_3$).

In order to showcase the process of synthesizing the ZCTSM scheme in detail, one possible power flow combination of the Δ-TAB is kept under consideration for this paper, as illustrated in Fig. 12. In both the Δ-models, illustrated in Fig. 12, the power transfer direction is identified by: $P_{12} > 0$, $P_{13} > 0$, $P_{23} > 0$; or, $\varphi_3 > \varphi_2$ and the relative volatges of the ports are defined as: $V_1 > V_2 > V_3$, or, $m_{12} < 1$, $m_{13} < 1$, $m_{23} < 1$. Further, different combinations oprating modes (as highlighted in Table I) of the three DAB cells (DAB-L_{12}, DAB-L_{13}, DAB-L_{23}) are possible (total of $5 \times 5 \times 5 = 125$ cases) under a specific power transfer direction category. However, it is known through existing research [9] and our identified ZVS conditions (see Table I) that the DAB-L_{xy} needs to operate in mode-1 (if $(\varphi_y - \varphi_x) > (1 - m_{xy})\pi/2$) or mode-5 (if $(\varphi_y - \varphi_x) \leq (1 - m_{xy})\pi/2$) in order to avoid complete hard-switching of some of the switching legs. Thus, we considered the three DAB cells of the TAB model to be operative under mode-1 or mode-5. Thus, the total possible combinations under study reduces down to 8 ($= 2 \times 2 \times 2$) from 125. Among 8 such cases, two of them are discussed below, as illustrated in Fig. 12(a) and (b), for which the optimized duty variables are synthesized in detail. The summarized ZVS current tracked optimial TAB duty expressions for all 8 operating modes are given in the Appendix section of the paper.

A. Mode-555 (DAB-L_{12} in Mode 5, DAB-L_{13} in Mode 5, DAB-L_{23} in Mode 5)

This mode appears at light load TAB operations defined by $\varphi_2 \leq (1 - m_{12})\pi/2$, $\varphi_3 \leq (1 - m_{13})\pi/2$, and $(\varphi_3 - \varphi_2) \leq (1 - m_{23})\pi/2$. This is the most important operating mode where securing ZVS is utmost necessary to significantly reduce the power loss associated with the MOSFET switching and in turn attain better light load efficiency at corner voltage gain conditions. To ensure the ZVS transition of a TAB port's switching legs its turn-ON switching current and its relation to the duty variable of that particular port needs to be identified first. Hence, using (5) and Table I for the switching current expressions, the

port-1 switching leg currents $i_{L1,1}$ and $i_{L1,2}$ are formulated in (19) shown at the bottom of the this page. Both the expressions highlight that the port-1 switching currents only depend on duty variable δ_1 associated with its own port among all three existing duty variables. It can be also observed that for $m_{12} < 1$ and $m_{13} < 1$, $|i_{L1,2}| > |i_{L1,1}|$ holds true, which indicates that the lagging leg of port-1 will always undergo soft-turn ON if the leading leg turns ON under ZVS. Thus, the optimal value of δ_1, $\delta_{1,\text{opt}}$ can be identified by equating $i_{L1,1}$ to the critical ZVS current requirement for leading leg of Port-1 $i_{L1,1,\text{crit}}$, calculated from Table II. In real implementation, while calculating optimal duty $\delta_{1,\text{opt}}$, the phase-shift varibles (φ_2 and φ_3) given in (22) are fetched from PI controller outputs those dynamically varies to track the output voltages and loads.

Similar to Port-1, the switching currents of port-2, $i_{L2,1}$, $i_{L2,2}$, and port-3, $i_{L3,1}$, $i_{L3,2}$, are also calculated using superposition theorem of (5) and DAB current expressions from Table I, and are shown in (20) and (21) shown at the bottom of the this page.

Now, it is observed from (20) and (21) that $|i_{L2,2}| > |i_{L2,1}|$ and $|i_{L3,1}| = |i_{L3,2}|$ hold true for same set of control variables. In other words, the soft-switching performance of port-2 should be determined by actively setting $i_{L2,1}$ at a current above or at its critical ZVS current requirement, $i_{L2,1,\text{crit}}$ as found from Table II. Further, under this operating mode combination, both the legs of port-3 experience the same switching current stress. Thus, equating $i_{L3,1}$ to $i_{L3,1,\text{crit}}$ will give the optimized duty for port-3. The optimal duty values are presented in (22)–(24) shown at the bottom of the this page.

B. Mode-111 (DAB-L_{12} in Mode 1, DAB-L_{13} in Mode 1, DAB-L_{23} in Mode 1)

TAB operates at this mode in heavy loading scenarios, which is defined as $\varphi_2 > (1-m_{12})\pi/2$, $\varphi_3 > (1-m_{13})\pi/2$ and $(\varphi_3-\varphi_2) > (1-m_{23})\pi/2$. The formulated port-1 switching leg currents $i_{L1,1}$ and $i_{L1,2}$, in this mode are expressed in (25)

$$\begin{cases} i_{L1,1} = -pu_{12}\left[-m_{12}\varphi_2 + (1-m_{12})\,\pi/2\,\right] - pu_{13}\left[-m_{13}\varphi_3 + (1-m_{13})\,\pi/2\,\right] + \delta_1\left[pu_{12}\,(1-m_{12}) + pu_{13}\,(1-m_{13})\right] \\ i_{L1,2} = pu_{12}\left[m_{12}\varphi_2 + (1-m_{12})\,\pi/2\right] + pu_{13}\left[m_{13}\varphi_3 + (1-m_{13})\,\pi/2\right] - \delta_1\left[pu_{12}\,(1-m_{12}) + pu_{13}\,(1-m_{13})\right] \end{cases} \tag{19}$$

$$\begin{cases} i_{L2,1} = -pu_{12}\left[\delta_1 - m_{12}\delta_2 - (1-m_{12})\,\pi/2\right] - pu_{23}\left[-m_{23}\,(\varphi_3-\varphi_2) - (1-m_{23})\,\delta_2 + (1-m_{23})\,\pi/2\right] \\ i_{L2,2} = pu_{12}\left[\delta_1 - m_{12}\delta_2 - (1-m_{12})\,\pi/2\right] + pu_{23}\left[m_{23}\,(\varphi_3-\varphi_2) - (1-m_{23})\,\delta_2 + (1-m_{23})\,\pi/2\right] \end{cases} \tag{20}$$

$$\begin{cases} i_{L3,1} = -pu_{13}\left[\delta_1 - m_{13}\delta_3 - (1-m_{13})\,\pi/2\right] - pu_{23}\left[\delta_2 - m_{23}\delta_3 - (1-m_{23})\,\pi/2\right] \\ i_{L3,2} = pu_{13}\left[\delta_1 - m_{13}\delta_3 - (1-m_{13})\,\pi/2\right] + pu_{23}\left[\delta_2 - m_{23}\delta_3 - (1-m_{23})\,\pi/2\right] = -i_{L3,1} \end{cases} \tag{21}$$

$$\delta_{1,\text{opt}} = \max\left[0, \frac{i_{L1,1,\text{crit}} + pu_{12}\left[-m_{12}\varphi_2 + (1-m_{12})\,\pi/2\,\right] + pu_{13}\left[-m_{13}\varphi_3 + (1-m_{13})\,\pi/2\right]}{pu_{12}\,(1-m_{12}) + pu_{13}\,(1-m_{13})}\right] \tag{22}$$

$$\delta_{2,\text{opt}} = \max\left[0, \frac{i_{L2,1,\text{crit}} + pu_{12}\left[\delta_{1,\text{opt}} - (1-m_{12})\,\pi/2\right] + pu_{23}\left[-m_{23}\,(\varphi_3-\varphi_2) + (1-m_{23})\,\pi/2\right]}{pu_{12}m_{12} + pu_{23}\,(1-m_{23})}\right]. \tag{23}$$

$$\delta_{3,\text{opt}} = \max\left[0, \frac{i_{L3,1,\text{crit}} + pu_{13}\left[\delta_{1,\text{opt}} - (1-m_{13})\,\pi/2\right] + pu_{23}\left[\delta_{2,\text{opt}} - (1-m_{23})\,\pi/2\right]}{pu_{13}m_{13} + pu_{23}m_{23}}\right]. \tag{24}$$

$$\begin{cases} i_{L1,1} = -pu_{12}\left[m_{12}\varphi_2 + (1-m_{12})\,\pi/2\,\right] - pu_{13}\left[m_{13}\varphi_3 + (1-m_{13})\,\pi/2\,\right] + \delta_1\left[pu_{12}\,(1+m_{12}) + pu_{13}\,(1+m_{13})\right] \\ i_{L1,2} = pu_{12}\left[m_{12}\varphi_2 - (1-m_{12})\,\pi/2\right] + pu_{13}\left[m_{13}\varphi_3 - (1-m_{13})\,\pi/2\right] - \delta_1\left[pu_{12}\,(1-m_{12}) + pu_{13}\,(1-m_{13})\right] \end{cases} \tag{25}$$

$$\begin{cases} i_{L2,1} = -pu_{12}\left[\varphi_2 - (1-m_{12})\,\pi/2\right] - pu_{23}\left[m_{23}\,(\varphi_3-\varphi_2) + (1-m_{23})\,\pi/2\right] - \delta_2\left[pu_{12}\,(1-m_{12}) - pu_{23}\,(1+m_{23})\right] \\ i_{L2,2} = pu_{12}\left[\varphi_2 - (1+m_{12})\,\delta_2 - (1-m_{12})\,\pi/2\right] + pu_{23}\left[m_{23}\,(\varphi_3-\varphi_2) - (1-m_{23})\,\delta_2 + (1-m_{23})\,\pi/2\right] \end{cases} \tag{26}$$

$$\begin{cases} i_{L3,1} = -pu_{13}\left[\varphi_3 + (1-m_{13})\,\delta_3 - (1-m_{13})\,\pi/2\right] - pu_{13}\left[(\varphi_3-\varphi_2) + (1-m_{23})\,\delta_3 - (1-m_{23})\,\pi/2\right] \\ i_{L3,2} = pu_{13}\left[\varphi_3 - (1+m_{13})\,\delta_3 - (1-m_{13})\,\pi/2\right] + pu_{23}\left[(\varphi_3-\varphi_2) - (1+m_{23})\,\delta_3 - (1-m_{23})\,\pi/2\right] \end{cases} \tag{27}$$

$$\delta_{1,\text{opt}} = \max\left[0, \frac{i_{L1,1,\text{crit}} + pu_{12}\left[m_{12}\varphi_2 + (1-m_{12})\,\pi/2\,\right] + pu_{13}\left[m_{13}\varphi_3 + (1-m_{13})\,\pi/2\,\right]}{pu_{12}\,(1+m_{12}) + pu_{13}\,(1+m_{13})}\right]. \tag{28}$$

$$\delta_{2,\text{opt}} = \max\left[0, \frac{-i_{L2,1,\text{crit}} - pu_{12}\left[\varphi_2 - \frac{(1-m_{12})\pi}{2}\right] - pu_{23}\left[m_{23}\,(\varphi_3-\varphi_2) + (1-m_{23})\,\pi/2\right]}{pu_{12}\,(1-m_{12}) - pu_{23}\,(1+m_{23})}\right] \tag{29}$$

$$\delta_{3,\text{opt}} = \max\left[0, \frac{-i_{L3,2,\text{crit}} + pu_{13}\left[\varphi_3 - (1-m_{13})\,\pi/2\right] + pu_{23}\left[(\varphi_3-\varphi_2) - (1-m_{23})\,\pi/2\right]}{pu_{13}\,(1+m_{13}) + pu_{23}\,(1+m_{23})}\right]. \tag{30}$$

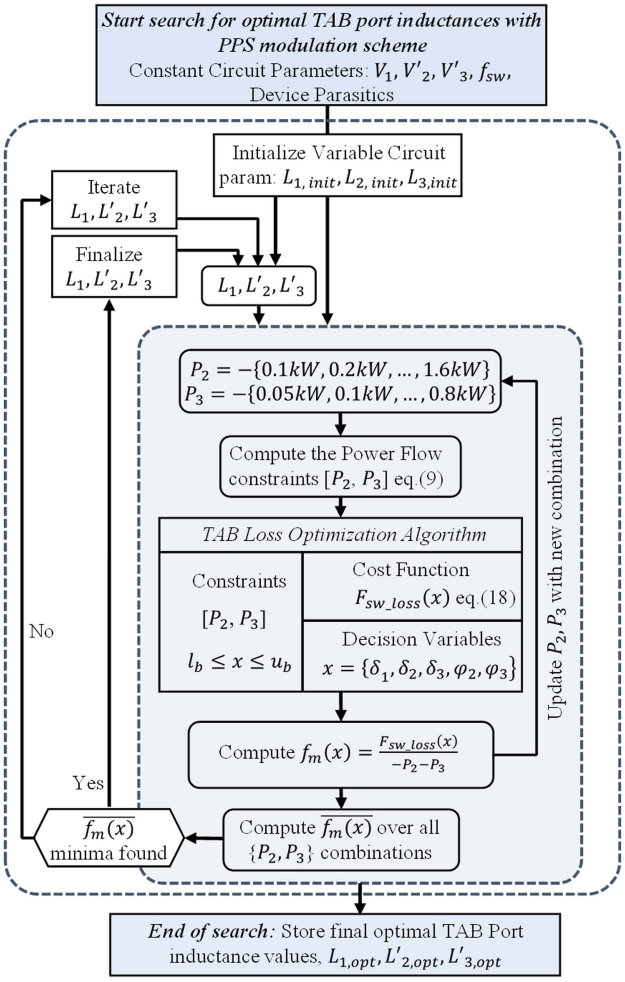

Fig. 10. Flowchart depicting the TAB Port inductance optimization process.

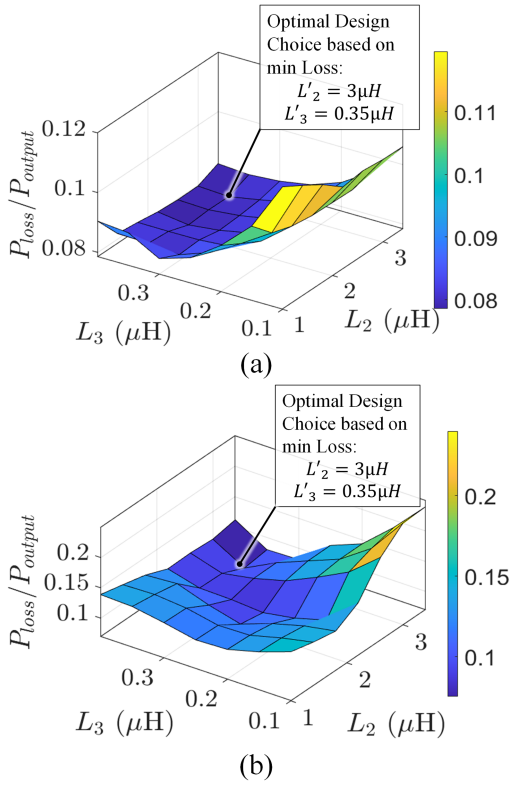

Fig. 11. Optimal choice of $L'_{2,\text{opt}}$ and $L'_{3,\text{opt}}$ for (a) $\{V_1, V'_2, V'_3\} = \{160\text{ V}, 120\text{ V}, 28\text{ V}\}$ and (b) $\{V_1, V'_2, V'_3\} = \{160\text{ V}, 110\text{ V}, 16\text{ V}\}$.

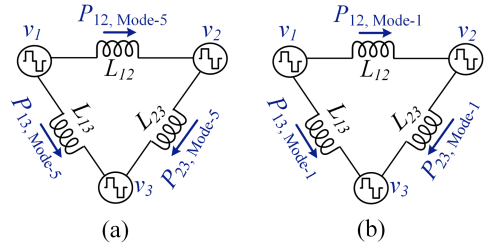

Fig. 12. TAB power flow modes under consideration for formulating the PWM scheme.

shown at the bottom of the previous page, which advocates that these currents only depend on δ_1, duty variable associated with its port-1. Thus, by compensating δ_1, the desired switching currents ($i_{L1,1}$ and $i_{L1,2}$) can be attained that ensures soft-switching. Notably, for $m_{12} < 1$ and $m_{13} < 1$, $|i_{L1,2}| > |i_{L1,1}|$, which indicates that the lagging leg of port-1 always undergo soft-turn ON if the leading leg turns ON under ZVS. Thus, the optimal value of δ_1, $\delta_{1,\text{opt}}$ can be identified by equating $i_{L1,1}$ to the critical ZVS current requirement for the leading leg of Port-1 $i_{L1,1,\text{crit}}$, calculated from Table II.

In a similar manner as with Port-1, the switching currents for Port-2, denoted as $i_{L2,1}$, $i_{L2,2}$ as well as for Port-3, denoted as $i_{L3,1}$, $i_{L3,2}$, are computed utilizing the superposition theorem. These calculations are presented in (26) and (27) shown at the bottom of the previous page, accordingly. Now, it is observed from (27) that $|i_{L3,1}|$ will always be smaller than $|i_{L3,2}|$ for same set of control variables. In other words, the soft-switching performance of port-3 should be determined by actively setting $i_{L3,2}$ at a current above or at its critical ZVS current requirement, $i_{L3,2,\text{crit}}$. Thus, the ZVS current tracked optimized duty values are presented in (28)–(30) shown at the bottom of the previous page.

Similar to the Mode-555 and Mode-111 mentioned above, the mathematically optimal duty synthesis work is rigorously carried out for other possible power flow combinations and presented in the Appendix. Thus, a complete soft-switching enabled switching modulation strategy (ZCTSM) is developed that optimizes the performance of the TAB converter by compensating the bridge duty variables online. The special feature of this PWM technique is its ability to track and intelligently set the switching instant currents at all three TAB ports, facilitating superior soft-switching performance throughout a wide load and gain range. In order to check its usefulness, its performance is validated against the existing TAB modulation techniques such as sum of RMS current optimized modulation (ROM) [12], [16], [17], [24] and the traditional DPS modulation (DPSM) [14]. It needs to be noted that the implementation of ROM is done

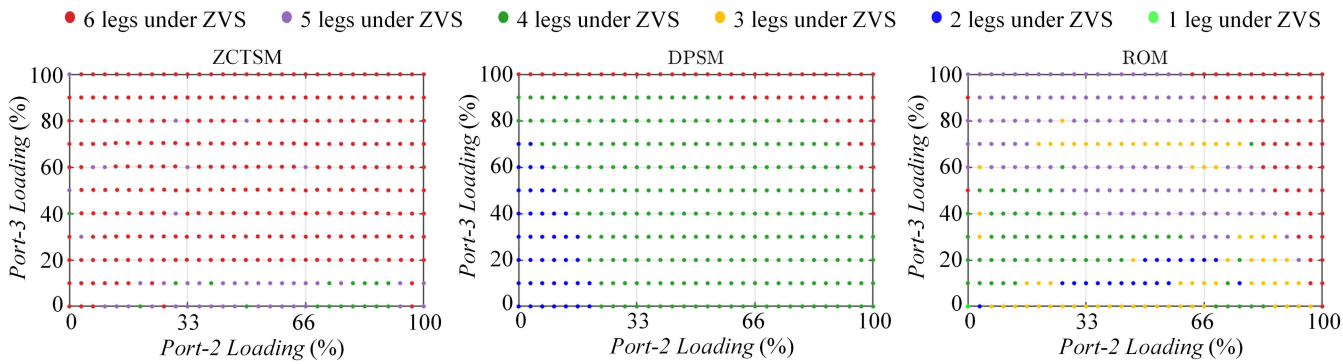

Fig. 13. Soft-switching performance analysis of different TAB control schemes (ZCTSM, DPSM, and ROM) with varying output loads under mismatched DC port-voltages $\{V_1, V'_2, V'_3\}$ ={160 V, 100 V, 16 V}.

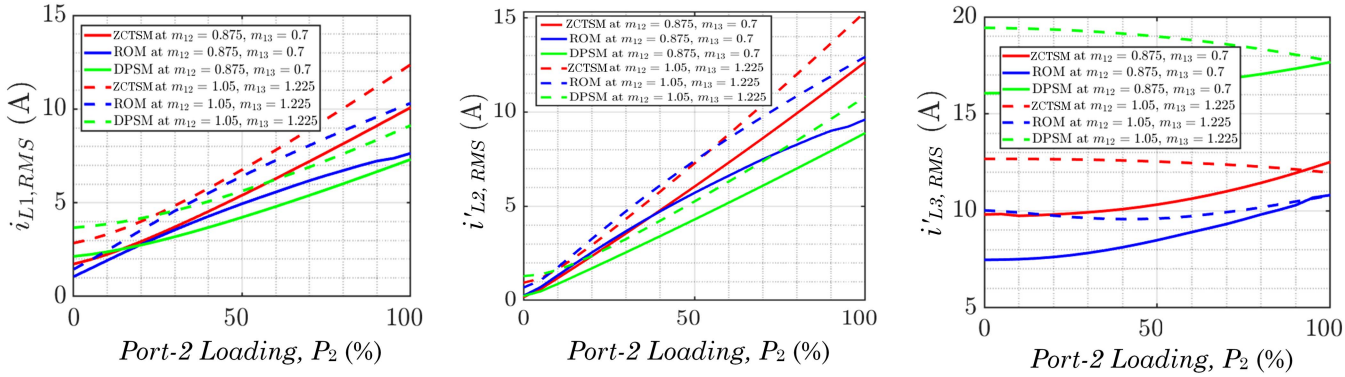

Fig. 14. Variation in the TAB port inductor current RMSs with increasing Port-2 load (P_2) while $P_3 = 20\%$ loading under different switching schemes: ZCTSM, ROM, and DPSM.

using LUT [16], or gradient decent method [12], [17], or ANN model [24] based approaches that are computationally expensive and memory intensive compared to the proposed ZCTSM algorithm.

Fig. 13 showcases a comparison of the ZVS performances of the three modulation techniques under a wide variation in the converter output powers P_2 and P_3 for under-unity gain output port voltages: $\{V_1, V'_2, V'_3\} = \{160\text{ V},\ 100\text{ V},\ 16\text{ V}\}$. The results are based on the TAB converter under study, the specifications of which are noted in Table III. It is clearly observable from Fig. 13 that under the application of the ZCTSM strategy, all the six switching legs undergo soft switching for most of the load range. However, with ROM and DPSM schemes, only 2–4 legs experience soft-switching at lighter load region. All six legs are soft-switched only for a limited load range near the highest load operating point, i.e., both port-2 and port-3 loading above 80%. Hence, it is clear that the ZVS performance of the ZCTSM is significantly better than its counterparts at very light load operation that ensures a better light load efficiency and better EMI performance of the converter throughout its entire load range.

In addition, we evaluate the performance of the ZCTSM scheme in comparison to ROM and DPSM schemes, focusing on TAB winding current root mean square (RMS) values, as depicted in Fig. 14. While ZCTSM may not directly optimize the inductor current RMS, it strategically sets one or more switching peak currents at their desired values. Consequently, it optimizes inductor current peaks, leading to a reduction in RMS, albeit not as explicitly as in optimized scenarios. Hence, we expect it to perform better than DPSM but worse than ROM in terms of inductor RMS currents over all load range. Furthermore, under lighter loading conditions, ZCTSM maintains MOSFET soft-switching by elevating switching peak currents. This strategy trades off some conduction loss to achieve significant gains in switching loss at such loading conditions. Consequently, we anticipate that ZCTSM will exhibit higher RMS current compared to other modulation techniques under extremely light loads. In Fig. 14, it can be observed that with increasing port-2 loading, P_2, while maintaining constant P_3 load at 20% the port-1 and port-2 current RMSs, $i_{L1,\,\mathrm{RMS}}$, $i'_{L2,\,\mathrm{RMS}}$ observes a rapid increase while the port-3 current RMS $i_{L3,\,\mathrm{RMS}}$ does not vary that significantly. Further, with DPSM the high-voltage port winding currents $i_{L1,\,\mathrm{RMS}}$ and $i_{L2,\,\mathrm{RMS}}$ are observed to be exhibiting lower values compared to values encountered during ZCTSM and ROM strategies. However, the average $i'_{L3,\,\mathrm{RMS}}$ under ZCTSM showcases a 55% reduction compared to the DPSM, which is further reduced by 14% when the ROM scheme is employed.

TABLE III
DESIGN SPECIFICATION OF THE FABRICATED TAB CONVERTER

Circuit Parameters	*Specifications*
Operating Voltages	Input Port: V_1 = 160 Vdc Output Port-1: V'_2 = 100–130 Vdc; 115 Vdc nominal Output Port-2: V'_3 = 16–28 Vdc
Max Operating Current	Output Port-1: I'_2 = 14 A Output Port-2: I'_3 = 30 A
Max Operating Power	Output Port-1: P_2 = 1.6 kW Output Port-2: P_3 = 0.8 kW
Port-1 H-Bridge Switches $S_{11} - S_{14}$	GS66516T, 650 V/60 A/25$m\Omega$ @ 25 °C GaN E-HEMT, 2 device in parallel per switch position, Driver: Si8271
Port-2 H-Bridge Switches $S_{21} - S_{24}$	EPC2215, 200 V/42 A/8$m\Omega$ @ 25 °C GaN E-HEMT, 2 device in parallel per switch position, Driver: NCP51820AMNTWG
Port-3 H-Bridge Switches $S_{31} - S_{34}$	EPC2020, 60 V/90 A/2.2$m\Omega$ @ 25 °C GaN E-HEMT, 2 device in parallel per switch position, Driver: µP1966E
Port-1 DC Link Capacitor (C_1)	40 µF/250 V 1 X B58033I5206M001 9 X C2220X225K251T 12 X CGA4J3X7R2E223K125AA
Port-2 DC Link Capacitor (C_2)	35 µF/250 V 10 X C2220X225K251T 4 X KTJ251B335M76BFT00 24 X CGA4J3X7R2E223K125AA
Port-3 DC Link Capacitor (C_3)	120 µF/63 V 5 X KCM55WR71J226MH01K 10 X 08051C105K4Z2A
DC Blocking Capacitors (C_{b1}, C_{b2}, C_{b3})	10 $\mu F/250\ V$, 12 $\mu F/250\ V$, 120 $\mu F/63\ V$
Transformer	Turns Ratio: $n_1 : n_2 : n_3 = 7 : 5 : 1$ Magnetizing Inductance: $L_m = 603\ \mu H$ Leakage Inductances of port-1, 2, 3: 0.4 µH, 0.4 µH, 14 nH PCB Winding-1: 10 layers, 5 Prim & 5 sec turns, 4oz PCB PCB Winding-2: 6 layers, 2 Prim & 1 ter turns (4 turns in parallel), 4oz PCB Core: 2X FR43808EC, R material, no airgap
Inductor L_1	Inductance: 5.8 µH Winding: 4 turns, AWG 14 Litz wire Core: 2 X 0R43618EC, R material, airgap = 0.45 mm
Inductor L'_2	Inductance: 2.8 µH Winding: 4 turns, AWG 10 Litz wire Core: 1 X 0R43618EC, R material, airgap = 0.45 mm
Inductor L'_3	Inductance: 0.32 µH Winding: 1 turn, 2 AWG 14 Litz wire in parallel Core: 1 X 0R43618EC, R material
Switching frequency (f_{sw})	100 kHz

VI. HARDWARE PROTOTYPING AND EXPERIMENTAL RESULTS

Upon finalizing the TAB control scheme, its performance is validated by implementing it in a fabricated TAB converter setup. The details of the experimental verification are highlighted in this section.

A. Hardware Details and Implemented Control Strategy

Following the design optimization methodology outlined in Section IV, a proof-of-concept 2.4-kW TAB hardware is designed and fabricated, as shown in Fig. 15. The design targeted a wide gain range operation as specified in Table III, which also lists the salient parameters of the converter. The port voltage specifications ($V_1 = 160$ V; $V'_2 = 100 - 130$ V; $V'_3 = 16 - 28$ V) comply with a targeted space shuttle application. To enhance the power density and take advantage of HF switching, all capacitors in the circuit were implemented using ceramic technology, and the magnetic components were made using planar cores and PCB integrated windings. A photograph of the switching circuit and its auxiliary components as part of the power stage excluding magnetic components is depicted in Fig. 16.

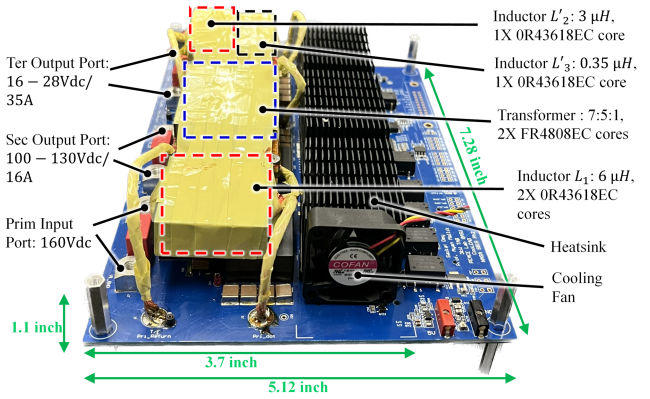

Fig. 15. Assembly of complete TAB converter prototype with marked magnetic components and thermal management system. The highlighted area of the converter excluding the control and gate driver components is used for power density calculation.

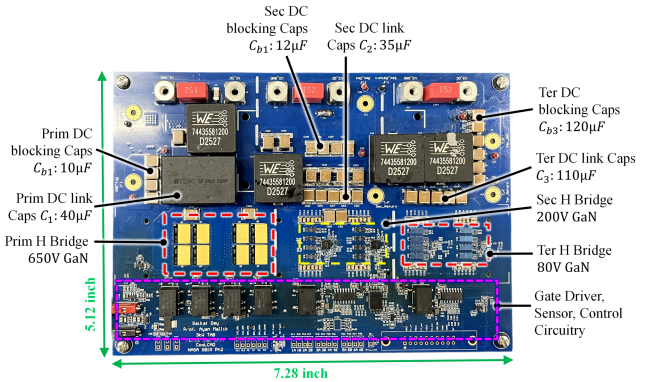

Fig. 16. Photograph of the fabricated TAB converter circuit board with highlighted parallel connected power devices, DC link and DC blocking capacitors, gate driver, and sensor circuitry.

In order to reduce the conduction and switching losses, all the switches in the TAB H-bridges are realized using parallelly connected GaN MOSFETs. The magnetic components' design utilized multiobjective loss optimization to determine core geometry, number of turns, number of layers, and copper thickness [34]. Dowell's equations [35] and the iGSE method [36] were employed for winding loss and core loss modeling, respectively. The final construction details of all four magnetic components: three-winding TAB transformer and three HF port inductors are summarized in Table III. Both the inductor L_1 and transformer cores are constructed by connecting two individual E-shaped cores in a 1X2 matrix fashion by analyzing the tradeoff between the core loss and the core volume. The completed prototype achieved a power density of 81 W/inch^3 and 60 W/inch^3 (5.4 kW/kg) while excluding and including the control stage in the calculation, respectively.

The proposed TAB control strategy is implemented using a dual-core TMS320F28379D control card. A block diagram of the control system is illustrated in Fig. 17. The controller

TABLE IV
PERFORMANCE COMPARISON OF THE PROPOSED CONTROL SCHEME WITH RECENTLY EVALUATED TAB CONTROL TECHNOLOGIES

Categories of Optimized Control Techniques for TAB		Criteria for Comparison: Research Works	Converter Specification	Modulation Technique	Switching Frequency	Peak-efficiency	Optimization Target	ZVS Analysis	Soft-switching Ability	Off-line Computation Needed	Accuracy in Optimization Process	Memory Allocation Burden	Code Execution Time	Scalability
Look-up Table based Computation		[14]	300 V/42 V/14 V 1.5 kW	PPS	100 kHz	91.70%	Conduction Loss	NA	Low	Yes	Low	High	Low	Low
		[13]	160 V/120 V/22 V 800 W	PPS	100 kHz	96.52%	Switching Loss	Not precise	High	Yes	High	High	Low	Low
		[17]	400 V/450 V/14 V 650 W	PPS	100 kHz	97.60%	Conduction Loss	NA	Low	Yes	Medium	High	Low	Low
		[18]	380 V/380 V/48 V 1.2 kW	PPS	100 kHz	96%	Conduction + Switching Loss	Not precise	High	Yes	High	High	Low	Low
Machine Learning based Computation		[20]	400 V/250 V/250 V 2 kW	PPS	20 kHz	96.50%	Winding RMS Currents	NA	Low	Yes	High	High	High	High
		[24]	400 V/400 V/400 V 10 kW	PPS	40 kHz	NA	Winding RMS Currents	NA	Low	Yes	High	High	High	High
Polynomial Regression fitted Model based Calculation		[31]	160 V/120 V/22 V 800 W	PPS	100 kHz	96.52%	Conduction + Switching Loss	Not precise	Medium	Yes	Medium	Low	Medium	High
On-line Calculation w/o Requiring Offline Computation	Gradient Decent	[12]	160 V/120 V/22 V 800 W	PPS	100 kHz	96.55%	Conduction Loss	NA	Low-Medium	No	High	Low	High	Low
	Multidimensional Ripple Correlation	[23]	400 V/400 V/400 V 10 kW	PPS	40 kHz	NA	Input Current/ Winding Current RMS	NA	Low-Medium	No	High	High	High	Low
	Magnetizing Inductance based ZVS	[19]	350 V/450 V/14 V 2.5 kW	QPS	100 kHz	96.60%	Switching Loss	Not precise	Medium-High	No	Low	Low	Medium	Low
	ZCTSM	**Proposed Work**	160 V/120 V/28 V 2.4 kW	PPS	100 kHz	96.80%	Switching Loss	Precise	High	No	High	Low	Medium	Medium

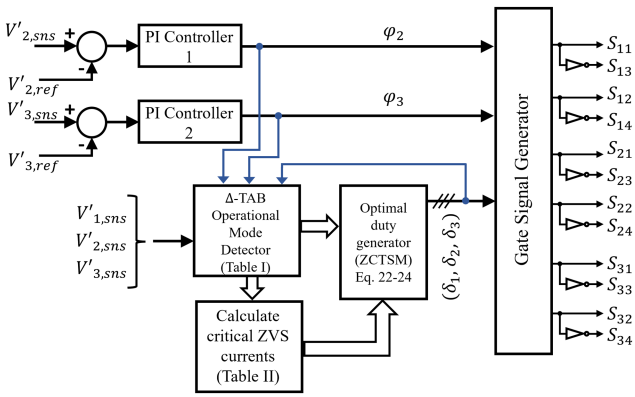

Fig. 17. Block diagram of the implemented ZCTSM control system.

utilized sensed output port voltages and control variables from previous samples to construct the required ZVS current thresholds for the present state. Operating duty variables are formulated based on the mode of TAB operation, and phase shift variables were generated from two individual proportional integral (PI) control loops. Finally, the desired gating signals were generated with the optimal phase compensations, ensuring ZVS-current tracked soft-switched operation of the converter. In order to enhance the computational efficiency of implemented code execution pertaining to calculation of the optimal TAB duty cycles within a microcontroller environment, which is characterized by multiple arithmetic operations such as multiplications, additions, and divisions a strategic optimization approach is proposed employing the following methods. First, precomputation and caching techniques are implemented by calculating frequently used multiplication results in advance and storing them in dedicated floating-point registers or memory locations. Second, the cached results are utilized by incorporating precomputed values into subsequent multiplication operations, thereby eliminating redundant recalculations and expediting execution. Third, division operations are minimized by substituting divisions with reciprocal multiplications whenever possible to mitigate resource-intensive computations. In addition, the use of fixed-point arithmetic is explored, evaluating its potential when precision requirements can be met with reduced bit-width representations. Thus, following this optimized program execution, the computation time of optimal TAB duty cycles using the TMS320F28379D DSP is benchmarked to be 2.3 μs, comfortably below a switching time period of 10 μs.

Furthermore, a detailed comparison between several recently proposed TAB control schemes and the proposed technology in terms of controller performance is presented in Table IV. Notably, among the online optimizable TAB control strategies, only the proposed ZCTSM scheme aims to ensure soft-switching operation across the entire load range, from no load to full load, without overburdening the controller with challenges related to memory allocation and code execution time. An optimized TAB control scheme can be chosen from the list given in Table IV, based on the converter design requirement and specifications related to the implemented control strategy.

B. *Verification of Steady State Operation*

For experimental benchmarking, the performance of the proposed soft-switching control (ZCTSM) is compared with the winding current RMS optimized modulation strategy (ROM) and the conventional simple phase compensation-based DPS control (DPSM). For the steady-state operation verification, two separate loading conditions (light as well as heavy load) at different port voltages are selected.

1) Light Load Operation Verification: Fig. 18 presents the steady-state operating waveforms of the TAB ac port voltages and HF inductor currents under the three PWM schemes at

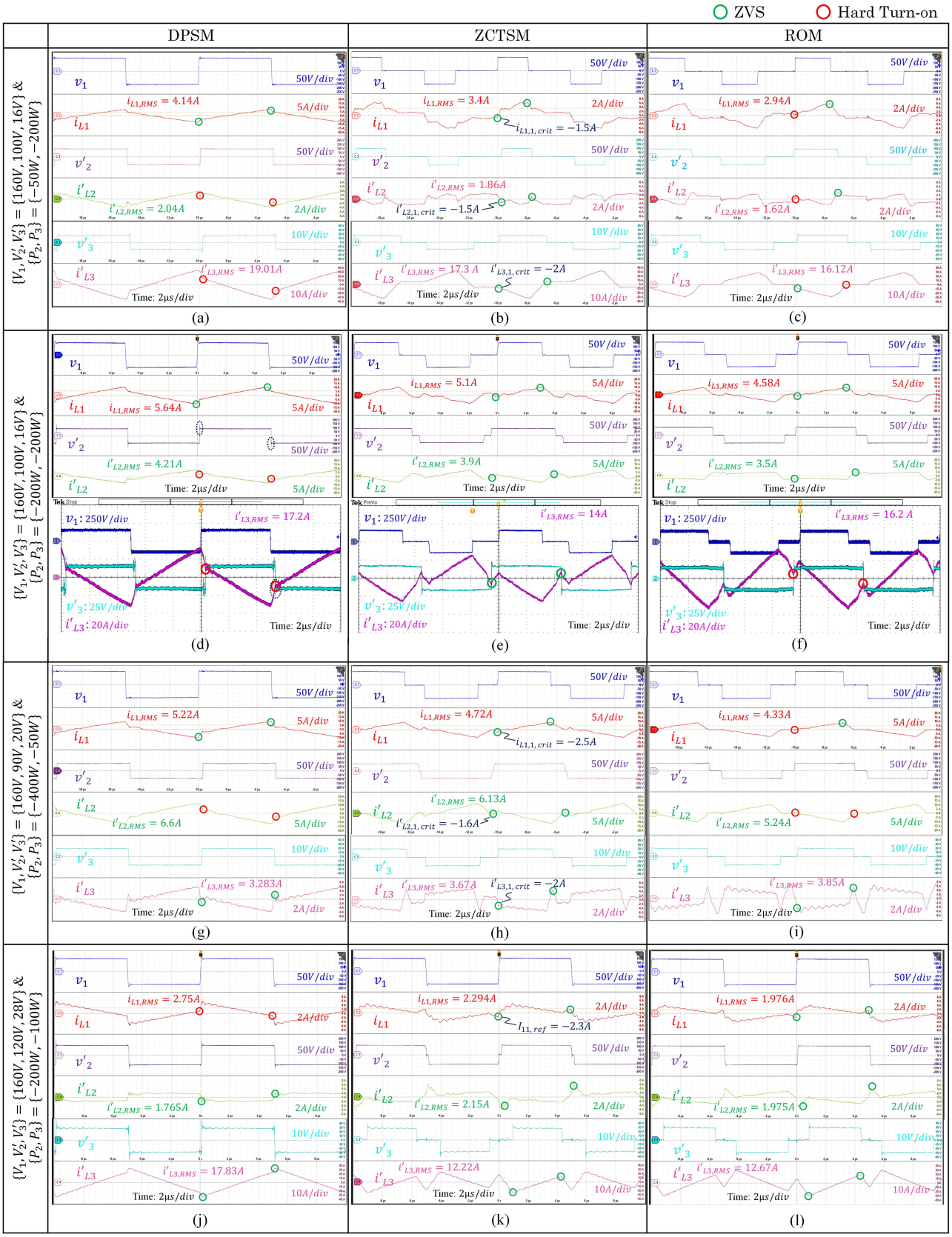

Fig. 18. Experimental steady state TAB circuit waveforms at four different light load conditions under following PWM schemes: (a), (d), (g), (i) DPSM, (b), (e), (h), (k) Proposed ZCTSM, and (c), (f), (i), (l) ROM. (a)–(c) Waveforms at $V_1 = 160$ V, $V'_2 = 100$ V, $V'_3 = 16$ V, $P_2 = -50$ W, and $P_3 = -200$ W. (d)–(f) Waveforms at $V_1 = 160$ V, $V'_2 = 100$ V, $V'_3 = 16$ V, $P_2 = -200$ W, and $P_3 = -200$ W. (g)–(i) Waveforms at $V_1 = 160$ V, $V'_2 = 90$ V, $V'_3 = 20$ V, $P_2 = -400$ W, and $P_3 = -50$ W. (j)–(l) Waveforms at $V_1 = 160$ V, $V'_2 = 120$ V, $V'_3 = 28$ V, $P_2 = -200$ W, and $P_3 =$–100 W.

four separate light load settings, whose operating conditions are defined as, expt-1: Fig. 18(a)–(c) $\{V_1, V'_2, V'_3, P_2, P_3\} = \{160\text{ V}, 100\text{ V}, 16\text{ V}, -50\text{ W}, -200\text{ W}\}$, expt-2: Fig. 18(d)–(f) $\{160\text{ V}, 100\text{ V}, 16\text{ V}, -200\text{ W}, -200\text{ W}\}$, expt-3: Fig. 18(g)–(i) $\{V_1, V'_2, V'_3, P_2, P_3\} = \{160\text{ V}, 90\text{ V}, 20\text{ V}, -400\text{ W}, -50\text{ W}\}$ and expt-4: Fig. 18(j)–(l) $\{V_1, V'_2, V'_3, P_2, P_3\} = \{160\text{ V}, 120\text{ V}, 28\text{ V}, -200\text{ W}, -100\text{ W}\}$. The proposed ZCTSM strategy determines the duty variables for the TAB bridges based on the specific TAB operating modes as highlighted in the earlier section. In expt-1 and 2, the TAB operates in mode 555 where DAB-L_{12}, DAB-L_{13}, and DAB-L_{23} are in mode 5. In expt-3, mode 555 is again utilized with power flowing from port-3 to port-2 in DAB-L_{23}. Finally, expt-4 highlights mode 144 operation, i.e., DAB-L_{12} in mode 1, while DAB-L_{13} and DAB-L_{23} both act in mode 4. It can be clearly seen in the waveforms that as desired by the proposed algorithm, ZCTSM tracks the switching instant port inductor currents at their required critical ZVS current values. With this approach, the port-1 duty variable δ_1 is determined as 0.97, 0.628, 0.417, and 0.03 radian with computed $i_{L1,1,\text{crit}}$ being set at -1.5 A, -1.6 A, -2.5 A, and -2.3 A, in expt-1, 2, 3, and 4, respectively. Similarly, the duty variables of the other bridges are also determined so that a complete ZVS operation can be attained. Further, under light load scenario, reducing the switching loss becomes a major goal as it mostly determines the system efficiency. Since the DPSM does not involve the duty-cycle modulation, it is more prone to losing soft-switching and it incurs a higher switching loss due to high switching peak currents accompanied by hard-switching at some HF legs. In expt-1 to 4, under DPSM control method four (all legs of port-2 and port-3), four (all legs of port-2 and port-3), two (both port-2 legs), and two (both port-1 legs) of the six switching legs experience hard turn-ON, respectively. Under the four test cases of expt-1 to 4, the total switching peak currents and RMS inductor currents under DPSM are measured to be 36% and 15% higher on average compared to ZCTSM, respectively. From the perspective of inductor current RMSs, the ROM scheme outperformed the ZCTSM and DPSM by an average of 6.8% and 18% less total RMS inductor current and thus, incurs the least conduction loss. However, with the ROM control, the TAB losses ZVS at three (leading legs of primary and secondary bridge, lagging leg of tertiary bridge), two (both legs of tertiary bridge), and three (both port-2 legs and leading port-1 bridge leg) switching legs in expt-1, 2, and 2, correspondingly. Therefore, the proposed ZCTSM scheme with all-ZVS legs and critical ZVS current tracked operation achieves a 26% lower average switching loss compared to the ROM scheme at these lighter load test conditions. The overall converter efficiency observed in the steady state operations stated in expt-1 to 4 are 86.4%, 88.7%, 90.3%, and 90.1%, under the DPSM strategy. The similar efficiency numbers evaluated under ZCTSM and ROM are measured as 91.7%, 93.4%, 94.1%, 93.9%, and 89.8%, 92.4%, 93.2%, 93.9%, respectively. It is concluded from the experimental results that at a lighter load, ZCTSM outperforms the ROM scheme by a substantial margin due to its soft-switched device performance with an average efficiency benefit of 0.7%.

2) Heavy-Load Operation Verification: The performance of the TAB is also examined at heavier loads under the three different PWM strategies, as illustrated in Fig. 19. Fig. 19(a)–(c) highlights the steady state results when port-1 is transferring 1000 and 500 W to port-2 and port-3 outputs regulated at 100 and 16 V, respectively. Conversely, Fig. 19(d)–(f) scrutinizes the TAB's behavior at the rated load of 2.4 kW, with port-2 and port-3 voltages stabilized at 120 and 28 V. It is observed from the waveforms that at such heavy loading conditions, all the six switching legs undergo ZVS with all three switching schemes. In Fig. 19(b) and (e), under the ZCTSM scheme the converter operates mode 115 (DAB-L_{12} in mode 1, DAB-L_{13} in mode 1, DAB-L_{23} in mode 5) and mode 111 (DAB-L_{12} in mode 1, DAB-L_{13} in mode 1, DAB-L_{23} in mode 1), respectively and accordingly the optimal duty variables are deduced that ensures soft-switching while tracking critical ZVS current. From Fig. 19(b), it is observable that the ZCTSM scheme tracks the implemented critical ZVS current ($i'_{L1,1,\text{crit}} = -3$ A) in order to optimize the primary bridge duty cycle that reduces the switching loss in the system. As a by-product of switching loss optimization, the RMS winding currents are also reduced by an average margin of 24% under ZCTSM when compared to DPSM. However, the ROM optimizes the RMS currents further and saves 9% more conduction loss compared to ZCTSM. The overall converter efficiency reveals values of 93.4%, 96.3%, and 96.5% under DPSM, ZCTSM, and ROM schemes, respectively, during power transfer of 1000 W (port-2) and 500 W (port-3) loads. Additionally, under the rated 2.4 kW loading scenario, the observed efficiencies are 93.6%, 96.57%, and 96.7% for DPSM, ZCTSM, and ROM, respectively.

C. Power Loss and Efficiency Results and Comparison

The efficiency of the developed TAB converter is thoroughly assessed through experimental evaluation, as depicted in Fig. 20. The evaluation considers the proposed modulation technique, ROM, alongside the conventional DPSM, across a broad spectrum of output loads connected at port-2 and port-3. The port-2 and port-3 voltages are maintained at 100 and 16 V, respectively, for consistency. Fig. 20(a) presents a comprehensive three-dimensional (3-D) efficiency map, supplemented by two 2-D efficiency plots in Fig. 20(b) and (c), illustrating varying loads at port-2 while port-3 remains at full and half loads, respectively. Furthermore, the estimated TAB converter efficiency calculated based on analytically developed loss models of the power stage components is compared with the measured hardware efficiency under the application of the proposed ZCTSM scheme, as showcased in Fig. 20(b) and (c).

The analytical efficiency data exhibits an average error of 0.4% compared to the experimental data. This discrepancy is primarily attributed to unaccounted losses caused by PCB parasitics, including trace resistances, termination resistances, and mismatch between practical device losses and the calculated conduction and switching losses derived using datasheet parameters.

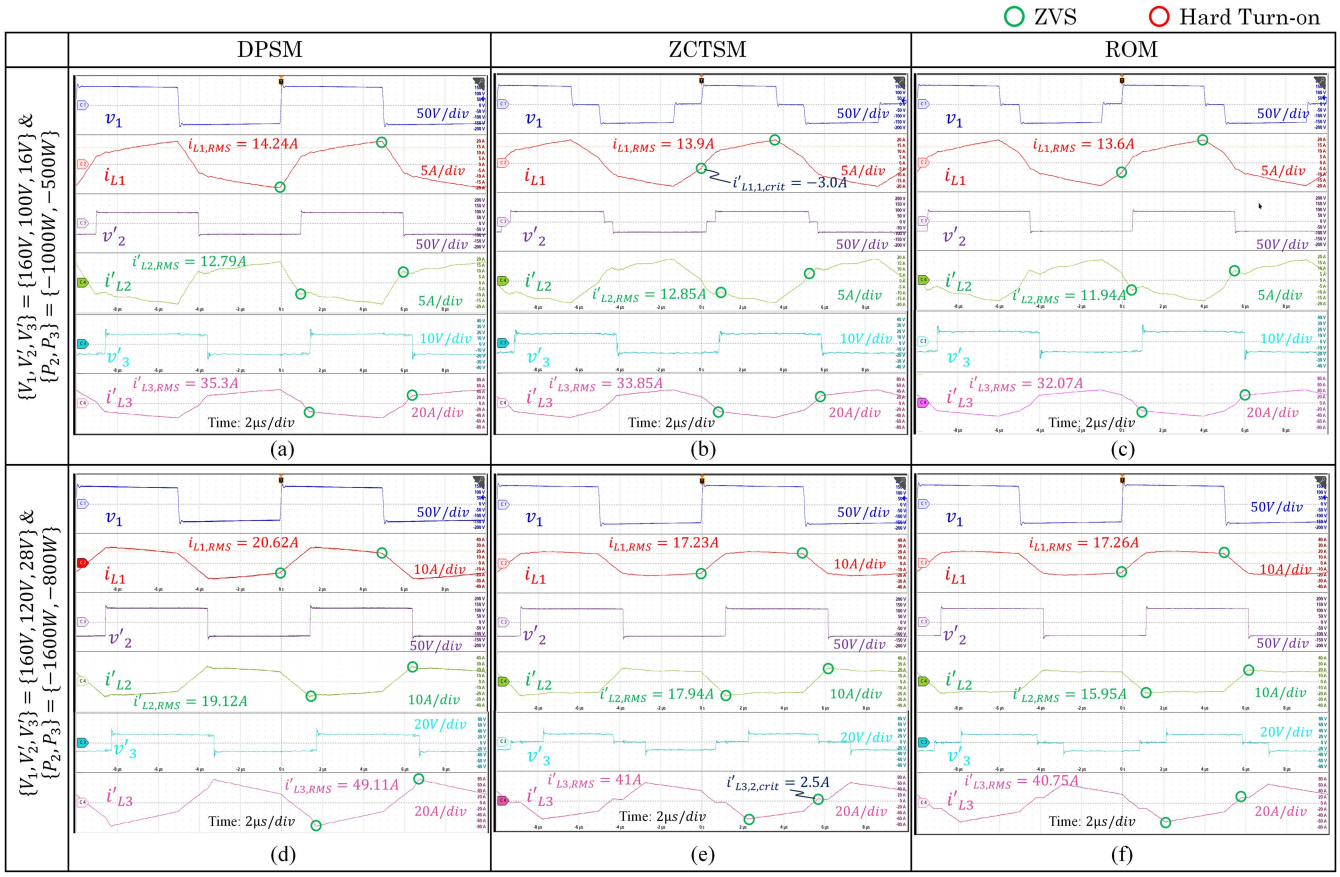

Fig. 19. Experimental steady state TAB circuit waveforms at two different heavy loading conditions under following PWM schemes: (a), (d) DPSM, (b), (e) Proposed ZCTSM, and (c), (f) ROM. (a)–(c) Waveforms at $V_1 = 160$ V, $V'_2 = 100$ V, $V'_3 = 16$ V, $P_2 = -1000$ W, and $P_3 = -500$ W, and (d)–(f) Waveforms at $V_1 = 160$ V, $V'_2 = 120$ V, $V'_3 = 28$ V, $P_2 = -1600$ W, and $P_3 = -800$ W.

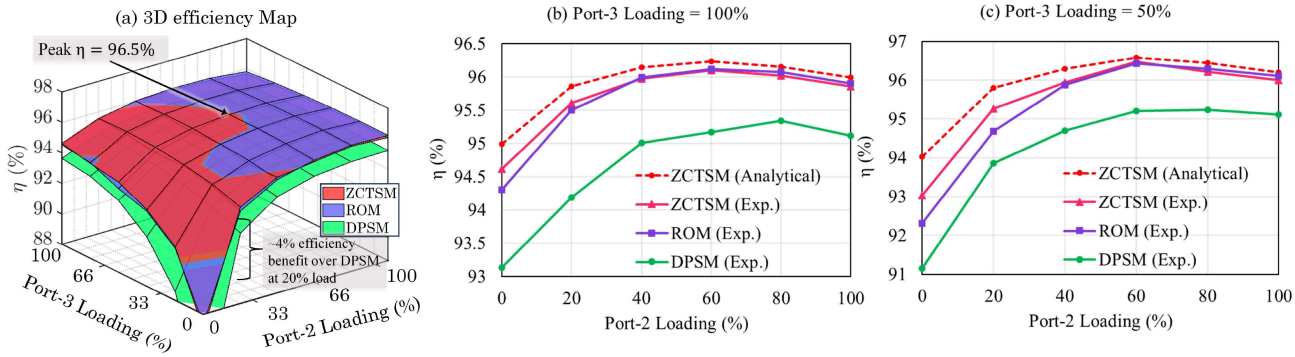

Fig. 20. TAB efficiency versus output load comparison between DPSM, ROM, and ZCTSM control strategy under the output port voltage of $V'_2 = 100$ V, $V'_3 = 16$ V. (a) 3-D efficiency map; 2-D efficiency plots with varying port-2 load, when port-3 load is fixed at (b) 100% and (c) 50%.

Notably, when hardware efficiency data under different modulations are compared, the DPSM exhibits the lowest efficiency throughout the full load range due to its inability to achieve soft-switching and minimize inductor current RMS. Conversely, the ZCTSM's capability to ensure soft-switching across most of the load range leads to superior light-load efficiency, where switching losses dominate. The efficiency plots also depict that the proposed PWM technique brings in an efficiency benefit of up to 4% and 0.5%–1% at a 20% loading condition compared to DPSM and ROM control strategies, respectively. However, at heavier loads, the ROM exhibits a better system efficiency (~0.15% to 0.25% greater) compared to ZCTSM due to optimized RMS currents leading to lower conduction loss. The peak converter efficiency with ZCTSM at this port voltage level

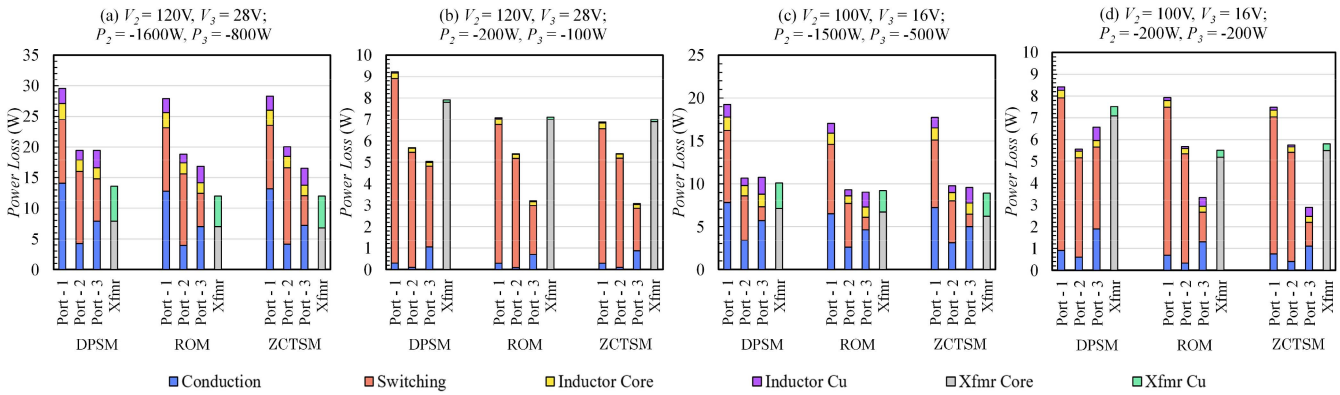

Fig. 21. Power loss distribution among the major power stage components of the TAB converter: semiconductor devices, inductors, and the transformer under the DPSM, ROM, and ZCTSM control strategy at different operating conditions defined by $\{V_1, V'_2, V'_3, P_2, P_3\}$ = (a) {160 V, 120 V, 28 V, −1600 W, −800 W}; (b) {160 V, 120 V, 28 V, −200 W, −100 W}; (c) {160 V, 100 V, 16 V, −1500 W, −500 W}; and {160 V, 100 V, 16 V, −200 W, −200 W}.

is observed to be 96.5%, while the highest measured efficiency under the ZCTSM control scheme is found to be 96.8% at 73% total output load with port voltages set at $\{V_1, V'_2, V'_3\} = \{160\text{ V}, 114\text{ V}, 21\text{ V}\}$.

Furthermore, the loss distributions among the major power stage components of the TAB under the three switching schemes are compared and illustrated in Fig. 21. It can be observed from the plots that at lighter loads, the ROM and DPSM incur 18% and 37% higher switching loss, respectively, compared to ZCTSM due to loss of soft-switching. It makes the ZCTSM to be the ideal choice as a TAB PWM control strategy for light load operation. As the load rises, the inductor current RMSs also increase that loads to more conduction loss compared to switching loss in the power MOSFETs. Although its ZVS switching peak current regulation technique ZCTSM attains a lower transformer winding current RMS compared to DPSM, the ROM that optimizes the current RMSs, outperforms ZCTSM at heavy loads by a small margin (∼4.2% lower total conduction loss).

In light of the comprehensive performance evaluation and feature-based comparison outlined in Table IV, crucial design considerations for optimizing control methods for a TAB converter are identified as follows.

1) *Operating Load Profile:* Tailor the choice of control method to the converter's operating load and voltage profile to ensure optimal performance across varying conditions. While a combination of ZCTSM and ROM may offer superior efficiency performance throughout the converter's full range, it comes with increased implementation complexity. Alternatively, if the converter primarily operates within the light to medium load range, ZCTSM proves to be the optimal choice. Conversely, ROM is preferable for maximizing system efficiency when the converter operates near full load for extended periods.
2) *EMI Performance:* Given the varying demands of applications, prioritize EMI performance. Opt for ZCTSM with its assurance of soft-switching capability to meet specific application requirements effectively.
3) *Computational Burden:* Factor in the computational burden associated with the chosen control method, including considerations such as dedicated control hardware, memory capacity, and clock speed. Select a control scheme that aligns with the design targets while ensuring compatibility with available resources.

These design considerations serve as essential guidelines for optimizing control methods tailored to the specific requirements and operational characteristics of TAB converters.

VIII. Conclusion

This research successfully addresses the modeling complexities of an isolated TAB dc–dc converter. The proposed time-domain TAB analytical model, rooted in DAB converter principles, simplifies switching transient current calculations and aids in optimizing TAB port inductances, minimizing switching losses. The charge-based ZVS process analysis of the converter switching leg helps with accurately identifying critical ZVS current requirements while accounting for the nonlinear characteristics of the parasitic device capacitances. Further, utilizing the developed time-domain converter model, an online computable switching loss minimized PWM modulation strategy is synthesized that maintains the switching peak currents at or above the critical ZVS currents and thus, ensures soft-switching of all the TAB legs. The performance comparison data highlights that the proposed soft-switching modulation strategy also significantly reduces inductor current RMSs compared to traditional dual phase-shift based control. Experimental results indicate that with the implementation of ZCTSM, the average switching loss in the converter at a lighter load range is reduced by 26% and 38% compared to ROM and dual-phase shift-based modulation technique, leading to an average efficiency improvement by 3.5% and 0.7%, respectively.

Finally, the proposed time-domain-oriented superposition theorem-based modeling and passive optimization approach for TAB converters is scalable to any converter within the MAB family. This scalability arises from the ability to decompose

any n-port MAB converter into C_2^n number of DAB switching cells using its Δ-equivalent circuit. However, as the number of ports in the MAB increases, the computational complexity escalates, making it challenging to find closed-form solutions for optimal duty cycle parameters. Consequently, the practical applicability of the proposed optimization technique is primarily limited to TAB and DAB converters within the MAB family.

APPENDIX

Adhering to the power flow direction presented in Section V, the expressions for the optimal TAB duty variables under all possible converter operating modes are showcased here. All of the eight total possible modes are determined based on the fundamental DAB cell's operational mode and can be categorized as 111, 115, 151, 155, 511, 515, 551, 555.

For TAB operating in Mode 111 (all three DAB cells DAB-L_{12}, DAB-L_{13}, and DAB-L_{23} are in Mode 1) and Mode 115 (both DAB-L_{12}, and DAB-L_{13} in Mode 1; DAB-L_{23} in Mode 5) $\delta_{1,\text{opt}}$ is derived from (31) shown at the bottom of the this page. Similarly, for Mode 551, Mode 511/515, and Mode 151/155 operation, the optimized bridge-1 duty variable $\delta_{1,\text{opt}}$ is determined using (32), (33), and (34) shown at the bottom of the this page, respectively. Further, the optimized port-2 ac voltage duty $\delta_{2,\text{opt}}$ for TAB operating in Mode 111/151, Mode 555/515, Mode 551/511, and Mode 115/155, is determined using (35), (36), (37), and (38) shown at the bottom of the this page, correspondingly. Lastly, for TAB operating in Mode 111 and Mode 511, $\delta_{3,\text{opt}}$ is derived from (39) shown at the bottom of the this page. Similarly, for Mode 155/555, Mode 551/151, and Mode 115/515 operation, the optimized bridge-3 duty variable $\delta_{3,\text{opt}}$ is determined using (40), (41), and (42) shown at the bottom of the this page, respectively.

$$\delta_{1,\text{opt}} = \max\left[0, \frac{i_{L1,1,\text{crit}} + pu_{12}\left[m_{12}\varphi_2 + (1-m_{12})\,\pi/2\,\right] + pu_{13}\left[m_{13}\varphi_3 + (1-m_{13})\,\pi/2\,\right]}{pu_{12}\,(1+m_{12}) + pu_{13}\,(1+m_{13})}\right] \tag{31}$$

$$\delta_{1,\text{opt}} = \max\left[0, \frac{i_{L1,1,\text{crit}} + pu_{12}\left[-m_{12}\varphi_2 + (1-m_{12})\,\pi/2\,\right] + pu_{13}\left[-m_{13}\varphi_3 + (1-m_{13})\,\pi/2\right]}{pu_{12}\,(1-m_{12}) + pu_{13}\,(1-m_{13})}\right] \tag{32}$$

$$\delta_{1,\text{opt}} = \max\left[0, \frac{i_{L1,1,\text{crit}} - pu_{12}\left[m_{12}\varphi_2 - (1-m_{12})\,\pi/2\,\right] + pu_{13}\left[m_{13}\varphi_3 + (1-m_{13})\,\pi/2\,\right]}{pu_{12}\,(1-m_{12}) + pu_{13}\,(1+m_{13})}\right] \tag{33}$$

$$\delta_{1,\text{opt}} = \max\left[0, \frac{i_{L1,1,\text{crit}} - pu_{13}\left[m_{13}\varphi_3 - (1-m_{13})\,\pi/2\,\right] + pu_{12}\left[m_{12}\varphi_2 + (1-m_{12})\,\pi/2\,\right]}{pu_{13}\,(1-m_{13}) + pu_{12}\,(1+m_{12})}\right] \tag{34}$$

$$\delta_{2,\text{opt}} = \max\left[0, \frac{-i_{L2,1,\text{crit}} - pu_{12}\left[\varphi_2 - (1-m_{12})\,\pi/2\right] - pu_{23}\left[m_{23}\,(\varphi_3-\varphi_2) + (1-m_{23})\,\pi/2\right]}{pu_{12}\,(1-m_{12}) - pu_{23}\,(1+m_{23})}\right] \tag{35}$$

$$\delta_{2,\text{opt}} = \max\left[0, \frac{i_{L2,1,\text{crit}} + pu_{12}\left[\delta_{1,opt} - (1-m_{12})\,\pi/2\right] + pu_{23}\left[-m_{23}\,(\varphi_3-\varphi_2) + (1-m_{23})\,\pi/2\right]}{pu_{12}m_{12} + pu_{23}\,(1-m_{23})}\right] \tag{36}$$

$$\delta_{2,\text{opt}} = \max\left[0, \frac{i_{L2,1,\text{crit}} + pu_{12}\left[\delta_{1,opt} - (1-m_{12})\,\pi/2\right] + pu_{23}\left[m_{23}\,(\varphi_3-\varphi_2) + (1-m_{23})\,\pi/2\right]}{pu_{12}m_{12} + pu_{23}\,(1+m_{23})}\right] \tag{37}$$

$$\delta_{2,\text{opt}} = \max\left[0, \frac{i_{L2,1,\text{crit}} - pu_{12}\left[\varphi_2 - \frac{(1-m_{12})\pi}{2}\right] - pu_{23}\left[m_{23}\,(\varphi_3-\varphi_2) - (1-m_{23})\,\pi/2\right]}{-pu_{12}\,(1-m_{12}) + pu_{23}\,(1-m_{23})}, \right.$$
$$\left. \frac{i_{L2,2,\text{crit}} + pu_{12}\left[\varphi_2 - \frac{(1-m_{12})\pi}{2}\right] + pu_{23}\left[m_{23}\,(\varphi_3-\varphi_2) + (1-m_{23})\,\pi/2\right]}{pu_{12}\,(1+m_{12}) + pu_{23}\,(1-m_{23})}\right] \tag{38}$$

$$\delta_{3,\text{opt}} = \max\left[0, \frac{-i_{L3,2,\text{crit}} + pu_{13}\left[\varphi_3 - (1-m_{13})\,\pi/2\right] + pu_{23}\left[(\varphi_3-\varphi_2) - (1-m_{23})\,\pi/2\right]}{pu_{13}\,(1+m_{13}) + pu_{23}\,(1+m_{23})}\right] \tag{39}$$

$$\delta_{3,\text{opt}} = \max\left[0, \frac{i_{L3,1,\text{crit}} + pu_{13}\left[\delta_{1,\text{opt}} - (1-m_{13})\,\pi/2\right] + pu_{23}\left[\delta_{2,\text{opt}} - (1-m_{23})\,\pi/2\right]}{pu_{13}m_{13} + pu_{23}m_{23}}\right] \tag{40}$$

$$\delta_{3,\text{opt}} = \max\left[0, \frac{-i_{L3,2,\text{crit}} + pu_{13}\left[\delta_{1,\text{opt}} - (1-m_{13})\,\pi/2\right] + pu_{23}\left[(\varphi_3-\varphi_2) - (1-m_{23})\,\pi/2\right]}{pu_{13}m_{13} + pu_{23}\,(1+m_{23})}\right] \tag{41}$$

$$\delta_{3,\text{opt}} = \max\left[0, \frac{-i_{L3,2,\text{crit}} + pu_{13}\left[\varphi_3 - (1-m_{13})\,\pi/2\right] + pu_{23}\left[\delta_2 - (1-m_{23})\,\pi/2\right]}{pu_{13}\,(1+m_{13}) + pu_{23}m_{23}}\right]. \tag{42}$$

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