An Isolated Identical Bipolar Buck-Boost AC–AC Converter With Step-Changed Frequency Operation and Reduced Active and Passive Components

Alireza Lahooti Eshkevari, Hafiz Furqan Ahmed, *Member, IEEE*, and Iman Abdoli

***Abstract*—This article introduces a novel buck-boost ac–ac converter with identical bipolar operation and high-frequency voltage isolation. The proposed converter offers several distinguishing features compared to existing isolated converters: First, it provides a significant reduction in the number of active and passive components. Second, it supplies continuous input and output currents with low harmonic contents. Third, it provides bipolar output with a two-winding transformer (instead of a three-winding transformer) with enhanced magnetic utilization and reduced cost and footprint. Finally, it can operate with different winding coefficients without compromising buck-boost functionality or limiting its magnitude coverage. Additionally, the converter facilitates buck-boost operation for all transformer winding ratio values, making it suitable for shallow and deep voltage sag/swell mitigation. The integration of a high-frequency transformer eliminates the need for a low-frequency coupling transformer. The proposed converter can provide a step control of output voltage frequency and performs normally under inductive and nonlinear loads. This article provides a detailed description of the proposed topology operation and its analysis, succeeded by experimental validations conducted on a laboratory-built converter, showcasing a peak efficiency of 93.3%. Extensive comparisons affirm that the proposed converter exhibits reduced input/output total harmonic distortion, broader voltage gain coverage, and superior efficiency compared to recently developed converters.**

***Index Terms*—AC–AC converter, bipolar output, buck-boost, variable frequency.**

I. Introduction

DIRECT ac–ac converters offer significant advantages over conventional back-to-back dc-link converters, including single-stage power conversion with a simpler structure, fewer components, easier modulation, and reduced cost and volume [1]. These converters are used in applications, such as dynamic voltage restorers [2], voltage sag/swell compensators [3], constant voltage and current regulators [4], induction heaters [5], [6], and wireless power transmitters [7]. Recent studies show that buck-boost-type direct ac–ac converters are more popular than buck- or boost-type converters due to their ability to perform both step-down and step-up operations. Key features of ac–ac converters include high power conversion efficiency, lower cost, low voltage/current stress, a suitable buck-boost factor, no commutation problems, and the ability to generate both inverting and noninverting outputs. However, using a common-ground converter without a low-frequency coupling transformer is impractical with the terra-neutral-combined (TNC) earthing method. Electrical isolation is also necessary in grid-interface applications to prevent fault propagation. Therefore, high-frequency isolated ac–ac converters are preferable to nonisolated ones with an additional low-frequency transformer.

Z-source (ZS), quasi-Z source (qZS), and trans-Z source (TZS) topologies are well-known in dc–dc and dc–ac power conversions [8], [9], [10]. These impedance-network concepts have also been applied to various nonisolated bipolar ac–ac converters [11], [12], [13], later equipped with high-frequency transformer isolation. Ahmed et al. [14] proposed a family of isolated impedance-source-based ac–ac converters, including ZS, qZS, TZS, trans-quasi-Z source, improved trans-Z source (iTZS), and Γ-Z source. Except for qZS and iTZS, other topologies lack input current continuity and operate only in in-phase boost or antiphase buck-boost mode. The transformer's turn ratio affects the buck-boost factor coverage. An isolated bipolar buck converter based on the "switching cell" concept [15] has been presented in [16], eliminating the commutation issue by discarding bidirectional switches but requiring low-pass filters on the input and output sides for harmonic mitigation. Khan et al. [17] improved this topology by inserting two switching cells into the output side for in-phase/antiphase buck-boost modes, increasing the component count and reducing efficiency. An isolated Δ-source ac–ac converter has also been introduced in [18], achieving high voltage gain through two coupled inductors. However, like isolated and nonisolated impedance-source-based topologies [19], [20], [21], its buck operating area is restricted when the winding coefficients of coupled inductors exceed one. A new class of isolated qZS ac–ac structures has been suggested [22], eliminating two series coupling capacitors on the primary

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and secondary sides of the high-frequency transformer in the isolated qZS converter [14], significantly reducing the passive component count but resulting in poor output power quality and limited bipolar voltage transfer ratios similar to previous Z-source ac–ac converters. Dual-active-bridge (DAB) is another well-known isolated structure in dc–dc power conversion. Filho et al. [23] proposed a class of ac–ac converters based on DABs without bidirectional switches. This topology benefits from soft-switching operations. However, all converters from this class require several magnetic components, increasing the magnetic requirement, size, and cost. Gupta and Mazumder [24] have developed an isolated differential-mode direct ac–ac converter for power electronics transformer (PET) application. It consists of two identical ac–ac power modules, each equipped with an high-frequency transforme (HFT). The output ac waveform is produced by the difference between the outputs of those two power modules. However, this differential mode structure requires two unipolar ac–ac converter modules with significantly enhanced passive component count. Moreover, only one ac module is active in each half-cycle, reducing the component utilization, while there is additional conduction loss from the inactive module. Recently, an isolated quasi-Z-source networks-based buck-boost ac–ac converter with no commutation problem has been proposed in [25]. It uses only four active switches with bipolar buck-boost outputs and step-changed frequency operation. However, it requires two unidirectional quasi-Z-source networks on the primary side, a tapped-winding (three-winding) transformer, and two voltage polarity shaping active rectifiers connected to center-tapped secondary winding. Therefore, this converter requires a very large passive component count, including four inductors and seven capacitors, while its output current remains discontinuous. Furthermore, it requires ten diodes, significantly increasing its semiconductor device requirement and cost. Like other Z-source-derived topologies, this converter also lacks the noninverting buck operation for the unity turns ratio ($n = 1$) of HFT. Also, for $n < 1$, the achievable noninverting buck is very narrow, making it unsuitable for shallow voltage sag compensation.

In order to overcome the limitations of these existing converters, this article proposes an improved single-phase high-frequency transformer isolated ac–ac converter. The proposed converter has the following key features.

1) It provides an identical bipolar buck-boost operation and can adjust the frequency of output voltage in fixed steps.
2) It ensures a continuous supply of load current in addition to maintaining continuity of input current.
3) It requires only five active switches. It utilizes an additional active switch compared to [25], which notably reduces the number of diodes to four (instead of ten in [25]), inductors to two (instead of four), and capacitors to two (instead of five). Consequently, this leads to a significant reduction in both the price and size of the converter.
4) It requires a two-winding high-frequency transformer instead of a three-winding transformer, improving transformer utilization and reducing its requirement and cost.

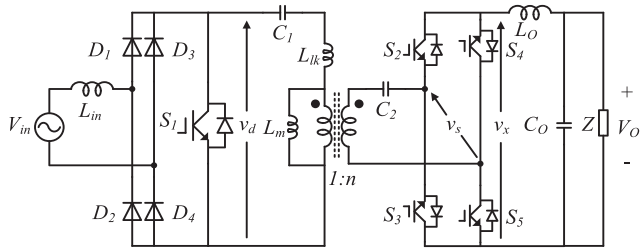

Fig. 1. Schematic diagram of the proposed topology.

5) Unlike existing Z-source-based ac–ac converters [14], [18], [22], [25], the proposed converter can provide a wide range of buck and boost operations even with a unity turns ratio of the transformer ($n = 1$). Therefore, it can mitigate both shallow and deep voltage sags. The turn-ratio n can be increased beyond unity for deep voltage sag compensation.

Also, thanks to integrating HFT into the proposed topology, a line-frequency transformer is no longer required for coupling in the TNC earthing system, application as a dynamic voltage restorer, and other grid-interfacing and traction applications.

II. Proposed Converter

Fig. 1 illustrates the schematic diagram of the proposed converter. It consists of five power switches (S_1-S_5), four diodes (D_1-D_4), two inductors (L_{in} and L_O), an HFT with magnetizing inductance L_m and leakage inductance L_{lk}, and three capacitors (C_1, C_2, C_O). The ac input voltage v_{in} is rectified through D_1-D_4, and a high-frequency link v_d is created using the switch S_1. This high-frequency link is fed to the primary side of HFT via a series capacitor (C_1) to cancel its dc component. The high-frequency component of the primary link voltage is reflected to the secondary side and fed to an active bridge through a series capacitor (C_2). The active bridge includes four power switches (S_2-S_5). It converts the reflected high-frequency link to pulsating ac voltage, the fundamental component of which is extracted by L_2 and C_O. The switching action on the secondary side shapes the inverting or noninverting polarity of output voltage and provides the step-changed frequency function. Fig. 2 depicts the critical waveforms of the converter. Accordingly, four switching states are defined for both half cycles, as shown in Fig. 3(a)–(c). Also, Fig. 2 displays the output step-changed frequency operation. As the switching states are common for both input half-cycles, only the states of the input positive half-cycles are described in the following.

A. NonInverting Buck-Boost Operation ($v_{in} > 0$)

According to Fig. 2, a carrier signal v_{tri} (with a specific switching frequency) is generated. Switch S_1 is triggered by a high-frequency pulse as generated by comparing the modulation wave (v_a) with the carrier signal. For each input voltage half-cycle, one secondary side switch pair (S_2, S_5) or (S_3, S_4) is operated complementary to switch S_1, and the other pair is fully turned ON. Diodes D_1 and D_4 keep conducting for the positive input half-cycle, so voltage V_{in} across switch S_1 is positive.

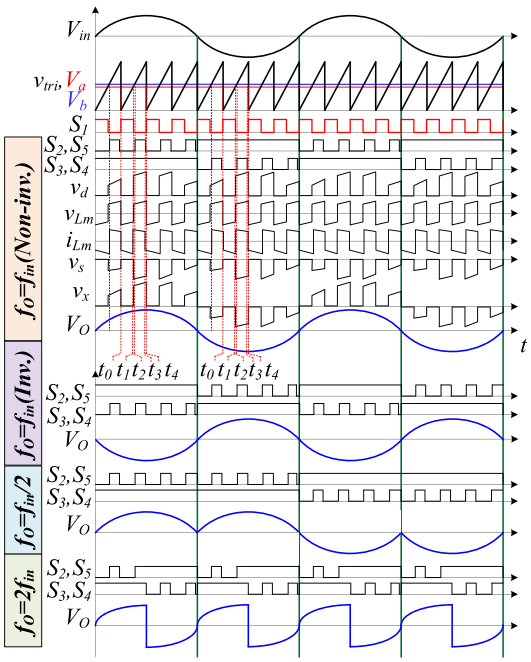

Fig. 2. Proposed switching strategy for noninverting, inverting, and step-changed frequency operations.

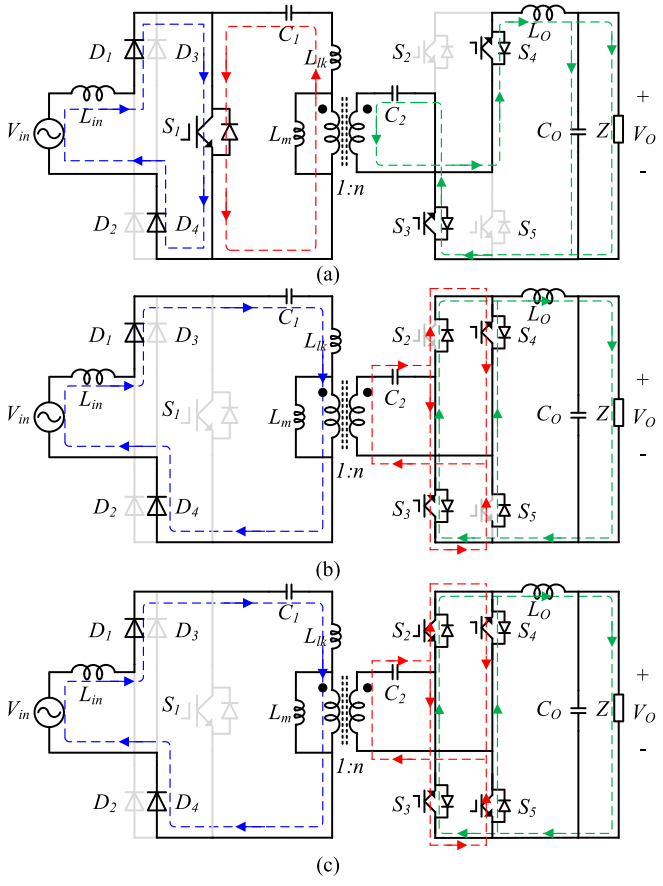

Fig. 3. Equivalent circuits for the noninverting buck-boost operation. (a) State I. (b) States II and IV. (c) State III.

State I – [$t_0 \sim t_1$]: The equivalent circuit of this mode is depicted in Fig. 3(a). S_1 is turned ON. L_{in} is charged through D_1, D_4, and S_1. The energy of capacitor C_1 (as transferred to the secondary side of HFT) and capacitor C_2 provide the energy to the output inductor (L_O), capacitor (C_O), and load (Z). Output inductor current is passed through capacitor C_2 and the secondary winding by switches S_3 and S_4. It is also reflected on the primary side and is passed through capacitor C_1 and primary winding. By assuming that the $DT_S = (t_1\text{-}t_0)$, where D and T_S are the duty cycle and switching period, respectively, the instantaneous current of the capacitors i_{C1}, i_{C2}, and i_{CO}, and the instantaneous voltage of magnetic elements v_{Lin}, v_{Lm}, and v_{LO} are calculated from

$$\begin{aligned} &v_{L_{in}} = V_{in},\ v_{L_m} = -v_{C1},\ v_{L_O} = nv_{C1} + v_{C2} - V_O \\ &i_{C1} = -ni_{L_O},\ i_{C2} = -i_{L_O},\ i_{C_O} = i_{L_O} - i_O \end{aligned} \tag{1}$$

v_{C1} and v_{C2} represent the instantaneous voltages of capacitors C_1 and C_2. In addition, n denotes the turn ratio of HFT and is equal to N_S/N_P. N_P and N_S are the number of windings in the primary and secondary sides of HFT, respectively.

State II – [$t_1 \sim t_2$]: The equivalent circuit is shown in Fig. 3(b). This time interval relates to dead time in which S_1 is switched OFF, and there is a small delay before turning on S_2 and S_5. Input source and inductor L_{in} charge the capacitor C_1. Their energy is partially reflected on the secondary side charging capacitor C_2 as well. Output inductor current freewheels through two parallel paths: S_3 and body diode of S_2 and S_4 and body diode of S_5. The reflected current of L_{in} on the secondary ($i_{C2} = i_{\text{Lin}}/n$) passes through the body diodes of S_2 and S_5. It is worth noting that only two secondary-side power switches operate with high-frequency pulsewidth modulation (PWM). Thus, the presence of a parallel switch path significantly relieves the current stresses of switching devices without increasing their switching loss. This would remarkably reduce the conduction losses of switching devices. state IV ([$t_3 \sim t_4$]) is the same as state II.

State III – [$t_2 \sim t_3$]: The dead time interval ends. Switch S_1 is turned OFF, and switches S_2 and S_5 are switched ON. The operation remains similar to that explained in state II. The equivalent circuit has been depicted in Fig. 3(c). It is assumed that $(1\text{-}D)T_S = (t_3\text{-}t_1)$. The instantaneous voltages and currents for inductors and capacitors are given as

$$\begin{aligned} &v_{L_{\text{in}}} = V_{\text{in}} - v_{C1} - \tfrac{v_{C2}}{n},\ v_{L_m} = \tfrac{v_{C2}}{n},\ v_{L_O} = -V_O \\ &i_{C1} = -ni_{L_O},\ i_{C2} = i_{L_{\text{in}}}/n,\ i_{C_O} = i_{L_O} - i_O. \end{aligned} \tag{2}$$

B. *Inverting Buck-Boost Operation* (v_{in}>0)

Fig. 2(a) also indicates the switching signals for inverting buck-boost operation. For the positive half-cycle, switches S_2 and S_5 are kept on for the entire duration to ensure safe commutation. Similarly, switches S_3 and S_4 are completely on in the negative half-cycle. Diodes D_1 and D_4 are conducting for the input positive half-cycle, while D_2 and D_3 are forward-biased for the negative half-cycle. Thus, the rectified voltage across switch S_1 remains positive. Similar to the noninverting mode, four switching states are defined.

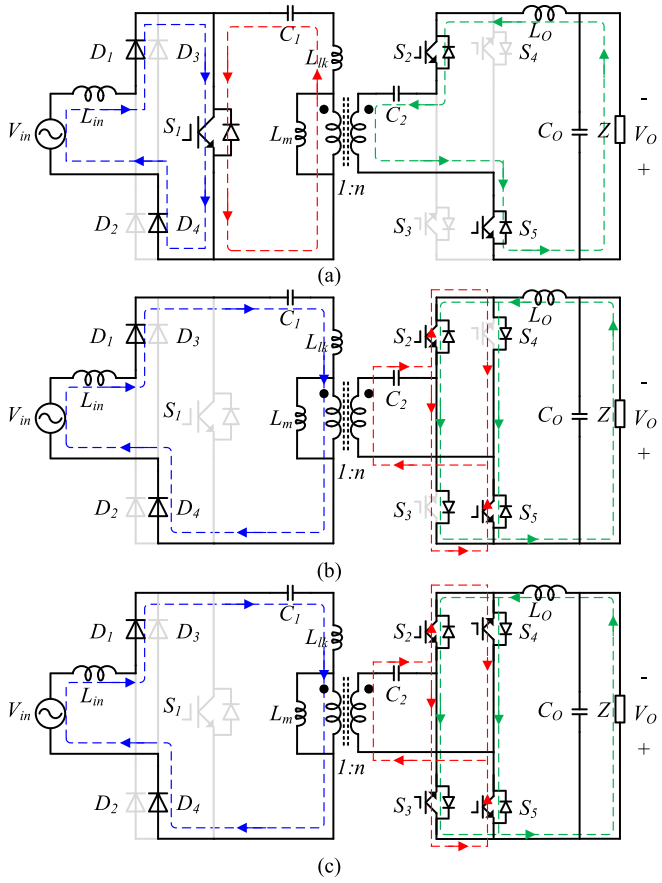

Fig. 4. Equivalent circuits for the inverting buck-boost operation. (a) State I. (b) States II and IV. (c) State III.

State I – [$t_0 \sim t_1$]: The equivalent circuit is depicted in Fig. 4(a). S_1 is switched on. V_{in} charges L_{in}. The energy stored in capacitor C_1 is reflected on the secondary side of HFT, and together with C_2, it delivers its energy to the output inductor, capacitor, and load. Output inductor current flows in reverse direction compared to the in-phase condition. The current is also reflected on the primary side and is passed through capacitor C_1 and primary winding. The instantaneous voltages and currents of passive components are derived from

$$\begin{aligned} &v_{L_{\text{in}}} = V_{\text{in}},\ v_{L_m} = -v_{C1},\ v_{L_O} = nv_{C1} + v_{C2} + V_O \\ &i_{C1} = ni_{L_O},\ i_{C2} = -i_{L_O},\ i_{C_O} = i_{L_O} - i_O. \end{aligned} \tag{3}$$

State II – [$t_1 \sim t_2$]: S_1 is switched OFF. There is a short delay before turning ON S_3 and S_4, as shown in Fig. 4(b). Input source and inductor L_{in} charge C_1. Their energy is partially reflected on the secondary side, and the capacitor C_2 is charged. Output inductor current freewheels through two parallel paths: S_2 and body diode of S_3 and S_5 and body diode of S_4. The reflected current of L_{in} on the secondary ($i_{C2} = i_{L\text{in}}/n$) passes through the body diodes of S_4 and S_3. States II and IV are the same.

State III – [$t_2 \sim t_3$]: S_1 switch is kept OFF, and S_4 and S_3 are switched ON. The operation remains similar to that explained in state II. The equivalent circuit has been illustrated in Fig. 4(c). The instantaneous voltages and currents of passive components

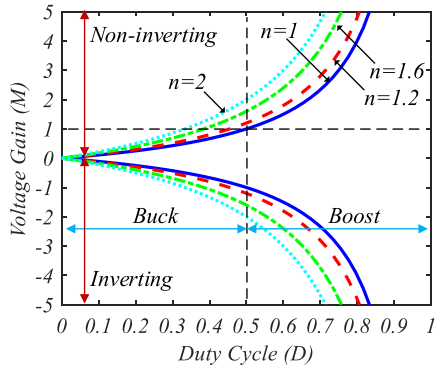

Fig. 5. Buck-boost factor vs. duty cycle.

are deduced from

$$\begin{aligned} &v_{L_{\text{in}}} = V_{\text{in}} - v_{C1} - \tfrac{v_{C2}}{n},\ v_{L_m} = \tfrac{v_{C2}}{n},\ v_{L_O} = -V_O. \\ &i_{C1} = -ni_{L_O},\ i_{C2} = i_{L_{\text{in}}}/n,\ i_{C_O} = i_{L_O} - i_O \end{aligned} \tag{4}$$

C. Steady-State Analysis

The average voltages and currents for passive elements are determined using voltage-second and ampere-second principles, as given in

$$V_{C1} = V_{\text{in}} \tag{5}$$

$$V_{C2} = \frac{nD}{1-D}V_{C1} = \frac{nD}{1-D}V_{\text{in}} \tag{6}$$

$$I_{L_O} = \frac{1-D}{nD}I_{L_{\text{in}}}. \tag{7}$$

The output voltage is determined by applying the voltage-second principle to the output inductor L_O. The output voltage in the inverting operation has a negative sign. This is because the output inductor current has a negative (reverse) polarity compared to the noninverting mode. So, the output voltage gain is obtained from

$$M = \frac{V_O}{V_{\text{in}}} = \frac{I_{\text{in}}}{I_O} = \pm\frac{nD}{1-D}. \tag{8}$$

Fig. 5 plots the voltage gain versus duty cycle and shows the effect of transformer turn ratio n on the gain. Hereupon, it is justified that the topology provides bipolar buck-boost operation. The proposed topology can perform buck and boost operations for $n = 1$. Also, the n can be increased for deep voltage sag/swell compensation. Moreover, the buck operating region can be increased by reducing the transformer turn ratio. In practice, the employed HFT includes leakage inductance, which may degrade the voltage gain. The coupling coefficient k is equal to $L_M/(L_M + L_{lk})$ and can be varied between zero and one based on the quality of HFT.

III. Components Voltage and Current Stresses/Ripples Their Design Guidelines

A. Components Voltage and Current Stresses

Equations (9) and (10) indicate peak voltage and current stresses across semiconductor devices located at the primary

side of HFT for both inverting and noninverting buck-boost operations

$$\begin{cases} V_{D1} = V_{D2} = V_{D3} = V_{D4} = \sqrt{2}V_{\text{inrms}} = \left(\sqrt{2}V_{O\text{rms}}\right)/M \\ i_{D1} = i_{D2} = i_{D3} = i_{D4} = \sqrt{2}i_{\text{inrms}} = \sqrt{2}Mi_{O\text{rms}} \end{cases} \tag{9}$$

$$\begin{cases} V_{S1} = \frac{\sqrt{2}V_{\text{inrms}}}{1-D} = \frac{\sqrt{2}V_{O\text{rms}}}{M(1-D)} \\ i_{S1} = \sqrt{2}\,(n+M)\,i_{O\text{rms}} \end{cases}. \tag{10}$$

Moreover, the following peak voltage and current stresses are determined for the semiconductor devices on the secondary side of HFT

$$\begin{cases} V_{S2} = V_{S3} = V_{S4} = V_{S5} = nV_{C1} + V_{C2} = \frac{\sqrt{2}nV_{\text{inrms}}}{1-D} \\ i_{S2} = i_{S3} = i_{S4} = i_{S5} = \sqrt{2}i_{O\text{rms}} \end{cases}. \tag{11}$$

If $n = 1$, the voltage stress across primary and secondary switches are identical. According to Fig. 3(b) and (c), body diodes of S_2 and S_5 conduct half of the output current. Equation (11) is valid for both inverting and noninverting modes. However, for anti-phase output voltage generation, body diodes of S_3 and S_4 conduct half of the output current.

B. Design Criteria for Passive Components

Regarding basic voltage and current relations for inductances and capacitances, the (12) and (13) are deduced, determining the voltage ripple of capacitors and the current ripple of inductances

$$\begin{aligned} &\Delta v_{C1} = \tfrac{i_{O\text{rms}}D}{nC_1 f_S},\ \Delta v_{C2} = \tfrac{i_{O\text{rms}}D}{C_2 f_S},\ \Delta v_{C3} = \tfrac{i_{O\text{rms}}D}{C_3 f_S} \\ &\Delta i_{L_{\text{in}}} = \tfrac{V_{\text{inrms}}D}{L_{in} f_S},\ \Delta i_{Lm} = \tfrac{V_{\text{inrms}}D}{L_m f_S},\ \Delta i_{L_O} = \tfrac{nV_{\text{inrms}}}{L_O f_S} \end{aligned} \tag{12}$$

$$\Delta i_{L_{in}} = \frac{V_{\text{inrms}}D}{L_{\text{in}} f_S},\ \Delta i_{Lm} = \frac{V_{\text{inrms}}D}{L_m f_S},\ \Delta i_{L_O} = \frac{nV_{\text{inrms}}}{L_O f_S}. \tag{13}$$

According to the power P_O transferred from the input source to the output terminal, the minimum required inductances and capacitances to ensure proper buck-boost operation are obtained, as given in

$$C_1 \geq \frac{D}{\alpha_1 n f_S}\left(\frac{P_O}{\text{MV}_{\text{inrms}}^2}\right) \tag{14}$$

$$C_2 \geq \frac{1-D}{\alpha_2 n f_S}\left(\frac{P_O}{\text{MV}_{\text{inrms}}^2}\right),\ C_3 \geq \frac{1-D}{\alpha_3 n f_S}\left(\frac{P_O}{\text{MV}_{\text{inrms}}^2}\right) \tag{15}$$

$$L_{\text{in}} \geq \frac{\text{DV}_{\text{inrms}}^2}{\beta_1 f_S P_O},\ L_m \geq \frac{n\text{MDV}_{\text{inrms}}^2}{\beta_2 f_S P_O},\ L_O \geq \frac{n\text{MV}_{\text{inrms}}^2}{\beta_3 f_S P_O}. \tag{16}$$

In (14)–(16), (α_1, α_2, α_3) and (β_1, β_2, β_3) denote the desired percentage of ripple values for capacitor voltages and inductors current, respectively. Magnetic elements must be designed to operate at high frequency. Hence, ferrite cores must be utilized. McLyman [26] presented the best guide for designing and fabricating magnetic components. This article uses the same method for determining the best core size, core type, and the number of required windings.

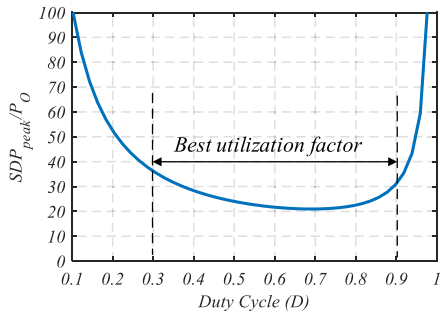

Fig. 6. SDP versus duty ratio for $n = 1$.

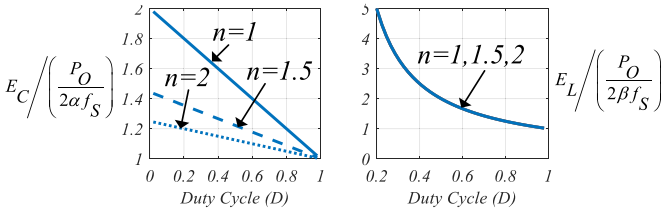

Fig. 7. Normalized value of E_C and E_L versus duty cycle for different winding coefficients.

C. Peak Switching Device Power (SDP) and Volume Metrics

The SDP is an index demonstrating the total power range of semiconductor devices. It directly relates to the converter cost, as defined in (17) for the proposed converter

$$\text{SDP}_{\text{Peak}} = \sum_{j=1}^{n} V_{Sj}^{\text{peak}} i_{Sj}^{\text{peak}} = \left(\frac{10n + 2M}{M(1-D)}\right) P_O. \tag{17}$$

Fig. 6 illustrates the SDP curve versus the duty cycle. Results show that increasing or decreasing the n does not affect the SDP value in the proposed converter. Accordingly, the suitable duty cycle range for obtaining an appropriate switch utilization factor is between 0.3 and 0.9. The volume metric of capacitors and inductors is the second index, which directly corresponds to the amount of energy stored in capacitors E_C and inductors E_L. The overall stored energy in capacitors C_1, C_2, and C_O and inductances are calculated by (18) considering $\alpha = \alpha_1 = \alpha_2 = \alpha_3$ and $\beta = \beta_1 = \beta_2 = \beta_3$. Fig. 7 shows the normalized value of E_C and E_L versus duty cycle variations for some winding coefficients. E_C and E_L are decreased by increasing the switching frequency f_S because smaller capacitances and inductances are used

$$\begin{aligned} E_C &= \left(\frac{1 + n^2 - D}{nM(1-D)}\right)\frac{DP_O}{2\alpha f_S}, \\ E_L &= \left(\frac{n + nD + MD}{M}\right)\frac{P_O}{2\beta f_S}. \end{aligned} \tag{18}$$

IV. Efficiency Analysis

There are two sources of power losses: conduction and switching losses. The series resistance of magnetic components ($r_{L\text{in}}$, r_{Lm}, r_{Lo}), the equivalent series resistance of capacitors (r_C), the

ON-resistance of the power switch (r_{DS}), and the forward voltage of diodes (V_F) and body diodes ($V_{\rm BD}$) have been accounted for in calculating the conduction losses of the converter. Two rectifier diodes are forward-biased in each input voltage half-cycle. Equation (19) expresses the conduction losses of rectifier diodes for each half-cycle. Equations (20)–(23) deduces the conduction losses of magnetic parts and the switch S_1 for a complete output cycle

$$P_{\rm cond}^{D} = 2V_F i_{D\rm avg} = 2\sqrt{2}V_F D M i_O \tag{19}$$

$$P_R^{L_{\rm in}} = r_{L\rm in} i_{L\rm in}^2 = r_{L\rm in} M^2 i_{O\rm rms}^2 \tag{20}$$

$$P_R^{L_m} = r_{Lm} i_{Lm}^2 = r_{Lm} n^2 i_{O\rm rms}^2 \tag{21}$$

$$P_R^{L_O} = r_{L_O} i_{L_O}^2 = r_{L_O} i_{O\rm rms}^2 \tag{22}$$

$$P_{\rm cond}^{S1} = r_{DS1} D (n+M)^2 i_{O\rm rms}^2. \tag{23}$$

According to Figs. 2, 3, and 4, two out of four secondary side power switches are operated with high-frequency PWM for each half-cycle. Based on Fig. 3(a), the current is passed through the body diodes of S_2 and S_5 when they are ON. The amplitude of the currents passed through S_2 and S_5 are identical to zero for the DT_S interval. It also equals $(i_{\rm in}+i_O)/2$ for the (1-D)T_S interval. Hence, the RMS current passed through the body diodes of S_2 and S_5 is calculated as

$$i_{\rm BD2rms} = i_{\rm BD5rms} = \sqrt{(1-D)\left(1+(1+nM)^2\right)}\frac{i_{O\rm rms}}{2}. \tag{24}$$

The main switch of S_3 and S_4 conduct $(i_{\rm in}+i_O)/2$ for the DT_S interval. Thus, the (25) is obtained. Their body diodes' currents are $i_O/2$

$$\begin{cases} i_{S3\rm rms} = i_{S4\rm rms} = \sqrt{D\left(1+(1+nM)^2\right)}\frac{i_{O\rm rms}}{2} \\ i_{\rm BD3rms} = i_{\rm BD4rms} = \frac{\sqrt{1-D}}{2} i_{O\rm rms} \end{cases}. \tag{25}$$

According to (24) and (25), the overall conduction losses of S_2-S_5 are determined as

$$\begin{cases} P_{\rm cond}^{S2} = P_{\rm cond}^{S5} = \sqrt{(1-D)\left(1+(1+nM)^2\right)}\frac{V_{\rm BD} i_{O\rm rms}}{2} \\ P_{\rm cond}^{S3} = P_{\rm cond}^{S4} = r_{DS}\frac{D\left(1+(1+nM)^2\right)^2}{4} i_{O\rm rms}^2 + \frac{\sqrt{1-D}}{2} V_{\rm BD} i_{O\rm rms} \end{cases}. \tag{26}$$

Switching losses comprise turn-ON/turn-OFF losses, $C_{\rm OSS}$, and reverse-recovery losses. Primary switch S_1 operates with high-frequency PWM. Accordingly, its switching and $C_{\rm OSS}$ losses have been given in (27) and (28), where $C_{\rm OSS}$, t_r, and t_f represent the effective output capacitance, rise time, and fall time found in the MOSFET datasheet. Switches S_2, S_3, S_4, and S_5 have a half-cycle high-frequency operation, and their switching losses are calculated as

$$\begin{aligned} P_{\rm SW}^{S1} &= \frac{1}{2} V_{\rm DS1} i_{\rm DS1} (t_r + t_f) f_S \\ &= \frac{(n+M) V_{O\rm rms} i_{O\rm rms}}{M(1-D)} (t_r + t_f) f_S \end{aligned} \tag{27}$$

$$P_{C\rm oss}^{S1} = \frac{1}{2} C_{\rm OSS1} V_{\rm DS1}^2 f_S = \frac{C_{\rm OSS1} V_{O\rm rms}^2 f_S}{M^2 (1-D)^2} \tag{28}$$

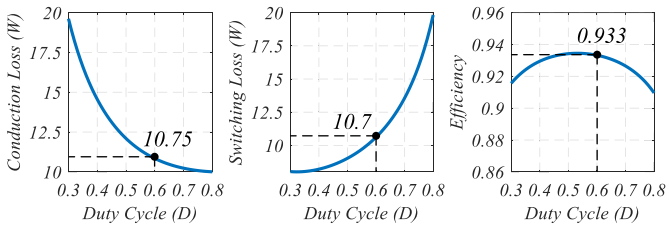

Fig. 8. Conduction losses, switching losses, efficiency in theory ($n=1$, r_{Lm}= $r_{L\rm in}=r_{LO}$= 10 mΩ, r_{DS}= 117 mΩ, V_F= 0.6, $V_{\rm BD}$ = 0.5 V, t_r= 53 ns, t_f= 17 ns, f_S= 20 kHz, $C_{\rm OSS}$ = 90 pF, Q_{rr}= 1.6 μC, and $V_{\rm in}$ = 70.7 $v_{\rm rms}$).

$$P_{\rm SW}^{S2} = P_{\rm SW}^{S3} = P_{\rm SW}^{S4} = P_{\rm SW}^{S5} = \frac{n V_{O\rm rms} i_{O\rm rms}}{2M(1-D)} (t_r + t_f) f_S \tag{29}$$

$$P_{C\rm oss}^{S2} = P_{C\rm oss}^{S3} = P_{C\rm oss}^{S4} = P_{C\rm oss}^{S5} = \frac{C_{\rm OSS} n^2 V_{O\rm rms}^2 f_S}{M^2 (1-D)^2}. \tag{30}$$

Each rectifier diode conducts for a certain half-cycle. Equation (31) presents the reverse recovery loss of each diode ($P^D{}_{RR}$). Likewise, (32) derives the reverse recovery loss of the S_2-S_5 body diodes

$$P_{RR}^{D} = \frac{1}{2} Q_{rr} V_{\rm OFF} f_S = \frac{\sqrt{2}}{2} Q_{rr} V_{\rm inrms} f_S \tag{31}$$

$$P_{RR}^{S2} = P_{RR}^{S3} = P_{RR}^{S4} = P_{RR}^{S5} = \frac{\sqrt{2} n}{2(1-D)} Q_{rr} V_{\rm inrms} f_S. \tag{32}$$

Steinmetz equality determines core losses, as shown in (33). λ, δ, and ζ are fitting parameters from the core datasheet. A_{Ck}, l_{Ck}, ΔB_k, and f_k show the core area, flux path length, magnetic flux density, and operating frequency of the kth inductances

$$P_{\rm core} = \sum_{k=1}^{3} \left(\lambda \Delta B_k^{\delta} f_k^{\zeta}\right) A_{Ck} l_{Ck}. \tag{33}$$

The RMS of passing currents through capacitors C_1 and C_2 are determined as

$$i_{C1\rm rms} = \frac{i_{C2\rm rms}}{n} = \frac{i_{O\rm rms}}{2\sqrt{2}n}\sqrt{1+(nM+1)^2}. \tag{34}$$

The current ripple of output inductor L_O is passed through the output capacitor C_O. The output inductor is big enough to have a small current ripple. So, this value is neglected, and the RMS value of capacitor C_O current is assumed to be negligible and zero. Capacitor conduction losses are obtained using

$$P_R^{C1} = \frac{P_R^{C2}}{n^2} = \frac{r_C i_{O\rm rms}^2}{8n^2}\left(1+(nM+1)^2\right). \tag{35}$$

By gathering all the mentioned losses, the total power losses of the proposed converter are calculated, which can be used to specify its efficiency (η) and nonideal voltage conversion ratio (M_{NI}), as presented in

$$\eta = P_O/(P_{\rm LOSS} + P_O),\ M_{NI} = \eta M. \tag{36}$$

Fig. 8 depicts the overall conduction and switching losses for constant output power (300 W). Different output voltages can be generated by varying the duty cycle, which consequently

TABLE I
COMPARISON OF THE PRESENTED TOPOLOGY WITH OTHER ISOLATED COUNTERPARTS

Ref.	[27]	[22]	[28]	[29]	[25]	Proposed
L/CL/C/S/D[1]	0/1/0/2/4	3/1/5/6/0	0/1/2/6/0	2/1/4/8/0	4/1/7/4/10	3/1/3/5/4
Total components	7	15	9	15	26	16
Voltage gain	$\pm n$	$\frac{n(1-D)}{1-2D}$	$\pm nD$	$\pm\frac{nD}{1-D}$	$\pm\frac{n(1-D)}{1-2D}$	$\pm\frac{nD}{1-D}$
Buck-boost operation	Buck or Boost	Buck-boost	Buck	Buck-boost	Buck-boost	Buck-boost
Buck-boost operation for $n\geq1$	N/A	Boost	Buck	Buck-boost	Boost	Buck-boost
Transformer type	LF	HF	HF	HF	HF	HF
Step-changed frequency operation	Yes	No	Yes	Yes	Yes	Yes
Number of high-frequency switches	2	6	6	8	2	3

1. Inductor, coupled inductor, capacitor, switch, diode

produces different output powers. For $n = 1$ and $D = 0.6$, the output power is 300W, and the theoretical efficiency is 93.3%. It means that 21.45W is dissipated. Practical efficiency is compared with the theoretical loss in later sections.

V. COMPARATIVE EVALUATION

Table I compares the proposed topology with isolated counterparts. Although [27] requires fewer components than the proposed converter, it does not provide buck-boost operation. There is no degree of freedom for adjusting its output voltage amplitude, and the topology works with a certain winding ratio n. Moreover, its built-in low-frequency transformer makes the topology massive and expensive. The employed qZS impedance source in [22] improves its voltage gain. However, the converter is unipolar and cannot cover buck-boost operation for $n \geq 1$, which is essential for voltage sag/swell compensation. Furthermore, it has a constant output frequency. Ahmed et al. [28] lack buck-boost operation and has six high-frequency switches, degrading its efficiency. Similarly, in [29], the number of high-frequency switches is high. The topology in [25] benefits from the provision of symmetric bipolar buck-boost operation and step-changed frequency output operation, reduced number of active switches (to four), and no commutation issue (as it does not use bidirectional switches). Nevertheless, its diode and passive component count is significantly greater than the proposed converter. Although the proposed converter has one more high-frequency switch than [25], it can save six diodes, four capacitors, and two inductors. It requires a two-winding transformer instead of a three-winding transformer in [25], increasing transformer utilization and reducing its requirement and cost. It provides continuous output current. Moreover, Fathi et al. [25] cannot provide buck operation for $n = 1$ or $n > 1$. Decreasing $n < 1$ can provide buck operation but with limited amplitude coverage. i.e., the converter of [25] cannot achieve zero output voltage. Hence, it is not suitable as DVR since it cannot mitigate shallow voltage sags. In contrast, the presented structure can provide buck and boost operations for $n = 1$ and $n > 1$. The HFT's turn ratio n can also be increased to mitigate deep voltage sag. Fathi et al. [25] has provided excellent simulation results for variable frequency ac–ac converters regarding output voltage THD and input current THD for different output frequencies. We have also added simulation results of our proposed converter to those data. Simulations have been done for the same converter specifications and output power. Table II gives the results. As the proposed topology benefits from input and output sinusoidal current with continuity and low current ripple, its output voltage THD and input current THD are better. It is worth noting that [28], [30], and [31] have discontinuous or pulsating output currents.

The maximum switch voltage stresses of the proposed and counterpart converters (see Table I) are compared in Fig. 9(a). As observed, the proposed converter has smaller switch voltage stresses. Fig. 9(b) and (c) compare the peak and average switching device power (SDPs) of the proposed and counterpart converters. $\mathrm{SDP_{PEAK}}$ is directly related to required semiconductor power ratings and cost. $\mathrm{SDP_{AVG}}$ is directly related to semiconductor device losses and their thermal management requirement [32], [33]. The proposed converter has smaller $\mathrm{SDP_{PEAK}}$ and $\mathrm{SDP_{AVG}}$ values, proving its better semiconductor device power utilization with smaller costs and losses. The passive component contributes greatly to the volume of a converter. The sizes of the passive components are approximated by their volume metrics, which are equal to the ratio of peak stored energy of inductors/capacitors and their volume metric energy densities [33]. Fig. 9(d) and (e) compare the inductor and capacitor volume metrics of the proposed and counterpart converters. As observed, the proposed converter has smaller inductor and capacitor volumes.

VI. EXPERIMENTAL RESULTS AND ANALYSIS

An experimental prototype has been designed and fabricated to examine the performance of the proposed converter. Fig. 10 represents the image of the fabricated prototype, and Table III indicates its specifications. First, it is tested by resistive, inductive, and nonlinear loads to confirm its operation. Then, its laboratory tests are carried out as a DVR. Besides the prototype, the control unit consists of a digital signal processor (DSP, TMS320F28335), and its control diagram is the same as in [29, Figs. 24 and 25]. However, to synchronize the controller with the grid, a DFT-based PLL is used, as demonstrated by [34]. The generated signals are fed to power switches through gate drivers (HCPL3120) with isolated voltage sources. In this design example, the leakage inductance of the coupled inductor is small. So, a small RC snubber circuit is used over the S_1 to restrain the voltage spike.

TABLE II
COMPARISON OF THE PRESENTED CONVERTER THD VALUES WITH REPORTED CONVERTER IN [25] BASED ON SIMULATION

Ref.	Type	Output voltage V_O THD (%)						Input current i_{in} THD (%)					
		25Hz		50Hz		100Hz		25Hz		50Hz		100Hz	
		Buck	Boost	Buck	Boost	Buck	Boost	Buck	Boost	Buck	Boost	Buck	Boost
Proposed	Isolated	62.50	62.50	0.47	0.58	62.23	61.6	3.01	1.99	2.20	1.99	7.85	5.59
[25]		62.99	62.94	2.17	2.15	62.71	62.6	3.39	3.18	3.35	3.16	7.04	5.85
[28]		63.05	-	1.82	-	65.47	-	14.1	-	3.58	-	18.11	-
[29]		62.54	62.5	0.52	0.61	60.84	59.71	4.32	4.72	3.93	3.70	5.76	6.49
[32]	Non-isolated	58.61	59.71	5.28	4.41	60.73	62.92	10.41	12.34	10.38	12.21	22.04	30.12
[33]		61.02	59.70	1.79	3.40	63.51	64.55	2.36	3.5	2.35	4.23	34.55	54.89
[31]		62.43	65.45	1.04	1.46	63.66	64.02	5.04	2.52	5.05	2.12	4.96	14.94

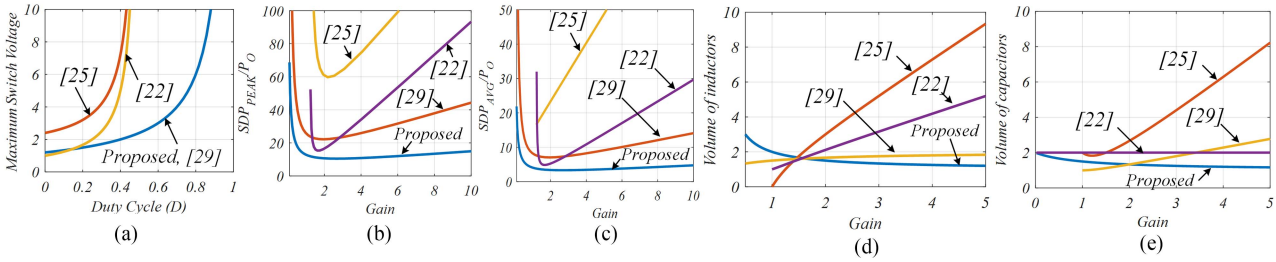

Fig. 9. Comparison of (a) maximum switch voltage, (b) $\mathrm{SDP_{PEAK}}$, (c) $\mathrm{SDP_{AVG}}$, and (d) magnetics volume metric, and (e) capacitors volume metric.

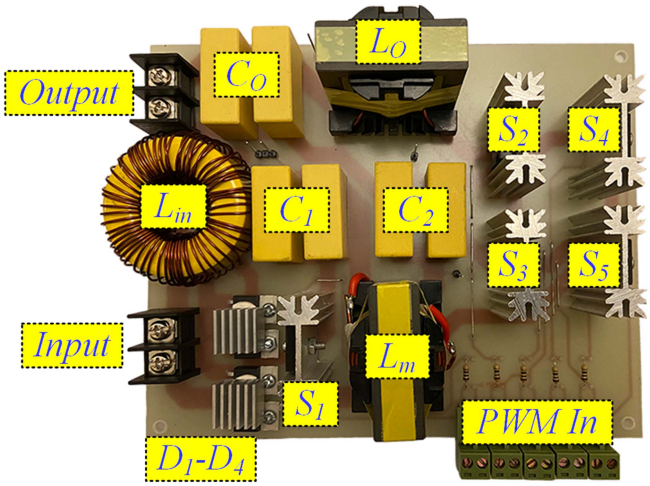

Fig. 10. Experimental prototype image.

TABLE III
CRITICAL SPECIFICATIONS OF THE PROPOSED CONVERTER

Parameters	Values	Parameters	Values
Nominal input voltage	$100V_{pk}$	C_O, C_1, C_2	2×2.2μF
Nominal output voltage	Buck mode: $60V_{pk}$ Boost mode: $125V_{pk}$	L_{in}, L_m, L_O	500μH
Maximum output power	Boost mode: 250W Buck mode: 120W	Measured inductance leakage	3μH
Output frequency	25Hz/50Hz/100Hz	Power switches and diodes	IXFH26N65, MUR1560
Switching frequency	40kHz	Cores	Material 25 and EER 42/20
Winding ratio	1:1	Open-loop duty ratios	*Dbuck* = 0.37, *Dboost*=0.55

Fig. 11(a), (b), and (c) show the input and output voltages (V_{in} and V_O) and currents (I_{in} and I_O), respectively, for resistive, inductive, and nonlinear loads. In this case, step-up and step-down

TABLE IV
MEASURED INPUT CURRENT AND OUTPUT VOLTAGE THDS FOR 50 HZ OUTPUT FREQUENCY

		Resistive (%)	Inductive (%)	Nonlinear (%)
Buck	**Input current**	2.5	4.7	62
	Output voltage	1.12	2.4	2.8
Boost	**Input current**	2.2	4.7	63
	Output voltage	1.23	2.3	3

operations, as well as inverting and noninverting operations, are confirmed for 50 Hz output frequency. For $D = 0.37$ and $n = 1$, the resulting voltage gain is 0.6. So, the input voltage ($100V_{\mathrm{pk}}$) is reduced to 60 V_{pk}. In contrast, for $D = 0.55$, the resulting gain is equal to 1.25, and the output voltage is increased to 125 V_{pk}. The converter performs regularly with an inductive load with PF $= 0.8$ [$(12 + j30)$ Ω], as shown in Fig. 11(b). In addition, to test a nonlinear load, a single-phase diode bridge rectifier has been connected to the converter output. Its rectified voltage supplies a 250W load through a (100 μH, 470 μF) smoothing filter.

As shown in Fig. 11(c), only the input current THD is affected, which is similar to other ac–ac converters because no compensation loop is designed to mitigate the harmonic effects of nonlinear loads. The output voltage and input current THD values are measured and organized in Table IV for the nominal output load. The voltages and currents of components have been presented in Fig. 12(a)–(e). The measured amplitudes are in accordance with (5), (6), (9), (10), and (11). Due to choosing $n = 1$, all power switches and diodes meet the same voltage stress. Voltage and current stresses of rectifier diodes and power switches are free of voltage spikes and current overshoots, as depicted in Fig. 12(f), so snubber circuits are no longer required. As mentioned earlier, the converter features step-changed frequency operation. Fig. 13(a) and (b) display input/output

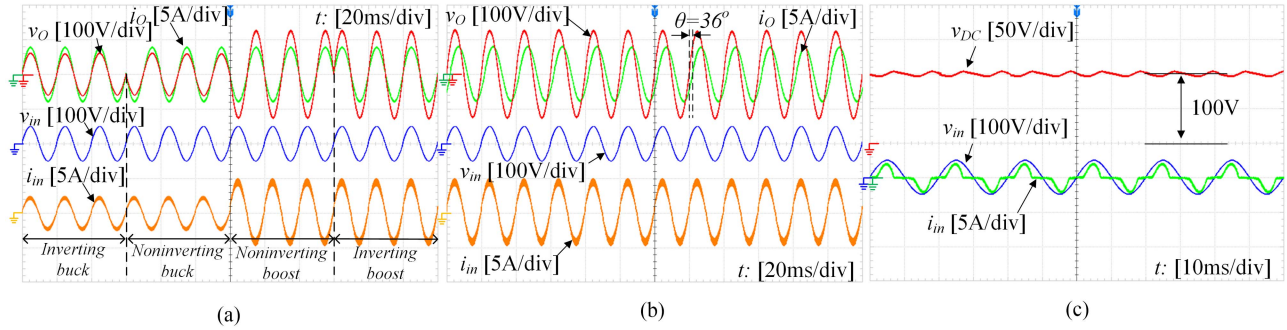

Fig. 11. Operation of the proposed converter. (a) Resistive load. (b) Inductive load with PF = 0.8. (c) Nonlinear load.

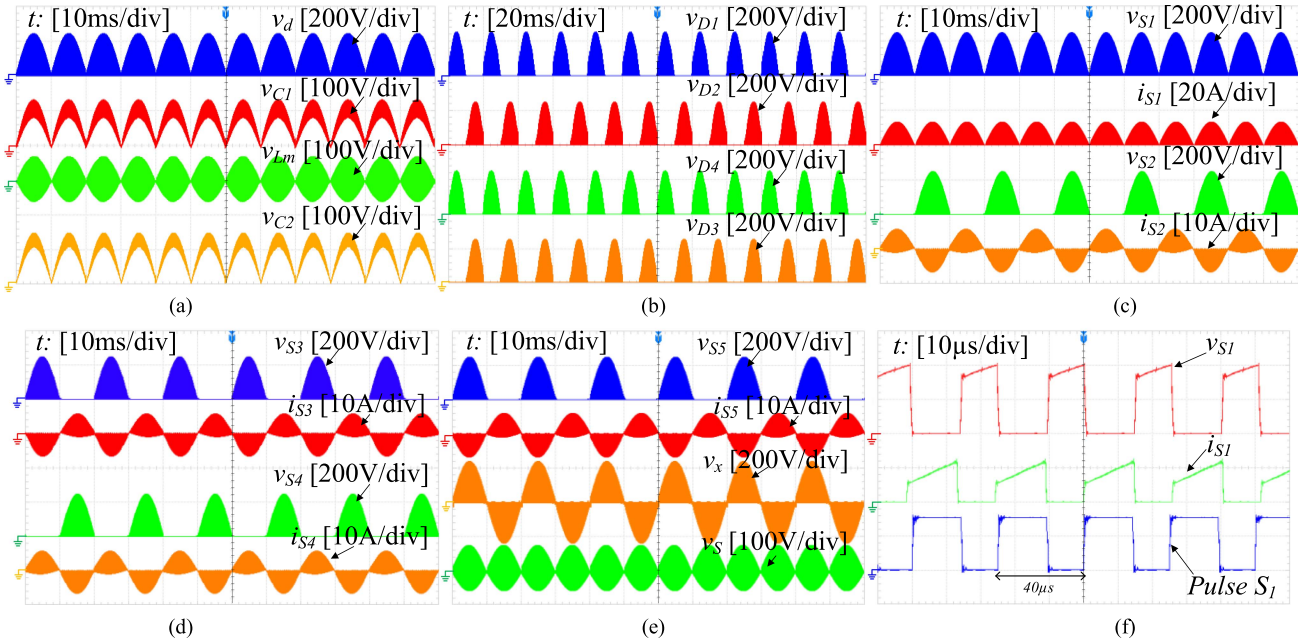

Fig. 12. Experimental waveforms of components. (a) Rectified voltage, voltages of capacitors *C1* and *C2*, and coupled inductor L_m. (b) Voltage stress on rectifier diodes *D1–D4*. (c) Voltage and current stresses on *S1* and *S2*, (d). Voltage and current stresses on *S3* and *S4*. (e) Voltage and current stress on *S5*, the secondary-side voltage of coupled inductor (*Vs*), and voltage prior to the output filter (V_X). (f) Magnified voltage and current stresses for *S1*.

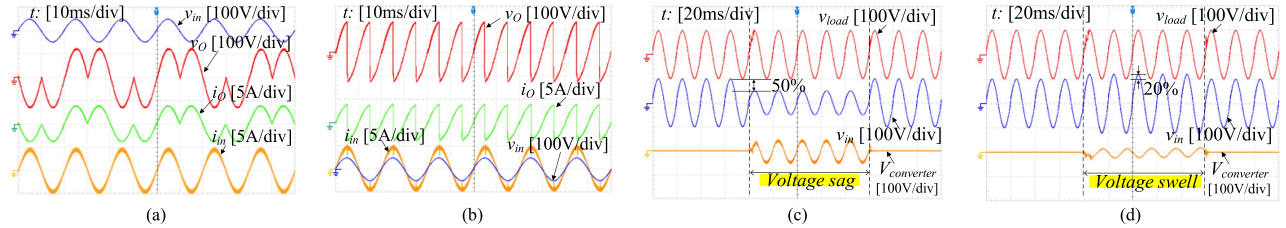

Fig. 13. Input and output waveforms. (a) For 25 Hz output frequency. (b) For 100 Hz output frequency. (c) Laboratory test of the converter as a DVR for voltage sag mitigation. (d) Laboratory test of the converter as a DVR for voltage swell mitigation.

voltages and input/output currents for 25 Hz and 100 Hz output frequencies, respectively. In order to evaluate the operation of the converter as a DVR, it is inserted in series with the load. In this case, a single-phase inverter with output sinusoidal voltage waveform is connected to the proposed converter instead of an autotransformer to provide a programmed step change in voltage amplitude. To evaluate the performance of the converter under a power sag condition, a 50% voltage sag has been applied to the input voltage. As shown in Fig. 13(c), when the controller detects voltage sag, it increases the duty cycle to mitigate this issue. For instance, in this case, the duty cycle has reached 0.5 and enters noninverting mode to eliminate the applied voltage sag. To test the performance of the converter for power swell, as shown in Fig. 13(d), a 25% voltage swell has been applied

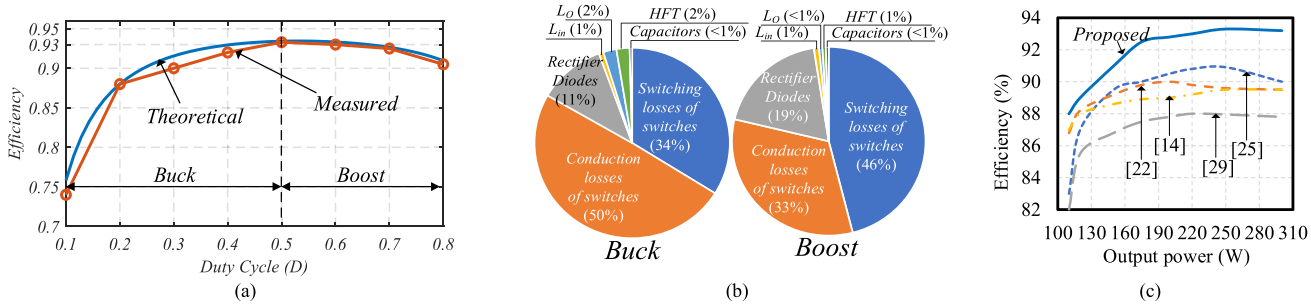

Fig. 14. Efficiency analysis. (a) Efficiency versus duty cycle for $n = 1$. (b) Division of power losses for buck and boost. (c) Efficiency comparison at the nominal load.

to the input voltage. Here, the controller increases the duty ratio to 0.16 from zero and enters inverting mode to reduce the load voltage. The efficiency versus the duty cycle change has been plotted, as shown in Fig. 14(a). The experimental efficiency is close to the theoretical one. The peak theoretical efficiency is 93.5%, while its practical value equals 93.3%. Thus, the theoretical loss and efficiency analysis are verified. Also, the best utilization area shown in Fig. 6 is validated where the achieved efficiency is placed over 90%, and the losses are significantly reduced. The practical efficiency is slightly different from the theoretical value due to the RC snubber circuit. Now, since the theoretical loss model has been verified, it is possible to deduce the division of power losses using (19)–(36), as depicted in Fig. 14(b). For buck operation, the duty cycle is assumed to be 0.37, and for boost operation, it is assumed to be 0.55. Fig. 14(c) compares the efficiency of the topology with its competitors for the same voltage, current and power. As shown, the proposed converter provides better power conversion efficiency.

VII. Conclusion

A new isolated buck-boost ac–ac converter was proposed. It produced inverting and noninverting modes of operation with identical characteristics and controlled the output voltage frequency in fixed steps. The converter requires a smaller count of active and passive components and generates continuous input and output currents. Using a high-frequency transformer instead of a line-frequency transformer reduced its size and cost, while the turns ratio of a high-frequency transformer provided an additional control variable for adjusting the voltage gain. The performance of the proposed topology was examined by using laboratory tests. Results indicate that the maximum efficiency of the converter is 93.3%, and its achieved efficiency is better than its counterparts. In addition, it was shown that the converter has a smaller input current and output voltage THDs than its competitors. Laboratory tests on the prototype as a DVR confirmed that it is suitable for both deep or shallow power sag and swell.

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