An Integrated Suppression Method of Both Gate-Source Voltage Oscillation and Crosstalk for GaN HEMT Gate Driver

Lurenhang Wang, *Student Member, IEEE*, Xizhi Sun, *Student Member, IEEE*, Yishun Yan, Mingcheng Ma, and Dianguo Xu, *Fellow, IEEE*

***Abstract*—There are serious gate-source oscillation and crosstalk problems in the application of gallium nitride (GaN) devices characterized by faster switching speed and lower threshold, which causes misconduction and breakdown of the gate. A gate diver integrated suppression of gate-source oscillation and crosstalk for GaN HEMT (ISGD) is proposed in this article as the solution for these problems. An additional capacitor in the proposed gate diver can be used to absorb gate-source voltage spike without affecting the switching speed by its precharging and be a part of the charge pump at the same time, which can generate negative voltage to leave margin for the influence of positive crosstalk and build a low impedance path to suppress negative crosstalk without an additional negative supply. By decoupling the precise generation timing of self-recovering negative voltage from the switching process, it becomes feasible to the implementation of negative voltage to almost avoid dead time, thereby further reducing reverse conduction loss during dead time. Furthermore, the integrated suppression of gate-source voltage oscillation and crosstalk can simplify the circuit, enhancing reliability for engineering applications. A double-pulse test based on the GS66508B verifies the effectiveness of ISGD as a solution for the gate-source voltage oscillation and crosstalk.**

***Index Terms*—Crosstalk suppression, gallium nitride high-electron mobility transistor (GaN HEMT), gate-source voltage oscillation suppression, negative voltage self-recovery.**

I. Introduction

GALLIUM nitride (GaN) devices have many advantages, such as smaller parasitic capacitance, superior switching performance, and no reverse recovery loss. In applications of GaN high-electron mobility transistor (HEMT), the switching frequency of power converters can reach several MHz or even tens of MHz, effectively improving the power density [1], [2], [3], [4], [5], [6], [7], [8], [9].

However, the advancement of GaN device applications towards high power density is impeded by technical challenges regarding reliability. The high *dv/dt* and *di/dt* associated with high switching frequency exacerbate the gate-source voltage oscillation during turn-ON and turn-OFF [10], [11], [12], [13], [14], [15], [16]. In high power applications, the serious gate-source voltage oscillation approaches or even exceeds the tolerance limit of GaN devices, which can easily cause the breakdown of the gate. The crosstalk problem is also significantly aggravated by the high *dv/dt* in GaN-based bridge leg topology [17], [18], [19], which severely threatens the reliability of GaN devices. Moreover, the crosstalk voltage level grows with the increasing bus voltage, making it challenging for the application of GaN devices in high power systems.

There are generally two traditional methods to suppress gate-source oscillation. One is to increase the gate resistance, which will slow down the turn-ON and turn-OFF process and increase the switching loss [20]. In [21], a method to predict the gate voltage overshoot in GaN HEMT is proposed by accurately calculating the gate voltage and then obtaining the precise value increment of the gate drive resistance to suppress the overshoot at the expense of the fast-switching characteristic of GaN HEMT. Another approach is optimizing the printed circuit board (PCB) layout to reduce the gate loop inductance for suppression of gate-source oscillation, but it is difficult to reduce the gate loop inductance in practical applications due to various factors.

There are three traditional methods of suppressing crosstalk problems. The first category is to reduce the *dv/dt* of the device, such as increasing the gate drive resistor and parallel external gate-source capacitor. While this method solves crosstalk, it reduces device turn-ON/turn-OFF speed, limiting the high-speed switching capabilities of GaN HEMT [22]. Secondly, an isolated negative power supply or charge pump applies a gate-source negative voltage. It is worth noting that a constant negative voltage on the gate causes higher reverse conduction loss during the dead time and a risk of gate reverse breakdown due to the negative crosstalk. The third category is to provide a low-impedance path for the crosstalk current which means the Miller current is shunted and the crosstalk voltage amplitude is reduced [23], [24], [25], [26], [27], [28]. One is active Miller clamping with the detection of the gate voltage. Not only does the detection require additional voltage detection circuits, but the voltage can also be measured inaccurately due to the presence of stray inductance in the circuit, leading to incorrect switching actions [23], [24],

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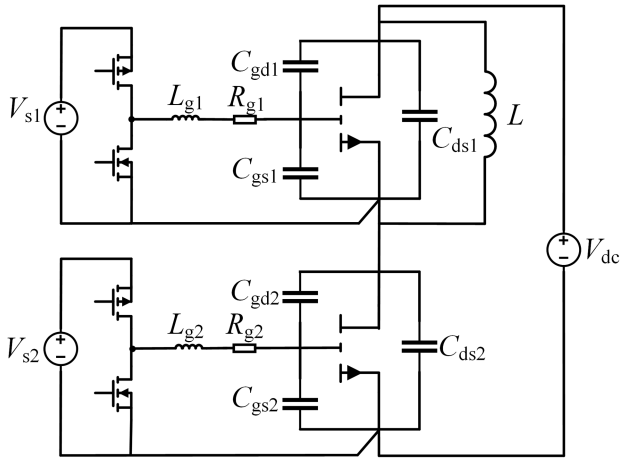

Fig. 1. Bridge configuration based on GaN HEMT.

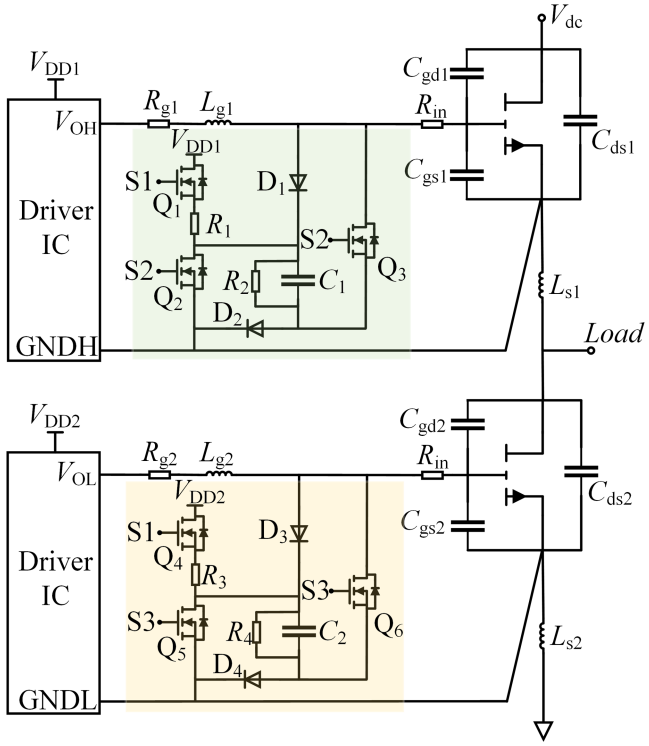

Fig. 2. Topology of proposed ISGD.

[25], [26], [27]. Another method is realized by passive devices [28]. However, the diode-based low-impedance path requires an elaborate design of the low-impedance path direction for the positive and negative crosstalk.

In this article, an integrated suppression method of both gate-source voltage oscillation and crosstalk for GaN HEMT gate driver by precharging capacitor and a self-recovery negative voltage is proposed. This design minimizes gate-source voltage peak, crosstalk voltage level, and dead-time reverse conduction loss. The double-pulse test experiment verifies the method and conclusions proposed in this design.

The rest of the article is organized as follows. Section II begins with an introduction to the structure and the operation mode of the ISGD. Section III analyzes the suppression process of transient oscillation and crosstalk. Then, the parameter design method is introduced. In Section IV, the experimental data is given and then analyzed to verify the validity of the proposed method. Finally, Section V concludes this article.

II. Topology and Operation Mode of ISGD

A. ISGD Topology

The application topology of the classic bridge leg structure based on GaN HEMT is shown in Fig. 1. $V_{\rm dc}$ is the bus voltage. L is the high-side transistor load inductance. R_g and L_g are the gate drive resistor and gate parasitic inductance. C_{gd}, C_{gs}, and C_{ds} are the GaN HEMT junction capacitances.

In the bridge circuit, when one transistor is turned ON and OFF at high speed, the rapid change of the voltage of the other transistor will result in the appearance of crosstalk. When the control transistor is turned ON, the switching node voltage rises rapidly, and the C_{gd} of the freewheeling transistor starts charging and generates an inductive current, which flows through the drive circuit and generates a forward voltage drop acting on the gate-source to form a voltage spike that generates positive crosstalk. When the spike exceeds the gate threshold voltage ($V_{\rm th}$), the freewheeling transistor is at risk of misconduction, which may damage the entire bridge. When the control transistor is turned OFF, the current in the opposite direction causes a negative voltage spike at the gate of the freewheeling transistor, resulting in negative crosstalk. This spike may approach or exceed the maximum negative voltage that the gate can withstand, causing damage to the device. Meanwhile, the gate-source voltage will generate severe overshoot when GaN HEMT is turned ON quickly, so it is easy to generate the risk of gate breakdown.

In this article, the ISGD is proposed to solve the gate-source voltage oscillation and crosstalk problems. As shown in Fig. 2, the proposed driving circuit can be used in bridge application topologies with alternating high and low side conduction or only one side conduction, such as an inverter, buck, buck-boost, etc. The topology consists of a precharging module (Q_1-R_1-C_1-D_2), an oscillation absorption module (D_1-C_1-D_2), a negative voltage generation module (Q_2-C_1-D_2), and a crosstalk suppression module (Q_2-C_1-Q_3). Meanwhile, the ISGD provides some ideas for further exploring the application of GaN HEMT in high-frequency and high-power applications.

B. Operation Modes of ISGD

The operation modes of the ISGD are shown in Fig. 3. Fig. 4 shows the control signal timing diagram and schematic waveforms. It should be noted that different topologies may produce crosstalk in the upper or lower transistors, or both transistors may produce crosstalk, such as the full bridge topology. In this article, the half-bridge topology of the load inductor in parallel with the upper transistor is selected to analyze the working mode. In this case, the lower transistor is the control transistor, and the upper transistor is the freewheeling transistor. When the lower

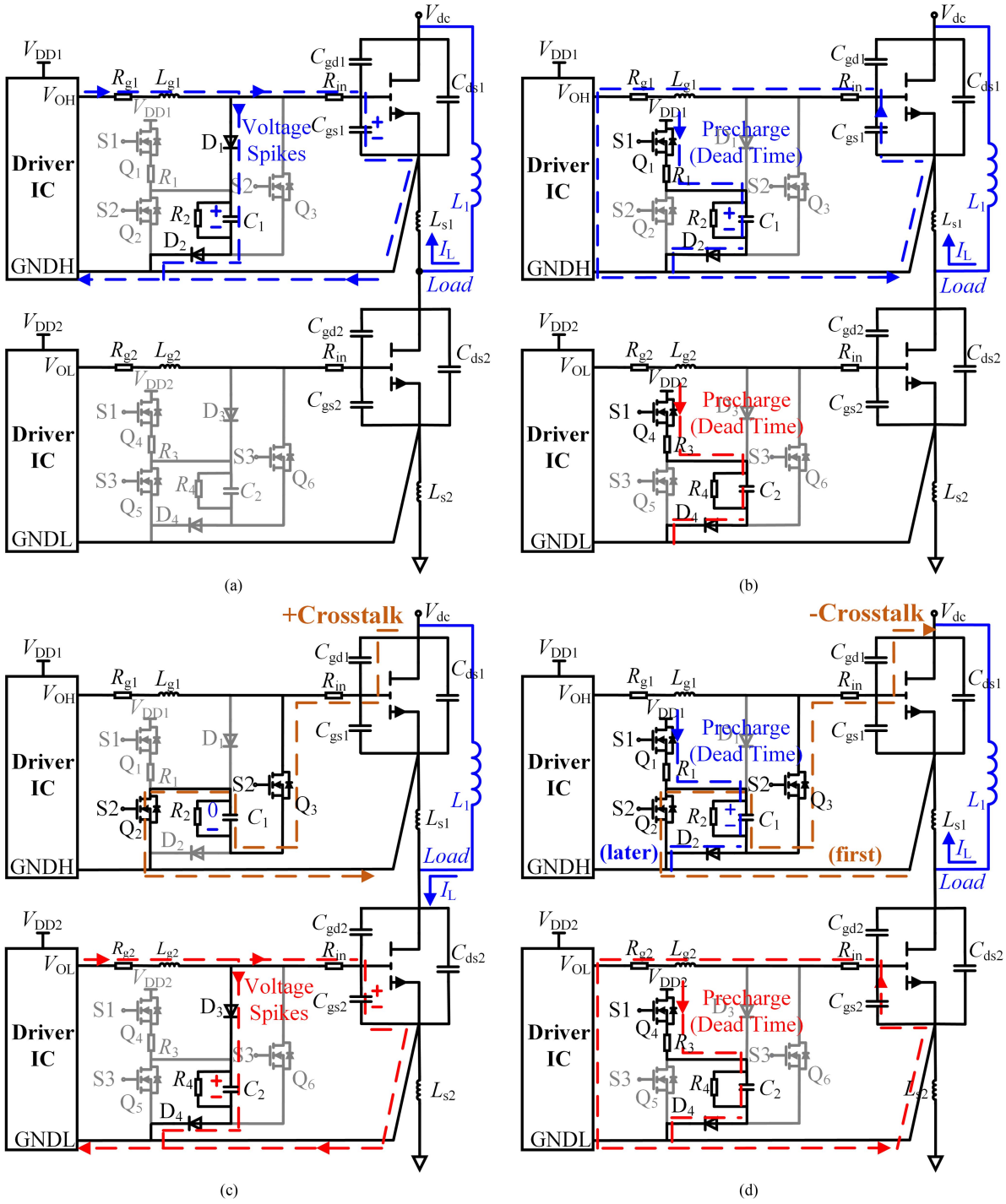

Fig. 3. Operation modes of ISGD. (a) Mode I, the process of the freewheeling transistor turn-ON. (b) Mode II, the process of the freewheeling transistor turn-OFF and dead time. (c) Mode III, the process of the control transistor turn-ON. (d) Mode IV, the process of the control transistor turn-OFF and dead time.

transistor is turned ON and OFF, crosstalk is generated on the gate of the upper transistor. Because of this, *S*3 can always be kept low in this topology. *S*2 and *S*3 are generated by the driving signal of GaN HEMT, and the specific generation method is explained in detail in Section III. The operation modes of the device are as follows.

1) *Mode* I (t_0-t_1): In this mode, the freewheeling GaN HEMT is turned ON. An overshoot occurs in the gate-source voltage. However, D_1 remains in the cut-OFF state until the overshoot reaches above 6 V, so it does not affect the normal turn-ON process. Once the gate-source voltage reaches a predetermined value or higher, D_1 conducts, and ISGD absorbs the voltage spike through C_1. The ability to absorb the voltage spike is related to the value of C_1. The gate-source voltage is clamped at the sum of V_{D1}, V_{D2}, and V_{C1}, which is V_{DD1}.

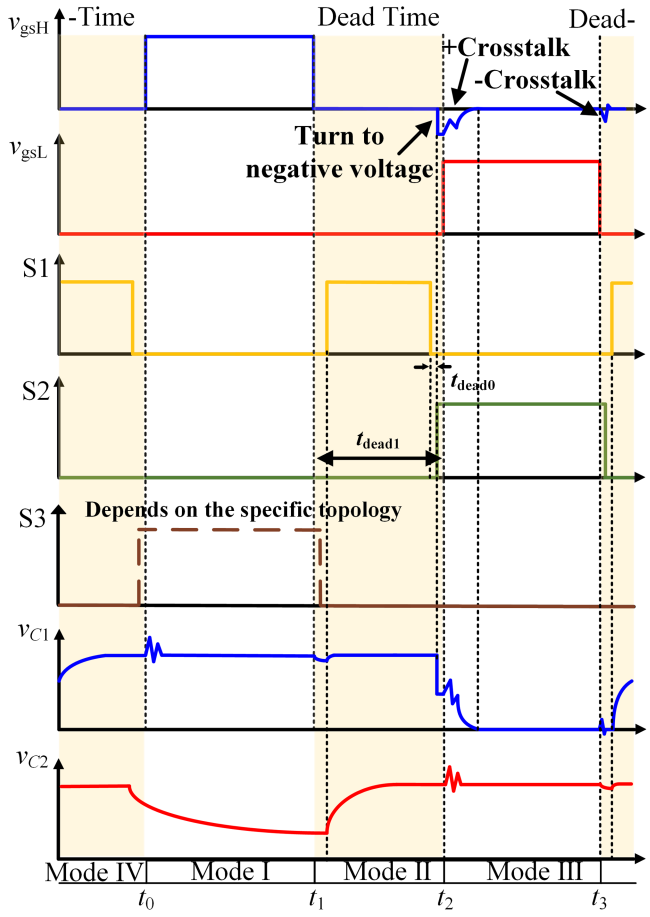

Fig. 4. Control signal timing diagram and the voltage waveforms of the precharging capacitors of the proposed ISGD.

2) *Mode* II (t_1-t_2): This mode is the dead time which is shown in Fig. 3(b). The designed gate-source voltage spike absorption module does not affect the turn-OFF process of the freewheeling transistor. Since the C_{gs} discharges through R_g much faster than C_1, D_1 always remains in a cut-OFF state during the turn-OFF process. In this mode, both the control transistor and the freewheeling transistor are under the process of precharging. The freewheeling transistor is taken as an example to analysis this process. The driving power supply used by the upper transistor precharge C_1 through Q_1-R_1-C_1-D_2. Considering the forward voltage drop of D_1 and the charging speed of C_1, R_1, and R_2 are designed to divide the V_{DD1} in the precharging path to ensure that C_1 is charged to the preset value, which makes sure D_1 conducts at the right time. R_2 is connected in parallel with C_1 to drain the charge in C_1, which prevents the high voltage that may occur in C_1 from damaging the power supply.
3) *Mode* III (t_2-t_3): In this mode, the control transistor is turned ON. The gate-source voltage oscillation suppression process is the same as described in mode I. Commutation occurs in the bridge leg, and the operation mode of the ISGD is shown in Fig. 3(c). The voltage of the switching node drops during the turn-ON process of the control transistor. Without a crosstalk suppression topology such as ISGD, the Miller current will charge C_{gs} of the freewheeling transistor via C_{gd}, causing the gate-source voltage to exceed the threshold voltage and risking misconduction. In this topology, the positive crosstalk is effectively suppressed by the negative voltage created by C_1. S_2 turns to the high level just a moment before t_2, turning ON Q_2 and Q_3 and applying the negative voltage of C_1 on the gate according to the charge pump principle. *S*2 is not an extra control signal, which is explained in detail in Section III. The value of positive crosstalk voltage gets far away from V_{th}, and the suppression effect is shown as the +Crosstalk in Fig. 4. In this topology, negative gate-source voltage generation is decoupled from the GaN HEMT switching process, which means there is no continuous negative V_{gs} during the whole dead time. It is helpful to decrease the reverse conduction loss.
4) *Mode* IV (t_3-t_0): Similar to the generation of positive crosstalk, negative crosstalk occurs when the control transistor is turned OFF. In ISGD, Q_2-C_1-Q_3 creates a low-impedance path, which shunts a large amount of Miller current and reduces the negative crosstalk voltage level. The negative crosstalk suppression effect is shown in Fig. 4 as—crosstalk. The negative voltage formed by C_1 at mode III quickly recovers itself to zero voltage and will not pose a risk of gate breakdown when negative crosstalk occurs.

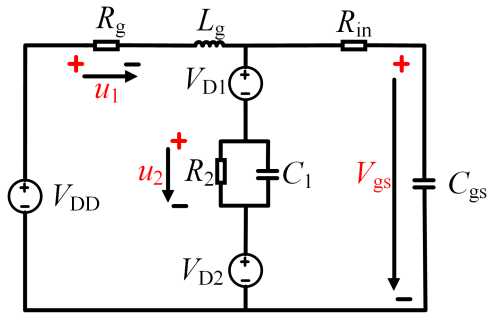

Fig. 5. Equivalent circuit diagram of the oscillation suppression.

III. Transient Analysis and Parameters Design of ISGD

A. Gate-Source Voltage Oscillation Suppression Process

The equivalent circuit diagram of ISGD during oscillation suppression is shown in Fig. 5. Considering the existence of a voltage drop V_{D1} of diode D_1, R_1 and R_2 are designed to divide the voltage and make the oscillation suppression function turn ON at the right moment. The relationship is

$$(V_{DD} - V_{D2})\frac{R_2}{R_1 + R_2} = V_{gs} - V_{D1} - V_{D2}. \quad (1)$$

When V_{gs} is higher than the preset value, D_1 conducts, and the oscillation suppression module works. According to Kirchhoff's law, the relationship between voltage and current in Fig. 5 can

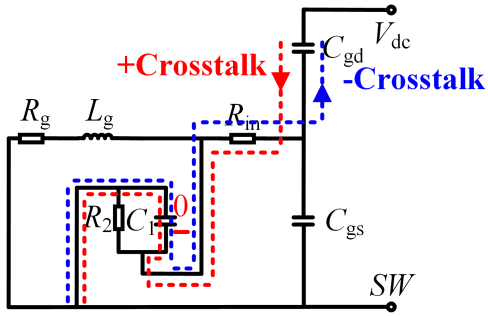

Fig. 6. Equivalent circuit diagram of the crosstalk suppression.

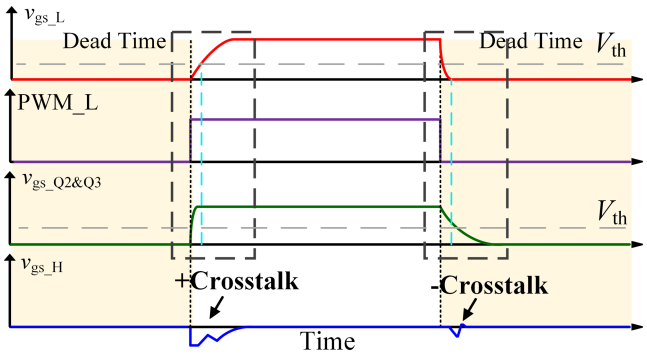

Fig. 7. The detail control signal timing diagram of v_{gs_L}, PWM_L, $v_{gs\_Q2\&Q2}$, and v_{gs_H}.

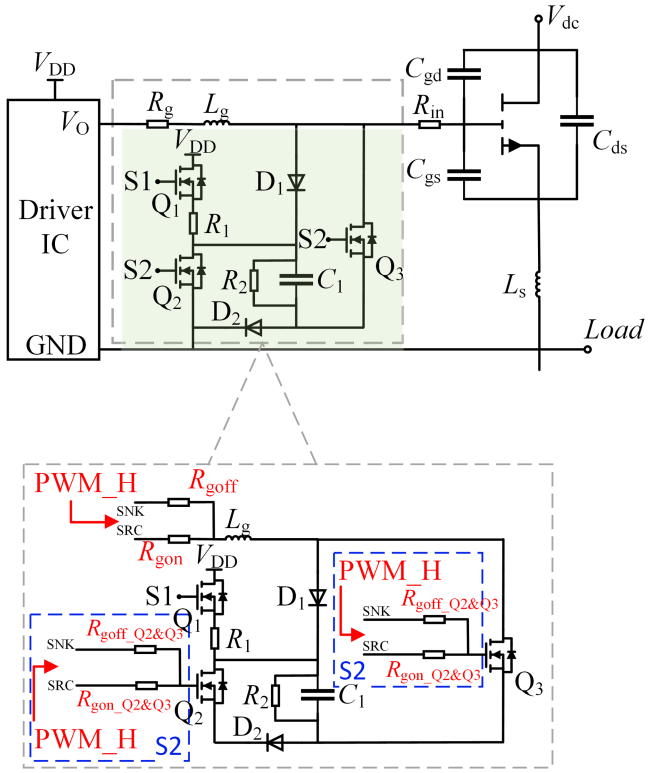

Fig. 8. Specific driving loop topology of GaN HEMT, Q_2, and Q_3.

be obtained as follows:

$$\begin{cases} V_{DD}=u_1+u_2+L_g\frac{di_{R_g}}{dt}+V_{D1}+V_{D2} \\ i_{R_g}=\frac{u_1}{R_g} \\ \frac{u_1}{R_g}=\frac{u_2}{R_2}+C_1\frac{du_2}{dt}+C_{gs}\frac{dV_{gs}}{dt} \\ V_{D1}+V_{D2}+u_2=R_{\text{in}}C_{gs}\frac{dV_{gs}}{dt}+V_{gs} \end{cases}. \tag{2}$$

Due to the considerable time constant of R_2 and C_1 compared to the dead time, C_1 discharges negligibly in the period from C_1 is precharged completely to the turn-ON timing of GaN HEMT. The initial voltage of C_1 and C_{gs} are

$$V_{C_1}(0^-)=(V_{DD}-V_{D2})\frac{R_2}{R_1+R_2} \tag{3}$$

$$V_{C_{gs}}(0^-)=V_{DD}. \tag{4}$$

According to the Laplace transform of (2), V_{gs} can be expressed as

$$V_{gs}(s)=\frac{\frac{V_{DD}}{s}+\left[(R_g+sL_g)\left(\frac{1}{R_g}+sC_1\right)\right]\frac{V_{D_1}+V_{D_2}}{s}+A}{B} \tag{5}$$

$$A=CV_g\left(0^-\right)+\left(R_g+sL_g\right)C_1u_2(0^-) \tag{6}$$

$$B=D+sC_{gs}\left(R_g+sL_g\right) \tag{7}$$

$$C=\left[(R_g+sL_g)\left(\frac{1}{R_2}+sC_1\right)+1\right]R_{\text{in}}C_{gs}+\left(R_g+sL_g\right)C_{gs} \tag{8}$$

$$D=\left[(R_g+sL_g)\left(\frac{1}{R_1}+sC_1\right)+1\right](sR_{\text{in}}C_{gs}+1)+sC_{gs}\left(R_g+sL_g\right). \tag{9}$$

To simplify the time-domain expressions, the intermediate variables M1, M2, M3, M4, N1, N2, N3, N4, N5, N6, k1, k2, k3, k4, k5, k6, and k7 are defined, and the specific expressions are shown as A.1 in Appendix. The time-domain expression of V_{gs} can be obtained as (10) by taking the inverse Laplace transform with the intermediate variable

$$V_{gs}(t)=k_4+k_5e^{-k_1t}+k_6e^{-k_2t}+k_7e^{-k_3t}. \tag{10}$$

B. Negative Voltage Generation Circuit and Crosstalk Suppression Process

The equivalent circuit diagram of ISGD for crosstalk suppression is shown in Fig. 6. From (1), it can be seen that the charge stored in advance of C_1 is

$$Q_{C_1}=(V_{DD}-V_{D2})\frac{R_2}{R_1+R_2}C_1. \tag{11}$$

When Q_2 and Q_3 are turned ON, the charge is transferred from C_1 to C_{gs}. Ignoring the transfer losses, the transferred charge can be calculated as

$$Q_{C_1+C_{gs}}=-V_N\left(C_{gs}+C_1\right). \tag{12}$$

The negative voltage depth can be calculated as

$$V_N=-\left(V_{DD}-V_{D2}\right)\frac{R_2C_1}{\left(R_1+R_2\right)\left(C_{gs}+C_1\right)}. \tag{13}$$

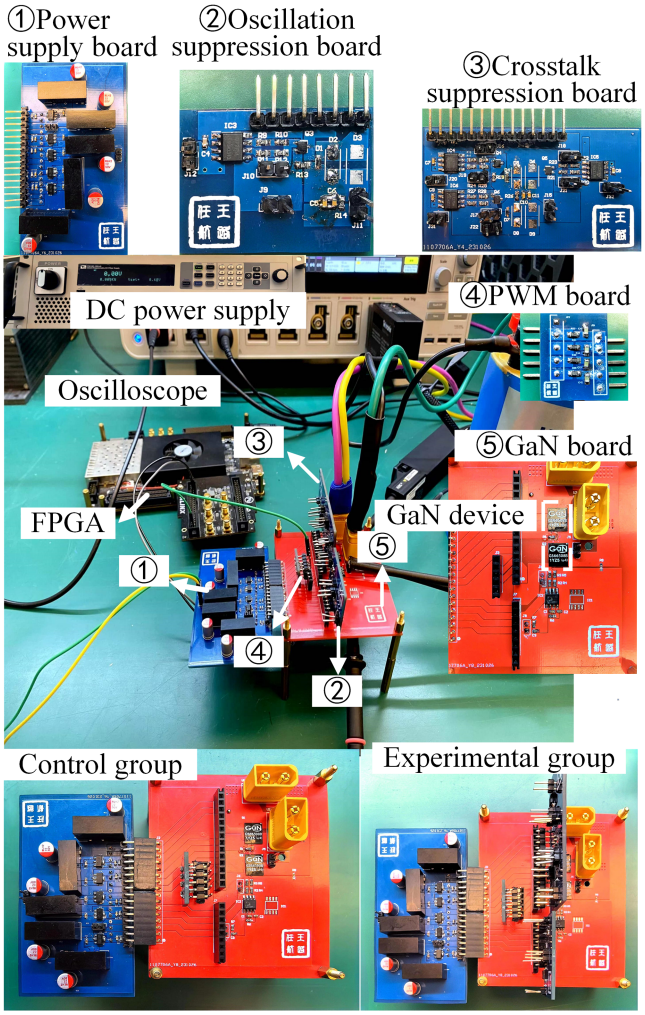

Fig. 9. Experimental platform for ISGD double-pulse experiment.

In order to ensure that the device is safely turned ON and OFF, the voltage value of positive and negative crosstalk needs to be guaranteed within a safe range. The following conditions need to be met

$$1.5\left(\Delta V_P + \Delta V_N\right) \le V_{\text{th}} - V_{ngs\_\max} \tag{14}$$

$$V_{gs\_\text{off}} + 1.5\Delta V_P \le V_{\text{th}} \tag{15}$$

$$V_{gs\_\text{off}} - 1.5\Delta V_N \ge V_{ngs\_\max} \tag{16}$$

where ΔV_P is the positive crosstalk, ΔV_N is the negative crosstalk, V_{th} is the device threshold voltage, and $V_{ngs\_\max}$ is the maximum negative voltage that the gate can withstand. According to the crosstalk voltage estimation in [23], ΔV_P and ΔV_N can be estimated as

$$\begin{cases} \Delta V_P = \dfrac{C_{gd}V_{\text{dc}}}{C_1+C_{iss}} + \dfrac{R_g {C_1}^2 C_{gd} V_{\text{dc}}}{(C_1+C_{iss})^2 T_f}\left(1 - e^{\frac{-(C_1+C_{iss})T_f}{R_g C_1 C_{iss}}}\right) \\ \Delta V_N = \dfrac{C_{gd}V_{\text{dc}}}{C_1+C_{iss}} + \dfrac{R_g {C_1}^2 C_{gd} V_{\text{dc}}}{(C_1+C_{iss})^2 T_r}\left(1 - e^{\frac{-(C_1+C_{iss})T_r}{R_g C_1 C_{iss}}}\right) \end{cases}. \tag{17}$$

Taking (14) to (17) as boundary conditions can provide a reference for the parameter design within the driving circuit.

C. ISGD Parameter Design

In the parameter design of ISGD, the parameter selection of C_1 is a key part. Assuming that the GaN HEMT dead time for t_{dead0}, Q_1, and Q_2 dead time for t_{dead1}, then there are

$$4R_1C_1 + t_{\text{dead1}} \le t_{\text{dead0}}. \tag{18}$$

The relationship between R_1 and R_2 is derived from (1), taking into account the voltage-dividing effects of both R_1 and R_2

$$R_2 = \frac{\left(V_{DD} - V_{D1} - V_{D2}\right) R_1}{V_{D1}}. \tag{19}$$

In ISGD, the precharging capacitor must be charged within the dead time, so there is a minimum limit of dead time in this article, which means there is a maximum switching frequency limit. If C_1 is taken to a large value, the effect of gate-source voltage oscillation suppression and crosstalk suppression will be better, but the precharging time will increase, which leads to a longer dead time and a smaller switching frequency. On the contrary, if C_1 is set to a small value, the switching frequency can increase, but the effect of gate-source voltage oscillation suppression and crosstalk suppression will worsen. The boundary condition of gate-source voltage oscillation suppression is that the peak of gate-source voltage oscillation cannot exceed the maximum transient voltage that the gate can withstand, and the boundary condition of positive and negative crosstalk suppression is (14)–(16). These boundary conditions must be met at the maximum power class.

To prevent the Q_1-Q_2 bridge leg from damaging the MOSFET device because of shooting through, R_1 has a minimum value. According to the datasheet of RSF014N03, the maximum current it can flow is 5.6 A, and the minimum R_1 can be calculated as 1.1 Ω. Set R_1 to 1.8 Ω. A method for calculating the peak value of gate-source voltage is proposed in [21]. Combining (A.2) [21] ((21) in [21]), (5)–(9), the inequality relationships of (14)–(16), (18), and the value of R_1 in this article, the minimum value of C_1 can be calculated as 4.83 nF, taking C_1 to be 5 nF. The precharging process of C_1 is considered complete after four time constants, so the precharging time is 36 ns. Considering that Q_1 and Q_2 need a certain dead time, the dead time of GaN HEMT bridge is set at 40 ns, which means ISGD can work at a maximum frequency of 2.5 MHz. According to (19), the calculated value of R_2 is determined to be 32.4 Ω.

Take the upper transistor as an example to illustrate. In order to occupy less I/O port resources of the controller and reduce the control complexity of ISGD, the control signals required for Q_2-Q_3 can be given by reusing the drive signals of GaN HEMTs. The Q_1 signal needs to be given by the FPGA. Q_2 and Q_3 should be turned ON before the lower GaN HEMT because the gate-source voltage of the freewheeling transistor should turn negative before positive crosstalk comes. Q_2 and Q_3 should be turned OFF later than the lower GaN HEMT because the low impedance path should be disconnected after the negative crosstalk has completely ended. In general, the method to generate differences in V_{gs_L} and $V_{gs\_Q2\&Q3}$ through PWM_L is to utilize the value of C_{iss} of GS66508B (GaN HEMT) and RSF014N03 (MOSFET, Q_2-Q_3) with nearly 4 times difference.

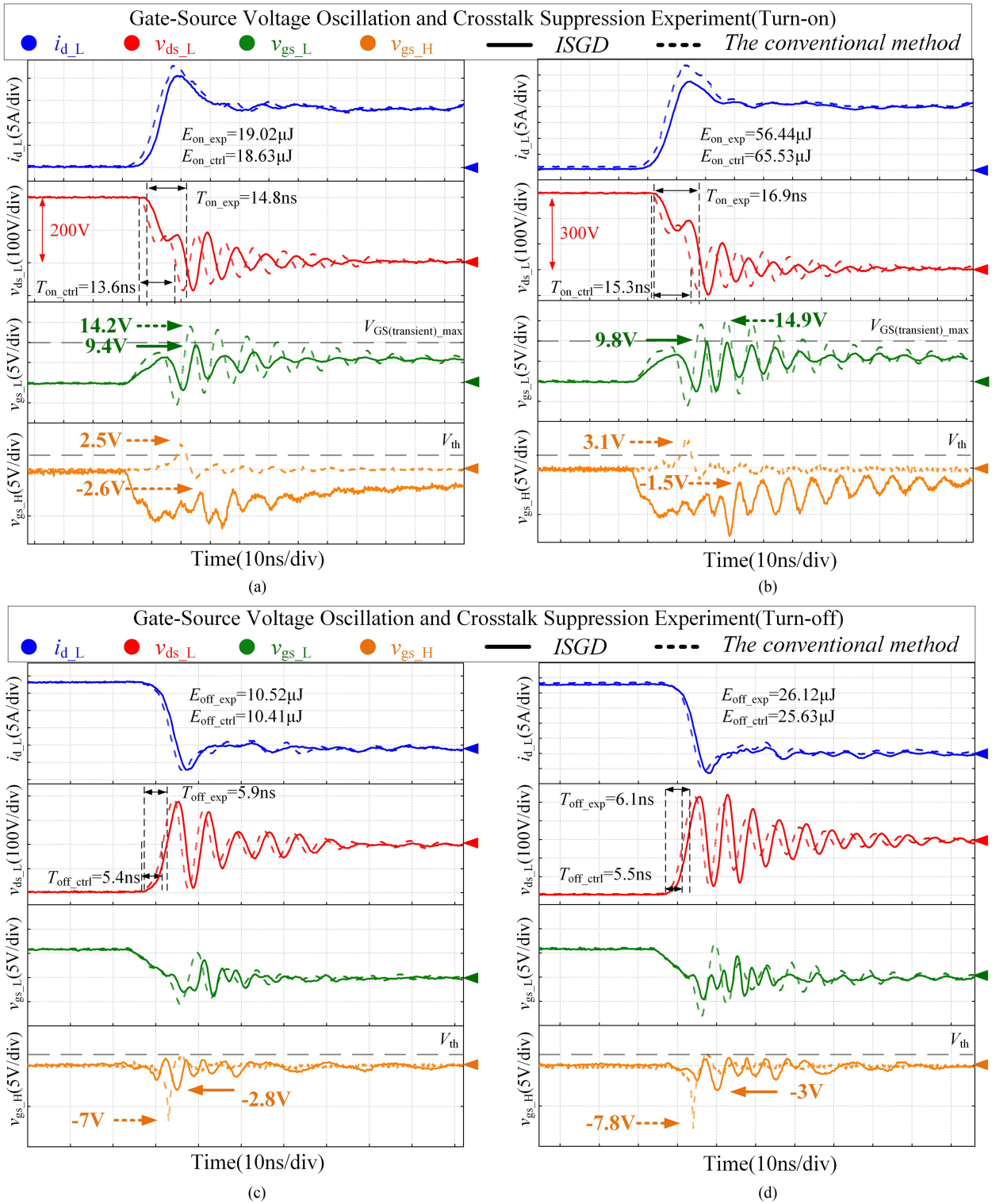

Fig. 10. Double-pulse experimental waveform of ISGD. (a) 200 V/15 A group (turn-ON). (b) 300 V/20 A group (turn-ON). (c) 200 V/15 A group (turn-OFF). (d) 300 V/20 A (turn-OFF).

The detailed control signal timing diagram is shown in Fig. 7. The specific driving loop topology of GaN HEMT, Q_2, and Q_3 is shown in Fig. 8. The specific parameters are designed as follows. For *RC* circuits, V_0 is the initial voltage of the capacitor, V_1 is the voltage at which the capacitor can eventually be charged or discharged, and V_t is the voltage of the capacitor at time t. There is

$$V_t = V_0 + (V_1 - V_0) \times \left(1 - e^{-t/RC}\right) \tag{20}$$

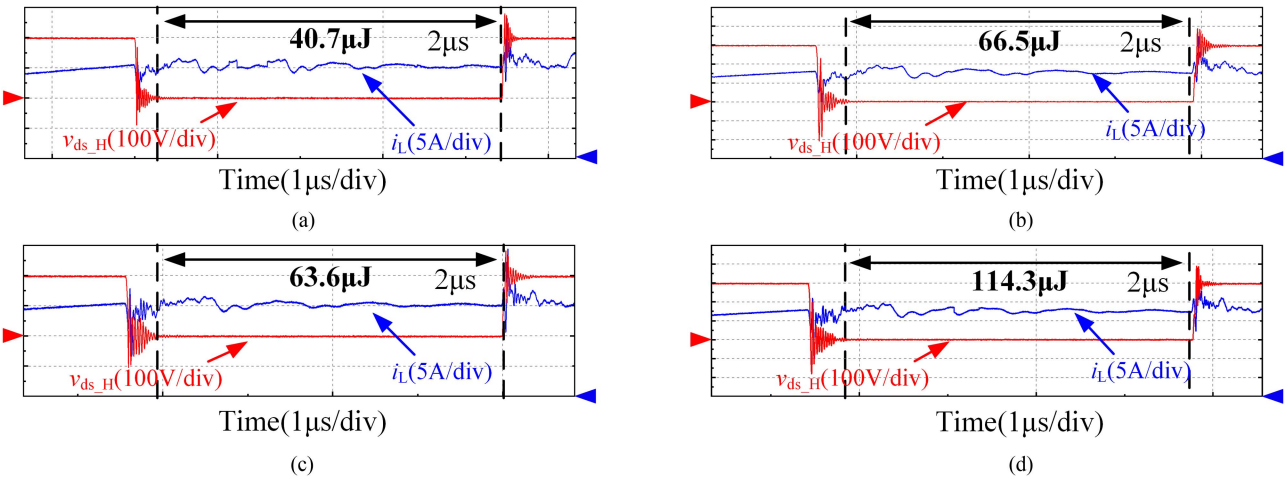

Fig. 11. Comparison of reverse conduction loss. (a) Experimental group of ISGD at 200 V/15 A. (b) Experimental group of ISGD at 300 V/23 A. (c) Control group of constant −2 V V_{gs} at 200 V/15 A. (d) Control group of constant −2 V V_{gs} at 300 V/23 A.

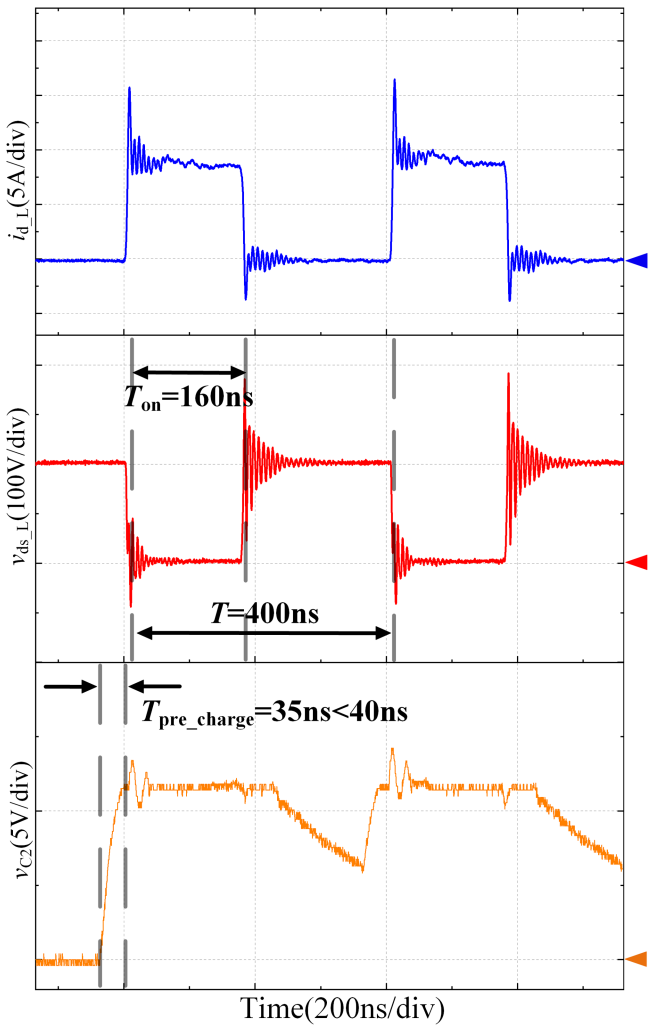

Fig. 12. Waveforms of v_{ds_L}, i_{d_L}, and v_{C2} at 2.5 MHz switching frequency.

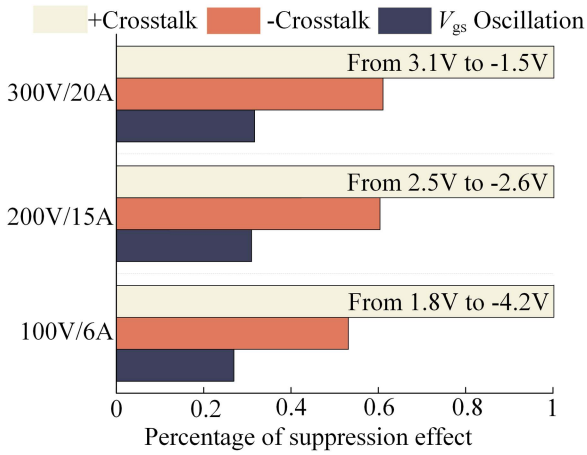

Fig. 13. Percentage of suppression effect under different working conditions.

namely

$$t = RC \times \ln\left[\left(V_1 - V_0\right) / \left(V_1 - V_t\right)\right]. \tag{21}$$

It is necessary to fully ensure that there is no mis-conduction of the freewheeling transistor, that is, to ensure that the negative gate-source voltage has been established before the positive crosstalk comes. Q_2 and Q_3 must be turned ON fully before the gate-source voltage of the lower GaN HEMT rises to V_{th}. The voltage of the capacitor is considered to be full after four time constants. The C_{iss} of Q_2&Q_3 and $R_{gon\_Q2\&Q3}$ must have passed four time constants before this. According to the datasheet, the C_{iss} of GS66508B (GaN HEMT) is 242 pF, the R_{gon} is 10 Ω, and the C_{iss} of RSF014N03 (MOSFET, Q_2-Q_3) is 70 pF. It can be calculated that the maximum $R_{gon\_Q2\&Q3}$ is 2.89 Ω. Finally, $R_{gon\_Q2\&Q3}$ is selected as 2 Ω. According to (21), it is easy to calculate that the time required for V_{gs} of GaN HEMT charging to V_{th} is 0.81 ns, and the time required for Q_2 and Q_3 fully turning ON is 0.56 ns.

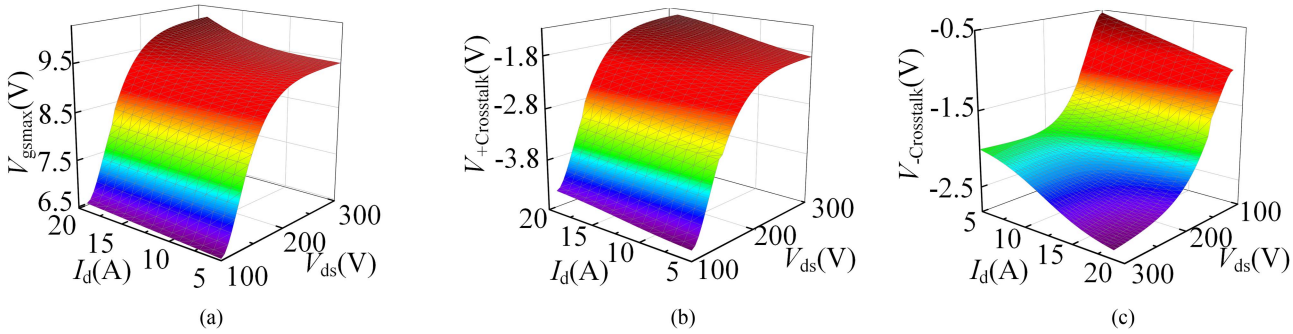

Fig. 14. Experimental results of ISGD under different working conditions. (a) Gate-source voltage oscillation suppression. (b) Positive crosstalk suppression. (c) Negative crosstalk suppression.

TABLE I
DETAILED PARAMETER LIST FOR THE ISGD

Symbol	Description	Value
C_1	X7R Capacitor	5 nF
R_1	Resistor	1.8 Ω
R_2	Resistor	32.4 Ω
$R_{gon\_GaN\ HEMT}$	Resistor	10 Ω
$R_{goff\_GaN\ HEMT}$	Resistor	3.3 Ω
$R_{gon\_Q2\&Q3}$	Resistor	2 Ω
$R_{goff\_Q2\&Q3}$	Resistor	50 Ω
D_1,D_2	Diode	NSR0520V2T1G
Q_1,Q_2,Q_3	NMOS	RSF014N03TL
GaN driver IC	4 Amp ISOdriver	Si8271AB
GaN HEMT	GaN HEMT	GS66508B

It is necessary to fully ensure that there is no possibility of a reverse breakdown in the gate of the freewheeling transistor, that is, to ensure that the low impedance path cannot be closed before the complete end of negative crosstalk. The gate-source voltage of Q_2 and Q_3 can only drop below $V_{\rm th}$ after the gate-source voltage of the lower GaN HEMT drops to 0 V. The R_{goff} of the GaN_HEMT is 3.3 Ω. It can be calculated that the R_{goff} of Q_2 and Q_3 is at least 36.18 Ω. Select $R_{goff\_Q2\&Q3}$ as 50 Ω. According to (21), it is easy to calculate that the time required for V_{gs} of GaN HEMT reaching 0 V is 3.2 ns, and the time required for V_{gs} of Q_2 and Q_3 discharging to $V_{\rm th}$ is 4.41 ns.

The ISGD circuit utilizes two diodes, D_1 and D_2. The function of D_1 is to control when the oscillation absorption module comes into play, while D_2 forms a charge pump in conjunction with C_1 to generate negative voltage. Both functions require low conduction loss and low reverse recovery characteristics. Schottky diodes are selected to meet these requirements. Furthermore, three MOSFETs are used in this circuit design, which necessitate low $R_{\rm dson}$, low Q_g, and low reverse recovery characteristics.

Based on the analysis above, the selected diode is NSR0520V2T1G, and the RSF014N03TL is chosen as the MOSFET. Table I presents a detailed parameter list.

IV. EXPERIMENTAL VERIFICATION

In order to validate the proposed method for suppressing gate-source voltage oscillation and crosstalk, a double-pulse test experimental platform is established, as shown in Fig. 9. The platform uses a 1 GHz-bandwidth optical isolation probe TIVP1 to measure the gate-source voltage of the high-side transistor. A 200 MHz-bandwidth differential probe THDP0200 is utilized to measure the drain-source voltage of the low-side transistor. A 1 GHz-bandwidth passive probe TPP1000 is used to measure the gate-source voltage of the lower transistor. The drain current of the low-side transistor is measured by Rogowski coil CWT/UM/03. The GaN HEMT selected for this platform is the GS66508B, which ISGD uses its Kelvin source with minimal common-source inductance [29]. The Si8271AB driver IC is chosen to drive the GaN HEMT. A load inductance of 100 μH is connected in parallel with the high-side transistor. The IT6018D DC power supply supplies the dc-bus voltage. The FPGA provides the GaN HEMT switching signals. The plug-in structure is designed to ensure fairness for the comparison between the experimental group and the control group, as shown in Fig. 9. Two groups use the same GaN device board 5. Plugging in boards 2 and 3 equals the ISGD working on the gate of high-side and low-side transistors.

In the experimental and control group of ISGD, the low-side transistor is turned ON at 6 V and off at 0 V. The conventional method with only R_g is regarded as the control group. The double-pulse test waveforms are shown in Fig. 10.

As shown in Fig. 10(a) and (b), by precharging C_1 for absorbing voltage spike, a 33.8% reduction of gate-source voltage oscillation from 14.2 to 9.4 V under 200 V/15 A is achieved compared to the control group. Similarly, a 34.2% decrease in gate-source voltage oscillation from 14.9 to 9.8 V under 300 V/20 A is also observed. The GS66508B has a transient maximum gate-source voltage of 10 V. And in the experimental group, all gate-source voltage spikes are effectively suppressed below the safe voltage. By pregenerating a negative voltage by a charge pump, under 200 V/15 A, the positive crosstalk voltage spike decreases from 2.5 to −2.6 V. Similarly, under 300 V/20 A, there is a reduction from 3.1 to −1.5 V. The threshold voltage of the GS66508B is 1.7 V. In the experimental group, all positive crosstalk voltage is reduced below $V_{\rm th}$. From Fig. 10(c) and (d), the value of the negative crosstalk voltage remains within the limit of -20 V of GS66508B. Under 200 V/15 A, a 60% reduction of peak negative crosstalk voltage from −7 to −2.8 V is achieved. Similarly, for 300 V/20 A, there is a 61.5% decrease in peak negative crosstalk voltage from −7.8 to −3.0 V.

TABLE II
COMPARISON OF SWITCHING LOSS BETWEEN ISGD AND CONVENTIONAL METHOD

Gate driver\Voltage(V)		100		200		300	
	Current(A)	E_{on}(μJ)	E_{off}(μJ)	E_{on}(μJ)	E_{off}(μJ)	E_{on}(μJ)	E_{off}(μJ)
Conventional method	5	2.72	1.36	6.32	3.81	9.71	5.13
	10	4.57	2.52	10.69	4.96	16.95	8.92
	15	5.58	4.93	18.63	10.41	37.21	16.92
	20	7.11	6.63	29.31	15.07	65.53	25.63
Proposed method	5	2.91	1.34	6.93	3.72	10.11	5.68
	10	4.84	2.55	11.58	5.12	15.86	9.21
	15	7.31	4.98	19.02	10.52	32.75	17.13
	20	9.92	6.75	27.4	15.23	56.44	26.12

TABLE III
COMPARISON BETWEEN ISGD AND OTHER AGDS

Items	Chen et al. [3]	Li et al. [28]	Nagao et al. [30]	Qiu et al. [31]	Takaha shi et al. [32]	Wang et al. [33]	Jin et al. [34]	Zhang et al. [35]	This Paper
Power class	300V 8A	100V 10A	48V 4A	400V 10A	48V 4A	24V 1A	400V 40A	800V 300A	300V 20A
Operating frequency	500kHz	100kHz	500kHz	100kHz	1MHz	5MHz	/	/	2.5MHz
Function of-	Only-Crosstalk	Only-Crosstalk	Only-Crosstalk	Only-Crosstalk	Only-Crosstalk	Only-Crosstalk	Only V_{gs} Oscillation	Only V_{gs} Oscillation	V_{gs} Oscillation and Crosstalk
Costs of Single Gate Driver($USD)	20.54	5.65	8.32	8.39	10.85	9.77	/	/	7.01
Control signal	3	1	2	1	1	1	1	1	2
Driving loss	375 μJ	135 nJ	103.8 nJ	93.8 nJ	/	55 nJ	1.68 μJ	9.4 μJ	84.5 nJ
V_{gs} drop	/	/	/	/	/	/	41.1%	16.6%	34.2%
Positive crosstalk drop	/	From -0.77 V to -0.57 V	/	From 2.7 V to 1.2 V	/	From -1.3 V to -0.5 V	/	/	From 3.1 V to -1.5 V
Negative crosstalk drop	/	From -6.7 V to -3.67 V	/	From -12.2 V to -6.7 V	/	From -4.8 V to -1.3 V	/	/	From -7.8 V to -3 V
Reverse conduction loss drop	/	27.45%	23%	/	50%	/	/	/	41.81%

The turn-ON and turn-OFF time are the rising and falling time of v_{ds} by measurement. In the experimental group, under 200 V/15 A, the turn-ON time is 14.8 ns, and the turn-OFF time is 5.9 ns. Under 300 V/20 A, the turn-ON and turn-OFF time are 16.9 ns and 6.1 ns. In the control group under 200 V/15 A, the turn-ON time is 13.6 ns and the turn-OFF time is 5.4 ns. The turn-ON time is 15.3 ns and the turn-OFF time is 5.5 ns under 300 V/20 A.

One distinguishing feature of ISGD is the very short time of negative gate-source voltage in the dead time, effectively reducing reverse conduction loss. A new control group is established to validate this characteristic, whose gate-source voltage of the freewheeling transistor is constant -2 V during reverse conduction. The duration for measuring reverse conduction loss is extended to 2 μs to minimize the probe measurement error as a proportion of the overall loss analysis. The experimental group achieves an average power of 20.35 W and a loss of 40.7 μJ in 2 μs under 200 V/15 A, and an average power of 33.25 W and a loss of 66.5 μJ under 300 V/23 A as shown in Fig. 11(a)

and (b). On the other hand, the control group by the high-side transistor with a constant -2 V gate-source voltage achieves an average power of 31.8 W and a loss of 63.6 μJ at 200 V/15 A, and an average power of 57.15 W and a loss of 114.3 μJ at 300 V/23 A, as shown in Fig. 11(c) and (d). The experimental group shows the reduction of reverse conduction loss by 36.01% under 200 V/15A and 41.81% under 300 V/23 A compared to constant -2 V driving. These experimental results demonstrate the effectiveness of ISGD in reducing reverse conduction loss.

The experimental waveforms of ISGD operating at 2.5 MHz are shown in Fig. 12. It can be seen that the precharging time of C_2 in Fig. 12, which is the precharging capacitor of the lower transistor, is only 35 ns. The dead time of 40 ns is completely achievable, which proves that ISGD can work at a 2.5 MHz switching frequency.

Fig. 13 shows the experimental results of ISGD. It lists the percentage of suppression effect under three working conditions.

It can show the performance of ISGD under these working conditions more clearly.

As shown in Fig. 14, the result confirms that the ISGD effectively reduces gate-source voltage oscillation and crosstalk under working conditions of V_{ds} from 100 to 300 V and $I_{\rm d}$ from 5 to 20 A. In Fig. 14(a), the highest oscillation occurs at 300 V/20 A but does not exceed 10 V, which is within the maximum transient gate-source voltage of the GS66508B. In Fig. 14(b), positive crosstalk peaks at 300 V/20 A and stays below 1.7 V, which is less than the $V_{\rm th}$ of the GS66508B. This effectively reduces the probability of misconduction. In Fig. 14(c), the maximum negative crosstalk occurs at 300 V/20 A, but it does not exceed -20 V. This is within the maximum transient negative gate-source voltage of the GS66508B, ensuring device reliability.

The switching loss under different working conditions is given in Table II. As the power class increases, the turn-ON switching loss of ISGD may be smaller than the conventional method. This is because the traditional method does not suppress crosstalk, which inevitably has a transient bridge shooting through and makes the current peak under the conventional method greater than ISGD, so the loss may be greater than ISGD.

The comparison of ISGD and other AGDs is given in Table III. As given in Table III, ISGD has two functions: gate-source voltage oscillation suppression and crosstalk suppression. At the same time, ISGD can also effectively reduce the reverse conduction loss. The effects of suppression and loss reduction are obvious compared with other AGDs. The ISGD can operate at up to 2.5 MHz, using only one additional signal. The costs and driving loss are similar to other AGDs.

V. Conclusion

This article proposes an ISGD-based suppression method of gate-source voltage oscillation and crosstalk for GaN HEMT gate drivers. In the first place, the integrated topology of ISGD can effectively suppress the gate-source voltage oscillation and crosstalk by a precharging capacitor at the same time. Second, there is no need for an additional negative voltage supply for the crosstalk problem. Third, it does not affect the turn-ON and turn-OFF speed of GaN HEMT. Finally, compared to keeping a constant negative gate voltage, the ISGD can effectively reduce reverse conduction loss, which helps maintain the operating temperature of the device and improve the efficiency of the converter. The double-pulse test confirms the effectiveness of ISGD in suppressing gate-source voltage oscillation (34.2% improvement) and crosstalk (61.5% improvement). Additionally, the reverse conduction loss is reduced by up to 41.81%.

Appendix

$$
\begin{cases}
M_1 = \frac{R_2+R_{g1}}{L_{g1}R_{\rm in}C_1R_2C_{gs1}} \\
M_2 = \frac{R_2R_{\rm in}C_{gs1}+L_{g1}+R_{g1}(R_2C_{gs1}+R_2C_1+R_{\rm in}C_{gs1})}{R_2L_{g1}R_{\rm in}C_1C_{gs1}} \\
M_3 = \frac{R_2R_gR_{\rm in}C_1C_{\rm gs1}+L_{g1}(R_2C_{gs1}+R_2C_1+R_{\rm in}C_{gs1})}{R_2L_{g1}R_{\rm in}C_1C_{gs1}} \\
M_4 = \sqrt[3]{\frac{{M_1}^2}{2}+\sqrt{\frac{{M_1}^4}{4}+\frac{(M_1M_3-M_2)^3}{27}}}+ \\
\sqrt[3]{\frac{{M_1}^2}{2}-\sqrt{\frac{{M_1}^4}{4}+\frac{(M_1M_3-M_2)^3}{27}}} \\
N_1 = \frac{L_{g1}+R_2R_{g1}C_1}{L_{g1}R_2C_1}V_{gs}(0^-)+\frac{V_{\rm D1}+V_{\rm D2}}{R_{\rm in}C_{gs1}} \\
N_2 = \frac{(L_{g1}+R_2R_{g1}C_1)(V_{\rm D1}+V_{\rm D2})}{L_{g1}R_2C_1R_{\rm in}C_{gs1}}+\frac{R_1+R_{g1}}{R_2L_{g1}C_1} \\
+\frac{(R_{g1}+sL_{g1})V_{gs}(0^-)}{L_{g1}C_1R_{\rm in}}+\frac{(R_{g1}+sL_{g1})u_2(0^-)}{L_{g1}C_{gs1}R_{\rm in}} \\
N_3 = \frac{V_{\rm DD1}}{R_{\rm in}L_{g1}C_1C_{gs1}}+\frac{R_{\rm g1}(V_{\rm D1}+V_{\rm D2})}{R_1R_{\rm in}C_1C_{gs1}L_{g1}} \\
N_4 = V_{gs}(0^-)-\frac{N_3}{k_1k_2k_3} \\
N_5 = N_1-\frac{N_3(k_1+k_2+k_3)}{k_1k_2k_3} \\
N_6 = N_2-\frac{N_3(k_1k_2+k_1k_3+k_2k_3)}{k_1k_2k_3} \\
k_1 = \frac{M_3-\frac{M_1}{M_4}+\sqrt{\left(M_3-\frac{M_1}{M_4}\right)^2-4M_4}}{2} \\
k_2 = \frac{M_3-\frac{M_1}{M_4}-\sqrt{\left(M_3-\frac{M_1}{M_4}\right)^2-4M_4}}{2} \\
k_3 = \frac{M_1}{M_4} \\
k_4 = \frac{N_3}{k_1k_2k_3} \\
k_5 = N_4-\frac{{k_3}^2N_4-k_3N_5+N_6}{(k_3-k_2)(k_3-k_1)}-\frac{-{k_2}^2N_4+k_2N_5-N_6}{(k_2-k_1)(k_3-k_2)} \\
k_6 = \frac{-{k_2}^2N_4+k_2N_5-N_6}{(k_2-k_1)(k_3-k_2)} \\
k_7 = \frac{{k_3}^2N_4-k_3N_5+N_6}{(k_3-k_2)(k_3-k_1)}
\end{cases}
\tag{A.1}
$$

$$
v_{GS}(s) = \frac{z_1V_{\rm DR}(s)+z_2V_{\rm IN}(s)}{1+p_1s+p_2s^2+p_3s^3+p_4s^4}
$$

$$
\begin{cases}
z_1 = s^2L_DC_{GD}+s\left(\frac{L_S+L_D}{R_{\rm ON}}\right)+1 \\
z_2 = s^2L_GC_{GD}+s\left(R_GC_{GD}-\left(\frac{L_S}{R_{\rm ON}}\right)\right) \\
p_1 = \left(\frac{L_S+L_D}{R_{\rm ON}}\right)+R_GC_{ISS} \\
p_2 = L_DC_{GD}+\left(\frac{L_S+L_D}{R_{\rm ON}}\right)R_GC_{ISS} \\
\quad +L_GC_{ISS}+L_SC_{GS} \\
p_3 = L_DC_{GD}R_GC_{ISS}+\left(\frac{L_S+L_D}{R_{\rm ON}}\right)(L_GC_{ISS}+L_SC_{GS}) \\
\quad +(L_GC_{GS}-L_DC_{GD})\left(R_G-\left(\frac{L_S}{R_{\rm ON}}\right)\right) \\
p_4 = L_DL_GC_{GD}C_{ISS}+L_DL_SC_{GD}C_{GS} \\
\quad +L_SL_GC_{GS}C_{GD}+L_DL_GC_{GD}^2
\end{cases}
\tag{A.2}
$$

REFERENCES

[1] W. Saito et al., "A 120-W boost converter operation using a high-voltage GaN-HEMT," *IEEE Electron Device Lett.*, vol. 29, no. 1, pp. 8–10, Jan. 2008.

[2] Z. Liu, X. Huang, F. C. Lee, and Q. Li, "Package parasitic inductance extraction and simulation model development for the high-voltage cascode GaN HEMT," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1977–1985, Apr. 2014.

[3] Y. Chen, R. Wang, X. Liu, and Y. Kang, "Gate-drive power supply with decayed negative voltage to solve crosstalk problem of GaN synchronous buck converter," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 6–11, Jan. 2021.

[4] B. Sun, R. Burgos, and D. Boroyevich, "Ultralow input–output capacitance PCB-embedded dual-output gate-drive power supply for 650 V GaN-based half-bridges," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1382–1393, Feb. 2019.

[5] T. Zhu, F. Zhuo, F. Zhao, F. Wang, and T. Zhao, "Quantitative model-based false turn-on evaluation and suppression for cascode GaN devices in half-bridge applications," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 10166–10179, Oct. 2019.

[6] M. Alsolami, K. A. Potty, and J. Wang, "A gallium-nitride-device-based switched capacitor multiport multilevel converter for UPS applications," *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 6853–6862, Sep. 2017.

[7] K. J. Chen et al., "GaN-on-Si power technology: Devices and applications," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 779–795, Mar. 2017.

[8] E. Gurpinar and A. Castellazzi, "Single-phase T-type inverter performance benchmark using Si IGBTs, SiC MOSFETs, and GaN HEMTs," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7148–7160, Oct. 2016.

[9] R. Xie et al., "Switching transient analysis for normally-off gan transistor with p-GaN gate in a phase-leg circuit," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3711–3728, Oct. 2019.

[10] S. Yu et al., "A 400-V half bridge gate driver for normally-off GaN HEMTs with effective *dv/dt* control and high *dv/dt* immunity," *IEEE Trans. Ind. Electron.*, vol. 70, no. 1, pp. 741–751, Jan. 2023.

[11] A. Lemmon, M. Mazzola, J. Gafford, and C. Parker, "Instability in half-bridge circuits switched with wide band-gap transistors," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2380–2392, May 2014.

[12] J. E. Makaran, "Gate charge control for MOSFET turn-off in PWM motor drives through empirical means," *IEEE Trans. Power Electron.*, vol. 25, no. 5, pp. 1339–1350, May 2010.

[13] Y. Wu, M. Jacob-Mitos, M. L. Moore, and S. Heikman, "A 97.8% efficient GaN HEMT boost converter with 300-W output power at 1 MHz," *IEEE Electron Device Lett.*, vol. 29, no. 8, pp. 824–826, Aug. 2008.

[14] X. Huang, Z. Liu, Q. Li, and F. C. Lee, "Evaluation and application of 600 V GaN HEMT in cascode structure," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2453–2461, May 2014.

[15] T. Yanagi, H. Otake, and K. Nakahara, "The mechanism of parasitic oscillation in a half bridge circuit including wide band-gap semiconductor devices," in *Proc. IEEE Int. Meeting Future Electron Devices*, 2014, pp. 1–2, doi: 10.1109/IMFEDK.2014.6867087.

[16] J. Wang and H. S.-H. Chung, "Impact of parasitic elements on the spurious triggering pulse in synchronous buck converter," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6672–6685, Dec. 2014.

[17] R. Xie, H. Wang, G. Tang, X. Yang, and K. J. Chen, "An analytical model for false turn-on evaluation of high-voltage enhancement-mode GaN transistor in bridge-leg configuration," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 6416–6433, Aug. 2017.

[18] J. Chen, Q. Luo, J. Huang, Q. He, P. Sun, and X. Du, "Analysis and design of an RC snubber circuit to suppress false triggering oscillation for GaN devices in half-bridge circuits," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2690–2704, Mar. 2020.

[19] H. Li et al., "Paralleled operation of high-voltage cascode GaN HEMTs," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 815–823, Sep. 2016.

[20] R. Hou, J. Xu, and D. Chen, "A multivariable turn-on/turn-off switching loss scaling approach for high-voltage GaN HEMTs in a hard-switching half-bridge configuration," in *Proc. IEEE 5th Workshop Wide Bandgap Power Devices Appl.*, 2017, pp. 171–176.

[21] J. P. Kozak et al., "An analytical model for predicting turn-ON overshoot in normally-OFF GaN HEMTs," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 99–110, Mar. 2020.

[22] S. Jahdi, O. Alatise, J. A. O. Gonzalez, R. Bonyadi, L. Ran, and P. Mawby, "Temperature and switching rate dependence of crosstalk in Si-IGBT and SiC power modules," *IEEE Trans. Ind. Electron.*, vol. 63, no. 2, pp. 849–863, Feb. 2016.

[23] Z. Zhang, F. Wang, L. M. Tolbert, and B. J. Blalock, "Active gate driver for crosstalk suppression of SiC devices in a phase-leg configuration," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1986–1997, Apr. 2014.

[24] Y. Li, M. Liang, J. Chen, T. Q. Zheng, and H. Guo, "A low gate turn-OFF impedance driver for suppressing crosstalk of SiC MOSFET based on different discrete packages," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 1, pp. 353–365, Mar. 2019.

[25] B. Yang and J. Zhang, "Effect and utilization of common source inductance in synchronous rectification," in *Proc. 20th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2005, vol. 3, pp. 1407–1411.

[26] A. G. Black, "Impact of source inductance on synchronous buck regulator FET shoot through performance," in *Proc. IEEE Power Electron. Specialists Conf.*, 2007, pp. 981–986.

[27] Z. Chen, M. Danilovic, D. Boroyevich, and Z. Shen, "Modularized design consideration of a general-purpose, high-speed phase-leg PEBB based on SiC MOSFETs," in *Proc. 14th Eur. Conf. Power Electron. Appl.*, 2011, pp. 1–10.

[28] B. Li, G. Zhang, C. Li, G. Wang, S. Liu, and D. Xu, "Crosstalk suppression method for GaN-based bridge configuration using negative voltage self-recovery gate drive," *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 4406–4418, Apr. 2022.

[29] Y. Li, Y. Zhang, Y. Gao, S. Du, and J. Liu, "Switching characteristic analysis and application assessment of SiC MOSFET with common source inductance and kelvin source connection," *IEEE Trans. Power Electron.*, vol. 37, no. 7, pp. 7941–7951, Jul. 2022.

[30] J. Nagao, J. Furuta, and K. Kobayashi, "Capacitor-based three-level gate driver for GaN HEMT only with a single voltage supply," in *Proc. IEEE 21st Workshop Control Model. Power Electron.*, 2020, pp. 1–7.

[31] Z. Qiu et al., "An intelligent three-level active gate driver for crosstalk suppression of SiC MOSFET," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2020, pp. 203–208.

[32] T. Takahashi, T. Takehisa, J. Furuta, M. Shintani, and K. Kobayashi, "A three-level GaN driver for high false turn-ON tolerance with minimal reverse conduction loss," *IEEE Open J. Power Electron.*, vol. 4, pp. 357–366, 2023.

[33] X. Wang et al., "High-frequency three-level gate driver for GaN HEMT bridge crosstalk suppression," *IEEE Trans. Power Electron.*, vol. 39, no. 1, pp. 1343–1352, Jan. 2024.

[34] D. Jin, N. Qi, J. Ouyang, and C. Luo, "Analysis and reduction of turn-on gate-source voltage oscillation on paralleled SiC MOSFETs application," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2022, pp. 1–7.

[35] W. Zhang, X. Wang, M. S. A. Dahidah, G. N. Thompson, V. Pickert, and M. A. Elgendy, "An investigation of gate voltage oscillation and its suppression for SiC MOSFET," *IEEE Access*, vol. 8, pp. 127781–127788, 2020.

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