Active-Clamp Soft-Switching Push-Pull Full-Bridge Bidirectional DC–DC Converter Over a Wide Load Range

Qunfang Wu, *Member, IEEE*, Sen Xue, Heng Xi, Jiangli Ren, Zhifeng Sun, and Qin Wang, *Member, IEEE*

***Abstract*—In the energy storage scenarios of low-voltage-high-current, the three-switch push-pull full-bridge bidirectional dc–dc converter (TPFBC) can be used with the characteristics of fewer number of power switches and low cost compared with dual-active-bridge. Nevertheless, it has the disadvantages of high voltage stress and difficulty in realizing full-load zero-voltage switching. To address these problems, an improved active clamp push-pull full-bridge bidirectional dc–dc converter is proposed in this article, which is composed by adding a clamping capacitor to the TPFBC. The proposed topology can realize the voltage clamping function, so the low-voltage and low-cost devices are allowed to be used in this circuit. Besides, a minimum inductor current effective value control strategy is proposed in this article to reduce the inductance loss, and the power switches can achieve soft switching in a wide load range. Then, the forward and backward operation characteristics are symmetrical with a smooth switching of charging and discharging modes under the PWM plus phase shift modulation strategy. In addition, the transformer winding voltage has a higher number of levels, and it is closer to the sine wave enabling it to reduce reactive power and improve operation efficiency. The operation principle, detail characteristic analysis, control strategy, power losses analysis, and parametric design are presented, and a 500-W experimental prototype is built to verify the effectiveness.**

***Index Terms*—Active clamp, bidirectional dc/dc converters, zero-voltage switching (ZVS).**

I. Introduction

NOWADAYS, isolated bidirectional dc–dc converters are widely used in energy storage systems due to their characteristics of galvanic isolation and bidirectional transmission of energy [1]. The isolated bidirectional converters include full bridge, half-bridge, push-pull, etc. The full-bridge bidirectional converter, such as a dual-active-bridge (DAB) converter, can realize power bidirectional transmission under the phase shift control, which has the advantages of symmetry of the structure, simple control, and easy expansion [2], [3], [4]. However, the traditional DAB converter has some limitations such as large circulation, narrow soft-switching load range, and hard switching when input and output voltage mismatch. Therefore, extended-phase-shift (EPS) control, dual-phase-shift control, and triple-phase-shift control have been proposed to address these problems [5], [6], [7], [8]. The half-bridge bidirectional converter has only half the power switches, resulting in a lower manufacturing cost and simpler circuit structure. However, the current stress of the power switch increases by twice under the same transmission power, and the current ripple is much larger. The push-pull bidirectional converter has the advantages of fewer power switches and lower current stress [9], [10], [11], [12], [13]. Although the voltage stress is relatively high, the push-pull bidirectional converters are more suitable in low-voltage and high-current operating scenarios such as low-voltage energy storage systems.

A three-switch push-pull full-bridge bidirectional dc–dc converter (TPFBC) has been proposed in [14]. The full-bridge circuit at the low-voltage side is replaced by a three-switch push-pull circuit to reduce the number and cost of devices, which can maintain the similar working principle as the DAB converter. Moreover, it can effectively reduce circulation loss and improve efficiency by adjusting the duty cycle of the auxiliary switch, achieving phase shift control. However, the operating frequency of the auxiliary power switch is twice that of the other switches, and it is hard to achieve zero-voltage switching (ZVS) operation under a light load, resulting in high switching loss. More importantly, there will be a large voltage spike when the switch turns OFF due to the influence of transformer leakage inductance. Thus, it is necessary to add the clamping circuit to absorb the leakage inductance energy to reduce the voltage stress.

The traditional clamping circuit is composed of the clamping switch and capacitor, and they are usually connected in parallel with the main power switch in a push-pull circuit [15], [16], [17], [18]. Even though these circuits are symmetrical, the power devices are doubled and the low-cost advantage is no longer existing. The two clamping circuits in [16] are designed to share a capacitor, hence, the number and cost of capacitors can be

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reduced, and the current ripple can also be reduced by adjusting the dc inductor position to the power source. On this basis, the resonant circuit is introduced to help the power switches realize ZVS over a wide load range. However, more powerful devices and clamping switch conduction loss will be inevitable. Moreover, it can also be designed as a three-phase active clamp push-pull converter to increase the rated power [19], [20], [21], [22], [23], [24], [25], [26].

The converter proposed in [27] moves the clamping circuit to the source terminal to achieve the purpose of sharing a clamping circuit between two main power transistors. Since only one active clamping circuit is introduced. It can reduce the manufacturing cost and converter size successfully. It is worth noting that it is difficult to switch smoothly between charging and discharging modes due to the different modulation strategies. In the other improved push-pull-forward half-bridge converter presented in [28], only a clamping capacitor is required and the circuit is relatively simple to reduce power device costs. Also, this converter can achieve smooth switching between the charging and discharging modes. However, the ZVS conditions for forward transmission and backward transmission are different. It is difficult to realize ZVS under a light load, and the voltage stress of the power switches is high, which is not beneficial to the selection of the power switches. Therefore, the operating efficiency is rather lower when operating at a light load.

In this article, an improved active clamped TPFBC (AC-TPFBC) is proposed. Compared with similar converters such as DAB, TPFBC, and PPFHB, the presented AC-TPFBC has some advantages.

1) The topology introduces a clamping capacitor into the TPFBC, which reduces the voltage stress of the power switches and facilitates device selection.
2) Switching losses can be reduced owing to the ZVS of all switches over a wide load range.
3) The energy stored in the transformer leakage inductance is used for the soft-switching action and no additional resonant inductor is required.
4) The number of levels in the transformer winding's voltage is increased and the reactive power can be reduced accordingly.

The rest of this article is organized as follows. Section II gives the topology and the operation principle of the proposed converter. The characteristics of the converter, the conditions of realizing ZVS, the control strategy, power losses, and the parametric design are analyzed in Section III. The existing similar topologies comparison study is discussed in Section IV. The experimental results are given in Section V, and finally, Section VI concludes this article.

II. Operation and Analysis of the Proposed Converter

Fig. 1 shows the proposed AC-TPFBC topology in this article. It is mainly composed of an active clamp three-switch push-pull circuit, a full-bridge circuit, and an isolated transformer, in which the L_{k1} and L_{k2} are the leakage inductance of the high-frequency transformer, and L represents the series inductance on the secondary side of the transformer. V_i and V_o represent the

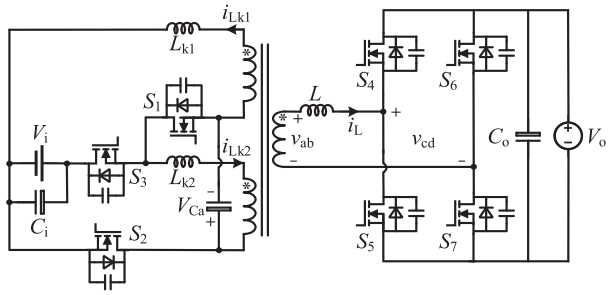

Fig. 1. Proposed topology of AC-TPFBC.

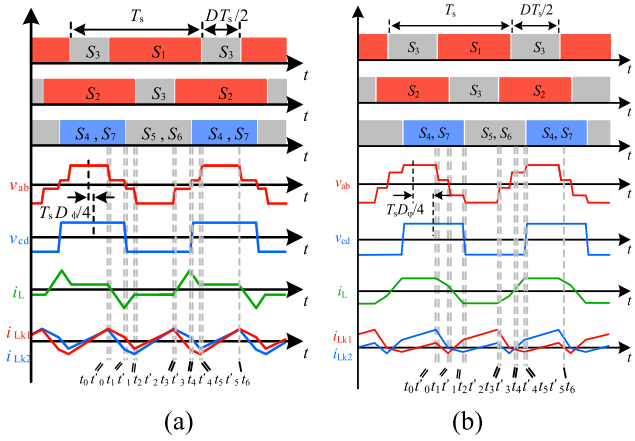

Fig. 2. Key steady-state operation waveforms (forward transmission). (a) Case A ($0 < D_\varphi < 1\text{-}D$). (b) Case B ($1\text{-}D < D_\varphi < 1$).

input and output voltages, and V_{Ca} represents the voltage of the clamping capacitor (C_a). i_{Lk1}, i_{Lk2}, and i_L represent the currents flowing through the transformer's primary and secondary sides, respectively.

The implementing modulation strategy for the proposed AC-TPFBC is similar to the EPS used for DAB, which keeps the duty cycle of v_{cd} at 0.5, where it can realize power regulation and commutation by changing the switch S_3 drive signal duty cycle and the phase shift angle between v_{ab} and the v_{cd}. The key waveforms under forward and backward transmission are shown in Figs. 2 and 3, respectively. The gate driving signals of S_1 and S_2 are phase-shifted by 180° with a duty cycle larger than 0.5, and the drive signal of S_3 is complementary to the drive signal of S_1 and S_2. The drive signals of S_4 and S_7, S_5 and S_6 are the same and their duty cycle keeps 0.5. Assuming that the driver signals duty cycle and frequency of S_3 are D and $2f_s$, respectively, and the shift ratio between v_{ab} and v_{cd} is D_φ. Taking the forward operation as an example, in Fig. 2, it could be found that the operation includes two cases: Case A and Case B. To simplify the analysis, some assumptions are given as follows.

1) The switches S_1–S_7 are ideal with antiparallel diodes and junction capacitances.
2) The transformer turns ratio is 1:1:n.
3) The voltage of C_a remains constant.
4) The leakage inductance is $L_{k1} = L_{k2} = L_k$.

The forward and backward operation can be divided into two cases according to the shift ratio between v_{ab} and v_{cd}, as shown

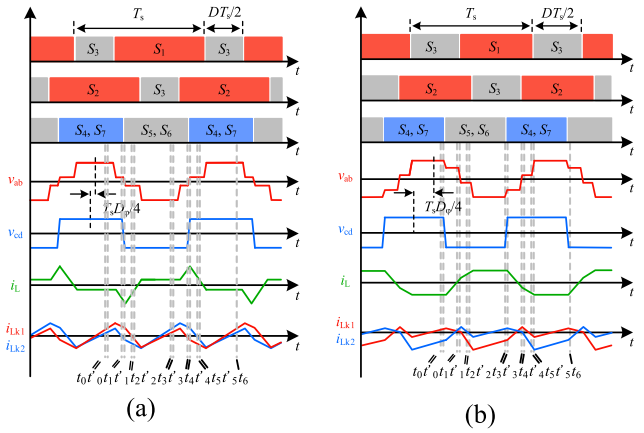

Fig. 3. Key steady-state operation waveforms (backward transmission). (a) Case A ($D-1<D_\varphi<0$). (b) Case B ($-1<D_\varphi<D-1$).

in Figs. 2 and 3. Since the analysis method of Case B is similar to Case A, this article mainly takes Case A as an example to analyze the forward and backward modes of the whole cycle.

A. Forward Operation Principle of Case A

When the converter works in Case A under the forward transmission, the working state includes 12 intervals during a full-switching cycle. The corresponding equivalent circuit during each interval is shown in Fig. 4.

Interval 1 [Fig. 4(a), $t_0 \le t < t_0'$]: At t_0, S_3 is turned OFF and can achieve ZVS-off with the presence of parallel capacitance. Primary current i_{Lk2} begins to charge the parallel capacitance of S_3 and discharge the parallel capacitance of S_1 at the same time. Then v_{ds3} rises to $V_{\mathrm{i}}+V_{\mathrm{Ca}}$ and v_{ds1} falls to 0. Hence, the diode of S_1 is naturally turn-ON at t_0', and v_{ds3} is clamped at $V_{\mathrm{i}}+V_{\mathrm{Ca}}$ to suppress the turn-OFF voltage spike.

Interval 2 [Fig. 4(b), $t_0' \le t < t_1$]: At t_0', S_1 is turned ON, and it can achieve ZVS-on with the current flowing through its antiparallel diode. Assuming that the secondary voltage of the transformer is nv_1, then, v_L, v_{Lk1}, and v_{Lk2} are equal to nv_1-V_{o}, v_1-V_{Ca}, and $-(V_{\mathrm{Ca}}+v_1)$, respectively. In this interval, i_L, i_{Lk1}, and i_{Lk2} change linearly, and the slopes are as

$$\begin{cases} di_L/dt = (nv_1 - V_{\mathrm{o}})/L \\ di_{\mathrm{Lk1}}/dt = (v_1 - V_{\mathrm{Ca}})/L_k \\ di_{\mathrm{Lk2}}/dt = -(V_{\mathrm{Ca}} + v_1)/L_k \end{cases}. \tag{1}$$

Interval 3 [Fig. 4(c), $t_1 \le t < t_1'$]: At t_1, S_4 and S_7 are turned OFF, and both of them can achieve ZVS-off with the presence of parallel capacitance. Secondary current i_{L} starts to charge the parallel capacitors of S_4 and S_7 and discharge the parallel capacitors of S_5 and S_6 at the same time. Then, v_{ds4} and v_{ds7} rise to V_{o} when v_{ds5} and v_{ds6} fall to 0. Hence, the diodes of S_5 and S_6 are naturally turn-ON at t_1'.

Interval 4 [Fig. 4(d), $t_1' \le t < t_2$]: At t_1', S_5 and S_6 are turned ON, and both of them can achieve ZVS-on with the current flowing through their antiparallel diodes. Assuming that the secondary voltage of the transformer is nv_2, then, v_{L}, v_{Lk1}, and v_{Lk2} can be expressed as nv_2+V_{o}, v_1-V_{Ca}, and $-(V_{\mathrm{Ca}}+v_2)$, respectively. In this interval, i_L, i_{Lk1}, and i_{Lk2} change linearly, and the slopes are as

$$\begin{cases} di_{\mathrm{L}}/dt = (nv_2 + V_{\mathrm{o}})/L \\ di_{\mathrm{Lk1}}/dt = (v_2 - V_{\mathrm{Ca}})/L_k \\ di_{\mathrm{Lk2}}/dt = -(V_{\mathrm{Ca}} + v_2)/L_k \end{cases}. \tag{2}$$

Interval 5 [Fig. 4(e), $t_2 \le t < t_2'$]: At t_2, S_2 is turned OFF, and it can achieve ZVS-off with the presence of parallel capacitance. Primary current i_{Lk1} begins to charge the parallel capacitance of S_2 and discharge the parallel capacitance of S_3 at the same time. Then, v_{ds2} rises to V_i+V_{Ca}, and v_{ds3} falls to 0. Hence, the diode of S_3 is naturally turn-ON at t_0', and v_{ds2} is clamped at V_i+V_{Ca} to suppress the turn-OFF voltage spike.

Interval 6 [Fig. 4(f), $t_2' \le t < t_3$]: At t_2', S_3 is turned ON, and it can achieve ZVS-on with the current flowing through its antiparallel diode. Assuming that the secondary voltage of the transformer is nv_3, then v_L, v_{Lk1} and v_{Lk2} are nv_3+V_{o}, $-(V_i+v_3)$ and $-(V_{\mathrm{Ca}}+v_3)$, respectively. In this interval, i_L, i_{Lk1}, and i_{Lk2} change linearly, and the slopes are as

$$\begin{cases} di_{\mathrm{L}}/dt = (nv_3 + V_{\mathrm{o}})/L \\ di_{\mathrm{Lk1}}/dt = (V_i + v_3)/L_k \\ di_{\mathrm{Lk2}}/dt = -(V_{\mathrm{Ca}} + v_3)/L_k \end{cases}. \tag{3}$$

Interval 7 [Fig. 4(g), $t_3 \le t < t_3'$]: At t_3, S_3 is turned OFF. Its operating mode is similar to Interval 1. Its working principle and operating mode are similar to Interval 1.

Interval 8 [Fig. 4(h), $t_3' \le \mathrm{t} < t_4$]: At t_3', S_2 is turned ON. Its operating mode is similar to Interval 2. So, the slopes of key currents can be expressed as

$$\begin{cases} di_{\mathrm{L}}/dt = (nv_1 + V_{\mathrm{o}})/L \\ di_{\mathrm{Lk1}}/dt = (v_1 - V_{\mathrm{Ca}})/L_K \\ di_{\mathrm{Lk2}}/dt = -(V_{\mathrm{Ca}} + v_1)/L_K \end{cases}. \tag{4}$$

Interval 9 [Fig. 4(i), $t_4 \le t < t_4'$]: At t_4, S_5 and S_6 are turned OFF. Its working principle and operating mode during this interval are similar to Interval 3.

Interval 10 [Fig. 4(j), $t_4' \le t < t_5$]: At t_4', S_4 and S_7 are turned ON. Its operating mode is similar to Interval 4. So, the currents' slopes are as

$$\begin{cases} di_L/dt = (nv_2 - V_{\mathrm{o}})/L \\ di_{\mathrm{Lk1}}/dt = (v_2 - V_{\mathrm{Ca}})/L_K \\ di_{\mathrm{Lk2}}/dt = -(V_{\mathrm{Ca}} + v_2)/L_K \end{cases}. \tag{5}$$

Interval 11 [Fig. 4(k), $t_5 \le t < t_5'$]: At t_5, S_1 is turned OFF. The working principle and operating mode are similar to Interval 5.

Interval 12 [Fig. 4(l), $t_5' \le t < t_6$]: At t_5', S_3 is turned ON. Its operating mode is similar to Interval 6 and the currents' slopes are as

$$\begin{cases} di_L/dt = (nv_1 - V_{\mathrm{in}})/L \\ di_{\mathrm{Lk1}}/dt = (v_1 - V_{\mathrm{Ca}})/L_K \\ di_{\mathrm{Lk2}}/dt = -(V_{\mathrm{Ca}} - v_1)/L_K \end{cases}. \tag{6}$$

B. Backward Operation Principle of Case A

When the converter operates at Case A under the backward transmission, there are 12 intervals during a full-switching cycle, which is shown in Fig. 5 by using the equivalent circuits.

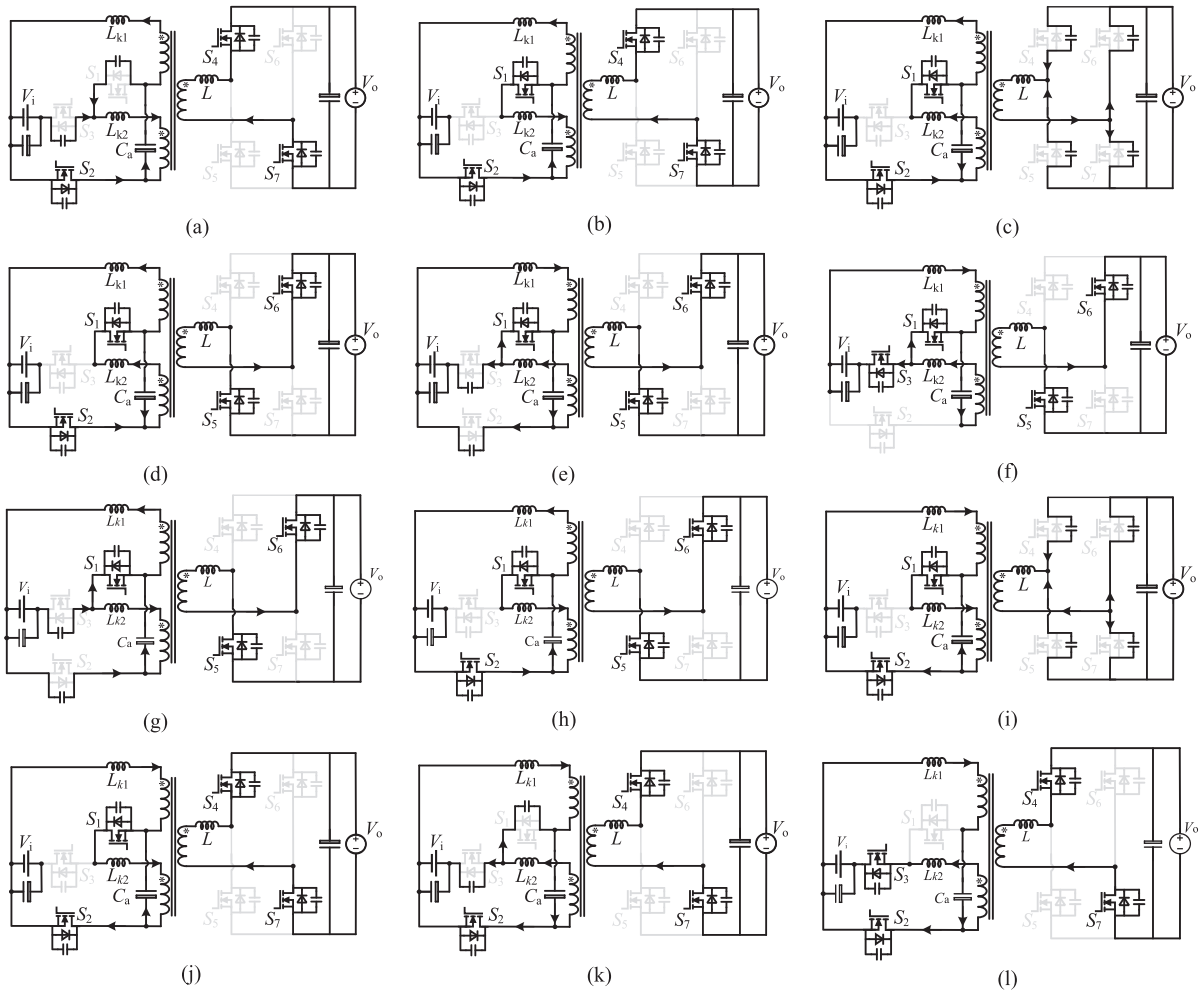

Fig. 4. Forward operation equivalent circuit of each interval in Case A.

Interval 1 [Fig. 5(a), $t_0 \le t < t_0'$]: At t_0, S_3 is turned OFF and it can achieve ZVS-off with the presence of parallel capacitance. Primary current i_{Lk2} begins to charge the parallel capacitance of S_3 and discharge the parallel capacitance of S_1 at the same time. Then, V_{ds3} rises to $V_o + V_{\mathrm{Ca}}$ and V_{ds1} falls to 0. Hence, the diode of S_1 is naturally turned-ON at t_0', and V_{ds3} is clamped at $V_o + V_{\mathrm{Ca}}$ to suppress the turn-OFF voltage spike.

Interval 2 [Fig. 5(b), $t_0' \le t < t_1$]: At t_0', S_1 is turned ON, and it can achieve ZVS-on with the current flowing through its antiparallel diode. Assuming that the secondary voltage of the transformer is nv_1, then, V_L, V_{Lk1}, and V_{Lk2} are equal to nv_1-V_{in}, v_1-V_{Ca}, and -($V_{\mathrm{Ca}} + v_1$), respectively. In this interval, i_L, i_{Lk1}, and i_{Lk2} change linearly, and the slopes are as

$$\begin{cases} di_L/dt = (nv_1 - V_{\mathrm{in}})/L \\ di_{\mathrm{Lk1}}/dt = (v_1 - V_{\mathrm{Ca}})/L_K \\ di_{\mathrm{Lk2}}/dt = -(V_{\mathrm{Ca}} + v_1)/L_K \end{cases}. \tag{7}$$

Interval 3 [Fig. 5(c), $t_1 \le t < t_1'$]: At t_1, S_4 and S_7 are turned OFF, and both of them can achieve ZVS-off with the presence of parallel capacitance. Secondary current i_L starts to charge the parallel capacitors of S_4 and S_7 and discharge the parallel capacitors of S_5 and S_6 at the same time. Then, V_{ds4} and V_{ds7} rise to V_{in} when V_{ds5} and V_{ds6} fall to 0. Hence, the diodes of S_5 and S_6 are naturally turn-ON at t_1'.

Interval 4 [Fig. 5(d), $t_1' \le t < t_2$]: At t_1', S_5 and S_6 are turned ON, and both of them can achieve ZVS-on with the current flowing through their antiparallel diodes. Assuming that the secondary voltage of the transformer is nv_2, then, V_L, V_{Lk1}, and V_{Lk2} can be expressed as $nv_2 + V_{\mathrm{in}}$, v_2-V_{Ca}, and -($V_{\mathrm{Ca}} + v_2$), respectively. In this interval, i_L, i_{Lk1}, and i_{Lk2} change linearly, and the slopes are as

$$\begin{cases} di_{\mathrm{L}}/dt = (nv_2 + V_{\mathrm{in}})/L \\ di_{\mathrm{LK1}}/dt = (v_2 - V_{\mathrm{Ca}})/L_{\mathrm{K}} \\ di_{\mathrm{LK2}}/dt = -(V_{\mathrm{Ca}} + v_2)/L_{\mathrm{K}} \end{cases} \tag{8}$$

Interval 5 [Fig. 5(e), $t_2 \le t < t_2'$]: At t_2, S_2 is turned OFF, and it can achieve ZVS-off with the presence of parallel capacitance. Primary current i_{Lk1} begins to charge the parallel capacitance of S_2 and discharge the parallel capacitance of S_3 at the same time. Then, V_{ds2} rises to $V_o + V_{\mathrm{Ca}}$, and V_{ds3} falls to 0. Hence, the diode of S_3 is naturally turn-ON at t_2', and V_{ds2} is clamped at $V_o + V_{\mathrm{Ca}}$ to suppress the turn-OFF voltage spike.

Interval 6 [Fig. 5(f), $t_2' \le t < t_3$]: At t_2', S_3 is turned ON, and it can achieve ZVS-on with the current flowing through its

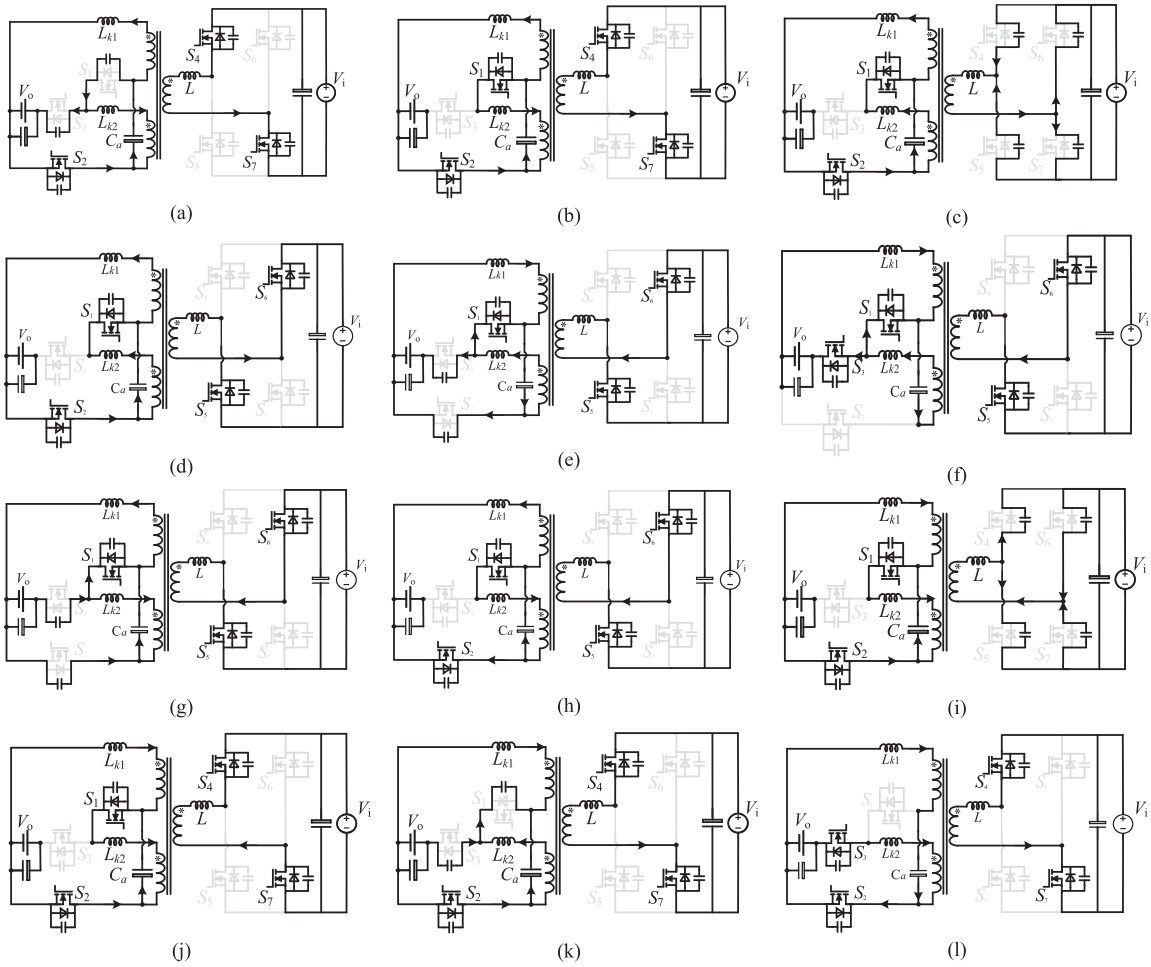

Fig. 5. Backward operation equivalent circuit of each interval in Case A.

antiparallel diode. Assuming that the secondary voltage of the transformer is nv_3, then V_L, V_{Lk1}, and V_{Lk2} are $nv_3 + V_{\mathrm{in}}$, $V_{\mathrm{o}} + v_3$, and -($V_{\mathrm{Ca}} + v_3$), respectively. In this interval, i_L, i_{Lk1}, and i_{Lk2} change linearly, and the slopes are as

$$\begin{cases} di_{\mathrm{L}}/dt = (nv_3 + V_{\mathrm{in}})/L \\ di_{\mathrm{LK1}}/dt = (v_{\mathrm{o}} + V_3)/L_{\mathrm{K}} \\ di_{\mathrm{LK2}}/dt = -(V_{\mathrm{Ca}} + v_3)/L_{\mathrm{K}} \end{cases} \tag{9}$$

Interval 7 [Fig. 5(g), $t_3 \le t < t_3'$]: At t_3, S_3 is turned OFF. The working principle and operating mode are similar to Interval 1.

Interval 8 [Fig. 5(h), $t_3' \le t < t_4$]: At t_3', S_2 is turned ON. Its operating mode is similar to Interval 2. So, the slopes can be derived as

$$\begin{cases} di_{\mathrm{L}}/dt = (nv_1 + V_{\mathrm{in}})/L \\ di_{\mathrm{Lk1}}/dt = (v_1 - V_{\mathrm{Ca}})/L_{\mathrm{K}} \\ di_{\mathrm{Lk2}}/dt = -(V_{\mathrm{Ca}} + v_1)/L_{\mathrm{K}} \end{cases}. \tag{10}$$

Interval 9 [Fig. 5(i), $t_4 \le t < t_4'$]: At t_4, S_5 and S_6 are turned OFF. The working principle and operating mode are similar to Interval 3. So the detailed analysis is omitted.

Interval 10 [Fig. 5(j), $t_4' \le t < t_5$]: At t_4', S_4 and S_7 are turned ON. Its operating mode is similar to Interval 4, and the slopes can be expressed as

$$\begin{cases} di_{\mathrm{L}}/dt = (nv_2 - V_{\mathrm{in}})/L \\ di_{\mathrm{Lk1}}/dt = (v_2 - V_{\mathrm{Ca}})/L_K \\ di_{\mathrm{Lk2}}/dt = -(V_{\mathrm{Ca}} + v_2)/L_K \end{cases}. \tag{11}$$

Interval 11 [Fig. 5(k), $t_5 \le t < t_5'$]: At t_5, S_1 is turned OFF. The working principle and operating mode are similar to Interval 5.

Interval 12 [Fig. 5(l), $t_5' \le t < t_6$]: At t_5', S_3 is turned ON. Its operating mode is similar to Interval 4, and the key current slopes can be expressed as

$$\begin{cases} di_{\mathrm{L}}/dt = (nv_3 - V_{\mathrm{in}})/L \\ di_{\mathrm{Lk1}}/dt = (v_3 - V_{\mathrm{Ca}})/L_K \\ di_{\mathrm{Lk2}}/dt = (V_{\mathrm{o}} - v_3)/L_K \end{cases}. \tag{12}$$

III. Analysis of the Proposed Converter

A. Inductor Current

Since intervals 1, 3, and 5 are very short compared with a switching period, they can be ignored in the next analysis. The voltage V_{Ca} can be deduced from the volt–second balance principle of L_{k1} and L_{k2}, and it is

$$V_{\mathrm{Ca}} = DV_i/(2 - D). \tag{13}$$

1) Case A: According to the transformer input and output relationship, the secondary voltage of the transformer can be derived as

$$\begin{cases} v_1 = \frac{nL_kV_o}{n^2L_k+2L}(t_0 \le t < t_1) \\ v_2 = -\frac{nL_kV_o}{n^2L_k+2L}(t_1 \le t < t_2) \\ v_3 = -\frac{LL_k}{n^2L_k+2L}\left[\frac{2V_i}{L_k(2-D)} + \frac{nV_o}{L}\right](t_2 \le t \le t_3) \end{cases}. \quad (14)$$

The expression of inductor current i_L in half a cycle can be obtained as

$$i_L(t) = \begin{cases} i_L(t_0) + \frac{nv_1-V_o}{L}(t-t_0)(t_0 \le t < t_1) \\ i_L(t_1) + \frac{nv_2+V_o}{L}(t-t_1)(t_1 \le t < t_2) \\ i_L(t_2) + \frac{nv_3+V_o}{L}(t-t_2)(t_2 \le t \le t_3) \end{cases} \quad (15)$$

where $t_1 = \frac{1+D_\varphi-D}{4f_s} + t_0$, $t_2 = \frac{1-D_\varphi-D}{4f_s} + t_1$, and $t_3 = \frac{D}{2f_s} + t_2$.

In combination with (14), (15), and the constraint condition$i_L(t_3) = -i_L(t_0)$, the initial current value of each stage of the inductor can be obtained, and they are as

$$\begin{cases} i_L(t_0) = \frac{Dn}{2(n^2L_k+2L)f_s(2-D)}V_i + \frac{D_\varphi-D}{2(n^2L_k+2L)f_s}V_o \\ i_L(t_1) = \frac{Dn}{2(n^2L_k+2L)f_s(2-D)}V_i - \frac{1}{2(n^2L_k+2L)f_s}V_o \\ i_L(t_2) = \frac{Dn}{2(n^2L_k+2L)f_s(2-D)}V_i - \frac{D_\varphi+D}{2(n^2L_k+2L)f_s}V_o \end{cases}. \quad (16)$$

Similarly, the initial current value of every stage of L_{k1} and L_{k2} can be obtained as

$$\begin{cases} i_{Lk1}(t_0) = \frac{(1-D)(n^2L_k+2L)-n^2L_k}{4(n^2L_k+2L)f_sL_k(2-D)}DV_i \\ \quad + \frac{(D-D_\varphi)(2-D)+DD_\varphi}{4(n^2L_k+2L)f_s(2-D)}nV_o \\ i_{Lk1}(t_1) = -\frac{D_\varphi(n^2L_k+2L)+n^2L_k}{4(n^2L_k+2L)f_sL_k(2-D)}DV_i \\ \quad + \frac{2-D(1-D_\varphi)}{4(n^2L_k+2L)f_s(2-D)}nV_o \\ i_{Lk1}(t_2) = -\frac{(1-D)(n^2L_k+2L)+n^2L_k}{4(n^2L_k+2L)f_sL_k(2-D)}DV_i \\ \quad + \frac{2(D+D_\varphi)-D^2}{4(n^2L_k+2L)f_s(2-D)}nV_o \\ i_{Lk1}(t_3) = \frac{(1-D)(n^2L_k+2L)+n^2L_k}{4(n^2L_k+2L)f_sL_k(2-D)}DV_i \\ \quad + \frac{2(D_\varphi-D)+D^2}{4(n^2L_k+2L)f_s(2-D)}nV_o \end{cases} \quad (17)$$

$$\begin{cases} i_{Lk2}(t_0) = i_{Lk1}(t_3) \\ i_{Lk2}(t_1) = \frac{n^2L_k-D_\varphi(n^2L_k+2L)}{4(n^2L_k+2L)f_sL_k(2-D)}DV_i \\ \quad + \frac{D(1+D_\varphi)-2}{4(n^2L_k+2L)f_s(2-D)}nV_o \\ i_{Lk2}(t_2) = \frac{n^2L_k-(1-D)(n^2L_k+2L)}{4(n^2L_k+2L)f_sL_k(2-D)}DV_i \\ \quad + \frac{DD_\varphi-(2-D)(D_\varphi+D)}{4(n^2L_k+2L)f_s(2-D)}nV_o \\ i_{Lk2}(t_3) = i_{Lk1}(t_0) \end{cases}. \quad (18)$$

2) Case B: The analytical method in Case B is the same as the one in Case A, thus the results are given directly as follows:

$$\begin{cases} i_L(t_0) = \frac{Dn}{2(n^2L_k+2L)f_s(2-D)}V_i + \frac{D_\varphi-D}{2(n^2L_k+2L)f_s}V_o \\ i_L(t_1) = \frac{Dn}{2(n^2L_k+2L)f_s(2-D)}V_i + \frac{D_\varphi+D-2}{2(n^2L_k+2L)f_s}V_o \\ i_L(t_2) = \frac{(1-D_\varphi)n}{2(n^2L_k+2L)f_s(2-D)}V_i - \frac{1}{2(n^2L_k+2L)f_s}V_o \end{cases} \quad (19)$$

$$\begin{cases} i_{Lk1}(t_0) = \frac{2L-D(n^2L_k+2L)}{4(n^2L_k+2L)f_sL_k(2-D)}DV_i \\ \quad + \frac{(1-D_\varphi-D)(3+D_\varphi-3D)+12D-6D^2-4}{8(n^2L_k+2L)f_s(2-D)}nV_o \\ i_{Lk1}(t_1) = \frac{(D-1)(n^2L_k+2L)-n^2L_k}{4(n^2L_k+2L)f_sL_k(2-D)}DV_i \\ \quad + \frac{2(D-2)(D_\varphi+D-2)+2D-D^2-(D_\varphi-1)^2}{8(n^2L_k+2L)f_s(2-D)}nV_o \\ i_{Lk1}(t_2) = \frac{(D_\varphi-1)\left[(1-D)(n^2L_k+2L)+n^2L_k\right]}{4(n^2L_k+2L)f_sL_k(2-D)}V_i \\ \quad + \frac{4-D^2-(D_\varphi-1)^2}{8(n^2L_k+2L)f_s(2-D)}nV_o \\ i_{Lk1}(t_3) = \frac{(1-D)(n^2L_k+2L)+n^2L_k}{4(n^2L_k+2L)f_sL_k(2-D)}DV_i \\ \quad + \frac{4D_\varphi-2D-2DD_\varphi-(D_\varphi+D-1)(D_\varphi+D-3)}{8(n^2L_k+2L)f_s(2-D)}nV_o \end{cases} \quad (20)$$

$$\begin{cases} i_{Lk2}(t_0) = i_{Lk1}(t_3) \\ i_{Lk2}(t_1) = \frac{n^2L_k-(1-D)(n^2L_k+2L)}{4(n^2L_k+2L)f_sL_k(2-D)}DV_i \\ \quad + \frac{2(2-D)(D_\varphi+D-2)+2D-D^2-(D_\varphi-1)^2}{8(n^2L_k+2L)f_s(2-D)}nV_o \\ i_{Lk2}(t_2) = \frac{(D_\varphi-1)\left[(1-D)(n^2L_k+2L)-n^2L_k\right]}{4(n^2L_k+2L)f_sL_k(2-D)}V_i \\ \quad + \frac{4D-4-D^2-(D_\varphi-1)^2}{8(n^2L_k+2L)f_s(2-D)}nV_o \\ i_{Lk2}(t_3) = i_{Lk1}(t_0) \end{cases} \quad (21)$$

where$t_1 = \frac{1-D}{2f_s} + t_0$, $t_2 = \frac{D_\varphi+D-1}{4f_s} + t_1$ and $t_3 = \frac{1+D-D_\varphi}{4f_s} + t_2$.

B. Transmission Power

Based on Fig. 2(a), the transmission power in Case A can be given by

$$\begin{aligned} P &= 2f_sV_o\left[\int_{t_0}^{t_1} i_L(t)dt - \int_{t_1}^{t_3} i_L(t)dt\right] \\ &= \frac{nV_iV_oDD_\varphi}{2(n^2L_k+2L)f_s(2-D)}. \end{aligned} \quad (22)$$

In Fig. 2(b), the transmission power in Case B can be expressed as

$$\begin{aligned} P &= 2f_sV_o\left[\int_{t_0}^{t_2} i_L(t)dt - \int_{t_2}^{t_3} i_L(t)dt\right] \\ &= \frac{nV_iV_o\left[1-(1-D)^2-(1-D_\varphi)^2\right]}{4(n^2L_k+2L)f_s(2-D)}. \end{aligned} \quad (23)$$

Providing that$P_{base} = \frac{nV_iV_o}{4(n^2L_k+2L)f_s}$, the normalized transmission power of the proposed AC-TPFBC can be written as

$$P^* = \begin{cases} \frac{2DD_\varphi}{2-D}, & \text{Case A} \\ \frac{1-(1-D)^2-(1-D_\varphi)^2}{2-D}, & \text{Case B} \end{cases}. \quad (24)$$

The backward transmission power is calculated in the same way as in the forward direction, and the results are shown as follows:

$$P^* = \begin{cases} \frac{2DD_\phi}{2-D}, & \text{Case A} \\ -\frac{1-(1-D)^2-(1+D_\phi)^2}{2-D}, & \text{Case B} \end{cases}. \quad (25)$$

Fig. 6 shows a 3-D graph of the transmission power, and it can be seen that P^* reaches a minimum value when D or D_φ is 0. The forward maximum power can be reached when D and D_φ are both 1 and the backward transmission power can be

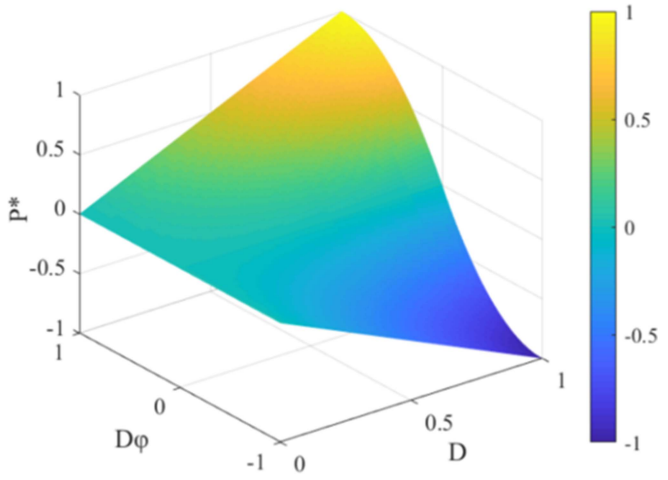

Fig. 6. Three-dimensional graph of the transmission power.

reached when D is 1 and D_φ is -1. It can be seen that the working characteristics of the forward and reverse operations are completely identical to the expression. The power transmission direction can be switched by adjusting the D_φ, thus simplifying the difficulty of the control loop design.

C. ZVS Condition

Assuming that the minimum currents of S_1–S_3 and S_4–S_7 achieving ZVS turn-ON are respectively

$$\begin{cases} I_{Z1} = \dfrac{4V_i C_{\mathrm{oss(S_1:S_3)}}}{(2-D)t_{\mathrm{dead}}} \\ I_{Z2} = \dfrac{2V_o C_{\mathrm{oss(S_4:S_7)}}}{t_{\mathrm{dead}}} \end{cases}. \tag{26}$$

1) Case A. ZVS Conditions for Switch S_1 (S_2): When S_3 is turned OFF, the current i_{Lk2} (i_{Lk1}) charges the junction capacitor of S_3 and discharges the junction capacitor of S_1 (S_2), so $i_{\mathrm{Lk2}}(t_0)$ can be calculated as

$$i_{\mathrm{Lk2}}(t_0) > I_{Z1}. \tag{27}$$

ZVS Conditions for Switch S_3: When S_1 (S_2) is turned OFF, the current i_{Lk2} (i_{Lk1}) charges the junction capacitor of S_1 (S_2) and discharges the junction capacitor of S_3, so $i_{\mathrm{Lk1}}(t_2)$ can be calculated as

$$-i_{\mathrm{Lk1}}(t_2) > I_{Z1}. \tag{28}$$

ZVS Conditions for Switch S_4–S_7: When S_4 and S_7 (S_5 and S_6) are turned OFF, the current i_L charges the junction capacitor of S_4 and S_7 and discharges the junction capacitor of S_5 and S_6, so $i_L(t_1)$ can be calculated as

$$-i_{\mathrm{L}}(t_1) > I_{Z2}. \tag{29}$$

2) Case B: Referring to the analysis in Case A, the conditions for realizing ZVS of power switches in Case B can be obtained as

$$-i_{\mathrm{Lk1}}(t_2) > I_{Z1}. \tag{30}$$

Fig. 7 gives all switches achieving ZVS turn-ON range when the L_{k} is different values. The shaded part indicates that all the power switches cannot be guaranteed to achieve soft switching

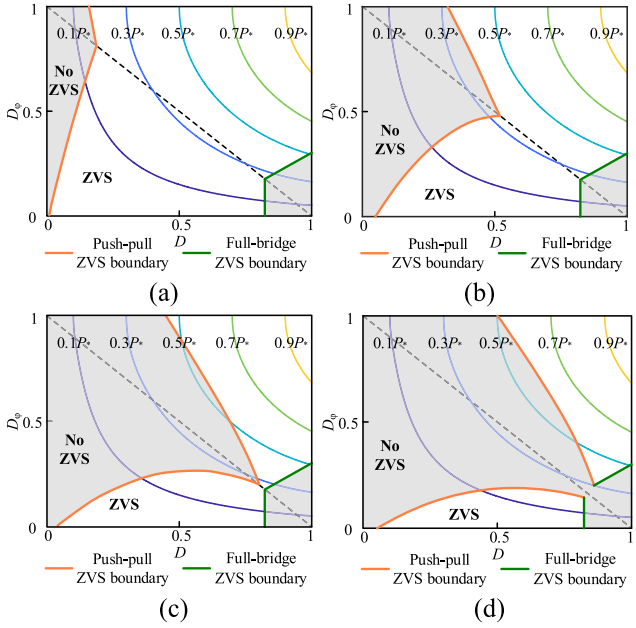

Fig. 7. Soft-switching range of AC-TPFBC at different leakage inductance. (a) $L_k = 1$ μH. (b) $L_k = 2.5$ μH. (c) $L_k = 4$ μH. (d) $L_k = 5$ μH.

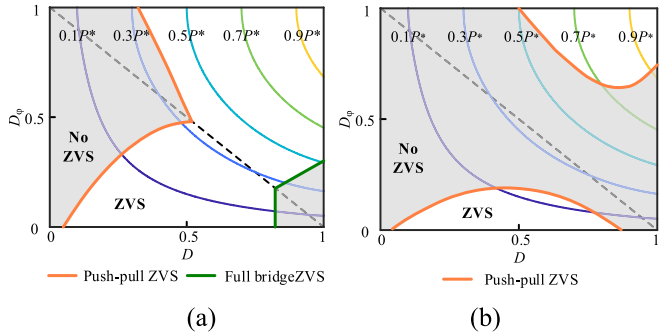

Fig. 8. Soft-switching range of AC-TPFBC at different voltage conversion ratios. (a) $k = 1.2$. (b) $k = 0.8$.

in this area. According to (27)–(30), it can be found that the soft switching range of the full-bridge circuit is only related to the inductance $n^2L_k + 2L$. When the rated power of the converter is given, the inductance value will also be determined, no matter how the inductance L_k changes, the soft switching range will always remain unchanged. For the Push-pull circuit, the soft switching range is closely related to the inductance L_k. With the increase of the inductance L_k value, the soft switching range shows a decreasing trend, and eventually, some power switches cannot realize the result of ZVS turn-ON.

Fig. 7 shows that the smaller the inductor L_k, the larger the soft switching range, but it does not mean that the operating characteristics of the converter are better and the work efficiency is higher. Moreover, with the decrease of inductance L_k, the peak value of inductor current i_{Lk1}, i_{Lk2}, and the RMS value will gradually increase.

Assuming that the voltage conversion ratio is $k = nV_i/V_o$, Fig. 8 shows the range for all switches achieving ZVS turn-ON,

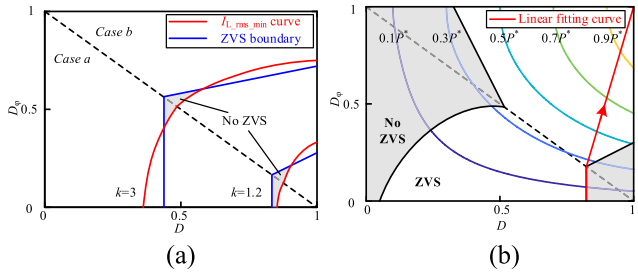

Fig. 9. Design of the control strategy. (a) Optimal trajectory and ZVS boundary. (b) Linear fitting curve.

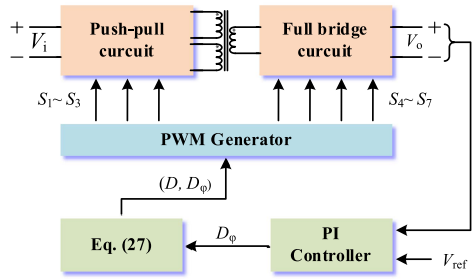

Fig. 10. Control block diagram.

which can be found that the larger k is, the wider the soft-switching range can be realized. In addition, it is noted that the increase of k will make the effective value of the inductance current larger under the same transmission power condition. Therefore, the value of k should not be too large in practice.

D. Control Strategy

Since the inductor current is directly related to the conduction loss and the transformer loss, it affects the operational efficiency of the converter. Therefore, on the premise of ensuring the realization of a wide range of soft switching, this article mainly takes the RMS value of inductor current iL as the objective to optimize the control. Firstly, according to (16) and (19), we can obtain

$$I_{\mathrm{L\_rms}}^2 = \begin{cases} A\left[\frac{k^2(3D^2-2D^3)}{(2-D)^2}+\frac{k(D^3+3DD_\varphi^2-3D)}{2-D}+1\right], & \text{Case A} \\ A\left[\frac{k(1-D_\varphi)^3}{2-D}+3kD\left(D_\varphi-1\right)+\frac{k^2D^2(3-2D)}{(2-D)^2}+1\right], & \text{Case B} \end{cases} \tag{31}$$

where A is the coefficient, and its expression can be obtained as

$$A=\frac{V_o^2}{12(n^2L_k+2L)^2f_s^2}. \tag{32}$$

The Lagrange multiplier method is used to solve the optimal problem, and the established optimization equation for the transmission power and inductance RMS current is

$$\begin{cases} \min \quad I_{\mathrm{L\_rms}}^2(D,D_\varphi) \\ \text{where} \quad P(D,D_\varphi)=0 \end{cases}. \tag{33}$$

Combining (12), (22), (31), and (32), the optimal solution of (33) can be drawn and it is shown in Fig. 9(a), from which we can find the curve is difficult to ensure all power transistors achieve soft switching. Meanwhile, it is hard to solve these functions. Herein, this article proposes a linear fitting scheme based on the RMS value of inductance current optimal control to simplify the analysis, and it is expressed as

$$\begin{cases} D=B, & \text{Case A} \\ D=\frac{(D_\varphi-1)(1-B)}{B}+1, & \text{Case B} \end{cases} \tag{34}$$

where B is a constant, and it is

$$B=\frac{2V_o-4\left(n^2L_k+2L\right)f_sI_{Z2}}{nV_i+V_o-2\left(n^2L_k+2L\right)f_sI_{Z2}}. \tag{35}$$

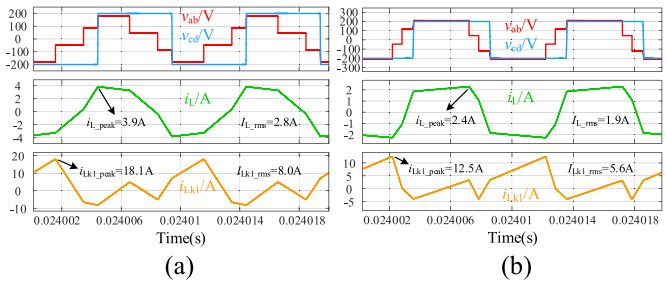

Fig. 11. Comparison of simulation waveforms. (a) Before optimization. (b) After optimization.

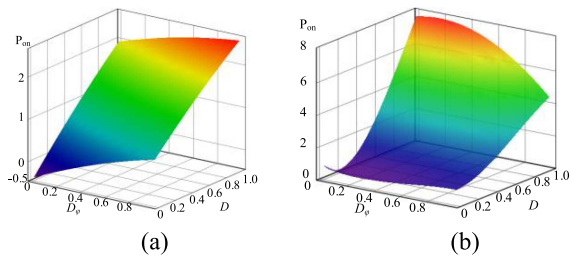

Fig. 12. Conduction loss difference between AC-TPFBC and TPFBC. (a) Case A. (b) Case B.

The complete linear fitting curve is shown in Fig. 9(b) when the k is 1.2, which can figure out the ZVS boundary of the full-bridge circuit in Case A and the linear function in Case B.

Fig. 10 shows closed-loop control of the block diagram of the proposed AC-TPFBC. When the relationship between the two duty cycles (D and D_φ) is obtained, the control variable of the converter is reduced from two degrees of freedom to one. As a result, control complexity is simplified. The shift ratio D_φ is obtained by voltage PI closed loop. Then, the duty ratio D is obtained by optimizing the control unit according to (34).

To verify the effectiveness of the control strategy, the AC-TPFBC simulation model is built in SIMULINK, and Fig. 11 shows the comparison of simulation waveforms under the same transmission power. it can be found that the RMS value and peak value of the inductor current are significantly reduced when the optimization control is adopted, which is conducive to improving the operation efficiency.

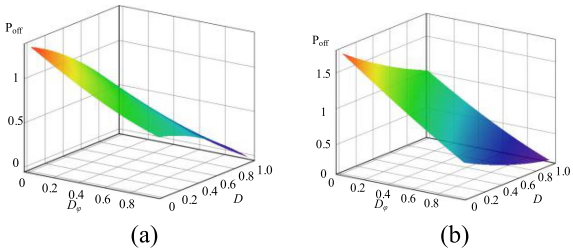

Fig. 13. Switching loss difference between AC-TPFBC and TPFBC. (a) Case A. (b) Case B.

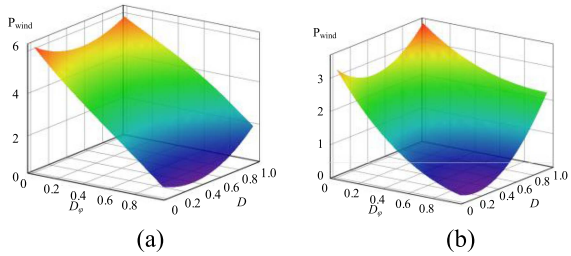

Fig. 14. Transformer loss difference between AC-TPFBC and TPFBC. (a) Case A. (b) Case B.

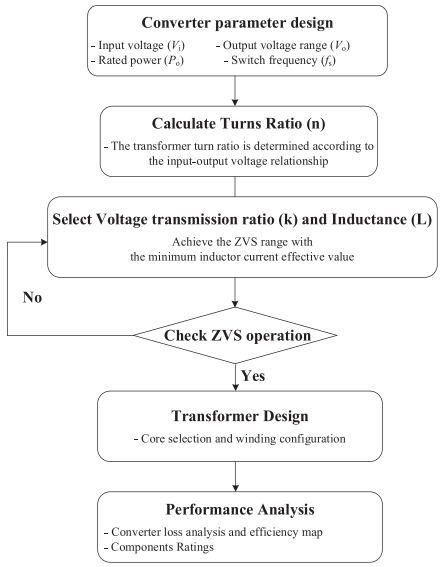

Fig. 15. Design flow chart of the presented converter.

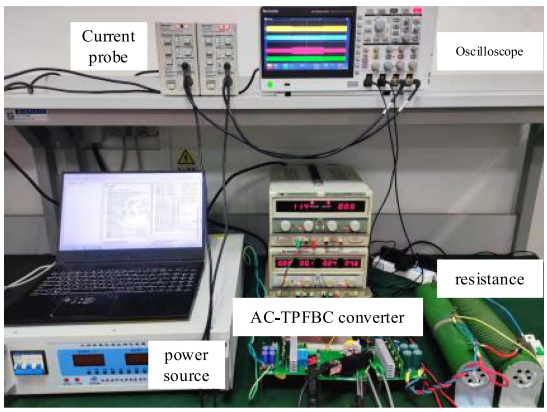

Fig. 16. Photograph of the experimental prototype.

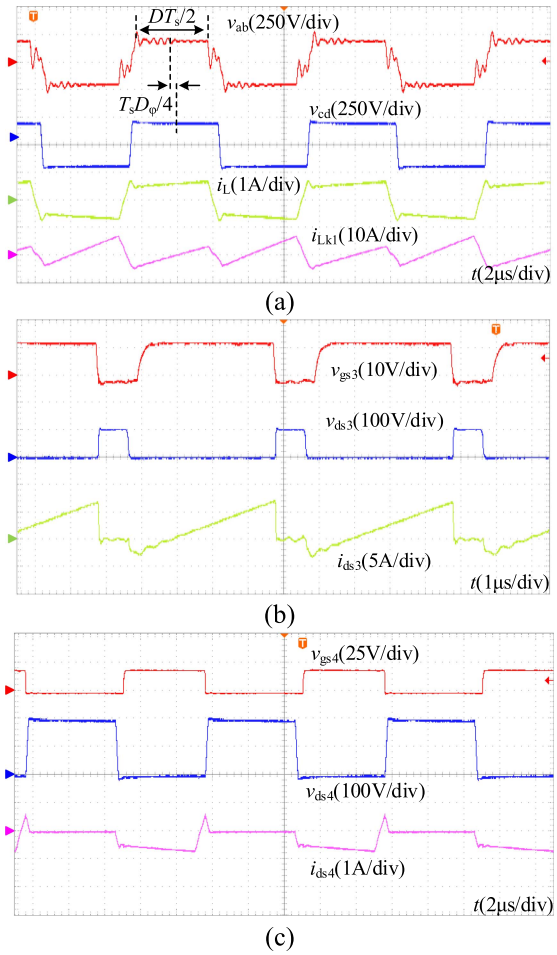

Fig. 17. Experimental waveforms of forward transmission under 20% power. (a) Secondary transformer voltage $v_{\rm ab}$, $v_{\rm cd}$, and inductor current i_L, $i_{\rm Lk1}$. (b) Switch S_3 voltage $v_{\rm gs3}$, $v_{\rm ds3}$, and current $i_{\rm ds3}$. (c) Switch S_4 voltage $v_{\rm gs4}$, $v_{\rm ds4}$, and current $i_{\rm ds4}$.

E. Power Losses Analysis

1) Conduction Loss: The conduction loss is mainly caused by the parasitic resistances of the power switch and antiparallel diode. Assuming that the values are both $R_{\rm on}$, the conduction loss can be obtained as

$$P_{\rm on} = I_{\rm ds}^2 R_{\rm on} \tag{36}$$

where I_{ds} represents the RMS value of the power switch conduction current. For S_1 and S_2, the value is equal to

$$I_{\rm ds1}^2 = \begin{cases} \frac{1}{T_{\rm s}}\left[\int_{t_0}^{t_2} i_{\rm Lk1}^2(t) + i_{\rm Lk2}^2(t)\,dt + n^2\int_{t_2}^{t_3} i_{\rm L}^2(t)\right], & \text{Case A} \\ \frac{1}{T_{\rm s}}\left[\int_{t_0}^{t_1} i_{\rm Lk1}^2(t) + i_{\rm Lk2}^2(t)\,dt + n^2\int_{t_1}^{t_3} i_{\rm L}^2(t)\right], & \text{Case B} \end{cases}. \tag{37}$$

For S_3, the value is equal to

$$I_{\rm ds2}^2 = \begin{cases} \frac{2}{T_{\rm s}}\left(\int_{t_2}^{t_3} i_{\rm Lk1}^2(t)\,dt\right), & \text{Case A} \\ \frac{2}{T_{\rm s}}\left(\int_{t_1}^{t_3} i_{\rm Lk1}^2(t)\,dt\right), & \text{Case B} \end{cases}. \tag{38}$$

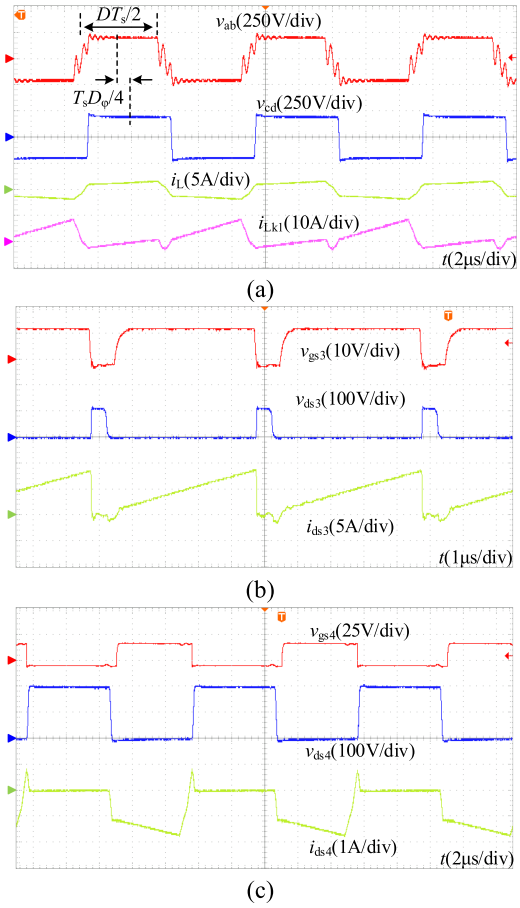

Fig. 18. Experimental waveforms of forward transmission under 50% power. (a) Secondary transformer voltage v_{ab}, v_{cd}, and inductor current i_L, i_{Lk1}. (b) Switch S_3 voltage v_{gs3}, v_{ds3}, and current i_{ds3}. (c) Switch S_4 voltage v_{gs4}, v_{ds4}, and current i_{ds4}.

For S_4–S_7, the value is equal to

$$I_{ds3}^2 = \frac{I_{L\_rms}}{\sqrt{2}} = \frac{1}{T_s}\int_{t_0}^{t_3} i_L^2(t)dt. \tag{39}$$

Then, all expressions can be obtained as

$$I_{ds1}^2 = \begin{cases} A\left[\dfrac{\left(D^3+12DD_\phi^2\right)n^2}{24(D-2)^2} + \dfrac{(D_\phi-D+1)^3(D^2M^2+D^2Mn^2+n^4)}{24(D-2)^2n^2}\right], & \text{Case A} \\ A\left[\dfrac{(24D-2D_\phi+13)(D-D_\phi+1)}{24(D-2)^2} + \dfrac{(D-3)^3(21D-6DD_\phi-21D^2+3D_\phi^2+3D_\phi-7)}{48(D-2)^2n^2}\right], & \text{Case B} \end{cases} \tag{40}$$

$$I_{ds2}^2 = \begin{cases} A\left[\dfrac{12D^2n^4+3M^2D}{3(D-2)^2n^2} + \dfrac{D^2M(10DM-12Dn^2-9M+12n^2)}{24(D-2)^2n^2}\right], & \text{Case A} \\ A\left[\dfrac{(M-DM)^2\left[(D+D_\phi-1)^3+8(D-D_\phi+1)^2\right]}{24(D-2)^2n^2}\right], & \text{Case B} \end{cases} \tag{41}$$

2) Switching Loss: Since the power switch realizes ZVS-on with a wide load range, the turn-ON loss can be ignored. and the turn-OFF loss can be calculated as

$$P_{off} = \begin{cases} \dfrac{V_0^2t_{off}^2(-2D^3n^2+D^2n^2+4D^2)}{48C_{oss}f_s(D-2)^2(L_kn^2+2L)^2} + \dfrac{V_0^2t_{off}^2(-4DD_\phi^2n^2-8D+4D_\phi^2n^2+4)}{48C_{oss}f_s(D-2)^2(L_kn^2+2L)^2}, & \text{Case A} \\ \dfrac{V_0^2t_{off}^2(-6D^3-4D^2D_\phi+17D^2-4DD_\phi^2)}{48C_{oss}f_s(D-2)^2(L_kn^2+2L)^2} + \dfrac{V_0^2t_{off}^2(12DD_\phi-20D+4D_\phi^2-8D_\phi^2+4)}{48C_{oss}f_s(D-2)^2(L_kn^2+2L)^2}, & \text{Case B} \end{cases} \tag{42}$$

where V_o is the output voltage, t_{off} is the turn-OFF time of the power switch, and C_{oss} is junction capacitance.

3) Transformer Loss: Transformer loss mainly includes winding loss and core loss. Among them, the winding loss can be obtained by

$$P_{wind} = I_{L\_rms}^2R_{sec} + 2I_{Lk\_rms}^2R_{pri} \tag{43}$$

where R_{sec} and R_{pri} refer to the equivalent resistance of the primary and secondary windings of the transformer. $I_{Lk_rms}^2$can be obtained from

$$I_{Lk\_rms}^2 = \begin{cases} AD\left[\dfrac{-36D^3M+24D^2M+12DMD_\phi-12D^2D_\phiM}{12(D-2)^2} + \dfrac{n^2(-12D^3+12D^2+12DD_\phi+3D_\phi-6D^2D_\phi)}{12(D-2)^2} + \dfrac{13D^2M^2-26D^3M^2}{12(D-2)^2n^2}\right], & \text{Case A} \\ A\left[\dfrac{(D+D_\phi-1)^3(M+2n^2-DM)}{24(D-2)^2n^2} - \dfrac{8(D-1)^3(DM-n^2)^2}{24(D-2)^2n^2}\right], & \text{Case B} \end{cases} \tag{44}$$

4) Power Loss Comparison: According to the TPFBC loss analysis in [14], combined with expressions (36)–(44), the power loss of the AC-TPFBC can be subtracted from the power loss of the TPFBC, and the results can be drawn as follows.

Figs. 12–14 show the key loss comparison results under different operating conditions. As seen, the conduction loss of the presented AC-TPFBC is slightly greater than that of TPFBC at a light load. Because, although all switches are working at a soft switching state, a somewhat larger circulation current would be generated when S_1 and S_2 are turned ON simultaneously, and the loss caused by the circulation current is the dominant part of this situation. However, as the load becomes heavier, the reflow power becomes small, and the conduction loss is lower than TPFBC. Moreover, the other losses of the presented converter, like switching loss and transformer loss, are lower than that of TPFBC, so the efficiency of AC-TPFBC would be higher than that of TPFBC.

F. Step-by-Step Design of the Proposed Converter

The equations presented in Section III are used to design the proposed converter, and the key design flow chart is shown in Fig. 15. Specifications needed to begin the design are input voltage V_i, output voltage V_o, rated power P_o, and switching frequency f_s. The main design procedure is illustrated below.

1) The transformer turns ratio n needs to comply with the full range of voltage conversion. Therefore, it is necessary to determine the maximum input voltage V_{imax} and the minimum output voltage V_{omin}.

TABLE I
COMPARISON OF THREE CONVERTER

Comparison of the primary side	The DAB in [1]	The TPFBC in [14]	The PPFHB in [28]	The proposed converter
Total components	Four power switches S_1–S_4	Three power switches S_1–S_3	Two power switches S_1–S_2	Three power switches S_1–S_3
Voltage stress	S_1–S_4: V_i	S_1 and S_2: $2V_i$ S_3: V_i	S_1 and S_2: $2V_i$	S_1–S_3: $2V_i/(2\text{-}D)$
Voltage clamping	Yes	No	Yes	Yes
Modulation strategy	PWM or phase shift	PWM + phase shift	Phase shift	PWM + phase shift
Switching characteristics	Soft switching range is limited	Soft switching range is limited	Soft switching range is limited	Soft switching over a wide load range
Switching losses	High	Relatively low	Relatively low	Low
Maximum number of levels of transformer winding voltage	3	3	2	6
VA rating	High	High	Low	Relatively low

TABLE II
PARAMETERS OF PROTOTYPE

parameter	value
Input voltage V_i	60 V
Output voltage V_o	200 V
Rated power P	500 W
Switching frequency f_s (S_1)	100 kHz
Transformer turn ratio	1:1:4
Clamping capacitor C_a	20 μF
Inductor L_k, L	4 μH, 68 μH
Primary switches: S_1–S_3	IXFH56N30X3
Secondary switches: S_4–S_7	UF3C065080K3S

2) The term $n^2L_k + 2L$ is determined by the maximum transmission power P_{base}. When the $n^2L_k + 2L$ is designed, the larger the inductor L_k, the smaller the effective current of the primary inductor. But the soft switching range also decreases, thus the L_k is increased as much as possible under the premise of ensuring that the converter realizes the soft switching over a wide load range. Since the converter operates in the minimum soft-switching range at $D_\varphi = 1 - D$, the maximum value of L_k can be determined by this condition.
3) Once the transformer turn ratio n and leakage inductance L_k parameters are determined, the planar transformer can be selected with the PCB windings to make sure that these two parameters are accurate in practical application.
4) Verify the soft switching and loss analysis of the converter according to the design parameters.

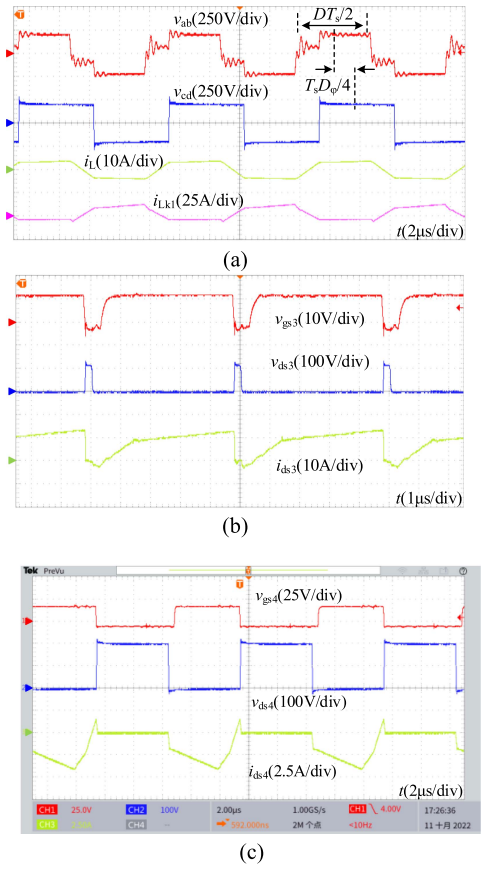

Fig. 19. Experimental waveforms of forward transmission underrated power. (a) Secondary transformer voltage v_{ab}, v_{cd}, and inductor current i_L, i_{Lk1}. (b) Switch S_3 voltage v_{gs3}, v_{ds3}, and current i_{ds3}. (c) Switch S_4 voltage v_{gs4}, v_{ds4}, and current i_{ds4}.

IV. COMPARISON WITH EXISTING TOPOLOGIES

A similar topologies comparison study is shown in Table I, from which it could be obtained that the proposed AC-TPFBC requires fewer power switches than DAB, but it can achieve the same function as the widely used DAB and has a lower device cost. Besides, the conduction loss is limited, and the driving circuit is simplified, which greatly reduces the cost and increases the efficiency of the circuit. The voltage stress of S_1 or S_2 is lower than that of TPFBC or PPFHB. The proposed AC-TPFBC in this article can achieve soft switching over a wide load range, while the other three similar topologies can only achieve soft switching under partial load conditions.

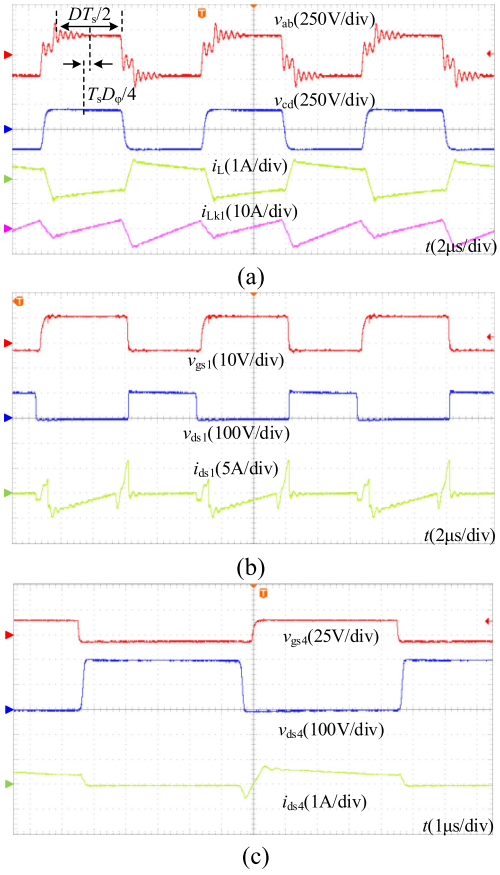

Fig. 20. Experimental waveforms of backward transmission under 20% power. (a) Secondary transformer voltage v_{ab}, v_{cd}, and inductor current i_L, i_{Lk1}. (b) Switch S_3 voltage v_{gs3}, v_{ds3}, and current i_{ds3}. (c) Switch S_4 voltage v_{gs4}, v_{ds4}, and current i_{ds4}.

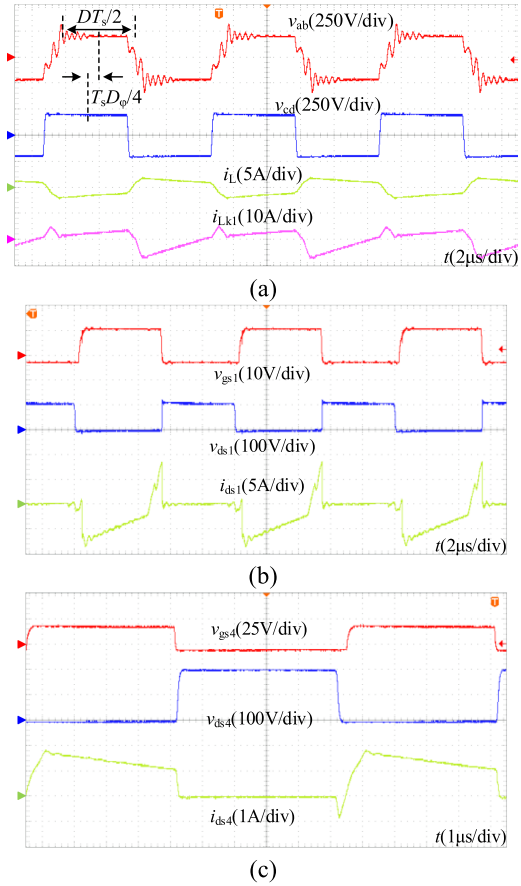

Fig. 21. Experimental waveforms of backward transmission under 50% power. (a) Secondary transformer voltage v_{ab}, v_{cd}, and inductor current i_L, i_{Lk1}. (b) Switch S_3 voltage v_{gs3}, v_{ds3}, and current i_{ds3}. (c) Switch S_4 voltage v_{gs4}, v_{ds4}, and current i_{ds4}.

Moreover, the maximum number of levels of transformer winding voltage in AC-TPFBC is much more than the other topologies, resulting in less harmonic content, reducing the reactive power, and improving the operation efficiency. Overall, the proposed AC-TPFBC can not only ensure the power switch turn-OFF voltage suppression but also have a relatively simple structure with a higher efficiency operation.

V. Experimental Verification

To verify the correctness of the proposed converter, an experimental prototype with 60 V input, 200 V output, and 500 W rated power is built, as shown in Fig. 16, and the key parameters are shown in Table II. In addition, Figs. 17–19 show experimental waveforms at 20% rated power, half-rated power, and rated power under the forward transmission, and Figs. 20–22 show experimental waveforms at 20% rated power, half-rated power, and rated power under backward transmission.

According to part (a) of Figs. 17–22, it can be found that the proposed AC-TPFBC works well under different load conditions and the operating waveforms match well with the theoretical waveforms as shown in Figs. 2 and 3. Moreover, there is a slight oscillation of the transformer secondary voltage v_{ab}, which is mainly caused by leakage inductance resonates with the power switches junction capacitors or parasitic parameters of the loop. It can be solved by optimizing the PCB layout and precise control of leakage inductance. In addition, the relationship between duty ratio D and shift ratio D_φ in the whole power range conforms to (34), to ensure the optimal control of the converter.

Part (b) of Figs. 17–19 shows the soft switch realization of S_3 under forward transmission when the soft switching range of S_1 or S_2 is wider than S_3, and part (b) of Figs. 20–22 show the soft- switching realization of S_1 under backward transmission where the soft switching range of S_3 is wider than S_1 or S_2. Both i_{ds3} and i_{ds1} are negative when switches are turned ON, which represents the currents flowing through the antiparallel body diodes to achieve ZVS-on. Moreover, it can be found that S_1 and S_3 can achieve turn-OFF clamping well under different load conditions from the drain-source voltage waveforms, thus reducing the voltage stress of the power switches.

The soft switching ranges of the switches in the full-bridge circuit are consistent with the analyzed modulation strategy, and part (c) of Figs. 17–22 shows the soft switch realization of S_4 under forward and backward transmission. Similarly, the switch in the full-bridge circuit can still achieve ZVS-on at a light load, and with the power increases, they are easy to achieve soft-switching performance.

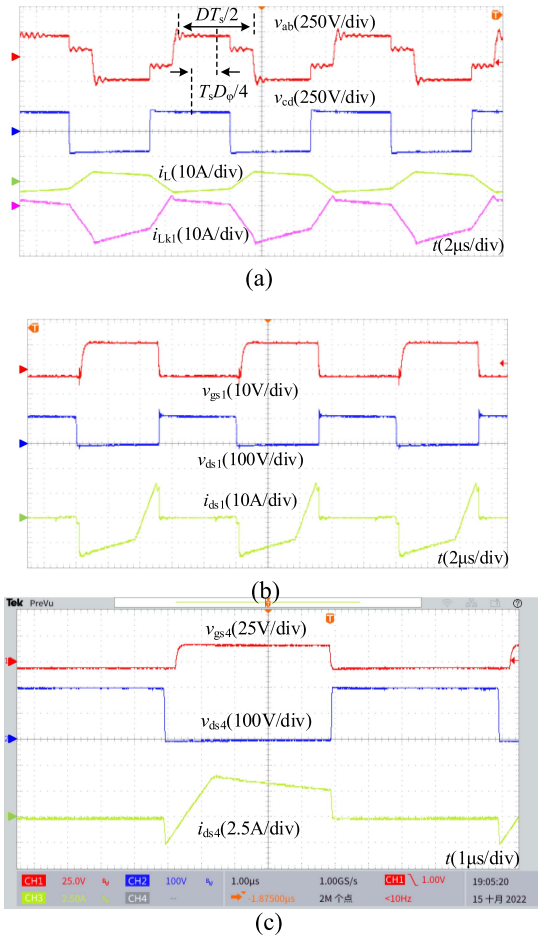

Fig. 22. Experimental waveforms of backward transmission under rated power. (a) Secondary transformer voltage v_{ab}, v_{cd}, and inductor current i_L, i_{Lk1}. (b) Switch S_3 voltage v_{gs3}, v_{ds3}, and current i_{ds3}. (c) Switch S_4 voltage v_{gs4}, v_{ds4}, and current i_{ds4}.

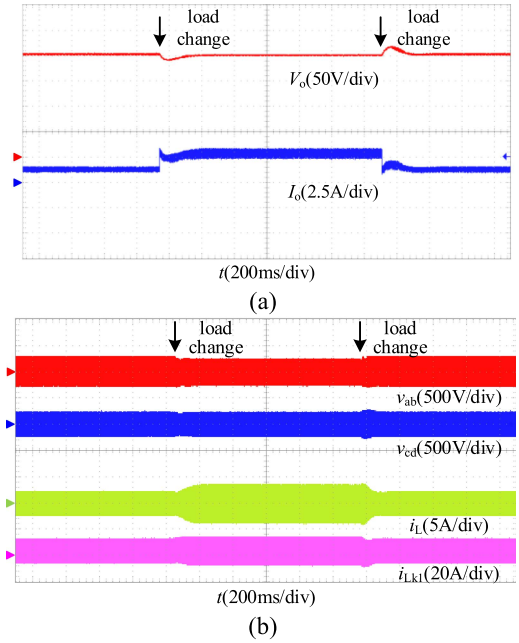

Fig. 23. Dynamic characteristic experimental waveform. (a) Output voltage V_o and current I_o. (b) Secondary transformer voltage v_{ab}, v_{cd}, and inductor current i_L, i_{Lk1}.

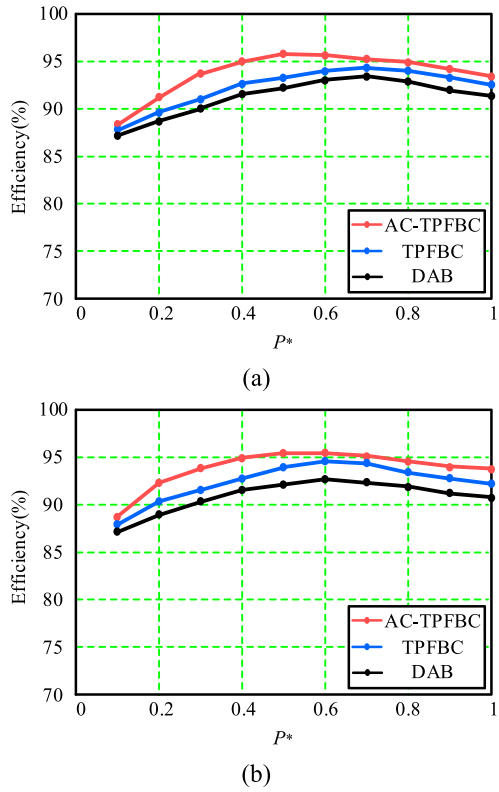

Fig. 24. Efficiency curves of the proposed converter, TPFBC, and DAB. (a) Forward transmission. (b) Backward transmission.

The closed-loop experiment of the proposed converter is carried out to verify the stability of the system. Fig. 23 shows the experimental results when the output current changes from half-rated power to rated power, and then to half-rated power. According to the experimental results, the output voltage amplitude fluctuates 20 V and the adjustment time reaches 180 ms when the load has a step change, which shows that the AC-TPFBC has a good steady-state performance.

Fig. 24 shows the efficiency curves of the proposed AC-TPFBC with a comparison to the TPFBC and DAB. Since the forward and backward characteristics of the converter are symmetrical, the efficiency curves of the two conditions are relatively similar overall. As seen, the peak efficiency value of the AC-TPFBC reaches 95.9%, and the experimental results are similar to the power loss analysis simulation. the overall operational efficiency is higher than that of the TPFBC and DAB since it has a wider soft-switching range and lower voltage stress.

According to the above-mentioned experimental results, the AC-TPFBC proposed in this article can achieve soft switching with a wider load range under the forward and backward transmission, which is more conducive to expanding to high-frequency and high-power density applications than the existing similar DAB or TPFBC converters.

VI. Conclusion

The TPFBC cannot realize soft switching under a light load and the voltage stress is still relatively high. To solve the above-mentioned problems, this article proposes an improved

AC-TPFBC, it only needs to add a clamping capacitor based on the TPFBC, which can realize voltage clamping for all the power switches, ZVS-on over a wide load range, more transformer voltage levels, and higher efficiency. These characteristics have some advantages in improving the reliability and efficiency of converter operation. In this solution, the Lagrange multiplier method is established to solve the optimal operation trajectory of the inductor's current effective value, and the feasibility of the linear fitting scheme is further discussed to reduce the control complexity. Besides, a detailed loss comparison is made with TPFBC, and the design steps of the converter are given. Finally, experimental results successfully verify the correctness and effectiveness of the proposed converter.

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