A Semiquadratic Trans-Inverse High Step-Up DC–DC Converter for Renewable Energy Applications

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***Abstract*—A new high step-up dc–dc converter that is suitable for renewable energy systems is proposed in this article. By integrating a three-winding coupled-inductor (CI), a semiquadratic configuration is established for considerably enhancing voltage gain by the CI turns' ratios, in addition to the converter duty cycle. Furthermore, a passive clamp circuit is integrated to recycle the leakage energy and prevent high spikes across the switch. This topology can be implemented using low-voltage MOSFETs, which reduces losses. Furthermore, zero current switching is achieved for the power switch and input diodes, which substantially reduces the switching losses and reverse recovery problems. Low input current ripple is another benefit that is an essential characteristic for photovoltaic and fuel cell systems to extend their life span and to improve maximum power point tracking characteristics. The proposed topology is analyzed and thoroughly compared with the latest counterparts. To verify the performance of the proposed converter, a 200 W 25–400 V prototype is provided. The voltage stress of the power MOSFET of the sample prototype of the suggested converter is 120 V, which is about 30% of the high output voltage. Moreover, at the full-load condition, the input current ripple is 1.6 A and the measured full-load efficiency is 94.9%.**

***Index Terms*—Renewable energy, step-up dc–dc converter, three-winding coupled-inductor(TWCI), trans-inverse.**

I. Introduction

In THE last decades, due to growing electrical energy demand, sustainable energy sources, such as photovoltaic (PV) panels, fuel cells (FC), wind energy, and batteries have been widely used to decrease fossil fuels. However, due to the low voltage generated by these resources, high step-up dc–dc converters as an interface circuit are required to provide the desired high output dc voltage for local loads [1]. For renewable energy resources, continuous input current with low ripple is essential which spurred much recent research on the current-fed structures of high voltage gain dc–dc circuits [2]. Furthermore, the other key performance indicators of the step-up dc–dc converters for renewable energy sources (RES) applications are high voltage conversion ratio, low voltage across the switching components, soft-switching performance, high efficiency, and low cost. On the other hand, for low-power applications, nonisolated step-up dc–dc structures that often have simple structures are preferred [1]. Also, some other applications of the high voltage gain dc–dc converters are: energy harvesting, uninterruptible power supplies, data centers, medical implantable devices, industrial, lighting technology, medical portable devices, gadgets, and telecommunications [1], [2].

To overcome the limitations of conventional step-up dc–dc converters including low voltage gain, along with very high voltage stresses across the switching components, a variety of high-gain techniques have been introduced. Some effective voltage boosting methods are switched capacitor/inductor, voltage lift, cascade/interleaved and multilevel techniques, and voltage multiplier (VM) cells [1], [3], [4], [5], [6]. However, very high voltage applications require many components, which can limit circuit performance [3], [7]. Accordingly, various recent studies have focused on employing magnetic devices consisting of a coupled-inductor (CI) and transformer (isolated/nonisolated) to provide an elevated gain converter for RES [8], [9]. In CI-based structures, higher voltage gains can be obtained in a wider range through turns' ratio without extreme duty cycles. Nevertheless, in such topologies, the voltage spikes across the active switch caused by the leakage inductance of the CI should be removed with the help of a clamp circuit [10], [11].

Until now, to achieve high voltage gain, many modified nonisolated dc–dc structures based on magnetic devices combined with other boosting methods have been proposed for low-power applications. In [12], [13], [14], and [15], some new ultrahigh step-up CI-based dc–dc topologies with quadratic voltage gain and low voltage stress are introduced. However, the mentioned converters suffer from high input current ripple, which limits their applications for RES. To solve this problem, in [16], [17], [18], and [19], single-switch quadratic step-up dc–dc converters based on two-winding CI-based with low input current ripple are proposed. Nonetheless, in these circuits, to create large voltage conversion ratios, the turns ratio of the CI should be set very high, which leads to producing a large leakage inductance. Besides, in [20], [21], [22], [23], and [24], using a two-winding CI, new

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types of step-up dc–dc topologies are presented. Nevertheless, these structures suffer from low voltage gain ratios. Moreover, two new types of high step-up soft-switched quadratic dc–dc circuits with low input current ripple and soft-switching for the power switch and low reverse recovery issue are introduced in [25] and [26]. However, in these structures, soft-switching performance is obtained using two active switches. Some new quadratic-based ultrahigh step-up dc–dc converters using a three-winding CI (TWCI) with more degrees of freedom with low input current and reduced voltage stress across the switching components are also proposed in [27], [28], [29], and [30]. Nevertheless, the mentioned circuits suffer from the lack of common ground between the input dc source and output load sides.

In recent years, high step-up CI-based dc–dc structures with a trans-inverse feature have been taken into consideration. In these topologies, unlike conventional converters, ultrahigh voltage gain ratios can be created with the help of a low number of CI turns' ratios, which decreases the wire consumption for magnetic devices. In [31], a new high voltage gain dc–dc converter with an ultrahigh voltage gain, low input current ripple, and trans-inverse characteristics has been presented. However, the lack of a clamp circuit is the main disadvantage of this topology. Also, in [32], a new single-switch high voltage gain topology based on quadratic Y-sources techniques is proposed. In this circuit, the power switch operates under hard-switching performance. Moreover, the input diodes of this converter withstand a high level of reverse recovery current during off transition. In [33], a novel double-switch TWCI-based high voltage gain dc–dc converter with the trans-inverse feature is introduced. Nevertheless, this proposed circuit is able to create an ultrahigh voltage gain with the help of two power switches. In addition, a cascaded CI-reverse converter based on TWCI and diode-capacitor technique is proposed in [34]. However, despite the trans-inverse feature in this circuit, the CI turns' ratio should be considered greater than unity. Two new nonisolated step-up quadratic converters with soft-switching operation and low switch voltage stress are presented in [35] and [36]. However, the voltage gain of these structures is limited. Moreover, in [37], an ultrahigh voltage gain quadratic topology based on CI and switched capacitor techniques is suggested. However, the disadvantage of this converter is the use of a large number of elements. In [38], a zero voltage switching (ZVS) high voltage gain converter based on a TWCI-assisted VM cell is proposed. However, two power switches are used in this converter. Some new types of impedance-source-based step-up dc–dc converters with soft-switching performance and trans-inverse features are provided in [39], [40], and [41]. Nevertheless, the voltage gain ratio of these structures has not improved significantly. In [42], an ultrahigh gain quadratic boost converter based on the conventional quadratic boost converter and a TWCI has been proposed. Despite the high voltage gain, this converter suffers from the lack of a common ground between the input source and the output load. Also, in [43] and [44], two new TWCI-based high voltage gain dc–dc converters with low switch stress and continuous input current are suggested. However, the low voltage gains and the lack of common ground have limited the use of these converters. In addition, with the help of a TWCI, two step-up dc–dc topologies with low voltage stress and low input current ripple are presented in [45] and [46]. The use of a large number of components (for [45]) and hard switching performance (for [46]) are demerits of the mentioned structures.

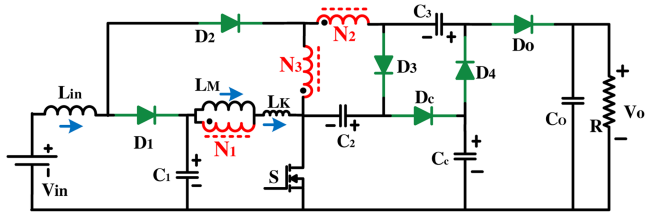


Fig. 1. Circuit schematic of the proposed converter.

According to the above discussions, this article introduces a new type of single-switch quadratic high step-up dc–dc converter based on TWCI with low input current ripple and soft-switching performance. The merits of the introduced converter are listed as follows.

1) Ultrahigh voltage gains under small turns ratios of the TWCI.
2) Three freedom degrees to obtain high voltage gains.
3) Trans-inverse features enable low turn ratios.
4) Using only one active switch.
5) Low input current ripple.
6) Low voltage stress across the switching components.
7) Integration of a regenerative clamp circuit to recycle the leakage inductance energy of CI.
8) Zero current switching (ZCS) is achieved for the power switch.
9) Diodes of the converter operate without a low reverse recovery problem.
10) Common ground between the input dc source and output load.

The rest of this article is organized as follows. Sections II and III describe the operating principles of the suggested topology and mathematical derivations, respectively. The performance of the proposed converter is compared with some similar topologies in Section IV. Furthermore, Section V presents the parameters and design guidelines. Section VI presents the experimental results of a laboratory prototype. Finally, Section VII concludes this article.

II. Proposed Converter and Its Operating Principle

Fig. 1 shows the circuit schematic of the proposed converter which consists of a power MOSFET S, two input diodes D_1 and D_2, a clamp diode D_c, two multiplier diodes D_3 and D_4, an output diode D_o, an energy storage capacitor C_1, two multiplier capacitors C_2 and C_3, a clamp capacitor C_c, an output capacitor C_o, an input filter inductor L_{in}, and a TWCI. L_M and L_K denote the magnetizing inductor and equivalent leakage inductor of the TWCI at the primary side, respectively, N_1, N_2, and N_3 symbolize the number of the turns of the TWCI windings, and $N_{21} = N_2/N_1$ and $N_{31} = N_3/N_1$ are defined as its turns ratios.

To simplify the analysis, the following statements are considered.

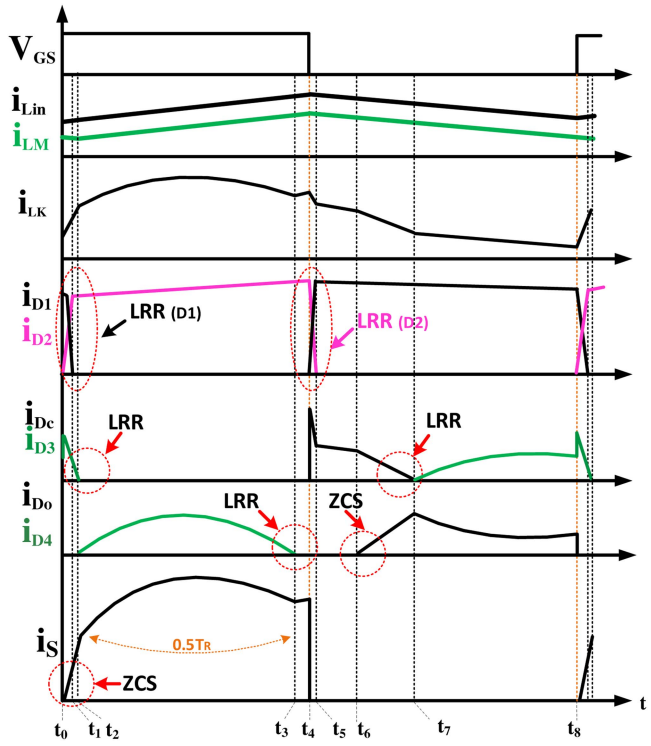


Fig. 2. Key waveforms of the proposed converter.

1) The values of L_M and L_{in} are large enough to guarantee continuous inductor current mode operation.
2) The capacitors are large enough and the associated voltage ripple in each switching cycle could be neglected.
3) The parasitic parameters such as ON-state resistances of the semiconductors, forward voltage drops of the diodes, and equivalent series resistances (ESR) of the capacitors and magnetic devices are only considered in losses analysis.

The key waveforms of the proposed converter are shown in Fig. 2. There are seven modes in a switching cycle and the related equivalent circuits are provided in Fig. 3.

Mode 1 [t_0–t_1]: The equivalent circuit of the proposed converter during this time interval is shown in Fig. 3(a). At the beginning of this mode, the gate pulse rises, and the MOSFET is turned ON. Diode D_o is reversed biased by the voltage of V_o–V_{C2}–V_{C3}. The value of $i_{Do}(t_0)$ is added to $i_{D3}(t_0)$ and $i_s(t_0)$ due to the fact that the passing current through the windings of the CI could not be changed instantaneously. Similarly, the anode of D_2 is connected to the inductive node between the secondary and tertiary windings of TWCI. Therefore, by turning ON the power switch, the passing current through diode D_1 is decreased from I_{in} to zero and the current of D_2 is increased from zero to I_{in} under a slow sleep. Thus, the diode D_1 is operated under an low reverse recovery (LRR) issue that minimizes switching losses. Meanwhile, during this mode, the current of the tertiary side of the TWCI (i_{N3}) is reduced to zero to reverse their direction.

Mode 2 [t_1–t_2]: At the time $t = t_1$, the current of the diode D_1 reaches zero at a slow sleep without a reverse recovery issue. According to Fig. 3(b), the input inductor receives from the input voltage source, therefore, its current increases linearly. During this mode, the diodes D_2 and D_3 remain forward-biased, whereas other diodes are OFF. In this operating mode, the energy of the capacitor C_1 is transferred to the magnetizing inductor of the TWCI. Moreover, the passing current through the secondary side of the TWCI (i_{N2}) tends to reduce to zero and reverse direction at the end of this mode. This time interval is finished when the current of the diode D_3 decreases to zero with LRR.

Mode 3 [t_2–t_3]: The equivalent circuit of the proposed converter during this mode is shown in Fig. 3(c). After reversing the passing current of the secondary side of the TWCI (i_{N2}), the diode D_4 starts to conduct with a slow sleep. V_{C1} and $V_{\text{in}} + N_{31}.V_{C1}$ are applied to L_M and L_{in}, respectively, which increases their current in a linear way and discharges C_1. Through this path, C_c and C_3 are discharged and charged, respectively. Meanwhile, C_o is supplying the output load. A resonant circuit is formed consisting of the leakage inductor and the capacitors C_1, C_3, and C_c. The provided quasi-resonance (QR) operation facilitates the ZCS operation of the diode D_4 during ON and OFF instants. This time interval ends at time t_2 when diode D_4 is turned OFF by crossing its current from zero. The resonant frequency (f_R) based on the *LC* resonant tank is obtained as

$$f_R = \frac{1}{T_R} = \frac{1}{2\pi\sqrt{L_k[C_1 \| (N_{21}+N_{31})^2 (C_3 \| C_C]}} \tag{1}$$

$$i_{D4}(t) = \frac{\pi I_{\text{OUT}}}{2D} \sin\left(\omega_R{}^{II} t\right) \tag{2}$$

$$i_S(t) = i_{LM}(t) + (1 + N_{21} + N_{31})\, i_{D4}(t) + (1 + N_{31})\, I_{\text{IN}}. \tag{3}$$

During this mode, to ensure the proper resonant operation in the circuit, the resonant frequency (1) should be enough higher than the switching frequency. In fact, the resonant operation in the suggested topology can occur in two ways, including below resonance ($T_R/2 < DT_S$) and above resonance ($T_R/2 > DT_S$). However, the best mode to reduce the switching and diode reverse recovery losses along with the minimum switch current stress is the critical mode ($T_R/2 \approx DT_s$).

Mode 4 [t_3–t_4]: The equivalent circuit of the proposed converter during this mode is shown in Fig. 3(d). The passing current through the leakage inductor equals $N_{31}I_{\text{in}} + I_{LM}$. This mode ends at t_3 when the power switch is turned OFF.

Mode 5 [t_4–t_5]: The equivalent circuit of the proposed converter during this time interval is shown in Fig. 3(e). At time t_3, the MOSFET is turned OFF and the clamp diode D_c is turned ON to handle $i_{s(t4)}$. As a result, the energy of the leakage inductor is recycled through the passive clamp circuit and high-voltage spikes are prevented. Similar to the discussions in mode I, D_1 is turned ON with LRR at the beginning of this mode and both of the input diodes are in ON state. This mode ends at t_4 when i_{D1} and i_{D2} reach I_{IN} and zero, respectively.

Mode 6 [t_5–t_6]: The equivalent circuit of this time interval is shown in Fig. 3(f). V_{in} - V_{C1} and $V_{C1} + V_{C2}$ - V_{Cc} are applied to

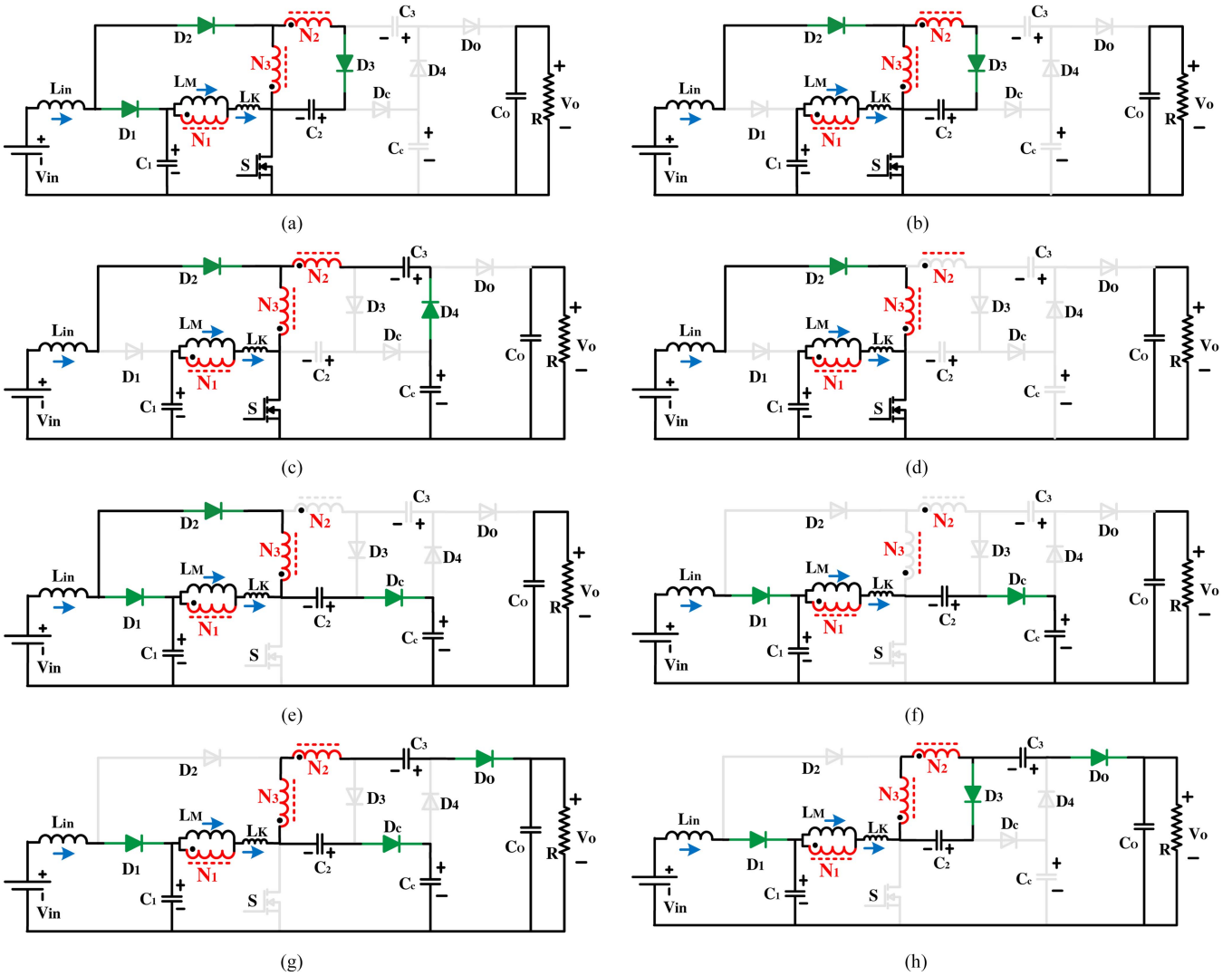


Fig. 3. Equivalent circuits of the proposed converter in different switching modes. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6. (g) Mode 7. (h) Mode 8.

L_{in} and L_M, respectively. L_{in} starts delivering part of its energy to capacitor C_1. As a result of these negative voltages, i_{Lin} and i_{LM} are decreasing during this mode. The passing current through the secondary and tertiary windings of the TWCI is zero. C_c and C_2 are charged and discharged by the current of the magnetizing inductor. The output load is still supplied by C_o. According to the proposed converter structure in operating mode 6, the condition for conducting the output diode is obtained as follows:

$$V_{Cc} - V_{C_2} + V_{C_3} - (n_{21} + n_{31})\,.V_{\text{LM}} > V_{C_o} \tag{4}$$

where

$$V_{\text{LM}} = V_{C_1} + V_{C_2} - V_{Cc}. \tag{5}$$

This mode ends at t_5 when diode D_o starts conducting.

Mode 7 [t_6–t_7]: The equivalent circuit of the proposed converter during this time interval is shown in Fig. 3(g). The secondary and tertiary windings of the TWCI transfer part of the stored energy in the magnetizing inductor to the output load via D_o. By increasing of $i_{Do(t)}$, $i_{Dc(t)}$ is decreased and at time t_6, while $i_{\text{DC}}(t)$ reaches zero, this mode ends.

$$i_{\text{DC}}(t) = i_{\text{LM}}(t) - (N_{21} + N_{31} + 1)i_{Do}(t) = i_{\text{LK}}(t) - i_{Do}(t). \tag{6}$$

Mode 8[t_7–t_8]: The equivalent circuit of the proposed converter during this time interval is shown in Fig. 3(h). At the beginning of this mode, D_3 is turned ON with LRR, and a resonant circuit is formed by L_K, C_1, C_2, and C_3. Part of the stored energy of L_M is charging C_2 via diode D_3 and the windings of the TWCI. Moreover, during this time interval, the output capacitor C_{o} is charged by the energy stored in the magnetizing and leakage inductors of the CI directly and the capacitor C_3 (which received the leakage inductor energy from the capacitor C_{c}). This mode ends at t_8 when the gate pulse of the MOSFET

rises for the next switching cycle.

$$T_R{}^{VII} = \frac{2\pi}{\omega_R{}^{VII}} = \sqrt{L_K\left[\frac{1}{C_{13}} + \left(\frac{1}{N_{21}+N_{31}}+1\right)^2 \times \frac{1}{C_2}\right]^{-1}}. \tag{7}$$

III. Steady-State Analysis

A. Voltage Gain

The durations of modes I, II, III, and IV compared to the period are not significant. Therefore, they are not considered in the derivation for voltage conversion ratio. When the power switch is ON

$$V_{\mathrm{LM}}^{\mathrm{ON}} = V_{C_1} \tag{8}$$

$$V_{\mathrm{LIN}}^{\mathrm{ON}} = V_{\mathrm{IN}} + N_{31}V_{C_1} \tag{9}$$

$$V_{C_3} = V_{C_C} + (N_{21}+N_{31})\,V_{C_1}. \tag{10}$$

When the power switch is OFF

$$V_{\mathrm{LM}}^{\mathrm{OFF}} = V_{C_1} + V_{C_2} - V_{C_C} \tag{11}$$

$$V_{\mathrm{LIN}}^{\mathrm{OFF}} = V_{\mathrm{IN}} - V_{C_1} \tag{12}$$

$$V_{C_2} = -(N_{21}+N_{31})\,(V_{C_1}+V_{C_2}-V_{C_C}) \tag{13}$$

$$V_O = (1+N_{21}+N_{31})\,(V_{C_C}-V_{C_2}) - (N_{21}+N_{31})\,V_{C_1} + V_{C_3}. \tag{14}$$

Using the volt–second balance principle on L_{IN} and L_M, the following equations are given

$$\int_0^{DT_S} V_{\mathrm{LM}}^{\mathrm{ON}}\,dt + \int_{DT}^{T_S} V_{\mathrm{LM}}^{\mathrm{ON}}\,dt = 0 \tag{15}$$

$$\int_0^{DT_S} V_{\mathrm{LIN}}^{\mathrm{ON}}\,dt + \int_{DT}^{T_S} V_{\mathrm{LIN}}^{\mathrm{ON}}\,dt = 0. \tag{16}$$

By substituting (8), (9), (11), and (12) into (15)–(16) and using (10) and (13), the voltages across C_C, C_1, C_2, and C_3 are obtained as

$$V_{C_C} = \frac{1+D\,(N_{21}+N_{31})}{(1-D)\,[1-(1+N_{31})\,D]}V_{\mathrm{IN}} \tag{17}$$

$$V_{C_1} = \frac{1}{1-(1+N_{31})\,D}V_{\mathrm{IN}} \tag{18}$$

$$V_{C_2} = \frac{D\,(N_{21}+N_{31})}{(1-D)\,[1-(1+N_{31})\,D]}V_{\mathrm{IN}} \tag{19}$$

$$V_{C_3} = \frac{1+N_{21}+N_{31}}{(1-D)\,[1-(1+N_{31})\,D]}V_{\mathrm{IN}}. \tag{20}$$

From (14) and (17)–(20), the voltage gain of the proposed converter is obtained as

$$M = \frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = \frac{2+(N_{21}+N_{31})\,(1+D)}{(1-D)\,[1-D\,(1+N_{31})]}. \tag{21}$$

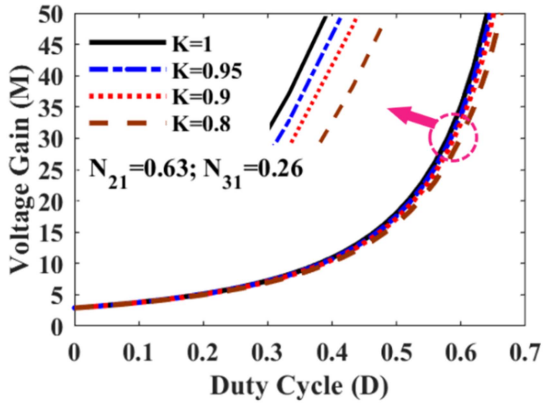


Fig. 4. Voltage gain of the proposed converter versus duty cycle for different values of k.

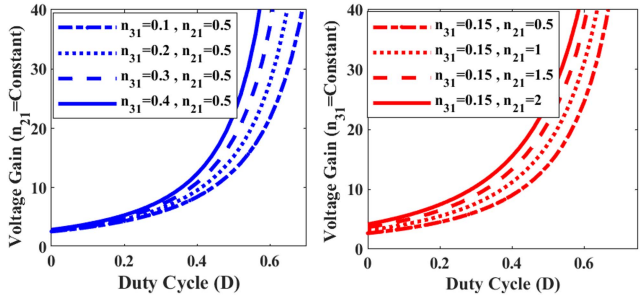


Fig. 5. Ideal DC voltage gain of the suggested topology versus the duty cycle for different turns ratios.

Actually, the leakage inductor of the TWCI affects the voltage gain. By defining the coupling coefficient as $k = L_M/(L_K+L_M)$, the voltage gain of the proposed converter is derived as

$$M = \frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = \frac{2+(N_{21}+N_{31})\,(1+kD)}{(1-D)\,[1-D\,(1+kN_{31})]}. \tag{22}$$

Fig. 4 shows the voltage gain of the proposed converter versus the duty cycle for different values of k. It is shown that the voltage gain of the proposed converter is considerably increased by increasing the duty cycle, whereas the leakage inductor has a negligible effect. Moreover, to have a clearer picture of the influence of the parameters n_{21} and n_{31} on the voltage gain (21) of the suggested topology, several voltage gain curves versus the duty cycle are shown in Fig. 5. From this figure, the voltage conversion ratio of the proposed circuit can be easily adjusted in a wide range with a slight increase of the parameter n_{31}. Therefore, higher output dc voltage can be achieved at fewer turns ratios of the CI.

B. Analysis of Voltage and Current Stresses of the Semiconductors

Through the equivalent circuits in Fig. 3, the blocking voltages across the semiconductors are obtained as

$$V_S = V_{\mathrm{DC}} = V_{C_C} - V_{C_2} = \frac{1}{2+(N_{21}+N_{31})\,(1+D)}V_{\mathrm{OUT}} \tag{23}$$

$$V_{D_1} = (1+N_{31})\,V_{C_1} = \frac{(1+N_{31})\,(1-D)}{2+(N_{21}+N_{31})\,(1+D)}V_{\text{OUT}} \tag{24}$$

$$V_{D_2} = \frac{(1+N_{31})\,D}{1-D}V_{C_1} = \frac{(1+N_{31})\,D}{2+(N_{21}+N_{31})\,(1+D)}V_{\text{OUT}} \tag{25}$$

$$V_{D_3} = (N_{21}+N_{31})\,V_{C_1} + V_{C_2} = \frac{(N_{21}+N_{31})}{2+(N_{21}+N_{31})\,(1+D)}V_{\text{OUT}} \tag{26}$$

$$V_{D_4} = V_{D_O} = V_{\text{OUT}} - V_{C_C} = \frac{(1+N_{21}+N_{31})}{2+(N_{21}+N_{31})\,(1+D)}V_{\text{OUT}}. \tag{27}$$

By the charge balance principle, the average current passing through each of the capacitors is zero. Therefore, the average currents of the MOSFET and diodes are given as

$$I_{S,Ave} = I_{\text{IN}} - I_{\text{OUT}} = (M_{\text{CCM}}-1)\,I_{\text{OUT}} \tag{28}$$

$$I_{D_1,Ave} = (1-D)\,I_{\text{IN}} = (1-D)\,M_{\text{CCM}}I_{\text{OUT}} \tag{29}$$

$$I_{D_2,Ave} = DI_{\text{IN}} = DM_{\text{CCM}}I_{\text{OUT}} \tag{30}$$

$$I_{\text{DC},Ave} = I_{D_3,Ave} = I_{D_4,Ave} = I_{D_O,Ave} = I_{\text{OUT}}. \tag{31}$$

By writing Kirchhoff's current law in node X in Fig. 1 and averaging the equation in a switching cycle, the following equation is obtained:

$$I_{D_1,Ave} = N_{31}I_{D_2,Ave} - (N_{31}+N_{21})\,I_{D_3,Ave} + I_{\text{LM}}. \tag{32}$$

Substituting (29)–(30) into (32) yields I_{LM} as

$$I_{\text{LM}} = \{[1-(1+N_{31})\,D]\,M + N_{21} + N_{31}\}\,I_{\text{OUT}} = \frac{2\,(1+N_{21}+N_{31})}{1-D}I_{\text{OUT}}. \tag{33}$$

The maximum currents of the diodes can be written as

$$I_{D_1,\text{Max}} = I_{D_2,\text{Max}} = i_{\text{LIN,Max}} = M_{\text{CCM}}I_{\text{OUT}} + \frac{D\,(V_{\text{IN}}+N_{31}V_{C_1})}{2L_{\text{IN}}f_S} \tag{34}$$

$$I_{D_3,\text{Max}} = \frac{2\,(1+N_{21}+N_{31})}{(1-D)}I_{\text{OUT}} \tag{35}$$

$$I_{D_4,\text{Max}} = \frac{\pi I_O}{2D} \tag{36}$$

$$I_{D_O,\text{Max}} = i_{Do}(t_7) = \frac{i_{\text{LM}}(t_7)}{1+N_{21}+N_{31}} \cong \frac{I_{\text{LM}}}{1+N_{21}+N_{31}} \tag{37}$$

$$I_{\text{DC,Max}} = i_{\text{DC}}(t_4) = i_S(t_4) = I_{\text{LM}} + \frac{DV_{C_1}}{2L_M f_S} + (1+N_{31})\,I_{D_2,\text{Max}}. \tag{38}$$

The maximum current of the MOSFET is obtained as

$$I_{S,\text{Max}} = I_{\text{LM}} + \frac{DV_{C_1}}{2L_M f_S} + (1+N_{31})\,I_{D_2,\text{Max}} + (1+N_{21}+N_{31})\,I_{D_4,\text{Max}}. \tag{39}$$

TABLE I
MAIN PARASITIC PARAMETERS OF THE CONVERTER COMPONENTS

Parameter	Description
$r_{DS(ON)}$	ON-state resistance of the switch
t_{ON}, t_{OFF}	Rise time and fall time of the switch
ESR_i	Equivalent Series Resistance of the capacitors
$V_{\text{FD}i}$	Forward voltage drop of diode
r_{Lin}, r_{Ni}	Parasitic resistances of the magnetic devices

The RMS values of different components of the proposed converter are, equation (46)–(48) shown at the bottom of the next page.

$$I_{D_1,\text{RMS}} = M_{\text{CCM}}I_{\text{OUT}}\sqrt{1-D} \tag{40}$$

$$I_{D_2,\text{RMS}} = M_{\text{CCM}}I_{\text{OUT}}\sqrt{D} \tag{41}$$

$$I_{D_3,\text{RMS}} = I_{D_3,\text{Max}}\sqrt{\frac{(1-D)\,(N_{21}+N_{31})}{3\,(1+N_{21}+N_{31})}} \tag{42}$$

$$I_{D_4,\text{RMS}} = \frac{\pi I_{\text{OUT}}}{2}\sqrt{\frac{1}{2D}} \tag{43}$$

$$I_{\text{DC,RMS}} = 2I_{\text{OUT}}\sqrt{\frac{1+N_{21}+N_{31}}{3\,(1-D)}} \tag{44}$$

$$I_{D_O,\text{RMS}} = I_{\text{OUT}}\sqrt{\frac{1}{1-D}} \tag{45}$$

$$I_{N_2,\text{RMS}} = \sqrt{{I_{D_3,\text{RMS}}}^2 + {I_{D_4,\text{RMS}}}^2 + {I_{D_O,\text{RMS}}}^2 + \frac{2{I_{\text{OUT}}}^2}{1-D}} \tag{49}$$

$$I_{C_1,\text{RMS}} = \sqrt{{I_{D_1,\text{RMS}}}^2 + {I_{LK,\text{RMS}}}^2 - 4M{I_{\text{OUT}}}^2} \tag{50}$$

$$I_{C_2,\text{RMS}} = \sqrt{{I_{D_3,\text{RMS}}}^2 + {I_{\text{DC,RMS}}}^2} \tag{51}$$

$$I_{C_3,\text{RMS}} = \sqrt{{I_{D_O,\text{RMS}}}^2 + {I_{D_4,\text{RMS}}}^2} \tag{52}$$

$$I_{C_C,\text{RMS}} = \sqrt{{I_{\text{DC,RMS}}}^2 + {I_{D_4,\text{RMS}}}^2} \tag{53}$$

$$I_{C_O,\text{RMS}} = \sqrt{{I_{D_O,\text{RMS}}}^2 - {I_O}^2}. \tag{54}$$

Fig. 6 shows the normalized voltage and current stresses of the power switch S. Moreover, at the operating experimental condition with $M=16$, $V_{\text{out}}=400$ V, and $I_{\text{out}}=0.5$ A, the values are respectively obtained to be 0.3 and 21.48, which results in 120 V and 10.93 A as the voltage and current stresses. Note that the voltage stress of the power switch is significantly lower than the output voltage. Moreover, considering the analysis carried out in Fig. 7, the best range of the duty cycle of the proposed converter is $0.1 < D < 0.65$.

C. Efficiency Analysis

The theoretical power loss mechanism of the introduced topology components is provided in this section. The parasitic parameters of the converter are listed in Table I. The total power

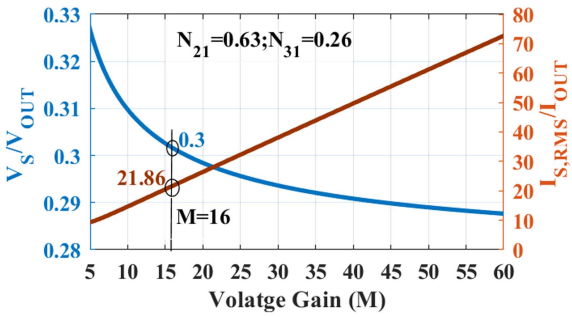


Fig. 6. Normalized voltage and current stresses of the MOSFET.

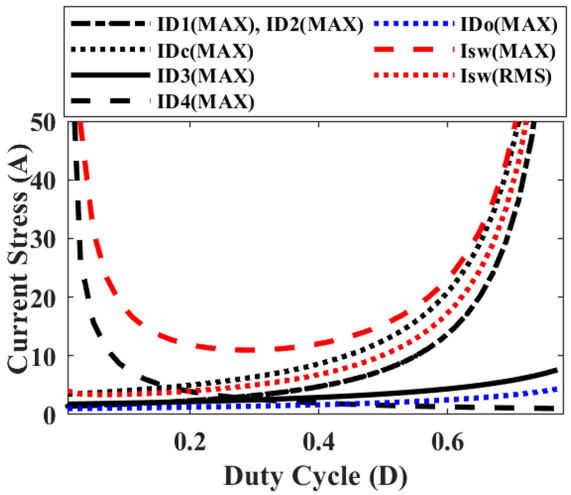


Fig. 7. Maximum current stress of the switching components of the proposed circuit.

dissipations of the circuit contain four main parts including a power switch, diodes, capacitors, and magnetic components.

The power loss of the main power switch in the presented circuit can be estimated by

$$P_{\text{Sw.}} = \frac{f_s}{2}.V_{DS}\left(i_{\text{Sw}}^{t=\text{off}}.t_{\text{off}}\right) + r_{DS(\text{on})}.I_{\text{Sw(RMS)}}^2 \tag{55}$$

where $i_{Sw}^{t=\text{off}}$ represent the current value of the switch at the turn-OFF instant (38). The conduction power losses of the circuit diodes can be given as

$$P_{Di} = r_{Di}.I_{D(\text{RMS})}^2 + V_{FDi}.I_{D(\text{AVG})}. \tag{56}$$

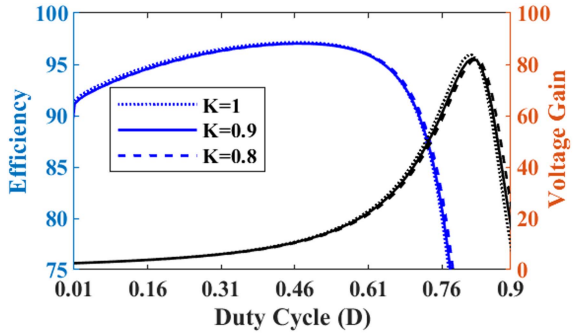


Fig. 8. Nonideal voltage gain and theoretical efficiency of the proposed converter as a function of the duty cycle and coupling coefficient (K).

Moreover, the power loss of the capacitors can be estimated as follows:

$$P_{\text{Cap.}i} = \text{ESR}_i.I_{C(\text{RMS})}^2. \tag{57}$$

In addition, the total power dissipations of the magnetic devices including L_{in} and TWCI (conduction and core losses) can be calculated as

$$P_{\text{Mag.}} = r_{L_1}.I_{L_1(\text{RMS})}^2 + r_{N1}.I_{N1(\text{RMS})}^2 + r_{N2}.I_{N2(\text{RMS})}^2 + P_{\text{Core}(L1,\ \text{CI})}. \tag{58}$$

The effect of the coupling coefficient (k) of the TWCI on the theoretical efficiency and voltage gain ratio is shown in Fig. 8. It is worth noting that for this curve, the nonideal voltage gain (22) of the converter is considered. For this curve, the parameters of the components are selected as $V_{\text{in}} = 25$ V, $R_L = 800\ \Omega$, $f_s = 50$ kHz, $n_{21} = 0.6$, $n_{31} = 0.2$, $r_{DS} = 7.6$ mΩ, $t_{\text{OFF}} = 4$ ns, $\text{ESR}_{Cc} = \text{ESR}_{C1} = \text{ESR}_{C2} = \text{ESR}_{C3} = 8$ mΩ, $\text{ESR}_{Co} = 100$ mΩ, $V_{\text{FDc}} = 0.55$ V, $V_{\text{FD1}} = V_{\text{FD2}} = 0.52$ V, $V_{\text{FD3}} = V_{\text{FDo}} = 0.65$ V, $r_{L\text{in}} = 10$ mΩ, $r_{N1} = 10$ mΩ, $r_{N2} = 5$ mΩ, and $r_{N3} = 15$ mΩ. From this figure, despite the selection of large values of the coupling coefficient, it does not have a significant effect on the efficiency of the suggested converter. It should be noted that in the case of the standard winding of the coupled inductor, the typical coupling coefficient is obtained about 0.99 to 0.97. Moreover, the effect of the winding parasitic resistances of the proposed circuit on the theoretical efficiency and voltage gain ratio is shown in Figs. 9 and 10. According to these figures, by increasing the parasitic resistance of the magnetic component's windings including the input inductor and TWCI, the efficiency is decreased slightly. For this purpose, the nonideal voltage gain

$$I_{S,\text{RMS}} = \sqrt{D\left[I_{LM}+(1+N_{31})\,MI_{\text{OUT}}\right]^2 + 2\left[I_{LM}+(1+N_{31})\,MI_{\text{OUT}}\right](1+N_{21}+N_{31})\,I_{\text{OUT}} + \left[(1+N_{21}+N_{31})\,I_{D_4,\text{RMS}}\right]^2} \tag{46}$$

$$I_{N_3,\text{RMS}} = \sqrt{{I_{D_2,\text{RMS}}}^2 + {I_{D_3,\text{RMS}}}^2 + {I_{D_4,\text{RMS}}}^2 + {I_{D_O,\text{RMS}}}^2 + 2{I_{\text{OUT}}}^2\left(M_{\text{CCM}} + \frac{1}{1-D}\right)} \tag{47}$$

$$I_{LK,\text{RMS}} = \sqrt{{I_{LM}}^2+(N_{21}I_{N_2})^2+(N_{31}I_{N_3})^2+2I_{LM}I_{\text{OUT}}\left[N_{21}\left(MD-1\right)-N_{31}\right]+2N_{21}N_{31}\left(M{I_{\text{OUT}}}^2+{I_{D_4,\text{RMS}}}^2+{I_{N_2,\text{RMS}}}^2\right)} \tag{48}$$

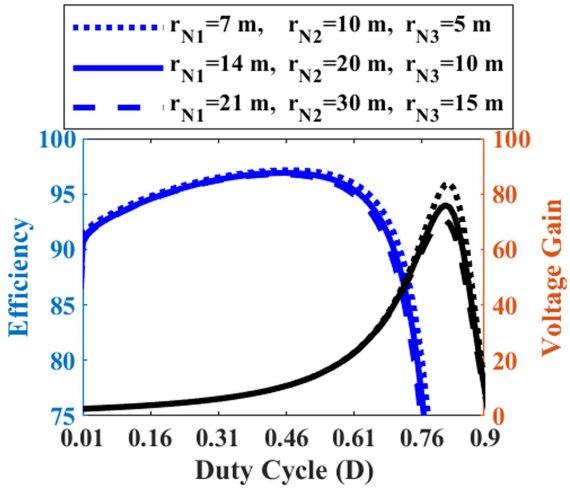


Fig. 9. Nonideal voltage gain and theoretical efficiency of the proposed converter as a function of the duty cycle and the CI parasitic resistances.

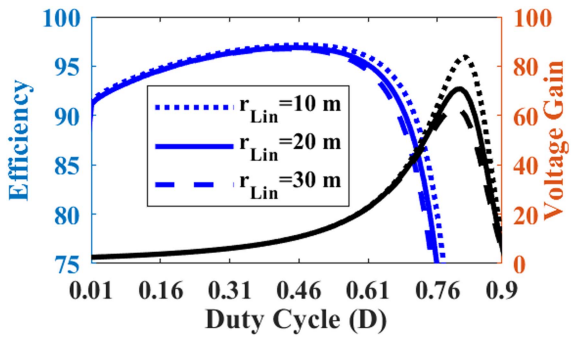


Fig. 10. Nonideal voltage gain and theoretical efficiency of the proposed converter as a function of the duty cycle at several values of the input inductor parasitic resistance.

is estimated as

$$M_{\text{Non-Ideal}} = \frac{V_o}{V_{\text{in}}} = \frac{2 + (n_{31} + n_{21})(1 + kD)}{(1 - D(1 + Kn_{31}))(1 - D)} .\eta \quad (59)$$

where η denotes the efficiency of the converter.

IV. Comparison Discussion

To verify the effectiveness of the proposed converter, a comprehensive comparison with similar relevant topologies has been summarized in Table II. The comparison covers important features, such as voltage gain, voltage stresses across semiconductors, the number of components, input current ripple, soft switching operation, and common ground between input power source and load. The turns' ratios of the TWCIs are considered $n_{21} = 0.5$ and $n_{31} = 0.3$. To ensure a fair comparison in the topologies with two-winding CIs, the turns' ratio is selected to be 0.8.

It can be observed from Fig. 11 that the proposed converter can provide higher dc voltage than the other converters. Moreover, the ratio of the voltage gain of the converters per number of components (M/N) is provided in Fig. 12. It is seen that again the proposed converter with 14 components along with the converter

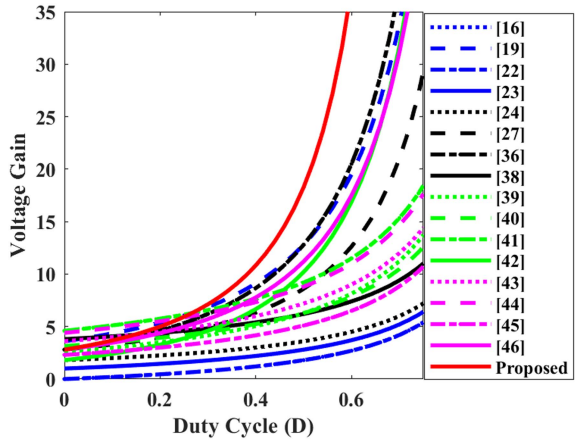


Fig. 11. Voltage gain comparison versus duty cycle D.

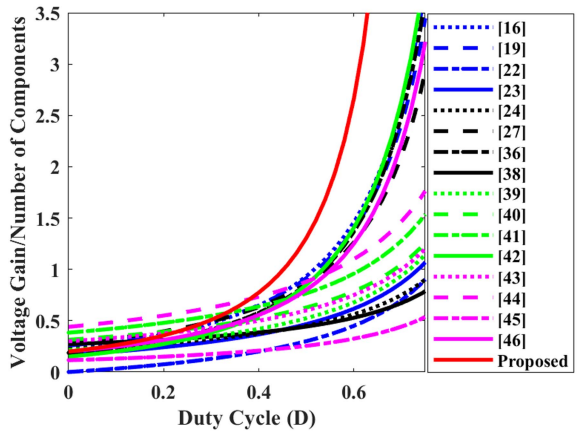


Fig. 12. Voltage gain per number of components comparison.

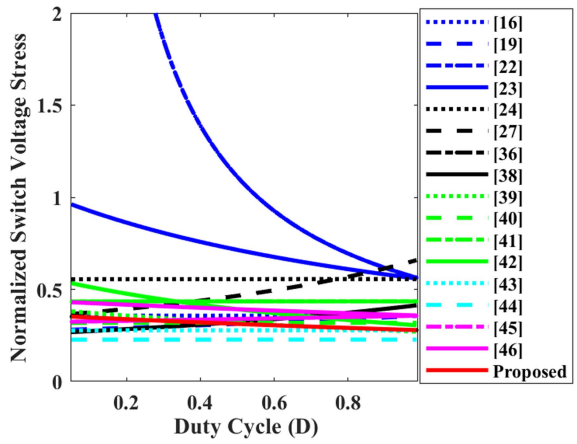


Fig. 13. Comparison of voltage stress across the main power switch.

in [44] has the best performance over the duty cycles of about 0.4. This point reveals the sufficient device utilization in voltage gain enhancement. It is worth noting that the converter in [44] suffers from the lack of a common ground.

Fig. 13 shows the comparison of the normalized voltage stresses across the power switches. It is clear that the power

TABLE II
COMPARISON BETWEEN THE PROPOSED CONVERTER AND THE LATEST COUNTERPARTS

Converter topology	No. of components *S/D/C/CI+L/T*	Voltage gain	L.I.C.R.	Voltage stress on main switch	Maximum voltage stress on diodes	S.S.M.S.	R.R.I.D.	C.G.
[16]	$1/5/4/1^{2w}+1/12$	$\frac{2+n}{(1-D)^2}$	Yes	$\frac{V_o}{2+n}$	$\frac{(1+n)V_o}{2+n}$	-	High	Yes
[19]	$1/6/5/1^{2w}+1/14$	$\frac{2+n(2-D)}{(1-D)^2}$	Yes	$\frac{V_o}{2+n(2-D)}$	$\frac{(1+n)V_o}{2+n(2-D)}$	-	High	Yes
[22]	$1/2/2/1^{2w}+0/6$	$\frac{(1+n)D}{(1-D)}$	No	$\frac{V_o}{(1+n)D}$	$\frac{(2D+n)V_o}{d(1+n)}$	ZVS	Very Low	Yes
[23]	$1/2/2/1^{2w}+0/6$	$\frac{1+nD}{(1-D)}$	No	$\frac{V_o}{1+nD}$	$\frac{nV_o}{1+nD}$	ZCS	Low	Yes
[24]	$1/3/3/1^{2w}+0/8$	$\frac{1+n}{(1-D)}$	No	$\frac{V_o}{1+n}$	$\frac{nV_o}{1+n}$	ZCS	Very Low	Yes
[27]	$1/4/3/1^{3w}+1/10$	$\frac{(2+n_{21}+n_{31})-(n_{31}+1)D}{(1-D)^2}$	Yes	$\frac{V_o}{(2+n_{21}+n_{31})-(n_{31}+1)D}$	$\frac{(1+n_{21}+n_{31})V_o}{(2+n_{21}+n_{31})-(n_{31}+1)D}$	-	High	No
[36]	$1/6/6/1^{3w}+1/15$	$\frac{2+n(1+D)}{(1-D)^2}$	Yes	$\frac{V_o}{2+n(1+D)}$	$\frac{(1+n)V_o}{2+n(1+D)}$	ZCS+QR	Very Low	Yes
[38]	$2/5/5/1^{3w}+1/14$ $n_{21}=n_{31}=n$	$\frac{3+2n-D(1+n)}{(1-D)}$	Yes	$\frac{V_o}{3+2n-D(1+n)}$	$\frac{(1+n)V_o}{3+2n-D(1+n)}$	ZVS+QR	Very Low	Yes
[39]	$2/3/5/1^{3w}+1/12$	$\frac{1+(1+n_{31}-n_{21})(1+D)}{[1-n_{31}].(1-D)}$	Yes	$\frac{[1-n_{31}]V_o}{1+(1+n_{31}-n_{21})(1+D)}$	$\frac{[1+n_{31}]V_o}{1+(1+n_{31}-n_{21})(1+D)}$	ZVS	High	No
[40]	$2/2/4/1^{3w}+1/10$	$\frac{2+n_{21}-n_{31}}{[1-n_{31}].(1-D)}$	Yes	$\frac{[1-n_{31}]V_o}{2+n_{21}-n_{31}}$	$\frac{[1+n_{21}]V_o}{2+n_{21}-n_{31}}$	ZVS	Very Low	Yes
[41]	$1/4/5/1^{3w}+1/12$	$\frac{2+n_{31}}{[1-n_{21}].(1-D)}$	Yes	$\frac{V_o}{2+n_{31}}$	$\frac{(1+n_{31})V_o}{2+n_{31}}$	ZCS	Very Low	Yes
[42]	$1/5/4/1^{3w}+1/12$	$\frac{(1+n_{21})(1+D)+n_{31}}{(1-D)^2}$	Yes	$\frac{V_o}{(1+n_{21})(1+D)+n_{31}}$	$\frac{(n_{21}+n_{21}+D)V_o}{(1+n_{21})(1+D)+n_{21}}$	-	High	No
[43]	$1/4/5/1^{3w}+1/12$	$\frac{1+n_{21}+n_{31}+D}{n_{21}.(1-D)}$	Yes	$\frac{n_{21}V_o}{1+n_{21}+n_{31}+D}$	$\frac{(1+n_{21})V_o}{1+n_{21}+n_{31}+D}$	-	Very Low	Yes
[44]	$1/3/4/1^{3w}+1/10$	$\frac{2+n_{21}-n_{31}}{[1-n_{21}].(1-D)}$	Yes	$\frac{(1-n_{21})V_o}{2+n_{21}-n_{31}}$	$\frac{(1+n_{21})V_o}{2+n_{21}-n_{31}}$	ZCS	Very Low	No
[45]	$1/8/8/1^{3w}+2/20$	$\frac{1+n_{21}+n_{31}+n_{21}(1+D)}{(1-D)}$	Yes	$\frac{V_o}{1+n_{21}+n_{31}+n_{21}(1+D)}$	$\frac{(n_{21}+n_{21})V_o}{1+n_{21}+n_{31}+n_{21}(1+D)}$	ZCS+QR	Very Low	Yes
[46]	$1/6/5/1^{3w}+1/14$	$\frac{2+n_{21}+n_{31}}{(1-D)^2}$	Yes	$\frac{V_o}{2+n_{21}+n_{31}}$	$\frac{(1+n_{21}+n_{31})V_o}{2+n_{21}+n_{31}}$	-	High	Yes
Proposed Converter	$1/6/5/1^{3w}+1/14$	$\frac{2+(n_{21}+n_{31})(1+D)}{[1-D(1+n_{31})].(1-D)}$	Yes	$\frac{V_o}{2+(n_{21}+n_{31})(1+D)}$	$\frac{1+n_{21}+n_{31}}{2+(n_{21}+n_{31})(1+D)}V_o$	ZCS+QR	Very Low	Yes

S = switch, *D* = diode, *C* = capacitor, CI = coupled-inductor, *L* = inductor, *T* = total device count, L.I.C.R. = low input current ripple, S.S.M.S. = soft switching for main power switch, R.R.I.D. = reverse recovery for input diodes, C.G. = common ground, and QR = quasi-resonant

TABLE III
POWER DENSITY (W/CM^3) OF THE PASSIVE ELEMENTS OF THE CONVERTERS IN THE COMPARISON TABLE AT 200 W

Converter	**[16]**	**[19]**	**[22]**	**[23]**	**[24]**	**[27]**	**[36]**	**[38]**	**[39]**	**[40]**	**[41]**	**[42]**	**[43]**	**[44]**	**[45]**	**[46]**	**Proposed**
Power Density (W/cm^3)	2.8	3.2	2.6	2.7	2.5	2.6	2.8	2.9	2.4	2.9	2.1	2.8	2.9	3.0	2.9	2.8	3.1

MOSFET of the proposed converter withstands very low voltage stress in comparison with many other converters. Although the converters of [43] and [44] exhibit better performance in voltage stress across the power switch; however, these circuits suffer from hard switching performance (for [43]) and the lack of common ground between input and output sides (for [44]). Moreover, Fig. 14 shows the comparison of the normalized maximum voltage stresses across the diodes in which the diodes with the highest voltage stresses have been selected in each of the competitors. The normalized voltage stress of the selected diode in the proposed converter has an acceptable curve in comparison with the other ones.

In addition, Table III shows the power density comparison of the converters in the comparison table. For this comparison, circuit capacitors and magnetic components are considered optimally. The dimensions of the passive components in this table are achieved under the same conditions as $V_{\rm in} = 25$ V, $V_{\rm o} = 400$ V, $P_{\rm o} = 200$ W, $\Delta_{\rm ILin} = 25\%$, $\Delta_{\rm ILm} = 50\%$, f = 50 kHz, $n_{21} = 0.5$, and $n_{31} = 0.23$. According to this table, the power density of the proposed converter along with the converters in [19] and [44] are at the highest level. Therefore, due to the unique structure, using three winding CI in the proposed converter does not lead to a decrease in power density.

According to the comparison discussions, it can be concluded that the proposed converter with the soft switching operation of the semiconductors, high voltage gain, low voltage stress across the semiconductor, low input current ripple, and common ground is an attractive solution for RES applications.

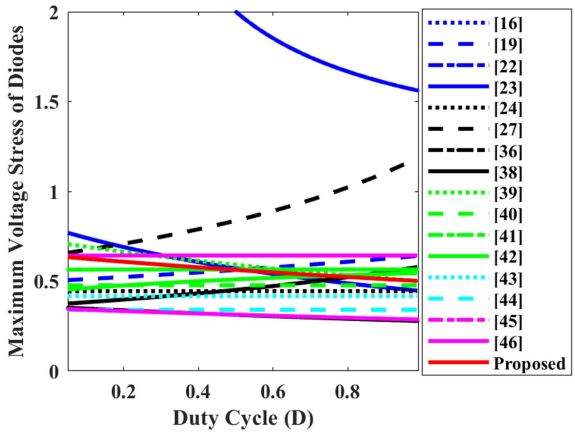


Fig. 14. Comparison results of maximum voltage stress of the diodes.

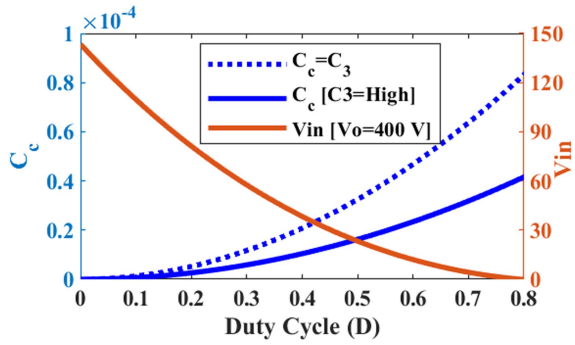


Fig. 15. Design of the capacitor C_c versus duty cycle and input voltage at a constant output voltage $V_o = 400$ V.

V. Design Considerations

The minimum value of the input inductor L_{in} is selected to limit the input current ripple (ΔI_{Lin}) within the desired value as

$$L_{in} > \frac{V_{in}.D}{\Delta I_{in}.f_s}. \tag{60}$$

Besides, the minimum magnetizing inductance of CI can be obtained as

$$L_M > \frac{V_{LM}.D}{\Delta I_{LM}.f_s} = \frac{v_{C_1}D}{\Delta I_{LM}.f_s}. \tag{61}$$

In (61), ΔI_{LM} denotes the allowable current ripple of L_M. In the presented topology, to guarantee a fixed dc output voltage, the voltage ripple on the output capacitor should be designed to be in a standard range (<1%); therefore, the output capacitance can be selected as

$$C_o > \frac{D}{\Delta V_{co}.f_s}\left(\frac{V_o}{R_L}\right). \tag{62}$$

Also, the minimum values of the middle capacitors of the proposed circuit can be given as follows:

$$C_1 > \frac{D\left(\frac{2(1+n_{21}+n_{31})}{(1-D)} + \frac{\pi n_{21}}{2D} + Mn_{31}\right)V_o}{\Delta V_{C_1} f_s R_L} \tag{63}$$

$$C_2 > \frac{2(1-D)^2 V_o}{\Delta V_{C_2}.R_L f_s} \tag{64}$$

$$C_3 > \frac{\pi V_o}{\Delta V_{C_3}.2.R_L f_s} \tag{65}$$

$$C_c > \frac{\pi V_o}{\Delta V_{Cc}.2.R_L f_s}. \tag{66}$$

In (63)–(66), ΔV_{Ci} is the acceptable voltage ripple of the capacitors. Moreover, regarding the resonant frequency (1) and considering the value of the turn's ratios of the TWCI, the simplest method to adjust the resonant frequency is using the capacitors C_c, C_1, and C_3 as

$$\pi\sqrt{L_k\left(C_1\|(n_{21}+n_{31})^2(C_3\|C_c\right)} = DT_S. \tag{67}$$

Due to the unique structure of the suggested circuit, even in a very high voltage gain ratio, the total number of turns ratio is often less than unity ($N_{21} + N_{31} < 0$). Thus, according to (1), the sensitivity of f_R to the capacitor C_1 is lower than the capacitors C_c and C_3. Therefore, to simplify the resonance tank design, the value of the capacitor C_1 can be considered as an enough large value. Moreover, due to the series connection of the capacitors C_3 and C_c during the ON state of the power switch, and by assuming the same voltage ripple, the resonant frequency of the proposed converter can be simplified as

$$\pi\left(n_{21}+n_{31}\right)\sqrt{0.5L_kC_c} = DT_S. \tag{68}$$

Also, to further simplify the design procedure, the value of the capacitor C_3 can also be considered to be sufficiently larger than the capacitor C_c. In this case, the resonant frequency can be adjusted with only one variable parameter (C_c). Fig. 15 shows the design of the capacitors C_c and C_3 versus duty cycle and input voltage at a constant output voltage $V_o = 400$ V. According to this figure, by increasing the input voltage of the converter, to have a constant output voltage, the duty cycle of the converter should be decreased. Thus, the value of the capacitors C_c and C_3 should be decreased.

In addition, to ensure the resonant performance of the converter in response to changes in the input voltage, it is more appropriate to set the resonance frequency as follows:

$$f_R = \frac{f_s}{2\left(D - \Delta D\%\right)} \tag{69}$$

where $\Delta D\%$ is the duty cycle changes under the maximum input voltage fluctuations.

VI. Small Singal Modeling and Control Design of the Proposed Converter

In this section, small signal derivation and low-frequency behavior along with the closed-loop control design of the suggested converter are provided.

A. Small Singal Modeling

To simplify the modeling process, the state-space averaging technique is used [47]. The state variable vector of the proposed

converter is given as

$$x(t) = [i_{L\text{in}}\ i_{LM}\ v_{C_1}\ v_{C_2}\ v_{C_3}\ v_{C_c}\ v_{C_o}] \tag{70}$$

To extract the state equations of the converter in three main modes 3, 7, and 8, considering the parasitic resistance r_{c3} in series with the capacitor C_3 is required. According to the proposed converter structure, the state equations of operating mode 3 are expressed as

$$L\frac{di_L}{dt} = V_{\text{in}} + n_3 v_{C_1} \tag{71}$$

$$L_M\ \frac{di_{\text{LM}}}{dt} = v_{C_1} \tag{72}$$

$$\begin{aligned} C_1\ \frac{dV_{C_1}}{dt} =\ & -n_3 i_{L\text{in}} - i_{\text{LM}} - X_0(n_{21}+n_{31})^2 V_{C_1} \\ & + X_0\left(n_{21}+n_{31}\right)V_{C_3} - X_0\left(n_{21}+n_{31}\right)V_{C_c} \end{aligned} \tag{73}$$

$$C_2\ \frac{dV_{C_2}}{dt} = 0 \tag{74}$$

$$C_3\ \frac{dV_{C_3}}{dt} =\ \left(n_{21}+n_{31}\right)X_0 V_{C_1} + X_0 V_{C_c} - X_0 V_{C_3} \tag{75}$$

$$C_c\ \frac{dV_{C_c}}{dt} =\ -\left(n_{21}+n_{31}\right)X_0 V_{C_1} - X_0 V_{C_c} + X_0 V_{C_3} \tag{76}$$

$$C_o\ \frac{dV_{C_o}}{dt} =\ -\frac{V_{C_o}}{R}. \tag{77}$$

The state equations of mode 7 are given as

$$L_{\text{in}}\ \frac{di_{L\text{in}}}{dt} = V_{\text{in}}\ - V_{C_1} \tag{78}$$

$$L_M\ \frac{di_{\text{LM}}}{dt} = V_{C_1} + V_{C_2} - V_{C_c} \tag{79}$$

$$\begin{aligned} C_1\ \frac{dV_{C_1}}{dt} =\ & i_{L\text{in}} - i_{\text{LM}} - X_2\left(-X_0 + X_0 X_1\right)V_{C_1} \\ & - X_0 X_1 X_2 V_{C_2} + X_0 X_2 V_{C_3} + X_0 X_1 X_2 V_{C_c} \\ & - X_0 X_2 V_{C_o} \end{aligned} \tag{80}$$

$$\begin{aligned} C_2\ \frac{dV_{C_2}}{dt} =\ & -i_{\text{LM}} - X_0 X_1\left(X_1 - 1\right)V_{C_1} - X_0 {X_1}^2 V_{C_2} \\ & + X_0 X_1 V_{C_3} + X_0 {X_1}^2 V_{C_c} - X_0 X_1 V_{C_o} \end{aligned} \tag{81}$$

$$\begin{aligned} C_3\ \frac{dV_{C_3}}{dt} =\ & X_0\left(X_1 - 1\right)V_{C_1} - X_0.X_1 V_{C_2} - X_0 V_{C_3} \\ & - X_0.X_1 V_{C_c} + X_0 V_{C_o} \end{aligned} \tag{82}$$

$$\begin{aligned} C_c\ \frac{dV_{C_c}}{dt} =\ & i_{\text{LM}} + X_0 X_1\left(X_1 - 1\right)V_{C_1} + X_0 {X_1}^2 V_{C_2} \\ & - X_0 X_1 V_{C_3} - X_0 {X_1}^2 V_{C_c} + X_0 X_1 V_{C_o} \end{aligned} \tag{83}$$

$$\begin{aligned} C_o\ \frac{dV_{C_o}}{dt} =\ & -X_0\left(X_1 - 1\right)V_{C_1} + X_0.X_1 V_{C_2} + X_0 V_{C_3} \\ & + X_0.X_1 V_{C_c} - X_0 V_{C_o} - \frac{V_{C_o}}{R}. \end{aligned} \tag{84}$$

Also, the state equations of mode 8 are expressed as follows:

$$L_{\text{in}}\ \frac{di_{L\text{in}}}{dt} = V_{\text{in}} - V_{C_1} \tag{85}$$

$$L_M\ \frac{di_{\text{LM}}}{dt} =\ -X_3 V_{C_2} \tag{86}$$

$$\begin{aligned} C_1\ \frac{dV_{C_1}}{dt} =\ & i_{L\text{in}} - X_0 V_{C_1} - X_0\left(X_3+1\right)V_{C_2} \\ & - X_0 V_{C_3} + X_0 V_{C_o} \end{aligned} \tag{87}$$

$$\begin{aligned} C_2\ \frac{dV_{C_2}}{dt} =\ & X_3.i_{\text{LM}} - X_0\left(X_3+1\right)V_{C_1} - X_0(X_3+1)^2 V_{C_2} \\ & - X_0\left(X_3+1\right)V_{C_3} + X_0\left(X_3+1\right)V_{C_o} \end{aligned} \tag{88}$$

$$\begin{aligned} C_3\ \frac{dV_{C_3}}{dt} =\ & -X_0 V_{C_1} - X_0\left(X_3+1\right)V_{C_2} - X_0 V_{C_3} \\ & + X_0 V_{C_o} \end{aligned} \tag{89}$$

$$C_c\ \frac{dV_{C_c}}{dt} = 0 \tag{90}$$

$$\begin{aligned} C_o\ \frac{dV_{C_o}}{dt} =\ & X_0\ V_{C_1} + X_0\left(X_3+1\right)V_{C_2} + X_0 V_{C_3} \\ & - X_0 V_{C_o} - \frac{V_{C_o}}{R} \end{aligned} \tag{91}$$

where X_0–X_3 are defined as follows:

$$\begin{aligned} X_0 = \frac{1}{r_{C_3}},\ X_1 = 1 + n_{21} + n_{31},\ X_2 = n_{21} + n_{31},\ X_3 \\ = \frac{1}{n_{21}+n_{31}}. \end{aligned} \tag{92}$$

By assuming the right triangle form of i_{Dc}, the time duration of the operating mode 7 (d_2) can be obtained as

$$d_2 = \frac{1-D}{(1+n2+n3)}. \tag{93}$$

Considering the weighting factors d, d_2, and (1-d-d_2) for the operational modes of the suggested topology, the averaged model is achieved as

$$\begin{cases} \dot{x} = Ax + Bu \\ y = Cx + Eu \end{cases} \tag{94}$$

$$\begin{cases} A = dA_1 + d_2 A_2 + (1-d-d_2)A_3 \\ B = dB_1 + d_2 B_2 + (1-d-d_2)B_3 \\ C = dC_1 + d_2 C_2 + (1-d-d_2)C_3 \\ E = dE_1 + d_2 E_2 + (1-d-d_2)E_3 \end{cases} \tag{95}$$

where A_i, B_i, C_i, and E_i are the state matrices, y denotes the output voltage, x is the averaged value of the state variables, and u represents the input source. To derive the small-signal model of the system, the small ac perturbations are superimposed to the variable states as

$$\begin{cases} d = D + \hat{d} \\ d_2 = D_2 + \hat{d}_2 \\ u = U + \hat{u} \\ x = X + \hat{x} \end{cases} \tag{96}$$

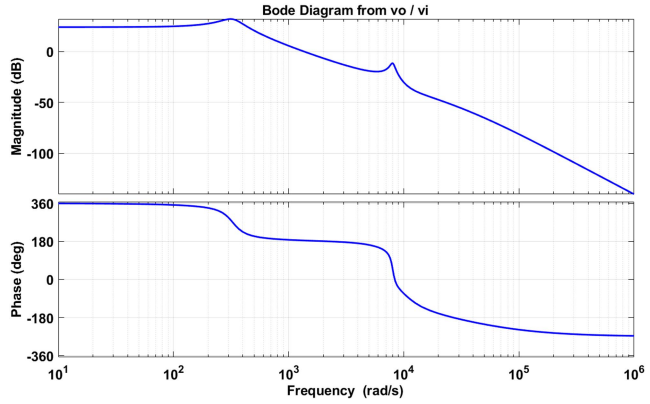


Fig. 16. Frequency response of the control-to-output transfer (G_{vov}) of the proposed converter.

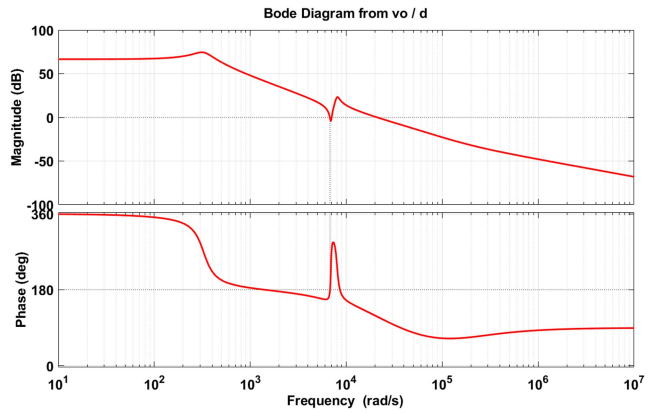


Fig. 17. Frequency response of the control-to-output transfer (G_{vod}) of the proposed converter.

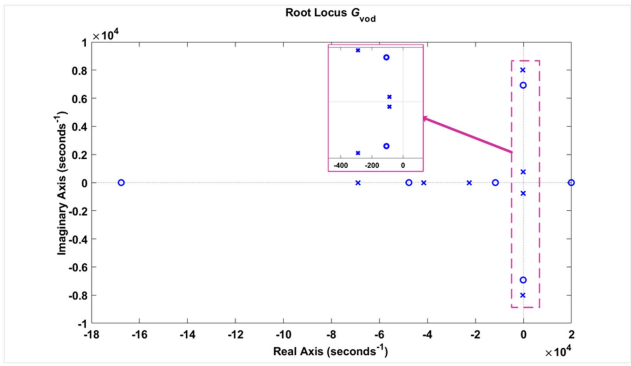


Fig. 18. Pole and zero map of the control-to-output transfer function of the proposed converter.

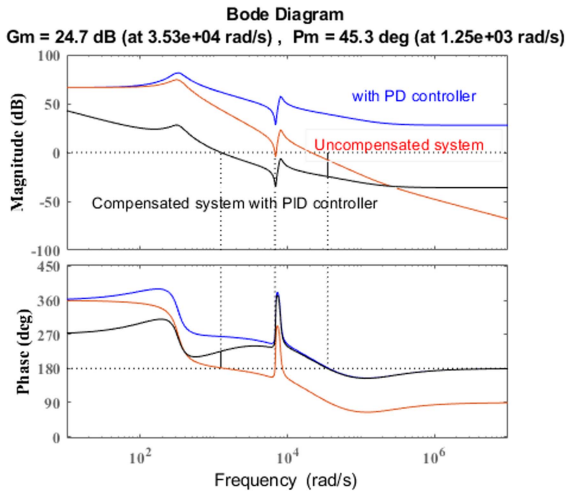


Fig. 19. Closed-loop controller design for the proposed converter.

where lowercase variables denote the small value of the parameters and capital variables are the steady-state values. By substituting (96) into (94) and neglecting steady-state terms, the transfer functions output-to-input (G_{vov}) and the output-to-duty cycle (G_{vod}) of the converter are obtained as

$$G_{vov}(s) = \frac{\hat{v}_o}{\hat{v}_{\text{in}}} = \left.\frac{\hat{y}(s)}{\hat{u}(s)}\right|_{\hat{d}=0} = C(SI - A)^{-1}B + E \quad (97)$$

$$\begin{aligned} G_{vod}(s) = \left.\frac{\hat{v}_o}{\hat{d}}\right|_{\hat{u}=0} &= C(SI - A)^{-1}\Bigg[(A_1 - A_3)X \\ &+ \left(1 - \frac{1}{1 + n_{21} + n_{31}}\right)(B_1 - B_3)U\Bigg] \\ &+ \left(1 - \frac{1}{1 + n_{21} + n_{31}}(C_1 - C_3)X\right. \\ &+ \left(1 - \frac{1}{1 + n_{21} + n_{31}}\right)(E_1 - E_3)U. \end{aligned} \quad (98)$$

The simulation results of the low-frequency behavior (G_{vov} and G_{vod}) of the proposed circuit at $R = 800\ \Omega$, $V_{\text{out}} = 400$ V, $n_{21} = 0.53$, $n_{31} = 0.22$, $V_{\text{in}} = 25$ V, and $M = 16$, $D = 0.5$ are illustrated in Figs. 16 and 17. In addition, Fig. 18 presents the pole and zero map graph for G_{vod}. Due to the right-half-plane (RHP) zero, the proposed converter has a nonminimum phase behavior. However, regarding Fig. 18, the RHP zero of the proposed converter is far away from the origin, which prevents a significant nonminimum phase effect.

B. Closed-Loop Control Design

The bode diagram of the uncompensated and compensated systems is shown in Fig. 19. The phase margin and the gain margin of the uncompensated system are about $-5.32°$ (at about 6.76 krad/s) and 1.11 dB, respectively. To provide sufficient phase and gain margins, PD and proportional-integral (PI) controllers are implemented, which provide proportional-integral-derivative (PID) controller characteristics as

$$T_{\text{PID}} = (1 + K_D S)\left(K_P + \frac{K_i}{S}\right). \quad (99)$$

The PD controller is responsible for achieving the maximum phase improvement beyond 1 krad/s. As a result, it is selected to be 160. The PI controller is responsible for reducing steady-state error and providing a sufficient phase margin for the system. The cutoff frequency and the phase margin of the compensated system are chosen at about 1.1 krad/s and 45°, respectively.

TABLE IV
PROTOTYPE SPECIFICATIONS

Parameter	Values
Output power (P_{OUT})	200 W
Input–output voltages (V_{IN}–V_{OUT})	25–400 V
Switching frequency (f_s)	50 kHz
Capacitor C_1	3*10 μF/100 V
Capacitor C_c	2.2 μF/250 V
Capacitor C_2	10 μF/100 V
Capacitor C_3	10 μF/250V
Capacitor C_{out}	10 μF/450 V
Power Switch S	IPP076N15N5/$R_{DS(ON)}$=7.6 mΩ
Input inductor L_{IN} / Core	150 μH/EE42/21/15
Magnetizing inductor (L_M)	325 μH
Turns' ratios of the TWCI/Core	(1:0.53:0.26)/ETD 44/22/15
Diodes D_4, D_O	MUR440
Diode D_3/ Diode D_C	MUR415/MBR820
Diodes D_1 and D_2	MBR10100

TABLE V
LOSS DISTRIBUTIONS OF THE PROPOSED TOPOLOGY

Components	Power loss relations	Loss value (W)	Percent (%)
Input inductor r_{lin}	$P_{ohmic}^{loss} + P_{core}^{loss}$	0.85	9.9
Coupled inductor loss		1.06	12.4
Turn-OFF loss (MOSFET)	$\frac{1}{2T_s}(I_{switch(\max)}.V_{DS}.t_{off})$	0.19	2.2
Conduction loss (MOSFET)	$I_{S(RMS)}^2.R_{DS(on)}$	0.93	10.9
Output capacitance loss (MOSFET)	$\frac{1}{2T_s}(C_{oss}.V_{DS}^2)$	0.2	2.3
D_1	$V_F.I_{D(AVG)}$	1.9	22.2
D_2		1.8	21.1
D_3		0.3	3.5
D_4		0.4	4.6
D_c		0.25	2.9
D_o		0.4	4.6
C_1	$I_{C(RMS)}^2.ESR$	0.16	1.8
C_2		0.02	0.2
C_3		0.01	0.1
C_c		0.03	0.35
C_o		0.03	0.35

The voltage feedback gain is selected such that 2 V is set as the voltage reference corresponding to the output voltage of 400 V. As a result, the gain of the sensor is obtained 1/200. Moreover, the gain of the modulator is considered 1/13. These considerations result in the PI controller parameters as $K_P = 1.6595$ and $K_i = 1676$. According to the bode diagram of the compensated system with PID, the gain and phase margins are 24.7 dB and 45.3° at 1.25 krad/s, which ensures sufficient dynamic and steady-state performance.

VII. EXPERIMENTAL VERIFICATIONS

The performance operation of the proposed converter is verified by a 200 W 25–400 V laboratory prototype with the specifications given in Table IV. The values of the circuit capacitors are considered based on the voltage ripple maximum of 1% for the output capacitor and 5% for other capacitors.

Fig. 20 shows the experimental results of the output voltage, input current, and the passing current of the leakage inductor of

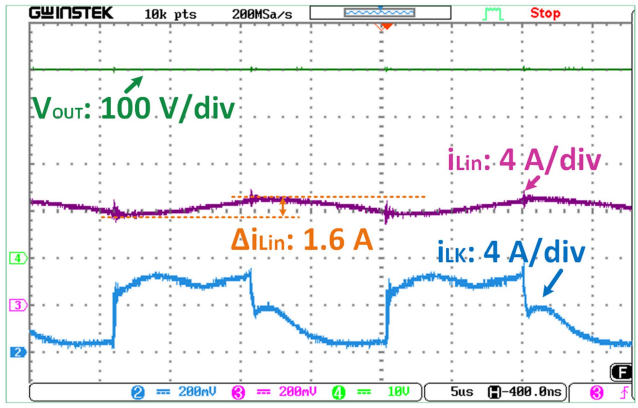


Fig. 20. Experimental results of V_o, i_{Lin}, and i_{LK}.

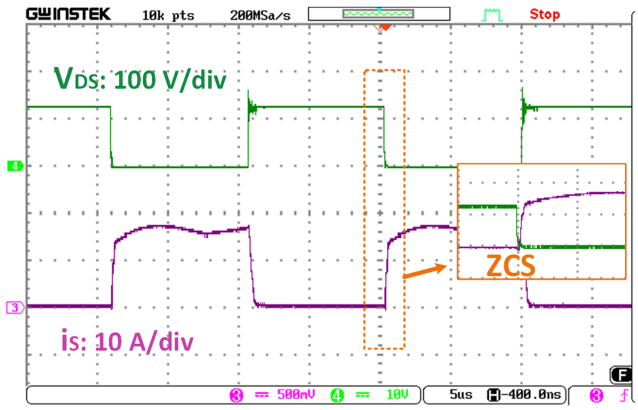
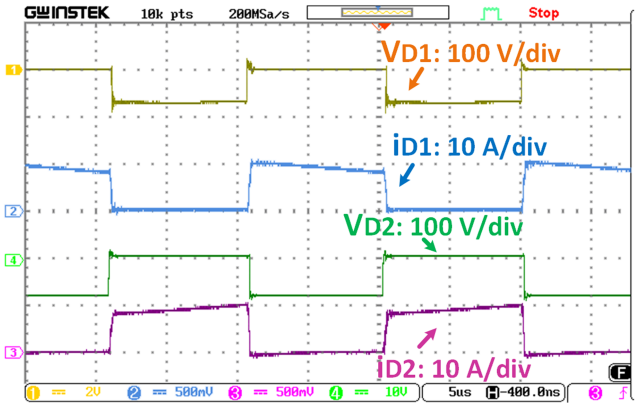


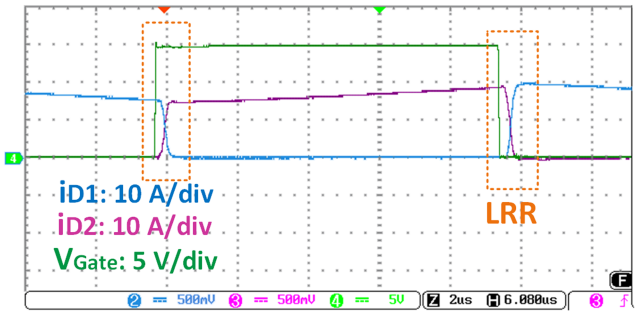
Fig. 21. Experimental results of v_{DS} and i_{SW}.

the TWCI. The high output voltage of 400 V is obtained from the low input voltage of 25 V with a duty cycle of about 50%. Moreover, the input current ripple is around 1.6 A and i_{LK} is consistent with the key waveform in Fig. 2. Fig. 21 shows the experimental results of the voltage and current of the switch. The voltage stress of the MOSFET is 120 V, which is about 30% of the high output voltage. Moreover, ZCS turn-ON is achieved for the switch which reduces the switching losses. Fig. 22 shows the voltages and currents of the input diodes D_1 and D_2. The voltage stresses are about $V_{D1} = 70$ V and $V_{D2} = 80$ V, which confirm the formulas (24) and (25). Meanwhile, the input diodes are switched with LRR performance.

Fig. 23 illustrates the voltage and current of the diode D_3. The voltage stress of the diode is about 110 V corroborating the formula (26). On the other hand, the ZCS ON and LRR at turn-OFF are provided for the diode. Fig. 24 shows the voltages and currents of the diodes D_c and D_4. The voltage stresses are about $V_{Dc} = 120$ V and $V_{D4} = 230$ V which support formulas (23) and (27). The clamp diode is turned OFF with LRR and QR operation provides LRR in OFF instant for D_4. Also, Fig. 25 shows the experimental results of the voltage and current of the diode D_o. The imposed voltage is about $V_{Do} = 225$ V which confirms formula (27). Moreover, ZCS turn-ON is achieved for the diode. Moreover, Fig. 26 shows the measured conversion



(a)



(b)

Fig. 22. (a) Experimental results of v_{D1} and i_{D1}. (b) Zoomed view of the current of the diodes D_1 and D_2.

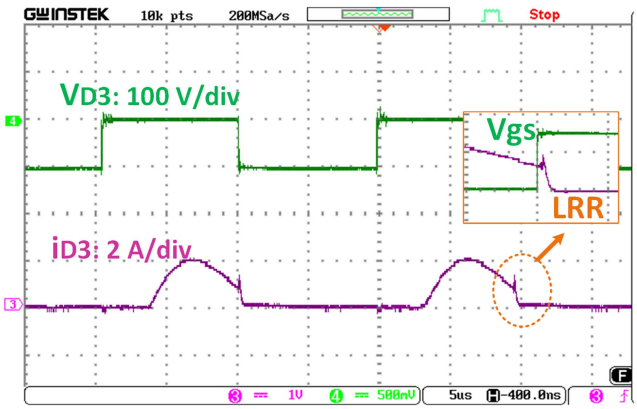


Fig. 23. Experimental results of v_{D3} and i_{D3}.

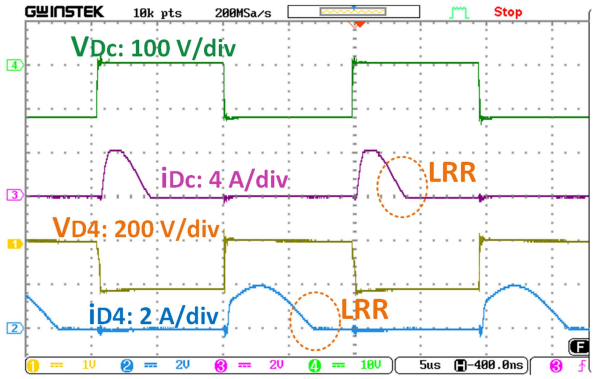


Fig. 24. Experimental results of v_{Dc}, i_{Dc}, $v_{D4,}$ and i_{D4}.

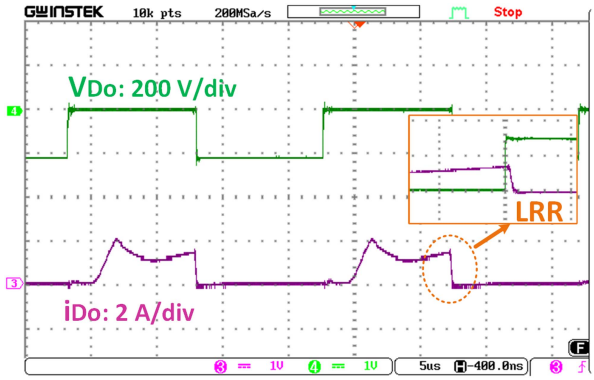


Fig. 25. Experimental results of v_{Do} and i_{Do}.

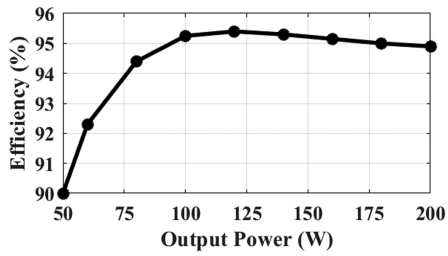


Fig. 26. Measured efficiency of the proposed converter.

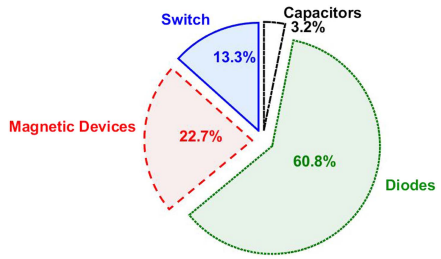


Fig. 27. Losses distribution at full load.

efficiency of the proposed converter versus the output power. The maximum efficiency is 95.4%, which occurs at 120 W and the full load efficiency is 94.9%.

Through the steady-state analysis in Section II, the RMS and average currents of the components can be obtained and utilized in dissipation evaluation in a given power. The power loss distribution of the circuit components of the converter sample prototype at full load condition of 200 W ($V_{\mathrm{in}} = 25$ V/$V_o =$ 400 V) is provided in Fig. 27. It is seen that the diodes still include the major portion of losses, which is mainly due to the losses of the input diodes. The input diodes D_1 and D_2 pass a portion of high input current, and as a result, the term of forward voltage multiplied by the average current for these diodes is high.

Fig. 28 shows the dynamic response of the suggested circuit at the output load variation. It is seen that when the load changes from $R_{\mathrm{Load1}} = 800\ \Omega$ to $R_{\mathrm{Load2}} = 1200\ \Omega$, the output dc voltage can be regulated at 400 V successfully. Moreover, in

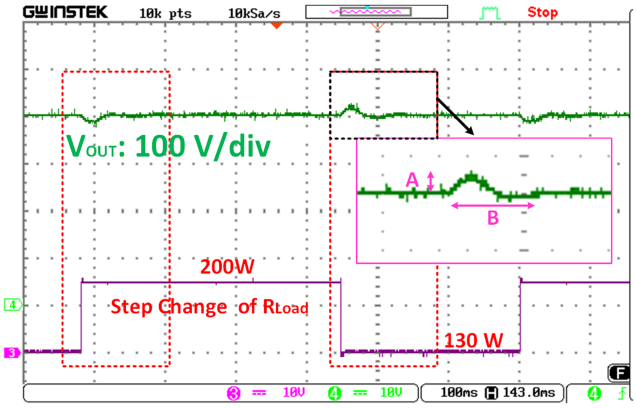


Fig. 28. Hardware measurement of the dynamic response of the output voltage for a 50% step change in the output load. A = Voltage overshoot = 20 V. B = Settling time = 70 ms.

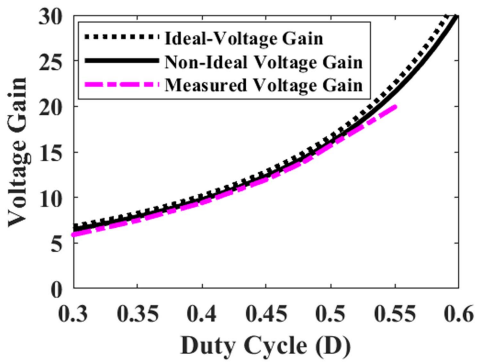


Fig. 29. Theoretical efficiency and nonideal voltage gain ratio of the proposed converter.

this figure, a crop of the transient response with more details of the dynamic response is included. Also, Fig. 29 shows the ideal and nonideal voltage gains along with the experimental voltage gain of the proposed circuit at the sample prototype specification. According to the figure, the measured voltage gains are close to the theoretical values. It should be noted that this curve is obtained based on the voltage stress tolerance of the components of the sample prototype of the suggested topology. A photograph of the sample prototype of the proposed converter is shown in Fig. 30. Dimensions and weight of the PCB of the proposed converter are $L = 20$ cm, $W = 12.5$ cm, $H = 1.5$ cm, and $W = 510$ g.

VIII. Conclusion

A semiquadratic trans-inverse high step-up dc–dc has been proposed in this article. Voltage gain is significantly enhanced by integrating a TWCI, which enables three degrees of freedom for controlling voltage gain through turns ratio along with the converter duty cycle. The trans-inverse operation is a remarkable advantage of the proposed converter where it avoids using high values of turns ratios of the TWCI. Through ZCS operation of the power switch and the diodes (mainly those conducting higher currents), the switching losses are minimized and the reverse recovery (RR) issues for the diodes are alleviated successfully.

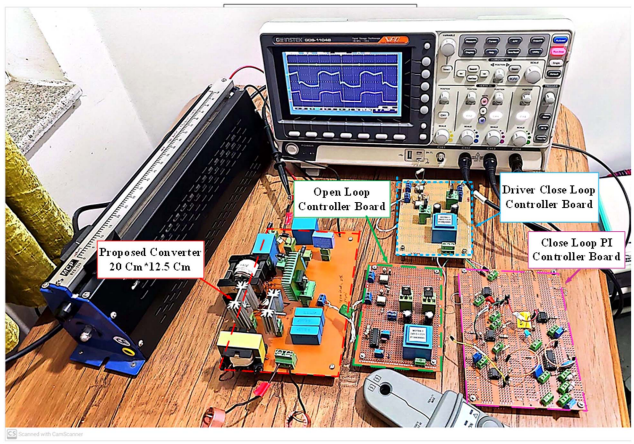


Fig. 30. Photograph of the proposed converter prototype.

Other advantages include low voltage stress across the semiconductors, low input current ripple, and common ground between input power source and load. Therefore, the proposed converter can be regarded as a suitable candidate for RES applications, such as PV and FC. Through a comprehensive comparison with similar topologies, it has been shown that the proposed converter outperforms its competitors in the critical expectable aspects. Tests conducted on a 200 W 25–400 V laboratory prototype have verified the operating principle of the proposed topology with a full-load efficiency of 94.9%. Hence, according to the proper performance of the proposed converter, this converter could be an attractive alternative for low-power dc–dc renewable energy applications. Moreover, with the help of modulation techniques, it can be used at higher powers. By modifying the input and output sides, the proposed converter can also be used in multi-input (such as three-port topologies) and multioutput converters.

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