Letters

A Hybrid Phase-Frequency Control of Dual Active Bridge Converters for Hold-Up Time Extension in More Electric Aircrafts Applications

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***Abstract*—Dual active bridge converters are extensively adopted in more electric aircrafts, wherein maintaining a sufficient hold-up time is crucial for air safety. As the current stress in conventional phase-shift controls couples with voltage gain, high-degree voltage gain occurred in the hold-up process would lead to terrible current stress higher than safe limit, which not only heightens the risk of device failure but also shortens the hold-up time due to the potential execution of protective measures. To address such issues, this letter proposes a novel hybrid phase-frequency (HPF) control method, particularly suitable for operations under low input voltage with high inductor currents. The HPF control facilitates the decoupling of the current stress from operation gain, offering advantages such as further optimized and fully regulated current stress, an extended hold-up time and enhanced operational safety. Experimental results show that current stress at full-load can be reduced 56% with HPF control, thereby extending hold-up time by 3 times. Additionally, the reduced current stress under certain power ranges contributes to improved steady-state efficiency**

***Index Terms*—Current stress, dual active bridge converter, hold-up time, phase shift and frequency hybrid control.**

I. Introduction

THE more-electric aircraft (MEA) concept represents a significant trend in contemporary aerospace engineering, focusing on reducing overall aircraft weight, operational costs, and environmental impact [1]. Leveraging its high power-density and bidirectional power flow capabilities, the dual active bridge (DAB) converter [2] emerges as a prominent solution in MEA applications [3]. A simplified dc power supply system for this application is illustrated in Fig. 1.

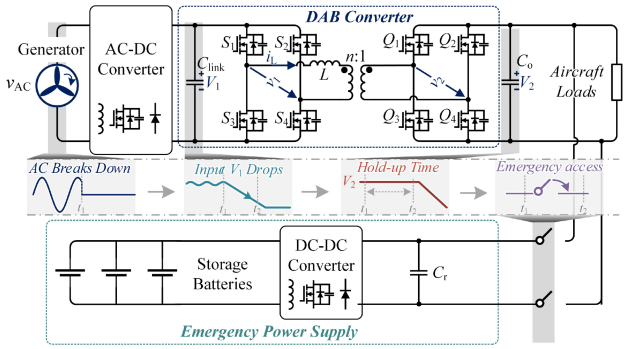

Fig. 1. Power supply architecture and the hold-up time of the MEA system.

For DAB converters, it is widely acknowledged that the converter can operate within a relatively broad voltage range, allowing for a sufficient hold-up time. However, during emergency scenarios like the hold-up process, the voltage gain of the system would inherently surpass the normal range and surge to a very high extent, causing the inductor current to exceed the safe stress limits. Therefore, protective measures may prematurely shut down the system, thereby diminishing available hold-up time.

The hold-up time is a critical requirement in MEAs. As depicted in Fig. 1, if the ac input voltage is abruptly disconnected, the output voltage needs to be sustained for several milliseconds, a period known as the hold-up time [4]. This duration is crucial for tasks such as data storage and accessing emergency power supply to ensure the uninterrupted operation of MEA systems.

Various control strategies based on the phase shift modulation scheme have been developed to optimize current stress in DAB converters, including dual phase shift (DPS) control [5], extended phase shift (EPS) control [6], and triple phase shift (TPS) control [7], where the TPS control can be recognized as the optimal control law features minimized current stress. Although optimizations have been contributed in [5], [6], and [7], the current stress in DAB converters remains coupled with transmitted power and voltage gain. Particularly under high-voltage

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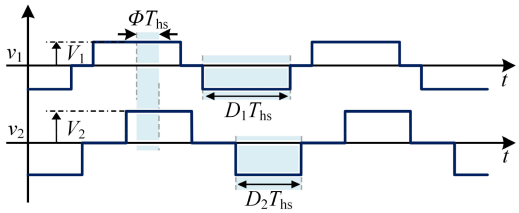

Fig. 2. Definition of phase shift angles in this letter.

gain conditions, the optimization performance of current stress becomes inadequate and the current stress cannot be actively regulated within safe limits, the issue of shortened hold-up time still cannot be addressed.

In this letter, a hybrid phase-frequency (HPF) control method is presented, specifically tailored for operations under low input voltage with high inductor currents. The key innovations of HPF control can be summarized as follows.

1) By decoupling the current stress from voltage gain and transfer power, current stress can be maintained under a wide input voltage range, leading to an enhanced duration and operation safety of hold-up process.
2) The frequency control can be seamlessly introduced to TPS and EPS modulation. During transient processes, all control variables change smoothly, preventing any occurrence of dc bias.
3) Benefiting from the low current stress characteristics of proposed control, steady state operation efficiency can be enhanced within certain power ranges.

II. Current Stress Analysis of Phase Shift Control

As shown in Fig. 1, the DAB converter comprises the input capacitor C_{link}, output capacitor C_{o}, primary/secondary switches $S_{\text{x}}/Q_{\text{x}}$, auxiliary inductance L, and transformer T. The transformer turn ratio is $n:1$ and the voltage gain ratio is defined as $M = nV_2/V_1$. The definition of phase shift angles in this letter is shown in Fig. 2, where D_1 and D_2 represent the duty cycle of v_1 and v_2, Φ represents the phase difference of the central axis in v_1 and v_2, and T_{hs} denotes the half switching cycle.

Fig. 3 illustrates the hold-up process under TPS control [7]. It is evident that during the process V_1 would fall outside the normal range, causing the DAB converter to operate at a very high voltage gain condition (M is typically designed around 0.5 to 2 to balance bidirectional operation). Consequently, the current stress exceeds the limit I_{safe}, leading to advance activations of protective measure and decreasing available hold-up time from 15.6 ms to 7.6 ms.

Theoretically, the shortened hold-up time results from the fact that $I_{\max}$ is positively rated to the voltage gain M and transmitted power P. According to phase-shift control laws in single phase-shift (SPS) [2], DPS [5], and TPS [7] controls, per unit current stress $I_{\max}*$ in all controls can be drawn in Fig. 4(a), where $I_{\max}* = I_{\max}/I_{\text{N}}, p = P/P_{\text{N}}, I_{\text{N}} = V_1/(4f_{\text{s}}L), P_{\text{N}} = nV_1V_2/(8f_{\text{s}}L)$.

It is clear that the $I_{\max}*$ in all phase-shit controls is coupled with p and M. Furthermore, although TPS control exhibits the minimum current stress, it still exceeds the $I_{\text{safe}}*$ limit across

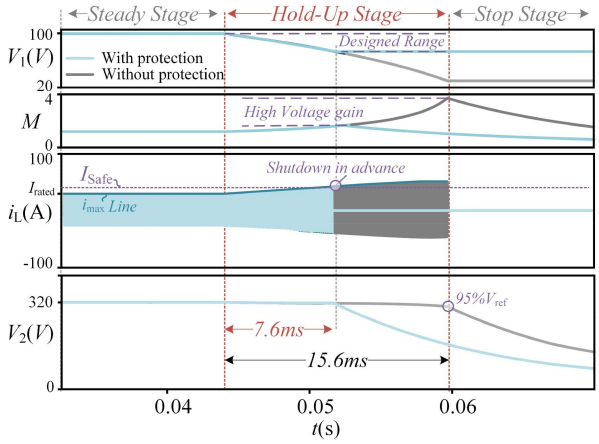

Fig. 3. Hold-up time variation due to the high current stress at full-load, where all parameters are identical to Table II. Herein, the I_{rated} represents the max inductor current at rated load, and I_{safe} denotes the max drain-source current of switches where $I_{\text{safe}} = 1.15I_{\text{rated}}$.

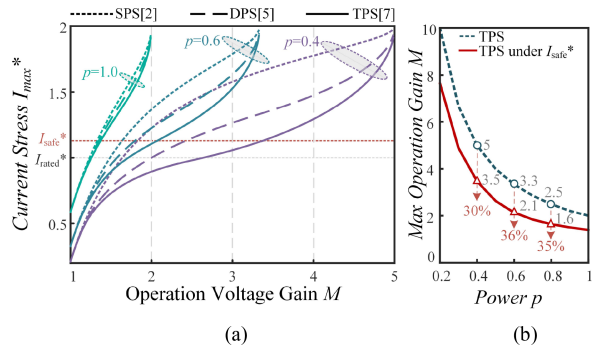

Fig. 4. Curves and effects of large current stress of DAB converters. (a) Current stress of all phase-shift controls. (b) Loss of operation gain of TPS control under the $I_{\text{safe}}*$ limit. Herein, I_{rated} is adopted as the normalization value of $I_{\max}$. Notably, the I_{rated} is typically set at 30% to 50% of I_{N} for high operational efficiency consideration, and here $I_{\text{rated}} = 0.5I_{\text{N}}$.

most power ranges, resulting in a large operation gain loss of 36% under the $I_{\text{safe}}*$ limit, as shown in Fig. 4(b).

Therefore, to extend the hold-up time of DAB converters, it is necessary to investigate how to further reduce current stress beyond phase-shift control, and sustainably regulate the stress below the limit for as long as possible.

III. Proposed HPF Control

Generally, the current stress in DAB converters can be simplified expressed as follows:

$$I_{\max} = I^*_{\max} \cdot I_{\text{N}} \tag{1}$$

where $I_{\max}*$ can be unified expressed as $f(D_1, D_2, \Phi)$, whose specific expression various with the type of phase-shift control. Meanwhile, $I_{\text{N}} = V_1/(4f_{\text{s}}L)$, indicating that current stress in any phase-shift control would be influenced by frequency f_{s}.

Fig. 5 illustrates the impact of changing frequency on regulating current stress and transfer power, where shaded areas represent the instantaneous output power, calculated as $v_2 \cdot i_{\text{L}}$.

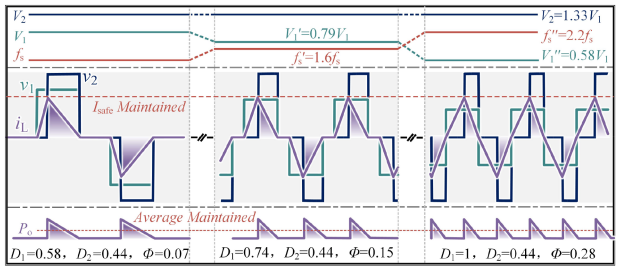

Fig. 5. Key waveforms under different phase-shift and frequency configuration.

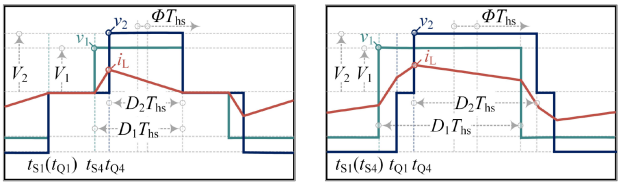

Fig. 6. Modes of TPS control. (a) M_1 under light load, where $p = 4D_2\Phi$ and $I_{max}* = 2\Phi - D_2 + D_2M$. (b) M_2 under heavy load, where $p = 1 - (2\Phi - 1)^2 - (D_2 - 1)^2$ and $I_{max}* = 2\Phi - D_2 + D_2M$.

As shown, when V_1 falls to V_1' and V_1'', current stress still can be maintained as long as the frequency is properly configured. For the transmitted power, although the shaded area shortens with the increase of f_s, according to

$$P_o = \frac{1}{T_s}\int_0^{D_2T_{hs}} v_2 i_L dt$$

average output power can be kept due to the reverse decrement of T_s. Therefore, I_{max} and P_o can be maintained simultaneously under high voltage gain by regulating the switching frequency. Combined with the following equations:

$$\begin{cases} P = f(D_1, D_2, \Phi, f_s, V_1, V_2, L) = P_o \\ I_{max} = f(D_1, D_2, \Phi, f_s, V_1, V_2, L) = I_{safe} \end{cases} \quad (2)$$

the optimal f_s in any types of phase shift control can be obtained. Herein, the TPS control with minimum current stress [7] is taken as the example for the following optimization content, whose modulation patterns are illustrated in Fig. 6.

According to the control laws in [7] and (2), the optimal f_s in M_1 mode can be obtained as follows:

$$f_s = (V_2 - V_1) P_o / \left(V_2 L I_{safe}^2\right). \quad (3)$$

Substituting the condition $V_1'' = 0.83V_1' = 0.63V_1 = 0.47V_2$ into (3), it can be observed that $f_s'' = 1.38f_s' = 2.2f_s$ holds true, proving that it is feasible to regulate frequency to maintain current stress under various voltage gain condition and constant output power requirement, especially suitable for the hold-up process.

Consequently, Fig. 7 shows the current stress under different frequency and voltage gain. As can be seen, at each voltage gain, there exists a corresponding frequency that meets $I_{max}* = I_{safe}*$. Hence, it is necessary to adjust frequency only when $I_{max}* > I_{safe}*$, and an optimal current path can be established.

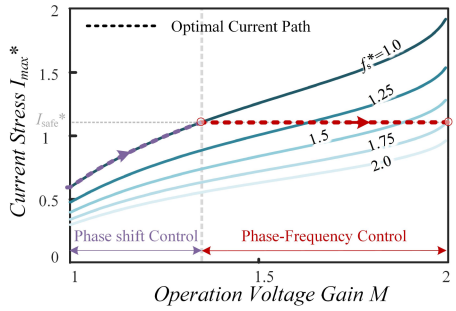

Fig. 7. $I_{max}*$ variation with per unit frequency f_s* under TPS control and $p = 1.0$.

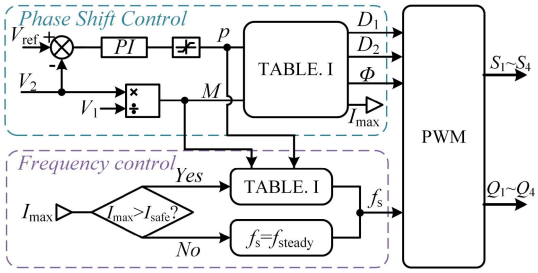

Fig. 8. Control loop of the proposed HPF control.

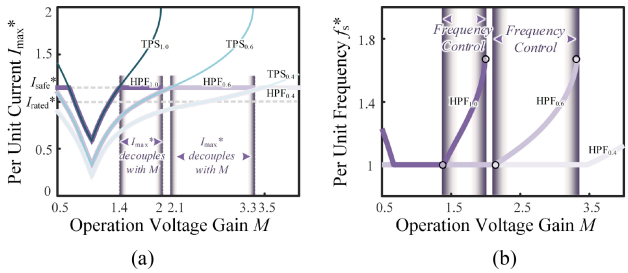

Fig. 9. Variation of $I_{max}*$ and f_s* under HPF control. (a) $I_{max}*$. (b) f_s*.

According to (2), the control law of the phase-frequency control can be obtained as listed in Table I, whose control loop is depicted in Fig. 8. In the proposed control system, the *PI* output from the voltage loop is set as the normalized power p, which is then applied to calculate the optimal phase shifts based on Table I. The calculation of the peak current I_{max} is simultaneously executed, and once $I_{max} > I_{safe}$ is detected the frequency control would be triggered. The optimal frequency value is determined by M, I_{safe} and p. If $I_{max} > I_{safe}$ is not detected, the system maintains the steady-state frequency f_{steady}. Finally, both the phase shifts and the frequency are input into the chip for pulse-width modulation (PWM) signal generation.

The current stress of the HPF control is shown in Fig. 9(a) and the variation of f_s* is illustrated in Fig. 9(b), where the subscript x of legends represents p = x. Compared to TPS control, the current stress of HPF control becomes decoupled from M when $I_{safe}* > I_{max}*$, indicating that the current stress of HPF control can be further optimized and maintained under the safe limit. Therefore, the operation gain of HPF control is extended from 1.4 to 2 under $p = 1.0$ and 2.1 to 3.3 under $p = 0.6$.

TABLE I
EXPRESSIONS OF THE PROPOSED HPF CONTROL

Mode	*Boundaries*	*Optimal Control Law*	I_{max}*
M_1	$0\le p<(2M-2)/M^2$ $p=4D_2\Phi$	$D_1=M\sqrt{\frac{p}{2(M-1)}}, D_2=\sqrt{\frac{p}{2(M-1)}}, \Phi=\frac{M-1}{2}\sqrt{\frac{p}{2(M-1)}}, f_s=\frac{V_1}{4I_{safe}L}\sqrt{2(M-1)p}$	$2\Phi-D_2+D_2M$
M_2	$(2M-2)/M^2\le p\le 1$ $p=1-(2\Phi-1)^2-(D_2-1)^2$	$D_1=1, D_2=1-(M-1)\sqrt{\frac{1-p}{(M-1)^2+1}}, \Phi=\frac{1-M}{2}\sqrt{\frac{p}{2M(1-M)}}, f_s=\frac{V_1}{4I_{safe}L}\left[M-\sqrt{(1-p)\left((M-1)^2+1\right)}\right]$	

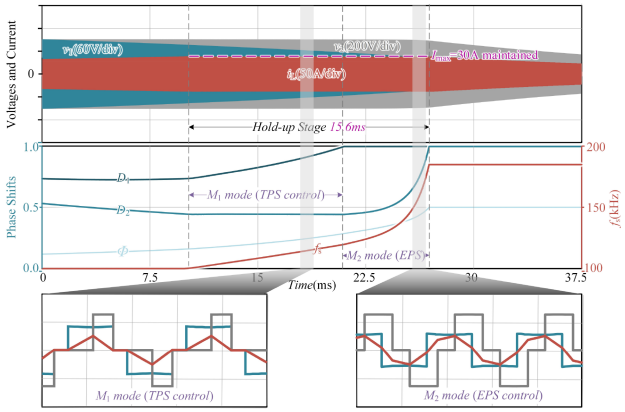

Fig. 10. Hold-up time of HPF control at full-load, where all parameters are identical to Table II.

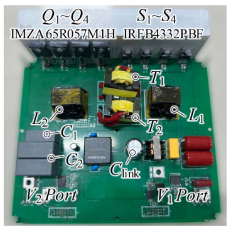

Fig. 11. Hardware prototype.

As shown in Fig. 10, compared to the TPS control, the current stress under the HPF can be maintained under the I_{safe} limit, thereby extending the operation voltage range and increasing the hold-up time from 7.6 ms to 15.6 ms. Furthermore, the frequency control can be seamlessly introduced to the TPS and EPS modulation. During transient processes, all control variables can be regulated smoothly, preventing any occurrence of dc bias issues.

IV. EXPERIMENTS

To validate the feasibility and effectiveness of the proposed HPF control, a 1 kW DAB converter is established, as shown in Fig. 11. Detailed parameters are provided in Table II. Notably, to prevent device damage in the experiment, relatively large values of max drain-source current are chosen for switches S_x ($I_D = 60A@T_J = 25\,°C$) and Q_x ($I_D = 35A@T_J = 25\,°C$). Furthermore, system control and sampling frequency is set to 10 kHz for other time-cost functions. Although this frequency is lower than 100 kHz, the maximum adjustment time difference between 10 kHz and 100 Hz is 97 μs, which is negligible as the hold-up time is usually on the level of milliseconds.

TABLE II
SYSTEM SPECIFICATIONS

Items	Value
Rated Power P_o	1k W
Input Voltage V_1	100 V
Output Voltage V_2	320 V
Rated frequency f_s	100 kHz
Transformer T	n = 1:2.6
Inductors L_1, L_2	2 μH, 13 μH
Input capacitor C_{link}	5 mF

Notably, the frequency adjustment in this work only requires an additional square root calculation, as listed in Table I, which can be quickly computed for an ARM chip with an floating point unit. Therefore, it will not be necessary to significantly upgrade the MCU at a higher cost.

A. Transient Hold-Up Process Verification

1) Full Load Verification: Fig. 12 compares the hold-up times of the TPS and HPF controls under rated power condition. In Fig. 12(a), the rated current of the TPS control at steady stage is 20 A and the safe current I_{safe} is set to 30 A. When V_1 drops, the max current rises rapidly and exceeds I_{safe} (herein, all protection measures are disabled). Therefore, the hold-up process terminates before V_2 drops, resulting in a shortened 5.9 ms hold-up time and a narrowed range [89, 100]V of V_1.

In Fig. 12(b), with HPF control, I_{max} is effectively constrained below I_{safe} throughout the entire process, and the hold-up process ends with the decline of V_2. Therefore, the hold-up time is extended from 5.9 ms to 15.5 ms, and the operation range of V_1 expands to [47, 100]V. Fig. 12(a), (b), and (c) presents detailed DAB waveforms under HPF control. During the hold-up process, the frequency adjustment is successfully executed with f_s dynamically increasing from 100 kHz to 183 kHz.

2) Half Load Verification: Fig. 13 compares the hold-up process of the two controls under $P_o = 0.5$ kW. As shown in Fig. 13(a), the transmitted power is decreased and I_{rated} is reduced to 14 A. However, I_{max} under TPS control still exceeds 30 A limitation during the process. The hold-up time of the TPS control is 13.6 ms and the operation range of V_1 is [53, 100]V.

In Fig. 13(b), the max inductor current under the HPF control is safely limited to 30 A, and the hold-up time increases from 13.6 ms to 17.6 ms. Due to the relatively small transfer power, the operation range of V_1 is significantly expanded from [53, 100]V to [20, 100]V. As shown in Fig. 13(c), (d), and (e), the frequency of HPF control is increased from 100 kHz to 172 kHz during the hold-up process, and all phase shift angles is dynamically adjusted with the drops of V_1.

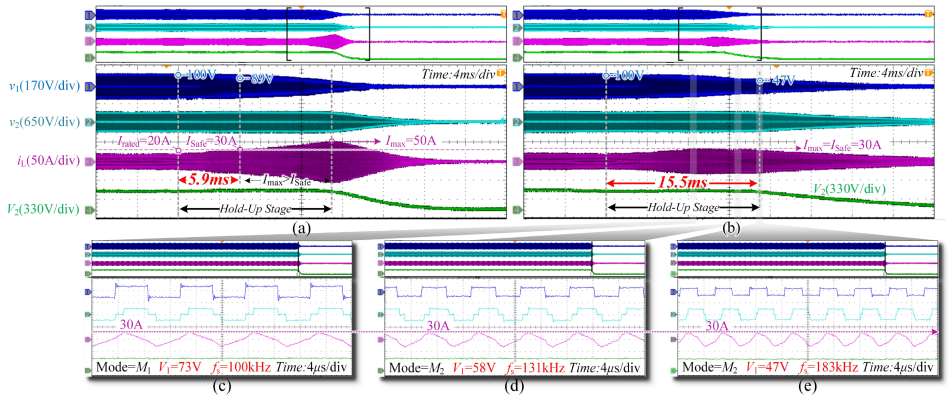

Fig. 12. Hold-up process under $P_o = 1$ kW. (a) TPS control. (b) HPF control and zoomed-in view. (c) At the beginning. (d) During the process. (e) At the end.

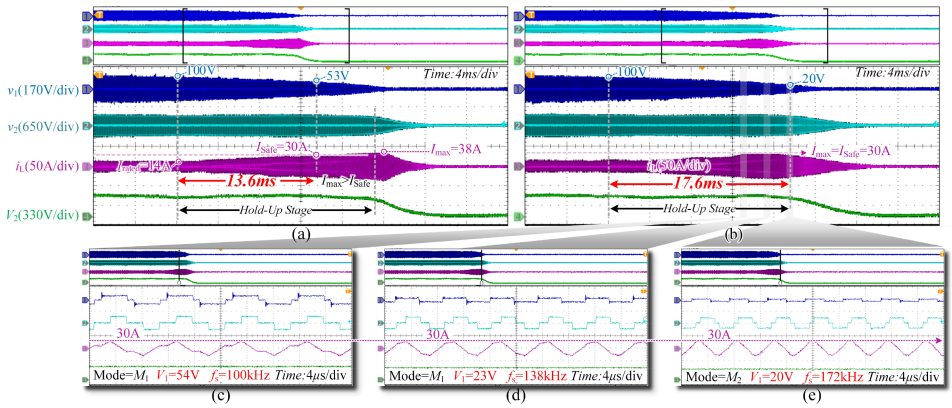

Fig. 13. Hold-up process under $P_o = 0.5$ kW. (a) TPS control. (b) HPF control and zoomed-in view. (c) At the beginning. (d) During the process. (e) At the end.

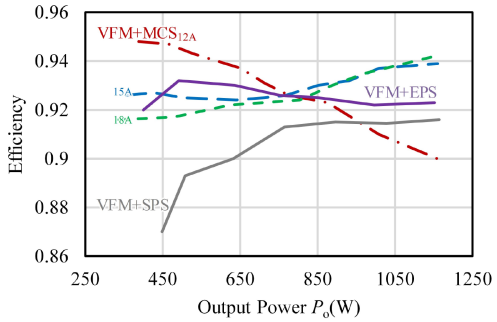

Fig. 14. Efficiency comparison of the three frequency + phase shifts control scheme under $V_1 = 100$ V, $V_2 = 320$ V.

B. Discussion of Steady State Operation Efficiency

Since a flattened current stress characteristic can be realized under wide voltage gain and power range, it is possible to adopt proposed control to optimize operational efficiency of DAB converters.

Fig. 14 compares the experimental tested efficiency of the variable frequency modulation + SPS (VFM + SPS) control for ZCS or ZVS operation [8], VFM + EPS control for extending ZVS range under partial medium load [9] and proposed VFM + multimode phase shifts (VFM + MPS) control with different limited current I_{Lim}, As can be seen, the VFM + MCS control with $I_{\mathrm{Lim}} = 12$A possess highest efficiency under light load conditions, while its advantages dimish with the increase of P_o. Under heavy load, the VFM + MCS control with $I_{\mathrm{Lim}} = 18$ A achieves the highest efficiency operation.

The reason that efficiency improvement under light load can be explained by Fig. 15. As shown, for the VFM + SPS control, a relatively high switching frequency 250 kHz is required to achieve ZCS or ZVS operation of switches, resulting in the lowest efficiency of all controls. For the VFM + MPS control with $I_{\mathrm{Lim}} = 15$ A, the operation efficiency is slightly lower than that of the VFM + EPS control due to the ZCS operation of switches. However, when I_{Lim} is decreased to 12 A, optimal efficiency of 94% can be achieved as both the peak and rms currents are reduced by 30% compared to the VFM + EPS scheme.

The steady-state waveforms under heavy load conditions of the three controls are shown in Fig. 16. To realize ZVS operation, the switching frequency of the VFM + EPS is increased to 150 kHz and VFM + SPS control is 176 kHz. For VFM + MCS control, if the optimal $I_{\mathrm{Lim}} = 12$ A under light load is still adopted under heavy load, as shown in

TABLE III
DIFFERENCES AND INNOVATIONS OF THIS WORK COMPARED TO OTHER SIMILAR CONTROLS

References	Targets	Real-time control	Hold-up time	Efficiency	Frequency control	Phase shift
Ref [8]	Efficiency	Yes	Short	Moderate	All range	SPS
Ref [9]		Yes	Short	High	Partial range	EPS
Ref [10]		No	Very short	Poor	Partial range	SPS
Ref [11]		Yes	Short	High	Partial range	TPS
Ref [12]		No	Very Short	Very High	All range	TPS
Proposed	Hold-up process	Yes	Long	High	All range	TPS+EPS

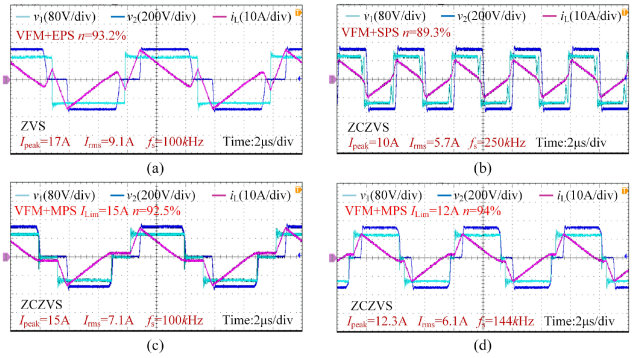

Fig. 15. Steady operation waveforms under $V_1 = 100$ V, $V_2 = 320$ V, $P_o = 500$ W light load condition. (a) VFM + EPS control. (b) VFM + SPS control. (c) VFM + MPS control under $I_{Lim} = 15$ A. (d) VFM + MPS control under $I_{Lim} = 12$ A.

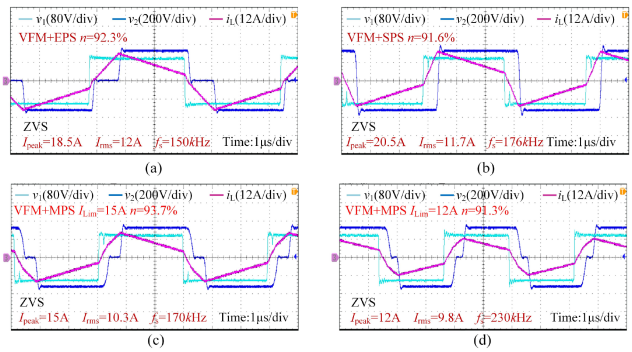

Fig. 16. Steady operation waveforms under $V_1 = 100$ V, $V_2 = 320$ V, $P_o = 1000$ W heavy load condition. (a) VFM + EPS control. (b) VFM + SPS control. (c) VFM + MPS control under $I_{Lim} = 15$ A. (d) VFM + MPS control under $I_{Lim} = 12$ A.

Fig. 16(d), the switching frequency would be greatly increased to 230 kHz, resulting in too much switching loss and a lower operation efficiency. Therefore, maintaining strict current stress under heavy load is inefficient, and the limitation should be appropriately relaxed. As shown in Fig. 16(c), if the I_{Lim} is relaxed to 15 A and system frequency would reduce to 170 kHz. Benefiting from a lower peak current (15 A) and rms current (10.3 A) compared to VFM + EPS control, the VFM + MPS control achieves the highest efficiency of 93.7%.

Therefore, since the proposed control can maintain a flattened current stress characteristic over a wide voltage gain and power range, steady state operation efficiency can be enhanced by proposed control method as the I_{Lim} is reasonably configured.

Finally, the differences and innovations of this work compared to other phase shift + frequency modulation controls are summarized in Table III. As can be seen, the proposed control incorporates frequency adjustment across the entire power range and various phase-shift control modes, providing the longest hold-up time. Additionally, it achieves higher operational efficiency within certain power ranges.

V. CONCLUSION

In this letter, a hybrid phase-frequency control of the DAB converter is proposed to extend the time length and enhance operation safety of the hold-up process in EMA system.

First, the current stress characteristics of the conventional phase shift controls are analyzed. It was found that the current stress generated in phase shift control is coupled with voltage gain, leading to terrible current stress higher than safe limit under high-voltage gain conditions, which not only heightens the risk of device failure but also shortens the hold-up time. To address this issue, the impact of switching frequency on current stress is investigated, showing that current stress can be decoupled from voltage gain by regulating the frequency. Consequently, through the proposed HPF control, current stress of DAB converters can be further optimized and maintained under safe limit throughout the entire process.

Experimental results show that the hold-up time of HPF control can be extended by 3 times compared to conventional TPS control, and current stress is decreased 67% at the full-load. Due to these low current stress characteristics, operation efficiency can be improved by HPF control with reasonable current stress configuration.

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