A Closed-Loop Soft Startup Strategy to Suppress Inrush Current for Full-Bridge Modular Multilevel Converters

Debin Zhang, Deshang Sha, *Senior Member, IEEE*, Congzhe Gao, *Member, IEEE*, Xiao Liu, Hanwen Long, Guangshan Tang, Yining Zhao, and Yang Gao

***Abstract*—Aim to charge all submodule (SM) capacitors of the full-bridge modular multilevel converter (FB-MMC) to their nominal voltage values smoothly and effectively, this article proposes a closed-loop soft startup strategy by utilizing the negative output voltage of FB-SM, which completely suppresses the potential inrush currents at the startup process. Based on the analysis of the precharging process of FB-MMC with load, when bypassing the current limiting resistors, the inrush currents are induced owing to the presence of load. To solve this issue, an improved startup strategy is further proposed by intentionally controlling the dc voltage to zero. With this strategy, the main ac contactor is closed with zero current, which is beneficial for extending the service life of mechanical switches. Besides, the overall control system is integrated and optimized because separately designed startup control is not required, thereby reducing the computational burden of digital controllers. Moreover, the SM capacitors can be charged rapidly by a ramp shaped charging current, and equal charging of all SMs during startup process can be guaranteed with the voltage balancing control algorithm. Simulation and experimental results of three-phase FB-MMC rectifier interfaced with grid and 5 kV dc are provided to validate the feasibility and effectiveness of the proposed startup strategy.**

***Index Terms*—Inrush current, modular multilevel converter, precharge, soft-start strategy.**

I. Introduction

In RECENT years, the modular multilevel converters (MMCs) have received increasing attention due to their attractive characteristics, such as flexible modularity and scalability, low voltage stress in power semiconductor devices, high-quality output voltage waveforms, enhanced reliability with redundant cells, and so on. With these distinctive advantages, they have been applied in many fields, including high-voltage direct current (HVDC) transmission systems [1], [2], [3], ac motor drives [4], [5], and static synchronous compensators (STATCOM) [6], [7], [8].

The MMCs benefit from their modular structure, but control challenges arise because of increased complexity on the power circuit, with startup control being one of the technical challenges worth studying. For MMCs, capacitors with zero initial voltage are distributed in each submodule (SM) and should be smoothly charged to nominal voltage value before normal operation. The precharging process is more complicated compared to other voltage source converters with concentrated capacitors, and serious inrush currents will be generated due to inappropriate startup strategies. In addition, the capacitors of all SMs should be charged equally during the startup stage; otherwise it will threaten the stable operation of the converter. Therefore, various startup methods have been proposed for MMCs, which can be roughly classified into closed-loop and open-loop strategies.

Adding auxiliary dc power sources is one of the conventional open-loop ways to precharge capacitors [9], [10], [11]. In Li and Zhao's [9] work, an auxiliary voltage source with the nominal voltage of capacitors is connected to the dc bus of the MMC, and then SMs in each phase are charged one by one within the same set time. To accelerate the startup process, four antiparalleled thyristors are added in each SM so that all the capacitors can be charged simultaneously in Li and Zhao's [9] work. In Tian et al.'s [11] work, by utilizing the inherent arm inductors, SM capacitors and power devices of MMC to form a boost circuit, a cost-effective precharge method can be implemented with a dc source whose voltage is lower than the nominal voltage of capacitors. Although these methods are straightforward, they are more complex in terms of control and require higher equipment costs. Furthermore, higher isolation level between the additional dc power supply and MMC is required in high-voltage applications. To get rid of auxiliary power supply, dynamically adjusting the number of inserted SMs being charged during the precharging process is another commonly used method. The method of adjusting the number of blocked and bypassed SMs based on the capacitor voltage sorting algorithm is proposed in Zhang et al.'s [12] work, which is applicable to various SMs. Besides, other novel open-loop startup methods have been proposed for MMCs [13], [14]. In Ghoneim and Aziz's [13]

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Debin Zhang, Deshang Sha, Congzhe Gao, Xiao Liu, Hanwen Long, Guangshan Tang, and Yining Zhao are with the Advanced Power Conversion Center, School of Automation, Beijing Institute of Technology, Beijing 100081, China (e-mail: 3120205481@bit.edu.cn; shadeshang@bit.edu.cn; gaocongzhe@bit.edu.cn; 3220220887@bit.edu.cn; 3120210971@bit.edu.cn; 3220210922@bit.edu.cn; 3220220888@bit.edu.cn).

Yang Gao is with the Global Energy Interconnection Research Institute Company Ltd., Beijing 100081, China (e-mail: gaoyang@geiri.sgcc.com.cn).

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work, the capacitance of each SM is split into small capacitors and independently charged to avoid inrush currents. The boost circuit formed inside MMC is used to absorb charging energy from the ac grid in Liu et al.'s [14] work. However, the strategies mentioned previously are separated from the control method at normal operation, which increases the burden on the digital controllers and reduces the reliability of the system. In addition, the charging current of most proposed open-loop methods usually decays exponentially, resulting in slow startup speed. Moreover, the open-loop method is parameter sensitive and has poor disturbance resistance, thus threatening the stability of the system. Consequently, different closed-loop strategies have been introduced [15], [16], [17], [18].

A constant charging current can be maintained during the startup process with the proposed method in Li et al.'s [15] work. However, separately designed control strategies are still required. In Shi et al.'s [16] work, the resonance between the arm inductor and the SM capacitors is identified to constrain the bandwidth of the capacitor voltage charging loop, and a capacitor voltage feedforward control is proposed to address this issue. A unified startup strategy based on deadbeat predictive current control is proposed, which does not require conventional controller design and parameter tuning in Wang et al.'s [17] work. In Lu et al.'s [18] work, the SM capacitors of cascaded H-bridge STATCOM are charged to their nominal value with current limiting resistors, and the resistors needs to be carefully designed considering power consumption. The majority of the startup strategies mentioned previously are based on the half-bridge MMC (HB-MMC). Startup procedures for specific topologies are also discussed, such as flying-capacitor MMC (FC-MMC), MMC with three-level flying capacitor submodules (3LFC-MMC), MMC with clamp double SMs and hybrid MMC [19], [20], [21], [22]. The FC-MMC is successfully used in medium voltage motor drive because the voltage fluctuation of SM capacitors is effectively suppressed under low-/zero-speed rated-torque condition. However, additional bypass switch and soft-start resistor are required to charge the SM capacitors and the flying capacitor to their nominal voltages, and the oscillation between the flying capacitor and inner inductors should be considered [19]. For 3LFC-MMC, smaller voltage ripple and circulating current are realized compared with the HB-MMC. However, the construction of the 3LFC-SM is more complex, and two floating capacitors should be charged to different nominal voltages simultaneously [20]. In addition, it cannot block the dc-side fault current. In Xue et al.'s [21] work, all of the CD-SMs are divided into several groups and then charged group by group until the rated capacitor voltage value is reached. Each CD-SM is composed of two HB-SMs, two diodes and a single IGBT device. Due to this structure, positive or negative output voltage levels can be generated, depending on the current direction. Therefore, dc short-circuit current can be blocked. Similar to Xue et al.'s [21] work, the HB-SMs and full-bridge submodules (FB-SMs) of the hybrid MMC in each arm are arranged into several groups, respectively, and then charged sequentially [22]. Compared with FB-MMC, the costs and losses of the hybrid MMC are reduced, while maintaining dc fault blocking capability. However, the complexity of the algorithm for capacitor voltages balancing is increased due to the different charging and discharging characteristics of the FB-SMs and HB-SMs [23], [24]. Hence, FB-MMC is still popular despite requiring more devices compared to hybrid MMC. However, the ability of FB-MMC to output negative voltage levels has not been fully explored during the startup process. In HVDC systems, MMC usually starts almost without load. However, before mass production of MMC converters, the factory acceptance testing of single MMC should be carried out, with a crucial part being the testing of active power transmission capacity. Testing with resistive load is a commonly chosen low-cost solution because the high-voltage dc sources are not required. To eliminate very expensive and high-voltage dc contactors, startup with load is a common solution. Therefore, a constant resistor load is used to explain the startup process in this article, but the behavior of FB-MMC in this situation has not been thoroughly investigated yet.

In this article, a flexible and effective closed-loop soft startup strategy for FB-MMC is proposed, and inrush currents can be completely suppressed at the startup process. Besides, a seamless transition to normal operation can be fulfilled without changing the control algorithm, thus the complexity of overall control system is reduced. Moreover, the operating stages of the precharging process with load are analyzed in detail, and a mathematical model is obtained to analyze the factors that affect the steady-state voltage of the SM capacitors. By utilizing the negative voltage levels of the FB-SM, the inrush current can be suppressed at the start of normal operation. Considering the effect of load, an improved startup strategy is further proposed to eliminate the inrush current when bypassing the current limiting resistors. Furthermore, the effectiveness of the voltage balancing algorithm is verified by analyzing the different operating modes of the FB-SM, and the capacitor voltage of the SMs can be well balanced experimentally with the proposed modulation.

The rest of this article is organized as follows. In Section II, the precharging process of FB-MMC is explained, including the analysis of the operating stages and the derivation of equivalent circuits and mathematical model. Then, based on operating principles of MMC, a closed-loop soft startup modulation for eliminating inrush current is proposed in Section III. Next, simulation and experimental results are shown in the Section IV to validate the theoretical analysis. Subsequently, discussion and comparison of different startup strategies are presented in Section V. Finally, Section VI concludes this article.

II. Precharging Process of Full-Bridge Modular Multilevel Converter (FB-MMC)

A. Operating Stages Analysis

The topology of the proposed FB-MMC is shown in Fig. 1. The MMC consists of three phases, where each phase is composed of two arms named the upper arm and the lower arm, respectively. N nominally identical FB-SMs ($\mathrm{SM}_{xyz}, x = a, b,$ or $c, y = u, l, z = 1, 2, 3...N$), arm inductor L, and its equivalent series resistance (ESR) R_L are connected in series to make up one arm. Each SM contains four IGBTs

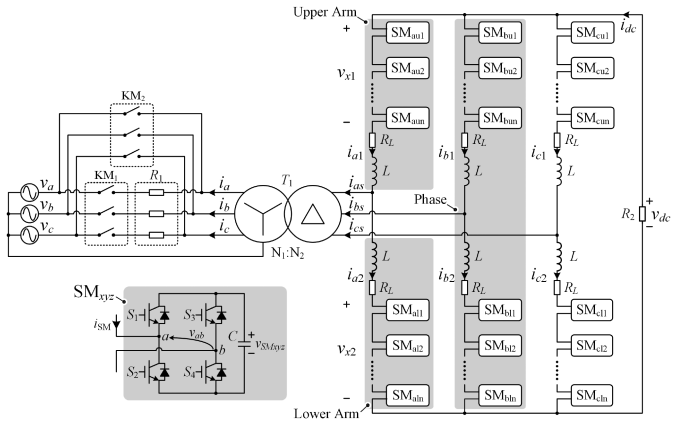

Fig. 1. Full-bridge modular multilevel converter.

($S_1, S_2, S_3,$ and S_4) and a dc storage capacitor C. $v_{\mathrm{SM}xyz}$ is the capacitor voltage of the corresponding SM. T_1 is a star-delta ($Yd11$) connected isolated power transformer, and $N_1 : N_2$ is the voltage ratio between the primary side and the secondary side. i_x and i_{xs} ($x = a, b,$ or c) are the currents of the primary and secondary sides of the transformer, respectively. v_x ($x = a, b,$ or c) represent the phase voltages of the power grid. i_{x1} and i_{x2} ($x = a, b,$ or c) denote the currents of the upper and lower arms, respectively. v_{x1} and v_{x2} ($x = a, b,$ or c) are the voltages of the upper and lower arms, respectively. v_{dc} and i_{dc} are the dc voltage and current, respectively, and V_{dc} is dc component of dc-link voltage. R_2 is the load resistor. The ac contactors KM_1, KM_2 and current limiting resistor R_1 form the precharging circuit of MMC, and KM_2 is regarded as the main ac contactor.

The startup strategy of MMC can be divided into the following three steps.

Step 1: KM_1 is closed, and S_4 of all SMs is turned ON. The capacitors of the SMs are charged with the current limiting resistor R_1.

Step 2: R_1 and KM_1 are bypassed by KM_2, and the voltage of capacitors in the SMs increases to $\frac{\sqrt{3}N_2V_m}{N_1N}$, where V_m is the amplitude of the grid phase voltage.

Step 3: All gate drive signals are activated, and MMC naturally turns into normal operation with the proposed soft startup method.

It should be noted that the inrush current will be introduced at the beginning of step 2 due to the voltage difference between the secondary side of transformer and the valve side. Consequently, it is necessary to carefully analyze the precharging process with the load. Owing to the alternating symmetrical characteristics of three-phase grid voltage, only the operating status within one-third of the line cycle is analyzed, and six stages can be distinguished, as shown in Fig. 2. The corresponding typical voltage and current waveforms are shown in Fig. 3. N series connected SMs can be equivalent to one SM with an equivalent capacity value of $\frac{C}{N}$, and the voltage applied to the equivalent capacitor is $v_{\mathrm{SM}xy}(x = u$ or $l, y = a, b,$ or $c)$. The four IGBTs of the equivalent SM are also marked. The equivalent phase voltage of secondary side is $v_{xs}(x = a, b,$ or $c)$.

Stage 1 ($t_0 \sim t_1$): Prior to t_0, i_{a1}, i_{a2}, and i_{c2} are equal to zero. After t_0, the body diodes of S_{2au}, S_{1al}, and S_{4al} begin to conduct. i_{a1}, i_{a2}, and i_{b2} begin to increase, while i_{b1} and i_{c1} are decreasing. i_{dc} flows through the lower arm of phase b and then returns to the grid. During this stage, the capacitors of the upper arm of phase b and the lower arm of phase a are charged. At the end of this stage, i_{b1} is equal to zero.

Stage 2 ($t_1 \sim t_2$): In this stage, i_{c1} continues to decrease, and only the capacitors of the lower arm of phase a are charged. At the end of this stage, i_{c1} is equal to zero.

Stage 3 ($t_2 \sim t_3$): Because $v_{as} - v_{cs} < v_{\mathrm{SM}cu}$, the capacitors of the upper arm of phase c cannot be charged. Therefore, only the capacitors of the lower arm of phase a are charged at this stage. i_{dc} is equal to i_{a1}.

Stage 4 ($t_3 \sim t_4$): After t_3, the body diodes of S_{1cu}, S_{4cu}, and S_{2cl} begin to conduct. i_{a1}, i_{c1}, and i_{c2} begin to increase, while i_{a2} and i_{b2} are decreasing. During this stage, The capacitors of the lower arm of phase a and the upper arm of phase c are charged. At the end of this stage, i_{a2} is equal to zero.

Stage 5 ($t_4 \sim t_5$): During this stage, i_{b2} continues to decrease, and the upper arm of phase c are charged. At the end of this stage, i_{b2} is equal to zero.

Stage 6 ($t_5 \sim t_6$): Because $v_{bs} - v_{cs} < v_{\mathrm{SM}bl}$, the capacitors of the lower arm of phase b cannot be charged. Therefore, only the capacitors of the upper arm of phase c are charged at this stage. i_{dc} flows through the lower arm of phase c and then returns to the grid, and i_{dc} is equal to i_{c2}.

B. Equivalent Circuits and Mathematical Model

Based on the previous analysis, the precharging process of MMC can be simplified as an RLC equivalent circuit, as shown in Fig. 4. According to Fig. 3(b), the SM capacitors of each arm are alternately charged, and it can be considered that two equivalent capacitors (i.e., $\frac{2C}{N}$) are charged every one-third of the line cycle. Therefore, the equivalent capacitance of the simplified equivalent circuit is $\frac{6C}{N}$. Based on the charging loops shown in Fig. 2, the equivalent resistance R_{eq} and inductance L_{eq} are $\frac{2R_1N_2^2}{N_1^2} + 2R_L$ and $2L$, respectively, and the equivalent dc source V_{eq} is $\frac{\sqrt{3}V_mN_2}{N_1}$. The influence of equivalent inductance L_{eq} on the simplified circuit is neglected due to affect that the excitation is a dc source V_{eq}. Then, the expression of capacitor voltage considering the load can be deduced based on Kirchhoff's voltage law

$$v_2(t) = \frac{V_{\mathrm{eq}}R_2}{R_{\mathrm{eq}} + R_2}\left(1 - e^{-\frac{t}{(R_{\mathrm{eq}}//R_2)C_{\mathrm{eq}}}}\right). \quad (1)$$

The time constant τ is equal to $(R_{\mathrm{eq}}//R_2)C_{\mathrm{eq}}$, and the settling time t_s is defined as four times the time constant (i.e., $t_s = 4\tau$). It can be observed that the settling time decreases with increasing load. Fig. 5(a) shows the steady-state voltage values at different R_1 and R_2, where the experimental results at rated power ($R_2 = 1.43\,k\Omega$) are also presented to verify the theoretical analysis. It can be seen that the steady-state voltage value is inversely proportional to the current limiting resistance

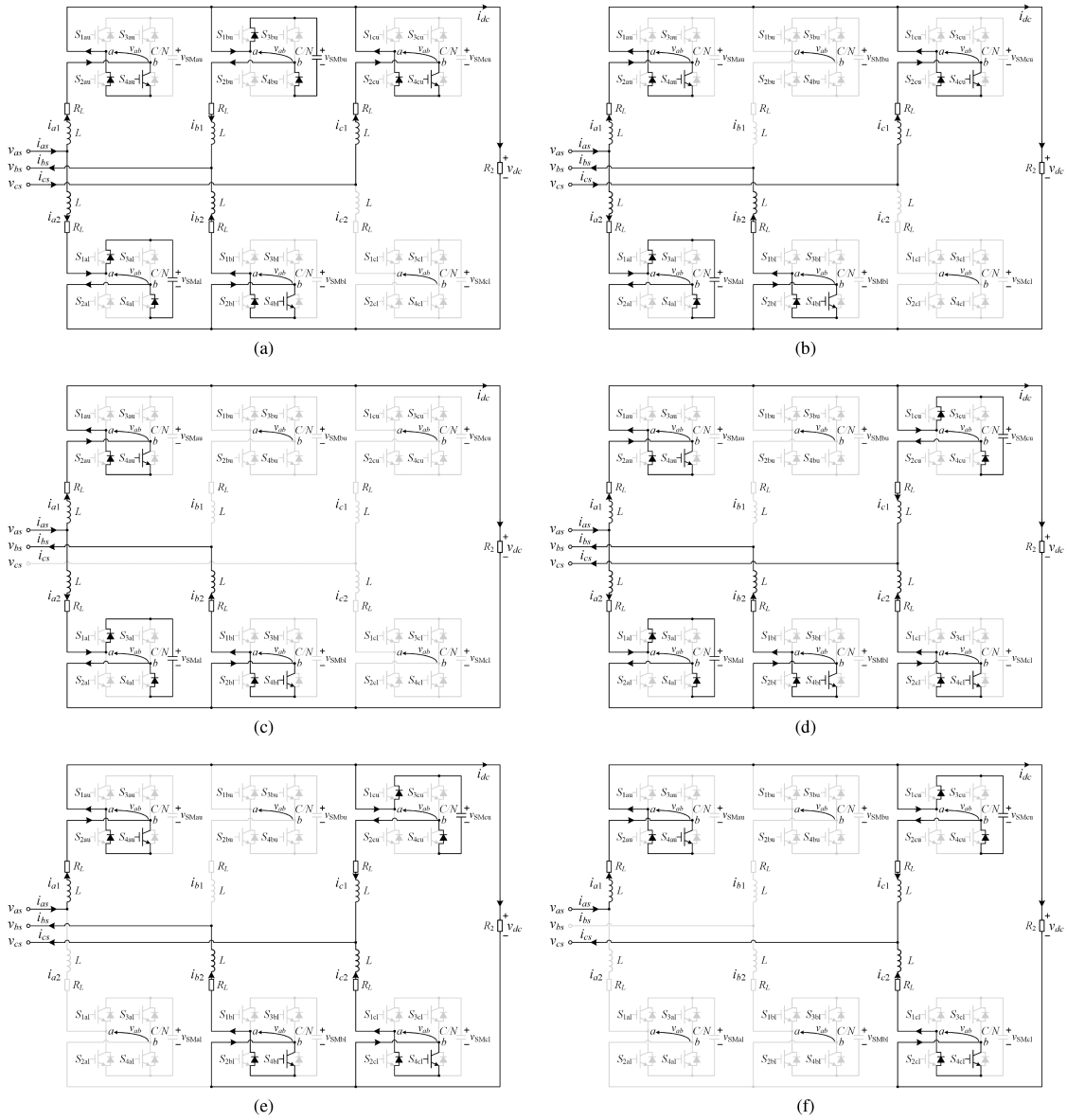

Fig. 2. Operating stages of FB-MMC during precharging process. (a) Stage 1 : $t_0 \sim t_1$. (b) Stage 2 : $t_1 \sim t_2$. (c) Stage 3 : $t_2 \sim t_3$. (d) Stage 4 : $t_3 \sim t_4$. (e) Stage 5 : $t_4 \sim t_5$. (f) Stage 6 : $t_5 \sim t_6$.

and load. At rated load, the steady-state voltage at $R_1 = 25\,\Omega$ is only 0.43 times the amplitude of line voltage of secondary side. This will cause serious inrush current at the beginning of step 2, thereby damaging the power semiconductor devices. In addition, simulations and experimental comparisons of the inrush currents for different values of R_1 are shown in Fig. 5(b). As can be seen, severe inrush current will also be generated at the start point of step 1 because of an excessively small R_1. Hence, the value of R_1 needs to be designed with tradeoff.

III. Proposed Soft Startup Strategy

A. Basic Operating Principles of MMC

Assuming a symmetrical three-phase ac system, the mathematical expressions for the internal dynamics of the FB-MMC are given by

$$\begin{cases} \frac{L}{2}\frac{di_{xs}}{dt} + \frac{R_L}{2} i_{xs} = v_{\text{diff}x} - v_{xs} \\ L\frac{di_{\text{cir}x}}{dt} + R_L i_{\text{cir}x} = \frac{V_{\text{dc}}}{2} - v_{\text{com}x} \end{cases} \tag{2}$$

where common mode voltage $v_{\text{com}x}$, differential mode voltage $v_{\text{diff}x}$, and circulating current $i_{\text{cir}x}$ ($x = a, b,$ or c) are written as

$$\begin{cases} v_{\text{com}x} = \frac{1}{2}(v_{x2} + v_{x1}) \\ v_{\text{diff}x} = \frac{1}{2}(v_{x2} - v_{x1}) \\ i_{\text{cir}x} = \frac{1}{2}(i_{x1} + i_{x2}). \end{cases} \tag{3}$$

According to (2) and (3), the ac current i_{xs} can be controlled directly by regulating the differential mode voltage $v_{\text{diff}x}$, which is regard as the ac output voltage of the MMC, and the circulating currents $i_{\text{cir}x}$ can be suppressed by adjusting the common mode voltage $v_{\text{com}x}$ without affecting the ac-side dynamics.

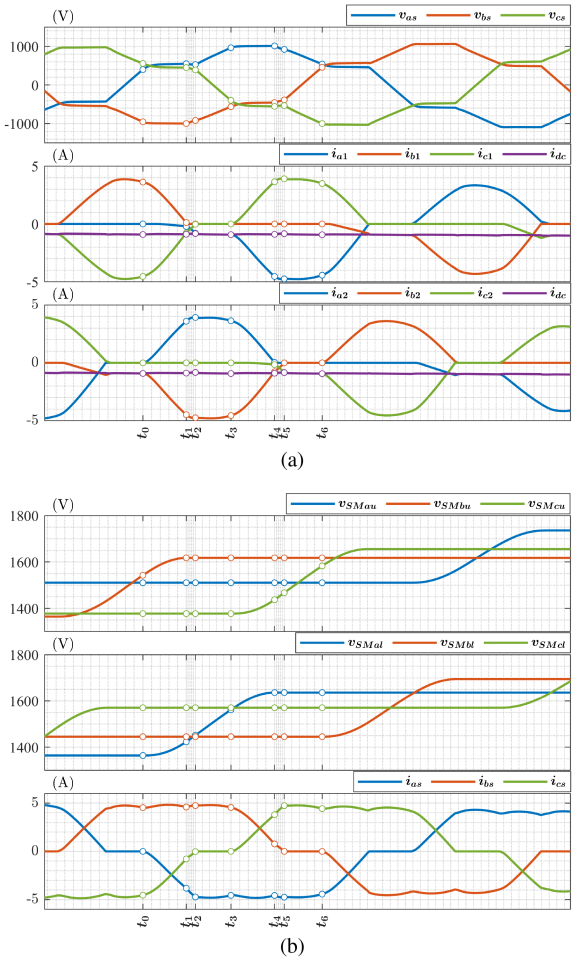

Fig. 3. Typical voltage and current waveforms of FB-MMC during precharging process. (a) Equivalent phase voltages of secondary side v_{xs}, upper arm currents i_{x1}, lower arm currents i_{x2} and DC current i_{dc}. (b) Voltages of the capacitors on the equivalent SMs $v_{\mathrm{SM}xy}$ and line currents of secondary side i_{xs}.

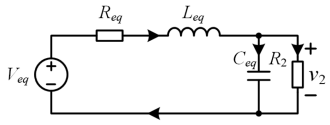

Fig. 4. Simplified equivalent circuit.

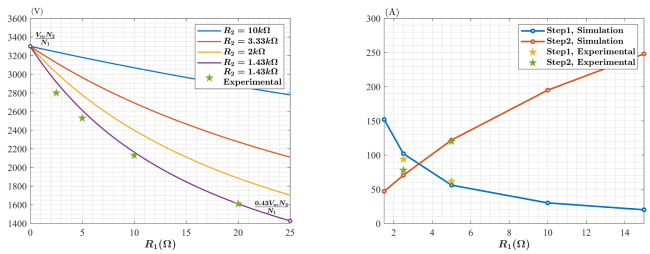

Fig. 5. (a) Steady-state voltage at different R_1 and R_2. (b) Inrush currents at different R_1.

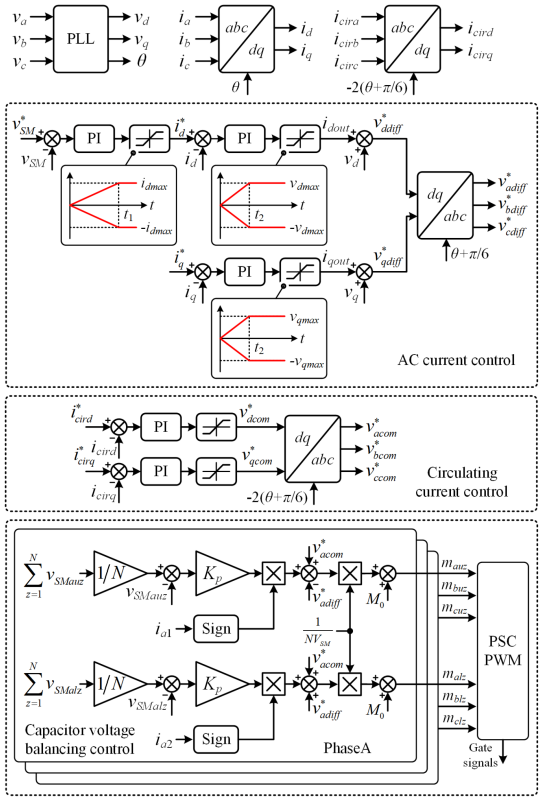

Fig. 6. Overall closed-loop implementation of FB-MMC.

B. Closed-Loop Modulation for Eliminating Inrush Current

As illustrated in Fig. 6, the overall closed-loop modulation of FB-MMC is composed of ac current control, circulating current suppression (CCS), and capacitor voltage balancing control. The CCS method proposed in Tu et al.'s [25] work is adopted in this article. First of all, the phase angle θ of the grid voltage can be tracked through a phase-locked loop, and the dq components of the negative-sequence double-frequency circulating current are calculated by a negative-sequence dq transformation, where $\frac{\pi}{6}$ should be added to θ to compensate for the phase difference between the primary and secondary sides of the isolated transformer. After that, the proportional–integral (PI) regulators are implemented to suppress the dq components to zero, and the control signals (i.e., $v^*_{d\mathrm{com}}$ and $v^*_{q\mathrm{com}}$) are obtained. Finally, the common mode voltage references of the three phases (i.e., $v^*_{x\mathrm{com}}, x = a, b, \text{or } c$) are generated by dq inverse transformation.

The phase-shifted carrier-based pulse width modulation (PSC-PWM) method is applied to generate the gate signals of SMs. Neglecting the voltage drop across the arm inductors, the reference voltages of the upper and lower arms can be derived from (2) and (3) and are represented as

$$\begin{cases} v_{x1} = \dfrac{V_{\mathrm{dc}}}{2} - v_{xs} = \dfrac{V_{\mathrm{dc}}}{2} - \dfrac{V_m N_2}{N_1}\cos\left(\omega t + \dfrac{\pi}{6} + \varphi_x\right) \\ v_{x2} = \dfrac{V_{\mathrm{dc}}}{2} + v_{xs} = \dfrac{V_{\mathrm{dc}}}{2} + \dfrac{V_m N_2}{N_1}\cos\left(\omega t + \dfrac{\pi}{6} + \varphi_x\right) \end{cases} \tag{4}$$

where ω is the grid frequency, and φ_x is the phase shift between the three phases (i.e., $\varphi_x = \{0, \frac{-2\pi}{3}, \frac{2\pi}{3}\}$ for $x = \{a, b, c\}$). Then, the modulation signals of SMs in the upper and lower

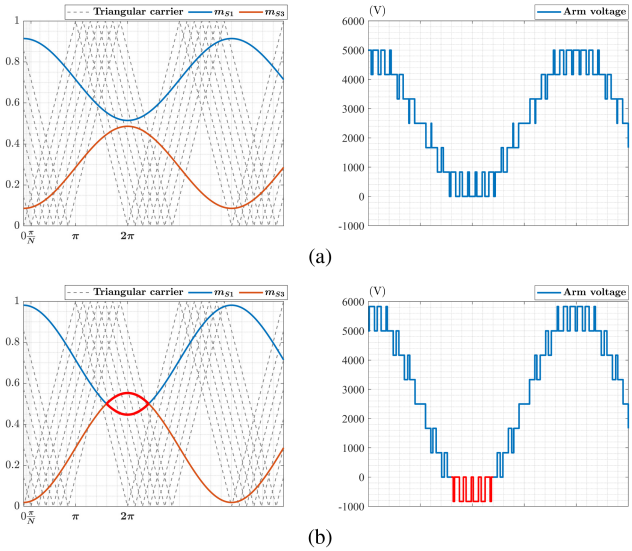

Fig. 7. Triangular carriers, modulation waves and corresponding arm voltage. (a) Conventional PSC-PWM. (b) Modified PSC-PWM.

arms are given by

$$\begin{cases} m_{x1} = \frac{v_{x1}}{NV_{\rm sm}} = M_0 - M_1 \cos\left(\omega t + \frac{\pi}{6} + \varphi_x\right) \\ m_{x2} = \frac{v_{x1}}{NV_{\rm sm}} = M_0 + M_1 \cos\left(\omega t + \frac{\pi}{6} + \varphi_x\right) \end{cases} \tag{5}$$

where M_0 is the dc modulation component, and M_1 is the amplitude of the fundamental modulation component, which are defined as

$$\begin{cases} M_0 = \frac{V_{\rm dc}}{2NV_{\rm sm}} \\ M_1 = \frac{V_m N_2}{NN_1 V_{\rm sm}} \end{cases} \tag{6}$$

where $V_{\rm sm}$ is the average capacitor voltage of SM, and it is controlled to be $\frac{V_{\rm dc}}{N-N_r}$ considering N_r hot-reserved SMs. Based on (6), the dc modulation component M_0 can be derived as

$$M_0 = \frac{N - N_r}{2N}. \tag{7}$$

Taking the SMs of upper arms as an example, neglecting the adjustment for voltage balancing control, the modulation signals of S_1 and S_3 can be expressed as

$$\begin{cases} m_{S1} = \frac{1}{2} + \frac{M_0}{2} - \frac{M_1}{2} \cos\left(\omega t + \frac{\pi}{6} + \varphi_x\right) \\ m_{S3} = \frac{1}{2} - \frac{M_0}{2} + \frac{M_1}{2} \cos\left(\omega t + \frac{\pi}{6} + \varphi_x\right). \end{cases} \tag{8}$$

The gate signals of S_1 and S_2 are complementary, and the same applies to S_3 and S_4. The triangular carriers, modulation waves and corresponding arm voltages are demonstrated in Fig. 7(a). The N triangular carriers of each SM in an arm are phase shifted by $\frac{\pi}{N}$ incrementally to realize best harmonic cancellation, and the displacement angle between the upper arm and the lower arm carriers is designed to be $\frac{\pi}{2N}$ for the ac output voltage harmonics minimization [26], [27], [28].

In terms of the ac current control, the classic *dq*-frame-based current control is utilized. According to (2), ac current is controllable only if there is enough margin in the ac output voltage of MMC to against grid voltage. For conventional PSC-PWM

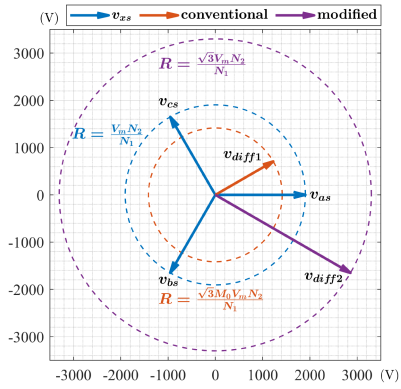

Fig. 8. AC output voltage vector of FB-MMC with different PSC-PWMs.

[shown in Fig. 7(a)], the FB-MMC is operated similar to an HB-MMC. The modulation waves m_{S1} and m_{S3} never cross each other, so there are only zero voltage and positive voltage levels employing this method, leading to limited ac output voltage of MMC. On the basis of the above-mentioned analysis, the conventional ac output voltage vector $v_{\rm diff1}$ and the grid voltage vector of secondary side v_{xs} at the start of normal operation are illustrated in Fig. 8. As observed from Fig. 8, uncontrolled startup inrush current will be generated due to insufficient ac output voltage vector amplitude, which cannot be suppressed until the capacitor voltage rises to a certain value. However, the attractive ability of the FB-SM to output negative voltage levels has been successfully applied in dc fault blocking, which can also be utilized to suppress inrush current with modified PSC-PWM [shown in Fig. 7(b)]. In Fig. 7(b), negative voltage levels are generated in the area where modulation waves intersect, which is highlighted in red, and thus the output voltage range is extended by the modified PSC-PWM. Furthermore, the range of ac output voltage vector adopting the modified PSC-PWM $v_{\rm diff2}$ is also shown in Fig. 8. It can be seen that the ac output voltage range is expanded $\frac{1}{M_0}$ times compared to conventional PSC-PWM.

The control of the sum of all capacitor voltages serves as the outer loop, Its reference and feedback are expressed as

$$\begin{cases} v^*_{\rm SM} = \frac{6NV_{\rm dc}}{N-N_r} \\ v_{\rm SM} = \sum_{x=a,b,c} \sum_{y=u,l} \sum_{z=1}^{N} v_{{\rm SM}xyz}. \end{cases} \tag{9}$$

The capacitor voltage of the faulty SMs in bypassed state should not participate in feedback and the reference voltage should be correspondingly reduced. The current reference i^*_d is obtained from the output of the outer-loop PI regulator, and the current reference i^*_q is set to zero so that the FB-MMC will start up with unity power factor. In addition, the real-time feedback value of SM capacitor voltage should be taken into account to improve dynamic performance of the proposed strategy.

Before the start of normal operation, the outputs of innerloop PI regulators are saturated due to unexpected feedback values. This results in unavoidable inrush currents in engineering practice. To solve this issue, the output limits of the PI regulators are intentionally set in the form of slope. Besides, the output limits of the voltage loop are also set to a slope shape so that the

TABLE I
DIFFERENT STATES OF SM

Current direction	Gate signals	v_{ab}	State	Voltage balancing
$i_{SM} > 0$	S_1 on, S_3 on	0	Bypassed	Incapable
	S_1 on, S_4 on	v_{SM}	Charged	Incapable
	S_2 on, S_3 on	$-v_{SM}$	Discharged	Capable
	S_2 on, S_4 on	0	Bypassed	Incapable
$i_{SM} < 0$	S_1 on, S_3 on	0	Bypassed	Incapable
	S_1 on, S_4 on	v_{SM}	Discharged	Capable
	S_2 on, S_3 on	$-v_{SM}$	Charged	Incapable
	S_2 on, S_4 on	0	Bypassed	Incapable

TABLE II
SYSTEM PARAMETERS

Symbol	Description	Value
V_m	Phase voltage amplitude	$311V$
f_g	Line frequency	$50Hz$
V_{dc}	DC voltage	$5kV$
f_s	Carrier frequency	$1kHz$
f_{ctr}	Control frequency	$10kHz$
R_1	Current-limiting resistance	$2.5\Omega, 5\Omega$
R_2	Load resistance	$1.43k\Omega$
$N_1 : N_2$	Transformer voltage ratio	$400 : 2450$
R_L	ESR of arm inductor	0.38Ω
L	Arm inductor	$30mH$
N	No. of SMs per arm	7
N_r	No. of hot-reserved SMs per arm	1
C	SM capacitance	$330\mu F$
V_{sm}	SM rated capacitor average voltage	$833V$

capacitors will be charged by the gradually increasing currents until their voltage rise to the reference value. Thus, the soft startup of FB-MMC is achieved. t_1 and t_2 are the times when the output limits of outer loop and inner loop are completely released, respectively. It should be mentioned that t_2 should be less than t_1, otherwise the current cannot accurately track the reference during the startup process. $i_{d\max}$ is the upper limit of outer loop. $v_{d\max}$ and $v_{q\max}$ are the upper limits of inner current loops, respectively. $i_{d\text{out}}$ and $i_{q\text{out}}$ are the outputs of inner current loops, respectively.

C. Improved Startup Strategy for Eliminating Inrush Current at the Start of Step 2

Although the potential inrush current at the start of normal operation can be suppressed by employing the modified PSC-PWM, the inrush current at the beginning of step 2 still exists due to the load. In this section, an improved startup strategy is proposed to solve this issue. According to (1), the ac output voltage range of MMC adopting the modified PSC-PWM at the end of step 1 is $\frac{V_{\text{eq}}R_2}{R_{\text{eq}}+R_2}$. If the grid currents are supposed to be controllable, the following relationship should be satisfied:

$$\frac{V_{\text{eq}}R_2}{R_{\text{eq}}+R_2} \geq \frac{V_m N_2}{N_1}. \tag{10}$$

By solving the above-mentioned inequality, R_1 should satisfy

$$R_1 \leq \frac{[(\sqrt{3}-1)R_2 - 2R_L]N_1^2}{2N_2^2}. \tag{11}$$

According to the parameters in Table II, one can obtain that $R_1 \leq 13.9\Omega$. Thus, the grid currents can be controllable at the end of step 1 by selecting the appropriate R_1. The step 1 of the improved startup strategy is unchanged. The step 2 and step 3 of the improved startup strategy are explained as follows.

Step 2: All gate drive signals are activated. The dc modulation component M_0 is set to 0, and the dc output voltage is 0. In other words, the load can be regarded bypassed. The output limits of the outer loop are not released, while the output limits of the inner loop are released. This means that the grid currents are controlled to be 0 (i.e., $i_d^* = 0$), so there is no voltage drop on the current limiting resistors. Then, R_1 and KM_1 are bypassed by KM_2, and the inrush currents can be avoided.

Step 3: The dc modulation component M_0 is gradually increased to the value at the normal operation (i.e., $\frac{N-N_r}{2N}$), and the output limits of the outer loop are released. Thus, all SM capacitors are charged to their nominal voltage values smoothly, and the dc voltage rises to the rated value.

D. Capacitor Voltage Balancing Control

The capacitor voltage balancing control is necessary to ensure that all SMs are charged equally. As shown in Fig. 6, the capacitor voltage of all SMs in an arm will be balanced to the average value of that arm with a proportional (P) controller, where K_p is the proportional parameter. In addition, the sign of arm current should be considered to determine the direction of adjustment. The adjustment from capacitor voltage balancing control, the reference of differential mode and common mode voltage, and dc modulation component constitute the modulation signal of FB-SMs ($m_{xyz}, x = a, b,$ or $c, y = u, l, z = 1, 2, 3...N$).

To further explore the behavior of voltage balancing control, eight different operating modes of SM are presented in Fig. 9. Moreover, the state and voltage balancing ability are summarized in Table I. It can be observed that voltage balancing control is only effective in two conditions: one is that the SM current is positive with negative voltage level output, and the other is that the SM current is negative with positive voltage level output. In other words, outputting negative voltage is beneficial for voltage balancing. In both situations, the SM works in discharged state. The principle of balancing capacitor voltage is roughly explained here. Assuming $i_{\text{SM}} > 0$ and $v_{ab} = -v_{\text{SM}}$, if the capacitor voltage is lower than the reference, the duty cycle of S_1 will increase, which means that the duty cycle of S_2 will decrease. As a result, the discharge time of the capacitor will decrease, and its voltage will increase compared with other SMs. Similarly, another case can be inferred.

IV. SIMULATION AND EXPERIMENTAL RESULTS

To verify the effectiveness of the proposed soft startup strategy, simulation and experimental results are given in this section. The system parameters are listed in Table II.

A. Simulation Results

The simulation waveforms of the overall startup process ($R_1 = 2.5\Omega$) are shown in Fig. 10(a). In Fig. 10(b), the detailed simulation results at the start of normal operation ($t = 0.6$s) are displayed. It can be seen that the capacitors are charged

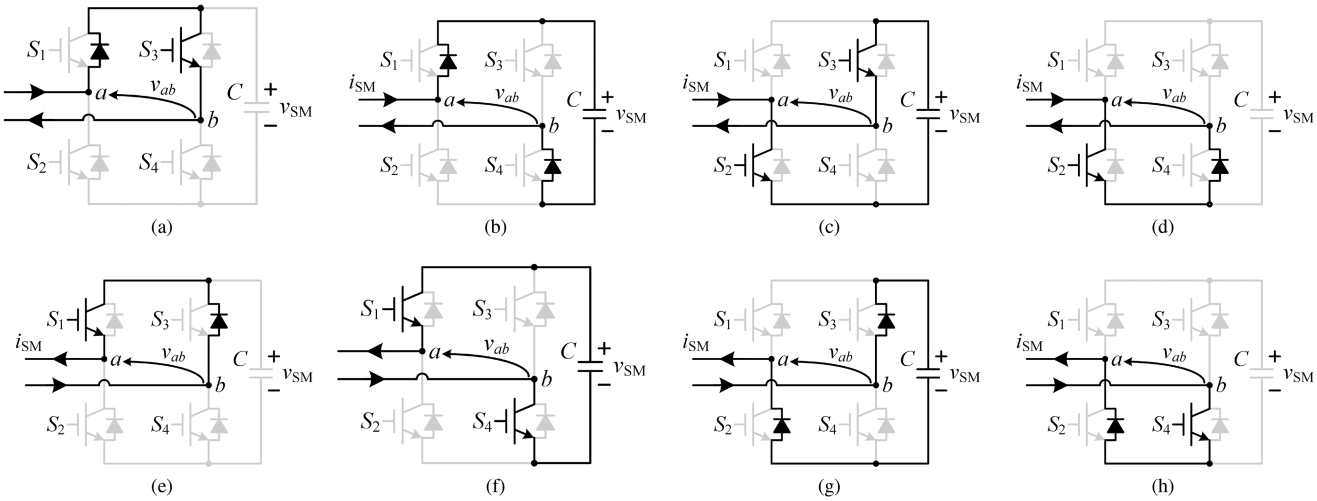

Fig. 9. Operating modes of SM. (a) $i_{\rm SM} > 0, S_1$ on, S_3 on. (b) $i_{\rm SM} > 0, S_1$ on, S_4 on. (c) $i_{\rm SM} > 0, S_2$ on, S_3 on. (d) $i_{\rm SM} > 0, S_2$ on, S_4 on. (e) $i_{\rm SM} < 0, S_1$ on, S_3 on. (f) $i_{\rm SM} < 0, S_1$ on, S_4 on. (g) $i_{\rm SM} < 0, S_2$ on, S_3 on. (h) $i_{\rm SM} < 0, S_2$ on, S_4 on.

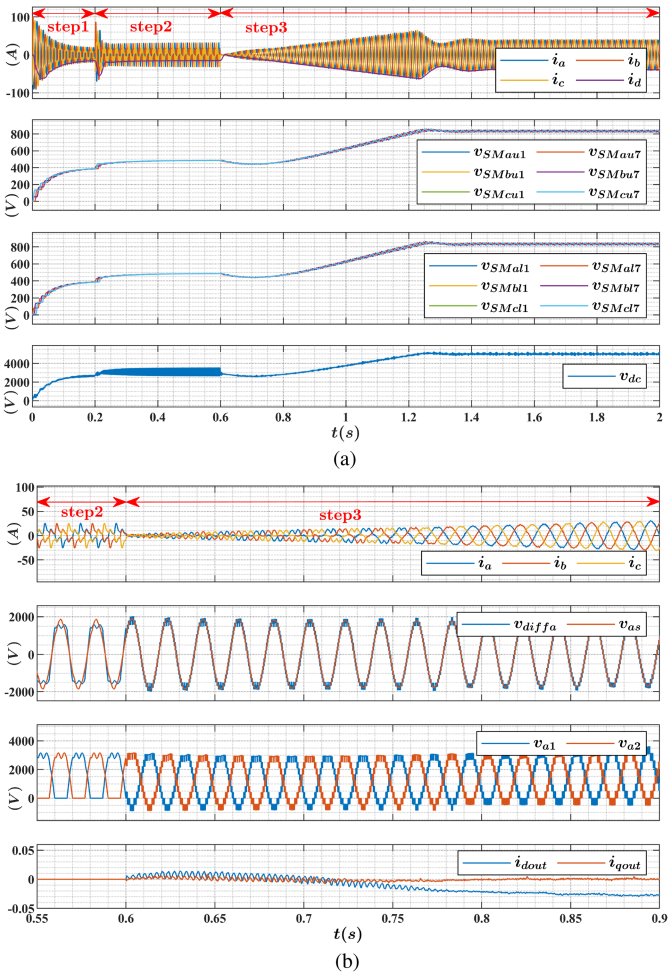

Fig. 10. Simulation results. (a) Overall startup process ($R_1 = 2.5\,\Omega$), grid current i_x and i_d, SM capacitor voltage $v_{\rm SMxyz}$, and DC voltage $v_{\rm dc}$. (b) Start of normal operation, grid current i_x, AC output voltage $v_{\rm diffa}$, phase voltage of the secondary side v_{as}, upper arm voltage v_{a1}, lower arm voltage v_{a2}, and outputs of the inner current loops $i_{d\rm out}$, $i_{q\rm out}$.

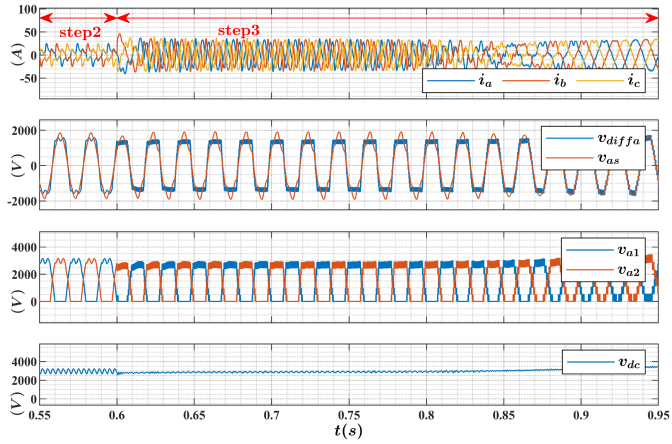

Fig. 11. Simulation results with conventional PSC-PWM, grid current i_x, AC output voltage $v_{\rm diff}a$, phase voltage of the secondary side v_{as}, upper arm voltage v_{a1}, lower arm voltage v_{a2}, and DC voltage $v_{\rm dc}$.

fast and smoothly by the slope shaped currents. In addition, all SM capacitors are charged equally with the proposed voltage balancing control and stabilized at 833 V. As observed in the waveforms of v_{a1} and v_{a2}, negative voltage levels are utilized to expand the output voltage range by employing the modified PSC-PWM. From the waveforms of $v_{\rm diff}a$ and v_{as}, it can be concluded that the ac output voltage of MMC can quickly and accurately follow the grid voltage. The standardized $i_{d\rm out}$ and $i_{q\rm out}$ are limited to zero at the beginning of normal operation due to the ramp shaped output limits. As a result, the inrush currents at the start of normal operation are completely eliminated.

Fig. 11 presents the simulation results with conventional PSC-PWM. As illustrated, ac current is uncontrollable because of insufficient ac output voltage of MMC. Therefore, the inrush current is inevitable and will be more severe with smaller M_0. In Fig. 12, the capacitor voltage is set to a constant, which is equal to the rated value without regard to the real-time feedback capacitor voltage. Large inrush currents are introduced due to

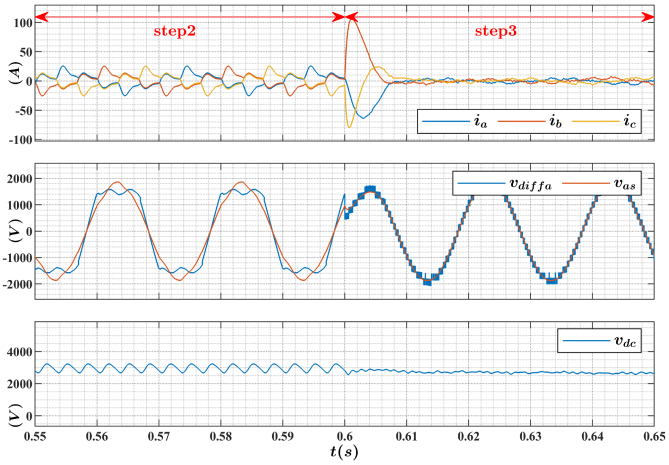

Fig. 12. Simulation results without regard to the real-time feedback capacitor voltage, grid current i_x, AC output voltage $v_{\mathrm{diff}a}$, phase voltage of the secondary side v_{as}, and DC voltage v_{dc}.

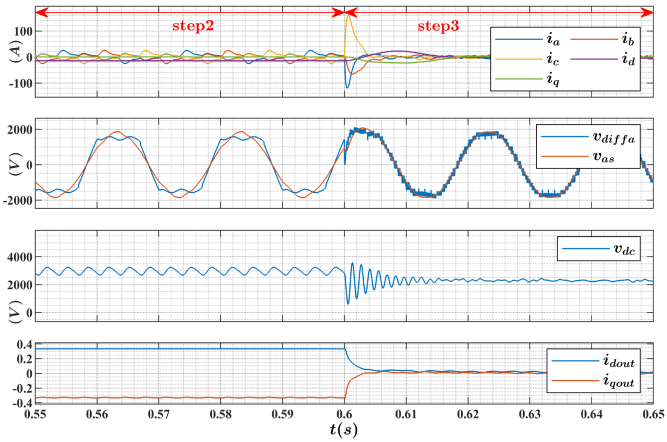

Fig. 13. Simulation results without intentionally setting the output limits of the innerloop PI regulators in the form of slope, grid currents i_x, i_d, i_q. AC output voltage $v_{\mathrm{diff}a}$, phase voltage of the secondary side v_{as}, DC voltage v_{dc}, and outputs of the inner current loops $i_{d\mathrm{out}}$, $i_{q\mathrm{out}}$.

the decreased dynamic performance. Simulation results without intentionally setting the output limits of the innerloop PI regulators in the form of slope are shown in Fig. 13. The inrush currents are unavoidably generated due to the already saturated outputs of the current loops.

The simulation waveforms of the overall startup process employing the improved startup strategy are shown in Fig. 14(a). According to (11), the current limiting resistor is selected as 5Ω to ensure fast charging speed. As can be seen, the ac currents are controlled to be 0 at the start of step 2 ($t = 0.4\,\mathrm{s}$), and the dc voltage is gradually reduced to 0. At $t = 0.45\,\mathrm{s}$, the current limiting resistor is bypassed, and the inrush currents are eliminated compared with Fig. 10(a). Then, the dc modulation component M_0 is gradually increased to the value at the normal operation, and the dc voltage rises to the rated value. At the same time, all the SM capacitors are charged smoothly and effectively in the closed-loop manner.

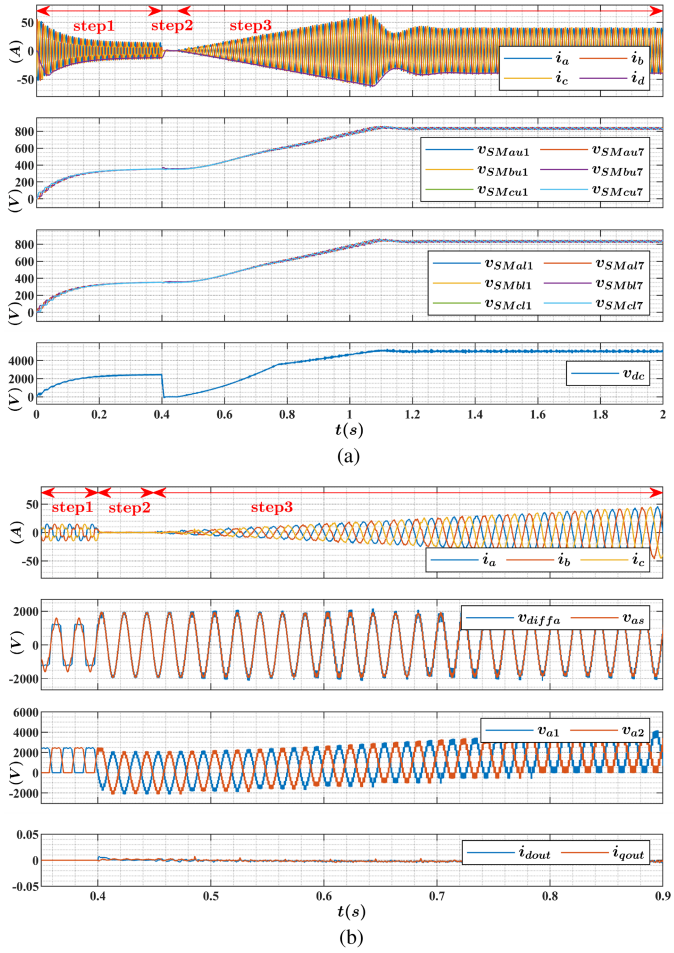

Fig. 14. Simulation results. (a) Overall startup process employing the improved startup strategy ($R_1 = 5\,\Omega$), grid currents i_x and i_d, SM capacitor voltage $v_{\mathrm{SM}xyz}$, and DC voltage v_{dc}. (b) Start of step 2, grid current i_x, AC output voltage $v_{\mathrm{diff}a}$, phase voltage of the secondary side v_{as}, upper arm voltage v_{a1}, lower arm voltage v_{a2}, and outputs of the inner current loops $i_{d\mathrm{out}}$, $i_{q\mathrm{out}}$.

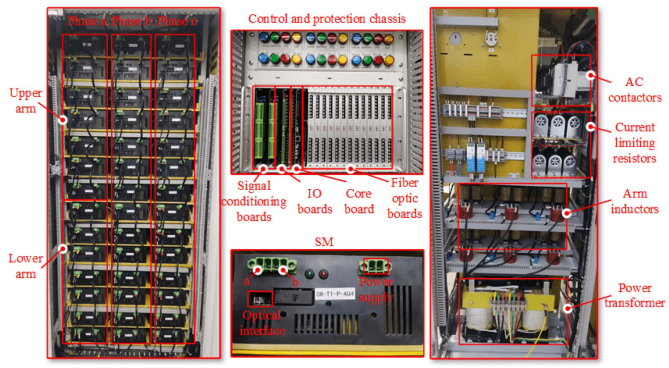

Fig. 15. Experimental prototype.

B. Experimental Results

As shown in Fig. 15, a prototype is built to verify the effectiveness of the proposed startup strategy. The control and protection chassis is comprised of a core board, signal conditioning boards, input/output interface boards, and fiber optic boards. Through

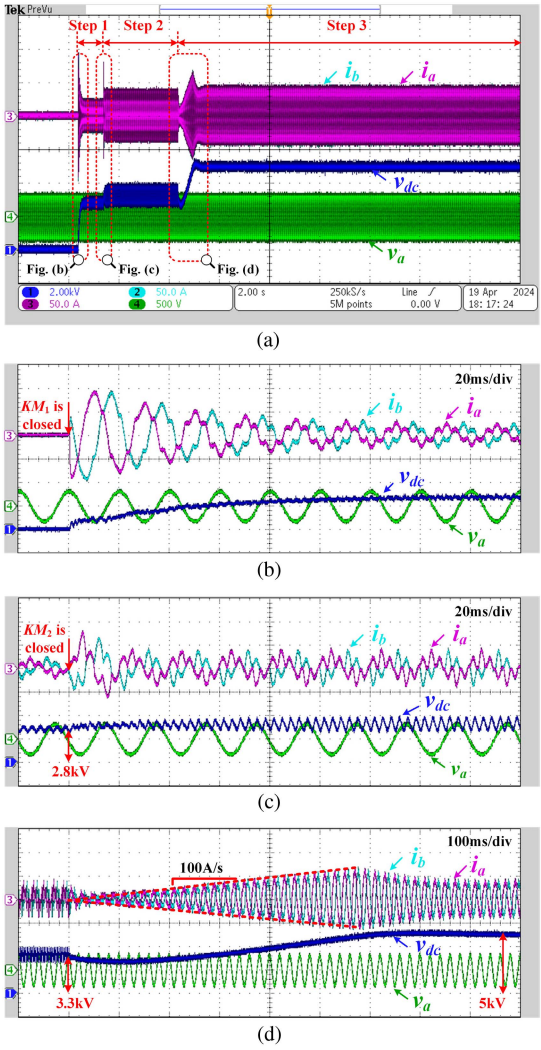

Fig. 16. Typical voltage and current experimental waveforms of FB-MMC during startup process ($R_1 = 2.5\,\Omega$), grid currents i_a, i_b, grid phase voltage v_a and DC voltage $v_{\rm dc}$. (a) Overall process. (b) Step 1. (c) Step 2. (d) Step 3.

the fiber optic boards, the SMs receive modulation signals from the core board, and send back the monitored capacitor voltages and real-time status. DSP TMS320F28379 and FPGA EP4CE22F17 are integrated on the core board to implement control algorithms with a control cycle of 100μs.

Fig. 16 shows the performance of the proposed soft start strategy. According to Fig. 5(b), the current limiting resistor is selected as 2.5Ω. At the end of step 1, the dc voltage can only rise to 2.8 kV due to the presence of the load, which agrees well with theoretical analysis. The average value of dc voltage rises to nearly 3.3 kV $\left(\frac{\sqrt{3}N_2V_m}{N_1N}\right)$ after step 2 is finished. At the instant of start for step 3, the inrush current is completely eliminated, and the grid currents ramp up according to the set slope $\left(\frac{i_{d\max}}{t_1} = 100\text{A/s}\right)$. In the experiment, t_1 (0.65 s) is set to be longer than t_2 (20 ms). Finally, the capacitor voltage is charged to the rated value and the dc voltage reaches 5kV. Moreover, the startup process can be flexibly accelerated by choosing a larger slope. In Fig. 17, the upper and lower arm voltage are

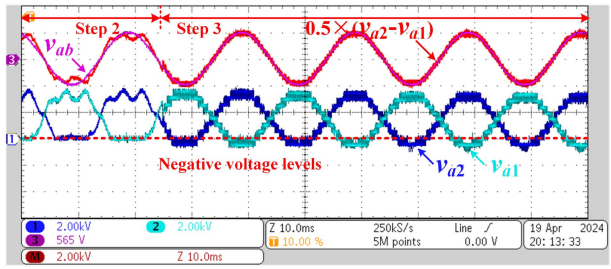

Fig. 17. Typical voltage waveforms of FB-MMC at the start of normal operation ($R_1 = 2.5\,\Omega$), AC output voltage $v_{\text{diff}a} = 0.5 \times (v_{a2} - v_{a1})$, grid line voltage v_{ab}, upper arm voltage v_{a1}, and lower arm voltage v_{a2}.

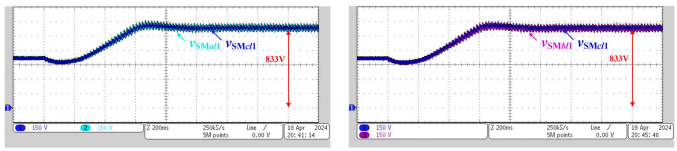

Fig. 18. SM capacitor voltage waveforms with voltage balancing control ($R_1 = 2.5\,\Omega$). (a) SM capacitor voltages $v_{\text{SM}al1}$, $v_{\text{SM}cl1}$. (b) SM capacitor voltages $v_{\text{SM}bl1}$, $v_{\text{SM}cl1}$.

shown, and the ac output voltage is obtained from them (i.e., $v_{\text{diff}} = 0.5 \times (v_{a2} - v_{a1})$). Line-to-line voltage v_{ab} is presented considering the phase difference between the primary and the secondary side. It can be seen that the negative voltage levels are utilizing to expand the output voltage range of the MMC, thus, the output voltage of MMC is enough to against the grid voltage. In Fig. 18, the capacitor voltages of the lower arm are presented to demonstrate that the capacitor voltage can be well balanced during the controlled start-up process. The capacitor voltage is controlled to be 833 V and remains stable.

Fig. 19 presents the startup process employing the improved startup strategy. As can be seen, compared with Fig. 16(b) and (c), when KM_2 is closed, the inrush currents are completely suppressed even though $R_1 = 5\Omega$, and the inrush currents are significantly reduced at the start of precharging process (i.e., KM_1 is closed), which agrees well the theoretical analysis and simulation results. Typical waveforms of FB-MMC at transition between different steps are shown in Fig. 20. In Fig. 20(a), the dc bias of v_{a1} and v_{a2} is 0 because M_0 is set to 0. Hence, the dc voltage is reduced to 0 in Fig. 19(c). In Fig. 20(b), the M_0 is gradually increased to be the value at normal operation, while the SM capacitors are charged to the nominal value. As a result, the dc voltage is regulated to 5kV in Fig. 19(d). As shown in Fig. 21, the capacitor voltages are well balanced with the improved startup strategy.

V. Discussion and Comparison of Different Startup Strategies

A comparison of different startup strategies proposed for MMC is summarized in Table III. In terms of extra elements, the auxiliary dc power supply is required in [9], [10], and [11], and the equipment cost is increased compared with using current

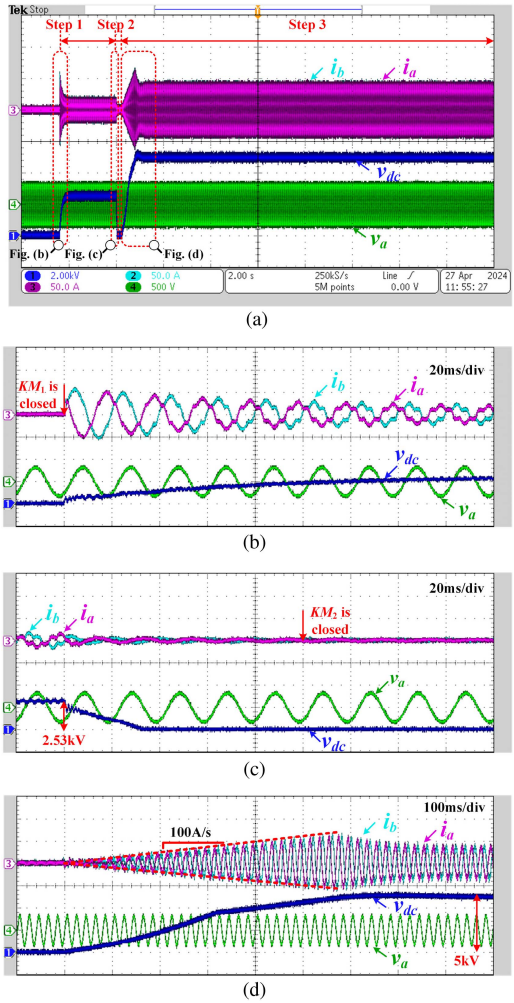

Fig. 19. Typical voltage and current experimental waveforms of FB-MMC employing the improved startup strategy ($R_1 = 5\,\Omega$), grid currents i_a, i_b, grid phase voltage v_a and DC voltage $v_{\rm dc}$. (a) Overall process. (b) Step 1. (c) Step 2. (d) Step 3.

TABLE III
COMPARISON OF DIFFERENT STARTUP STRATEGIES

Strategies	Extra elements	Control complexity	Startup speed	Inrush currents	Separate algorithms	Cost
In [9]	Nominal voltage dc source	Simple	Slower	None	Yes	High
In [10]	Thyristors and dc source	Simple	Medium	None	Yes	Higher
In [11]	Low-voltage dc source	Moderate	Medium	None	Yes	Medium
In [12]	None	Moderate	Slow	Medium	Yes	Low
In [15]	None	Moderate	Fast	None	Yes	Low
In [16]	None	Moderate	Fast	Medium	Yes	Low
In [17]	None	Simple	Fast	None	No	Low
This paper	None	Simplest	Fast	None	No	Low

limiting resistors. In Li and Zhao's [9] work, a dc source with nominal capacitor voltage is connected to the dc link, and SMs of each phase are charged one by one. Two switches composed of four transistors are added to each SM, so that all SMs can be charged synchronously by triggering all the transistors simultaneously in Xu et al.'s [10] work. The charging time is shortened while the cost is increased. In Tian et al.'s [11] work, the existing switches, arm inductors, and SM capacitors and

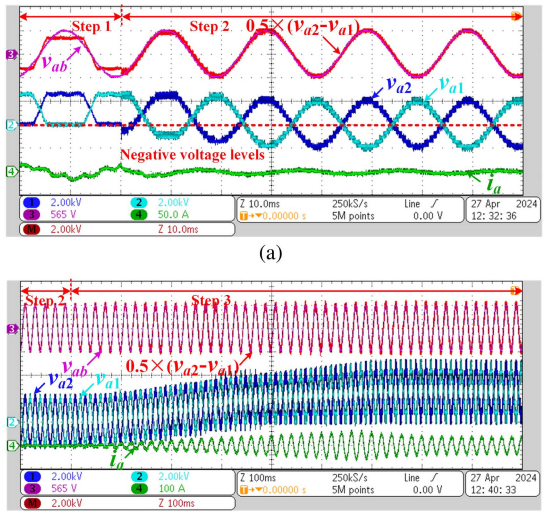

Fig. 20. Typical waveforms of FB-MMC employing the improved startup strategy at transition between different steps ($R_1 = 5\,\Omega$), AC output voltage $v_{\rm diff}a = 0.5 \times (v_{a2} - v_{a1})$, grid current i_a, grid line voltage v_{ab}, upper arm voltage v_{a1}, and lower arm voltage v_{a2}.

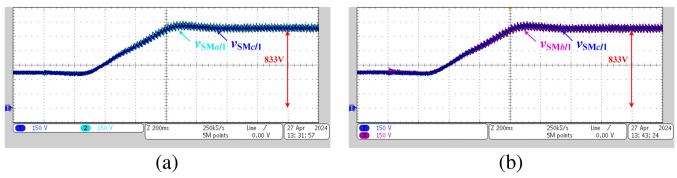

Fig. 21. SM capacitor voltage waveforms employing the improved startup strategy ($R_1 = 5\,\Omega$). (a) SM capacitor voltages $v_{\rm SM}al1$, $v_{\rm SM}cl1$. (b) SM capacitor voltages $v_{\rm SM}bl1$, $v_{\rm SM}cl1$.

additional dc source are combined to form a boost circuit, thus, a low-voltage dc source can be applied for charging. Nevertheless, these methods may not be practical in high-voltage applications due to stringent insulation requirements. The SM capacitors are charged to their nominal voltage by dynamically adjusting the number of bypassed and blocked SMs in Zhang et al.'s [12] work. For the startup speed, the method proposed in Li and Zhao's [9] work is regarded as slowest because the SMs are charged one by one with exponentially decaying currents. Since the SMs in Zhang et al.'s [12] work are charged group by group, the charge speed is improved compared with Li and Zhao's [9] work. However, their charging time is significantly increased as the number of SMs increases. In Xu et al.'s [10] work, all the SMs are charged simultaneously by exponentially decaying currents. In Tian et al.'s [11] work, the SMs are charged in different groups with boost circuit. Although the charging current is increased in Tian et al.'s [11] work, the number of SMs being charged at the same time is reduced. Therefore, the strategies proposed in [10] and [11] have similar startup speed. In Li et al.'s [15] work, separately designed closed-loop precharge control is proposed to charge the capacitors with a constant current. However, the charging speed is limited because the upper arm SMs and the lower arm SMs are charged separately.

In Shi et al.'s [16] work, a capacitor voltage feedforward control along with the averaging capacitor voltage control is proposed to improve the dynamic performance. However, it is bypassed during normal operation and replaced by a sorting and balancing algorithm. Fast charging can be realized with these closed-loop methods, but the overall control structure is complicated. In Wang et al.'s [17] work, deadbeat predictive current control is adopted, and the startup process is accomplished with a constant charging current. For the deadbeat control, the parameters variation needs to be carefully considered because of its dependence on circuit parameters. In this article, the capacitor is controlled to be charged with a gradually increasing current, and the startup process can be further shortened with a larger current slope. In addition, the proposed strategy is realized with conventional PI controllers, which is easy to be implemented. With respect to the inrush currents, when the SMs are bypassed in Zhang et al.'s [12] work, the inrush currents are induced due to the voltage difference between the ac side and valve side. In Shi et al.'s [16] work, the inrush currents are generated because of the insufficient ac output voltage of MMC. In this article, the potential inrush currents are completely suppressed at the start of step 2 and normal operation with the improved startup strategy.

VI. Conclusion

In this article, a simple and effective soft startup strategy is proposed for FB-MMC in closed loop manner. It does not require any auxiliary elements and separately designed startup algorithms. Operating stages of the uncontrolled precharging process with load are analyzed in detail. According to the analysis, the simplified equivalent circuit is given, and then a mathematical model is obtained to analyze the factors that affect the steady-state voltage of the SM capacitors. By utilizing the negative voltage levels of the FB-SM, the inrush current at the start of normal operation can be suppressed. However, at the instant of bypassing the current limiting resistors, the inrush currents are induced owing to the presence of load. Subsequently, an improved startup strategy is further proposed by intentionally controlling the dc voltage to zero. With this strategy, the main ac contactor is closed with zero current, which is beneficial for extending the service life of mechanical switches. In addition, the charging current in the form of a slope is achieved too fast and smoothly charge the capacitors, and the capacitor voltages are well balanced with the proposed voltage balancing algorithm. Finally, the performance of the proposed startup control is verified by the simulation and experimental results of a grid connected three-phase FB-MMC rectifier with 5 kV dc.

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Debin Zhang was born in Jiangxi, China, in 1999. He received the B.S. degree in electrical engineering from the Beijing Institute of Technology, Beijing, China, in 2020, where he is currently working toward the Ph.D. degree in electrical engineering.

His research interests include dc/dc converters and ac/dc converters.

Deshang Sha (Senior Member, IEEE) received the B.S. degree from the Luoyang Institute of Technology, Luoyang, China, in 1998, the M.S. degree from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2001, and the Ph.D. degree from the Institute of Electrical Engineering, Chinese Academy of Sciences, Beijing, China, in 2005, all in electrical engineering.

Since 2008, he has been with the School of Automation, Beijing Institute of Technology, Beijing, China, where he is currently a tenured Full Professor. From 2012 to 2013, he was a Visiting Scholar with the Future Energy Electronics Center, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA. He has authored more than 100 papers and four books. His research interests include the modeling and control of power converters, high-efficiency power conversion, and power electronics applications in renewable energy power generation.

Congzhe Gao (Member, IEEE) was born in Hebei, China, in 1984. He received the B.S. degree in electrical engineering from the Department of Electrical Engineering, Chongqing University, Chongqing, China, in 2007, and the Ph.D. degree in electrical engineering from the Department of Electrical Engineering, Tsinghua University, Beijing, China, in 2012.

He is currently an Associate Professor with the School of Automation, Beijing Institute of Technology, Beijing, China. His research interests include power converters and power quality, both in low-voltage and medium-voltage distributing networks.

Xiao Liu was born in 1999. He received the B.S. degree in electrical engineering and automation from the Beijing Institute of Technology, Beijing, China, in 2021, where he is currently working toward the M.S. degree in electrical engineering.

His research interest includes dc–ac inverter and modular multilevel converters.

Hanwen Long received the B.S. and M.S. degrees in electrical engineering from the School of Automation, Beijing Institute of Technology, Beijing, China, in 2021 and 2024, respectively. He is currently working toward the Ph.D. degree in electrical engineering with the College of Electrical and Information Engineering, Hunan University, Changsha, China.

His research interests include resonant converters and high-voltage power converters.

Guangshan Tang was born in 1999. He received the B.S. degree in automation from Shenyang Ligong University, Shenyang, China, in 2020, and the M.S. degree in control engineering from the Beijing Institute of Technology, Beijing, China, in 2024.

His research focuses on multiport dc/dc bidirectional power conversion.

Yining Zhao was born in 1999. He received the B.S. degree in electrical engineering and automation from the Hebei University of Technology, Tianjin, China, in 2022. He is currently working toward the M.S. degree in electrical engineering with the Beijing Institute of Technology, Beijing, China.

His research interests include dc/dc power conversion and modular multilevel converters.

Yang Gao was born in Shandong, China, in 1983. He received the B.S. and M.S. degrees in electrical engineering from the Department of Electrical Engineering, China University of Mining and Technology, Beijing, China, in 2002 and 2009, respectively.

He is currently a Professor level Senior Engineer with China Electric Power Research Institute, Beijing, China. His research interests include HVDC and dc grid system and equipment.