A Bipolar DC Grid-Interfaced Integrated Dual Input Converter With Reduced Overloading Under Unbalanced Line Voltage Conditions

Kausik Biswas, *Graduate Student Member, IEEE*, Chandrashekhar N. Bhende, *Senior Member, IEEE*, and Olive Ray, *Member, IEEE*

***Abstract*—The bipolar dc microgrid configuration ensures enhanced efficiency, flexibility, and improved power quality compared to unipolar dc-based distribution. However, a bipolar structure is susceptible to voltage imbalance caused by asymmetric loading between its two poles. In such cases, power electronic converters with constant power characteristics can provide additional overload to these bipolar lines. This article presents a novel three-port dc–dc power electronic interface whose impedance can be dynamically adjusted to regulate both the pole voltage magnitudes (under balanced or unbalanced conditions) with reduced overloading while feeding a constant power load. The performance of the proposed configuration has been assessed using a three-port structure referred to as the integrated dual input converter (IDIC). The analysis of the converter operating modes, its pulsewidth modulation control, and the closed-loop system design for the bipolar dc distribution interface has been developed in this article. The theory of operation and control behavior has been validated using experimental testing on a laboratory scale prototype of IDIC.**

***Index Terms*—Bipolar dc distribution, current-mode control, multiport dc–dc converter.**

I. Introduction

THE advancement of the dc–dc power electronics converter boosts the formation of dc microgrids. The dc microgrid structure increases the flexibility to integrate micro dc power sources like solar photovoltaics (PVs), fuel cells (FCs), batteries, wind energy, etc., into the system [1], [2]. Furthermore, dc microgrid systems are unaffected by synchronization issues, skin effects, reactive power, and other associated problems. Therefore, the adoption of dc microgrid is expected to be compelling, practical, and advantageous in modern power systems [3], [4].

DC microgrid distribution systems can be specified into two categories—unipolar dc distribution system and bipolar dc distribution system. Bipolar dc microgrid provides enhanced reliability, safety, and efficiency than its counterpart and is becoming more and more prevalent [5]. Fig. 1 shows a conventional bipolar dc microgrid structure where different power sources and loads are connected to the bipolar dc microgrid systems. This type of structure consists of a positive line, a negative line, and a neutral line. Furthermore, to support this type of system, different distributed sources are interfaced to the line. Both the sources and loads can be connected to the positive line or the negative line or both with the positive and negative line based on the type of application. The dc distribution is used in various voltage-level applications, a large portion of the market share of the dc distribution system is the low voltage dc distribution (LVdc) system [6]. As per the *IEEE standards* for rural electrification discussed in [7], for a 48 V LVdc system, the allowable range of voltage level is 36–58 V at PCC (i.e., 25% change corresponding to nominal voltage level). Due to this wide voltage variation, it is a challenging task to feed constant power loads (CPLs) connected to a system without overloading it [8]. The review of the effects of CPL, voltage unbalance issue and existing solutions are mentioned below.

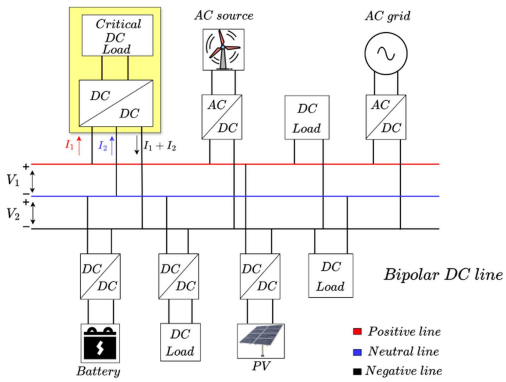


Fig. 1. Bipolar DC microgrid system.

1) Constant Power Loads: In dc microgrids, electronic loads make up the majority of end users. POL converters are used by these loads to regulate voltage and power processing. These loads are referred to as CPLs because of their active regulation capacity, which enables them to extract constant power even under variable voltage conditions at the point of common coupling [9]. Therefore, these types of loads exhibit negative

Manuscript received 28 March 2024; revised 30 June 2024; accepted 29 July 2024. Date of publication 6 August 2024; date of current version 11 September 2024. This work was supported in part by the Ministry of Education, Government of India, through a doctoral fellowship under PMRF scheme and in part by the Ministry of Electronics and Information Technology, Government of India, through "Development of Electric Vehicle Subsystems Program (Part -I) " under OM 25(2)/2021-ESDA. Recommended for publication by Associate Editor Y. Yan. *(Corresponding author: Kausik Biswas.)*

The authors are with the Department of Electrical Engineering, School of Electrical and Computer Sciences, IIT Bhubaneswar, Bhubaneswar 752050, India (e-mail: s23ee09004@iitbbs.ac.in; cnb@iitbbs.ac.in; olive@iitbbs.ac.in).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3438794.

Digital Object Identifier 10.1109/TPEL.2024.3438794

incremental load (i.e., draw high current when voltage is low and draw less current when voltage is high). Hence, during low-voltage conditions, the drop in the line further increases due to the connection of CPLs, which further decreases the voltage at PCC. Furthermore, these kind of loads also reduces the input impedance of the load which affects the voltage stability of the dc microgrid system [10].

2) Voltage Unbalance Due to Asymmetrical Loading in Bipolar DC Distribution System: Another major problem associated with bipolar dc distribution systems is voltage unbalance due to asymmetrical loading. To address this, voltage balancer (VB)-based solutions are reported in [11], [12], and [13]. Furthermore, source-side power converters with inherent voltage balancing capabilities are reported in [14], [15], and [16]. However, in the case of a distribution line with multiple load nodes, these methods do not provide satisfactory results and voltage unbalance persists in the line as the line length increases from the source side. The number of VBs can be increased to resolve the problem; however, it requires coordination control between the supplies and the VBs, which makes the system more complicated [17]. To overcome these issues of voltage unbalancing measures need to be taken from the load-interfaced converters that consistently feed a CPL during voltage imbalance conditions without overloading a specific line.

3) Dual Input Converter Used in Bipolar DC Grid for Load-Side Voltage Unbalance Compensation (Existing Solutions): To process power independently from a bipolar dc line dual input converters are widely recommended [18]. Dual-input dc–dc converters for a load-side solution to voltage unbalance in bipolar dc distribution systems are reported in [19], [20], [21], [22], [23], [24], and [25]. Yadav et al. [19] proposed a dual input converter. The converter is connected to the load-side converter to suppress the voltage imbalance in the bipolar dc distribution system due to asymmetrical loading. The converter uses the *LC* resonating circuit to suppress the voltage imbalance at the load side. However, this is an auxiliary converter and does not regulate the output voltage. Byun et al. [20] presented an input series output parallel bipolar converter. Although the converter provides a load-side solution, it requires a higher number of switches and a complex phase-shifted control algorithm to maintain the power flow management of the converter. Liao et al. [21] presented a dual input converter, the converter works on the dc-spring concept to suppress the voltage imbalance. Furthermore, this method uses lossy elements and a perplex control strategy. These converters are used as an add-on to the existing regulating converters as they do not feed the load directly. Another dual input converter for bipolar dc-microgrid is reported in [22], this is a load-side converter that requires coordination control (i.e., communication is required) from the grid side to generate the switching signals and the operation is limited to a certain level of voltage imbalance. Tavakoli et al. [23] presented an improved version of the converter presented in [22] by adding an extra inductor. However, due to DCM operation inductor current, the switches experience more stress than the prior one. A full bridge-based bipolar dc–dc converter is presented in [24] that uses eight semiconductor switches that require a complex control strategy for operation. Another load-end dual input bipolar converter is proposed in [25], it has four control loops in this scheme, which eventually increases the number of sensor counts and overall complexity of the control system of the converter. Therefore, there is a requirement for a dual input converter with a simple control strategy that can be connected to the load side and can process power independently from the bipolar line irrespective of the voltage profile of the lines.

To overcome the aforementioned issues, this article proposes a power converter architecture denoted as an integrated dual input converter (IDIC), which can be used for power processing when interfaced to a bipolar dc microgrid system. The major contributions of the article are as follows.

1) We proposed a power converter architecture denoted as an IDIC. IDIC topology is designed in such a fashion that the line current of positive and negative poles can be independently controlled with reduced switches.
2) The proposed IDIC is capable of regulating the output voltage while reducing the overloading effect in bipolar lines during voltage-unbalanced and reduced voltage conditions.
3) A suitable control scheme is developed for the IDIC which provides the flexibility to vary the converter input impedance dynamically to compensate for the unbalance voltage.

Furthermore, the power-sharing between the positive and negative lines depends on the voltage profile of each of the lines. The proposed converter provides a load-side solution and does not require additional VB circuits during voltage imbalance. The converter finds its suitability in different applications such as intermediate bus voltage-controlling converters connected to point-of-load converters [26], replacement of conventional boost converters or interleaved boost converters feeding CPLs [27], and it also can be used for both constant power and contact voltage loads [28].

The rest of this article is organized as follows. Section II discusses the stability criteria of a bipolar dc microgrid. Section III describes the synthesis of the proposed converter from a conventional boost converter along with the analysis, modeling, and design aspects of the proposed converter topology. The control strategy for the converter has been discussed in Section IV. The validation of the converter is shown in Section V. Finally, Section VI concludes this article.

II. Stability Analysis of Bipolar DC Microgrid

In the case of a bipolar dc microgrid system, two lines have different input impedances due to the uneven loading of the lines, which is also the reason for voltage unbalance. The voltage unbalance factor (VUF) of a bipolar dc line can be expressed by the following [29]:

$$\%\text{VUF} = \frac{|V_p - V_n|}{|V_p + V_n|/2} \times 100 \tag{1}$$

where $|V_p|$ and $|V_n|$ are the positive and negative terminal voltage of the line, respectively.

For instance, Fig. 2(a) shows the condition where V_p and V_n are equal at the converter side voltage (V_{conv}) due to the balanced

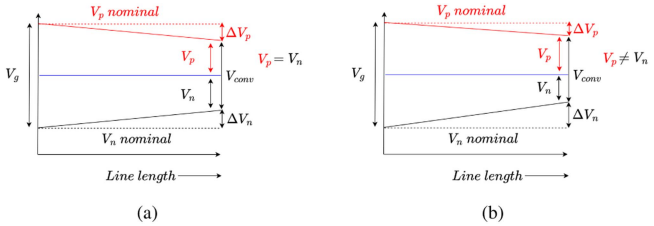


Fig. 2. Drop in voltage from grid side voltage to converter side voltage of bipolar dc line with (a) symmetrical loading in both lines and (b) asymmetrical loading.

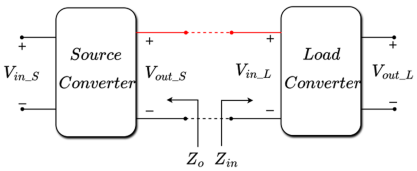


Fig. 3. Cascaded system connection.

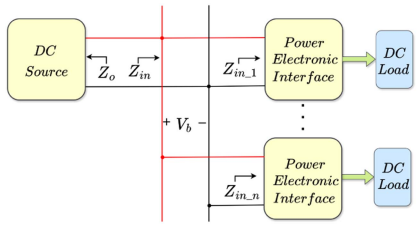


Fig. 4. Parallel connection of load to a DC bus.

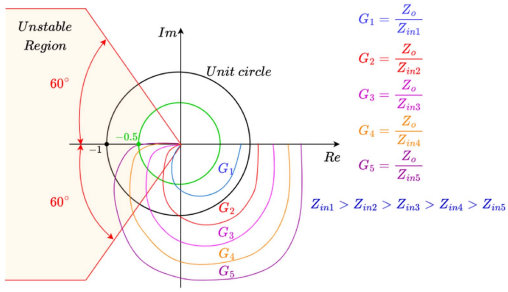


Fig. 5. Polar plot of G_{GP} for fixed source side output impedance and different values of load side input impedance.

loading of both the lines. Whereas, Fig. 2(b) shows a condition where the V_{conv} is the same as before but V_n is significantly less than V_p due to asymmetrical loading and unequal voltage drop in the lines. In this scenario, the VUF of the unbalanced line is higher than the balanced line which eventually leads to a difference in the input impedance of the load for the positive and negative lines.

The stability of the dc distribution system extensively depends on the input impedance of the load. Due to the unbalanced pole voltages in the bipolar dc distribution system, the load side input impedance may cross the stability limit, which eventually leads to sustained oscillations in the system or failure of source side converters [30]. The importance of the load input impedance to assess the stability of the dc distribution system is elaborately discussed using two extensively used stability criteria and they are as follows.

A. *Impedance Specification Based Stability Criteria of DC Distributed System*

Middlebrook's stability criteria was introduced to assess the stability of a cascaded system due to the introduction of an input filter. The fundamental objective of this was to ensure the system's stability and the converter dynamics should not be affected by an input filter. However, the same is also applicable for cascaded systems. It involves analyzing the interaction between the source and load impedances of a power converter. The criteria help ensure that the system remains stable under various operating conditions. A cascaded system is shown in Fig. 3. This theorem analyses the ratio of the output impedance of the source converter (Z_o) and the input impedance (Z_{in}) of the load converter. If the ratio $\frac{|Z_o|}{Z_{\text{in}}} << 1$ (i.e., $|Z_o| << |Z_{\text{in}}|$) for every condition the system is said to be stable as per the criteria [31]. In this condition, the loading effect due to the connection of the load is negligible and the dynamics of the source side converter are not affected by the load side converter. The application of Middlebrook stability criteria is further extended to dc distribution systems [32], [33]. For a system where a single source is feeding multiple converters connected in parallel through a dc bus as shown in Fig. 4. The cumulative input impedance of the source converter is $Z_{\text{in}} = Z_{\text{in\_1}}||Z_{\text{in\_2}}||\ldots||Z_{\text{in\_}n}$ for n number of parallelly connected converters. Hence, the ratio of $\frac{|Z_o|}{|Z_{\text{in}}|}$ reduces which also reduces the stability of the system. However, this concept uses the magnitude of the impedances, and using this it is difficult to comment on the stability of a complex system [34].

B. *Phase Margin and Gain Margin-Based Stability Criteria.*

For complex systems, gain margin (GM) and phase margin (PM)-based stability criteria was proposed in [35]. This criterion facilitates the existence of Z_o/Z_{in} within a specific frequency range while ensuring the appropriate minimum levels of gain and PMs, hence satisfying the Nyquist criterion. The ratio of $\frac{Z_o}{Z_{\text{in}}}$ is defined by G_{GP}. It has been mentioned in the criterion that for a well-designed system the GM and the PM should be 60° and 6 dB. This can also be expressed by the following:

$$|G_{GP}| = \left|\frac{Z_o}{Z_{\text{in}}}\right| \leq \frac{1}{\text{GM}} \& |\arg(Z_o) - \arg(Z_{\text{in}})| \leq 180 - \text{PM}. \tag{2}$$

Therefore any frequency range where G_{GP} lies beyond the 0.5 (-6 dB) circle, its phase must consistently deviate by at least 60° from 180°. Specifically, when G_{GP} intersects the unit circle, the PM will be no less than 60°. Furthermore, whenever G_{GP} intersects the negative real axis, its GM will be no less than 6 dB. If the PM is less than 60° and GM is less than 0.5 the system will become unstable [35]. The unstable region is shown in Fig. 5.

Fig. 5 shows an example of polar plots in which the output impedance of the source side converter (Z_o) is fixed, but the input impedance of the load side (Z_{in}) changes due to the addition of

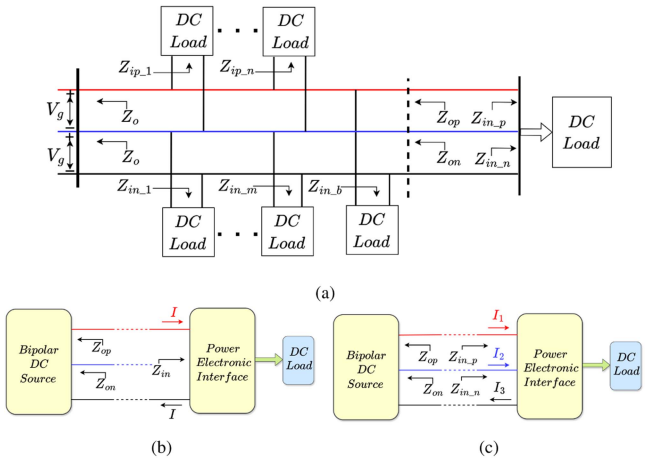


Fig. 6. (a) Impedance grouping of converter connected to bipolar dc distribution; connection of power converter to bipolar dc line. (b) Two-port converter. (c) Three-port converter.

further loads to the system. In Fig. 5, five different polar plots are plotted for five systems (i.e., $G_1, G_2, \ldots G_5$) by considering impedance variation of $Z_{\text{in}1} > Z_{\text{in}2} > Z_{\text{in}3} > Z_{\text{in}4} > Z_{\text{in}5}$. As load impedance reduces and the polar plot goes beyond the unit circle, the stability of the system tends to decrease. For example, when the system changes from G_1 to G_3, the stability margin reduces as G_3 plot is intersecting the unit circle close to PM limit. Further, when system changes from G_3 to G_4, the plot of G_4 intersects the unit circle in an unstable region and violates the PM criteria. Further, looking at the plot for system G_5, it can be observed that both the PM and GM criterion are violated. Under this scenario, the overall system becomes unstable which may lead to sustained oscillations in the distribution system or the failure of the source side converters.

C. Effect of Asymmetrical Loading in Bipolar DC Distribution System.

Fig. 6(a) shows a bipolar dc distribution network. The positive bus of the distribution is connected to "n" number of loads and the negative bus is connected to "m" number of loads with different input impedance and many loads are connected to both the positive line and negative line. Hence, the input impedance of each positive line and negative line from the converter side is expressed by (3) and (4), respectively. If both the lines are evenly loaded then $Z_{op} = Z_{on}$ (the load grouping is done as per [34]). However, in the case of practical scenarios due to the uncertainty of loading $Z_{op} \neq Z_{on}$

$$Z_{op} = \frac{Z_o}{Z_{ip\_1}||Z_{ip\_2}||\ldots||Z_{ip\_n}||(Z_{\text{in\_}b}/2)} \tag{3}$$

$$Z_{on} = \frac{Z_o}{Z_{\text{in}\_1}||Z_{\text{in}\_2}||\ldots||Z_{\text{in}\_m}||(Z_{\text{in\_}b}/2)} \tag{4}$$

Fig. 6(b) shows a two-port converter feeding a CPL connected to a voltage-unbalanced bipolar dc line (for instance, $V_p > V_n$). The input current from the positive line is I and so is the current in the negative line. In this case, the input impedance of the converter ($|Z_{\text{in}}| = (V_p + V_n)/I$) is equally divided between both of the lines. As the converter is feeding a CPL $G_p = \frac{|Z_{op}|}{|Z_{\text{in}}|/2}$ and $G_n = \frac{|Z_{on}|}{|Z_{\text{in}}|/2}$ (where, G_p and G_n in the ratio of source's output impedance and load's input impedance for the positive line and negative line, respectively) are different and G_p is lower than G_n as $V_p > V_n$ as per the assumption, and further increase in G_n also decreases the stability of the system. In order to solve this issue, we proposed that a three-port converter can be connected to a bipolar dc line feeding a CPL, as shown in Fig. 6(c). In this case, the neutral current can be varied such that $I_2 = I_1 - I_3$ (i.e., $I_1 \neq I_3$). Hence, positive input impedance $|Z_{\text{in\_}p}| = |V_p|/|I_1|$ and $|Z_{\text{in\_}n}| = |V_n|/|I_3|$ can be varied so that G_n and G_p can be chosen based on the condition of the line.

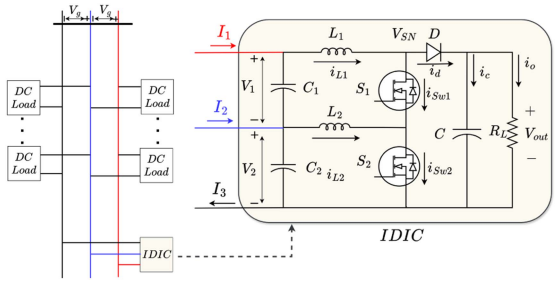


Fig. 7. Schematic of IDIC.

III. Analysis, Modeling, and Design of IDIC

A. Synthesis of Dual-Input-Single-Output Topology

Fig. 7 shows the schematic of the proposed IDIC topology interfaced to two series-connected dc sources (V_1 and V_2). This architecture has been derived from a conventional boost converter by replacing its controlled switch with series-connected switches. Each of the input sources is connected to the switch node through an inductor. The current in the topmost inductor L_1, which is connected with the V_1 source is unidirectional, while current through the L_2 inductor is bidirectional in nature. The power drawn from individual sources depends upon the average current of the inductor connected to the terminal of that particular source. The converter architecture facilitates power processing, wherein the control of power from each of the individual sources is possible.

B. Analysis and Modeling of IDIC

The proposed IDIC topology operates through three distinct states within a switching cycle. Fig. 8 shows different modes of operation of the converter and the corresponding states for the converter. Fig. 8(a) shows a condition when both the inductor currents are positive, and hence V_2 source is supplying more power than V_1 source (Mode-I). Fig. 8(b) shows a scenario when V_2 source is supplying less power than V_1 source and the average current through L_2 inductor is negative (Mode-II). Fig. 8(c) shows the condition when the L_2 inductor current is both positive and negative, the power drawn from the V_2 source depends on the average value of L_2 inductor current (Mode-III).

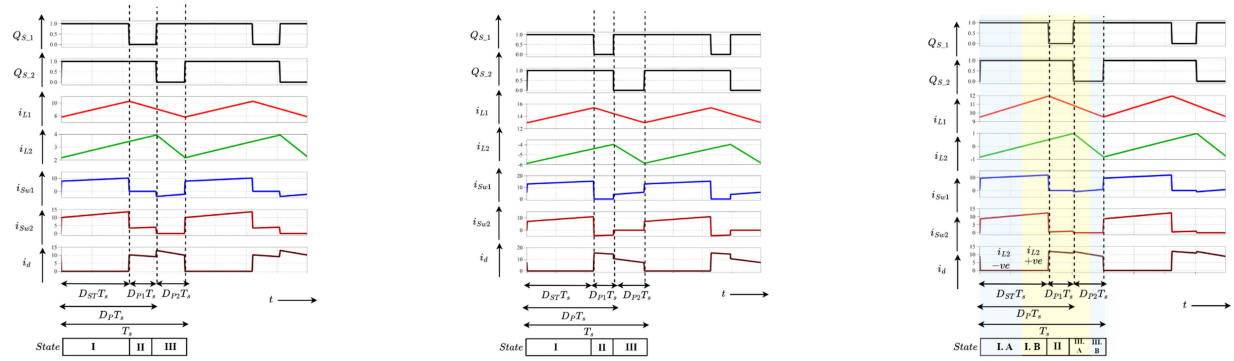


Fig. 8. Different modes of operation of IDIC. (a) Positive L_2 inductor current (i_{L2}). (b) Negative L_2 inductor current (i_{L2}). (c) Positive and negative L_2 inductor current (i_{L2}).

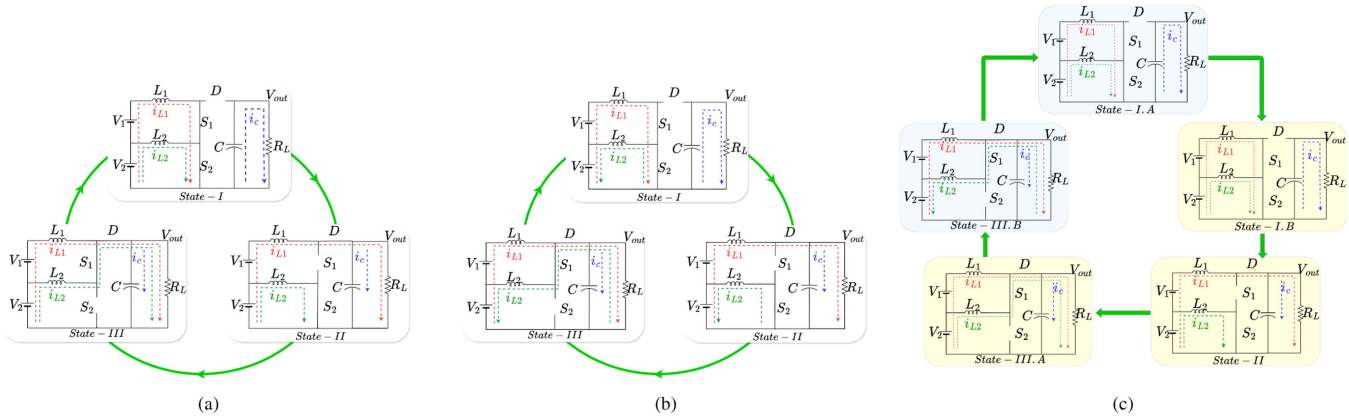


Fig. 9. Converter operation during different modes of operation. (a) Positive L_2 inductor current (i_{L2}). (b) Negative L_2 inductor current (i_{L2}). (c) Positive and negative L_2 inductor current (i_{L2}).

The analysis of the converter is performed in Mode-I operation. In $State$-I, both the switches (S_1 and S_2) are ON for duration $D_{\text{ST}} \cdot T_s$, where T_s is the time period (switching frequency f_s) and D_{ST} is shoot-through duty ratio [see Fig. 9(a)]. Both the inductor currents have positive slopes during this mode. The system equations during $State$-I are given by (5), where, r_{L1}, r_{L2}, and r_C are the series resistance of inductor L_1, L_2 and capacitor (C), respectively

$$\left.\begin{aligned} L_1 \tfrac{dI_{L1}}{dt} &= V_1 + V_2 - I_{L1} r_{L1} \\ L_2 \tfrac{dI_{L2}}{dt} &= V_2 - I_{L2} r_{L2} \\ C \tfrac{dV_c}{dt} &= -\tfrac{V_{out}}{R_L} \\ V_{\text{out}} &= V_c \tfrac{R_L}{r_C + R_L} \end{aligned}\right\} \tag{5}$$

In $State$-II, switch S_1 is OFF and S_2 is ON. The time duration of this state is $D_{P1} \cdot T_s$, where D_{P1} is the duty ratio of this interval and $D_{ST} + D_{P1} = D_P$ is total duty ratio for the V_2 source [see Fig. 9(a)]. The current in inductor L_1 freewheels through the diode to the load with a negative slope, while inductor L_2 current flows through switch S_2 with a positive slope. The system equations corresponding to $State$-II are given by the following:

$$\left.\begin{aligned} L_1 \tfrac{dI_{L1}}{dt} &= V_1 + V_2 - I_{L1} r_{L1} - V_{\text{out}} \\ L_2 \tfrac{dI_{L2}}{dt} &= V_2 - I_{L2} r_{L2} \\ C \tfrac{dV_c}{dt} &= -\tfrac{V_c}{R_L} + I_{L1} \tfrac{R_L}{r_c + R_L} \\ V_{\text{out}} &= V_c \tfrac{R_L}{r_C + R_L} + I_{L1} \tfrac{R_L r_C}{R_L + r_C} \end{aligned}\right\}. \tag{6}$$

In $State$-III, S_1 is ON and S_2 is OFF. The duration of this stage is $D_{P2} \cdot T_s$, where D_{P2} is the duty ratio of this interval [see Fig. 9(a)]. During this mode, the inductor current L_1 feeds into the load, and the direction of the L_2 inductor current (i_{L2}) can be positive or negative and this depends on the control strategy of the converter which is discussed in the Section IV. The system equations corresponding to $State$-III are given by the following:

$$\left.\begin{aligned} L_1 \tfrac{dI_{L1}}{dt} &= V_1 + V_2 - I_{L1} r_{L1} - V_{\text{out}} \\ L_2 \tfrac{dI_{L2}}{dt} &= V_2 - I_{L2} r_{L2} - V_{\text{out}} \\ C \tfrac{dV_c}{dt} &= -\tfrac{V_{\text{out}}}{R_L} + I_{L1} \tfrac{R_L}{r_c + R_L} + I_{L2} \tfrac{R_L}{r_c + R_L} \\ V_{\text{out}} &= V_c \tfrac{R_L}{r_C + R_L} + I_{L1} \tfrac{R_L r_C}{R_L + r_C} + I_{L2} \tfrac{R_L r_C}{R_L + r_C} \end{aligned}\right\} \tag{7}$$

$$\left.\begin{aligned} L_1\tfrac{dI_{L1}}{dt} &= V_1+V_2-I_{L1}r_{L1}-V_{\text{out}}(1-D_{ST}) \\ L_2\tfrac{dI_{L2}}{dt} &= V_2-I_{L2}r_{L2}-V_{\text{out}}(1-D_P) \\ C\tfrac{dV_c}{dt} &= -\tfrac{V_{\text{out}}}{R_L}+I_{L1}\tfrac{(1-D_{ST})R_L}{r_c+R_L}+I_{L2}\tfrac{(1-D_P)R_L}{r_c+R_L} \\ V_{\text{out}} &= V_c\tfrac{R_L}{r_C+R_L}+I_{L1}\tfrac{(1-D_{ST})R_Lr_C}{R_L+r_C}+I_{L2}\tfrac{(1-D_P)R_Lr_C}{R_L+r_C} \end{aligned}\right\}. \tag{8}$$

Evaluating the system dynamics in each state, the converter average model can be derived based on two fundamental duty ratios of the converter (i.e., D_{ST} and D_P). The output voltage and the L_1 inductor current of the converter are regulated by D_{ST} duty ratio, whereas the L_2 inductor current is regulated by D_P duty ratio. The average model of the converter can be expressed by (8). The inductor currents i_{L1} and i_{L2} and the capacitor voltage (v_C) are chosen as the states of the converter. The average model equation of the converter is perturbed and the small signal model of the converter is derived, neglecting the higher order perturbed terms. The small signal state-space model of the converter is given by (9). In the expression (9), the matrices A, B, and C show the relation between the dynamic quantity of the states with the small signal perturbed converter states ($\widetilde{i_{L1}}$, $\widetilde{i_{L2}}$, and $\widetilde{v_C}$), input voltages ($\widetilde{v_1}$ and $\widetilde{v_2}$) and the duty ratios ($\widetilde{d_{\text{ST}}}$ and $\widetilde{d_P}$), respectively. The values of the state space matrix coefficients of matrix A, B, and f are given by (10), (11), and (12), respectively, where $\alpha=\frac{R_L}{R_L+r_C}$

$$\begin{bmatrix}\dot{\widetilde{i_{L1}}}\\ \dot{\widetilde{i_{L2}}}\\ \dot{\widetilde{v_c}}\end{bmatrix}=\underbrace{\begin{bmatrix}a_{11}&a_{12}&a_{13}\\ a_{21}&a_{22}&a_{23}\\ a_{31}&a_{32}&a_{33}\end{bmatrix}}_{A}\begin{bmatrix}\widetilde{i_{L1}}\\ \widetilde{i_{L2}}\\ \widetilde{v_c}\end{bmatrix}+\underbrace{\begin{bmatrix}b_{11}&b_{12}\\ b_{21}&b_{22}\\ b_{31}&b_{32}\end{bmatrix}}_{B}\begin{bmatrix}\widetilde{v_1}\\ \widetilde{v_2}\end{bmatrix}+\underbrace{\begin{bmatrix}f_{11}&f_{12}\\ f_{21}&f_{22}\\ f_{31}&f_{32}\end{bmatrix}}_{f}\begin{bmatrix}\widetilde{d_{\text{ST}}}\\ \widetilde{d_P}\end{bmatrix} \tag{9}$$

$$\left.\begin{aligned} a_{11} &= -\tfrac{r_{L1}+(1-D_{\text{ST}})^2\alpha r_C}{L_1};\ a_{12}=-\tfrac{(1-D_{\text{ST}})(1-D_P)\alpha r_C}{L_1} \\ a_{13} &= -\tfrac{\alpha(1-D_{\text{ST}})}{L_1};\ a_{21}=-\tfrac{(1-D_{\text{ST}})(1-D_P)\alpha r_C}{L_2} \\ a_{22} &= -\tfrac{r_{L2}+(1-D_P)^2\alpha r_C}{L_2};\ a_{23}=-\tfrac{\alpha(1-D_P)}{L_2} \\ a_{31} &= \tfrac{\alpha(1-D_{\text{ST}})}{C};\ a_{32}=\tfrac{\alpha(1-D_P)}{C};\ a_{31}=-\tfrac{1}{C(R_L+r_C)} \end{aligned}\right\} \tag{10}$$

$$b_{11}=b_{12}=\tfrac{1}{L_1};\ b_{21}=0;\ b_{22}=\tfrac{1}{L_2};\ b_{31}=b_{32}=0 \tag{11}$$

$$\left.\begin{aligned} f_{11} &= \tfrac{\alpha V_c+\alpha I_{L1}r_C(1-D_{\text{ST}})+\alpha I_{L2}r_C(1-D_P)}{L_1};\ f_{12}=0 \\ f_{21} &= 0;\ f_{22}=\tfrac{\alpha V_c+\alpha I_{L1}r_C(1-D_{\text{ST}})+\alpha I_{L2}r_C(1-D_P)}{L_2} \\ f_{31} &= -\tfrac{\alpha I_{L1}}{C};\ f_{32}=-\tfrac{\alpha I_{L2}}{C} \end{aligned}\right\}. \tag{12}$$

Neglecting the nonidealities of the converter ($r_C=0$ and $r_{L1}=r_{L2}=0$), the plant transfer function for the current mode control of the converter is given by

$$G_P=\frac{\widetilde{v_{\text{out}}}}{\widetilde{i_{L1}}}=\frac{s\left(\frac{(1-D_{\text{ST}})V_{\text{out}}}{L_1C}-\frac{sI_{L1}}{C}\right)}{\left(s^2+\frac{s}{R_LC}+\frac{(1-D_P)^2}{L_2C}\right)\frac{V_{\text{out}}}{L_1}+\frac{s(1-D_{\text{ST}})I_{L1}}{L_1C}}. \tag{13}$$

The system equations for different states are derived considering current through the L_2 inductor (i_{L2}) is positive [i.e., from source to load (Mode-I)] for all the cases. However, depending on the control scheme the direction of the current through the inductor L_2 may change which subsequently alters the sign of I_{L2} used in the system equations. The corresponding path of the inductor current for L_2 inductor current negative (Mode-II) and both negative–positive (Mode-III) are shown in Fig. 9(b) and (c), respectively.

To alleviate the dependence on the L_2 inductor current, the plant transfer function of the converter can be realized using the current mode control plant transfer function of the boost converter. A decoupled term is introduced with the output of the voltage controller to generate the L_1 inductor current reference of the converter. The decoupled term is derived by implementing the charge balance concept on the output capacitor. The ideal expression for the capacitor current of the converter is given by

$$i_C=C\frac{dV_{\text{out}}}{dt}=-\frac{V_{\text{out}}}{R_L}+I_{L1}(1-D_{\text{ST}})\pm I_{L2}(1-D_P). \tag{14}$$

In steady-state conditions, due to charge balance, the average value of the capacitor current over a switching period is zero. Hence, the average value of the L_1 inductor current (I_{L1}) is obtained by equating (14) to zero. The expression for I_{L1} is expressed by the following:

$$-\frac{V_{\text{out}}}{R_L}+I_{L1}(1-D_{\text{ST}})\pm I_{L2}(1-D_P)=0$$
$$I_{L1}=\frac{V_{\text{out}}}{R_L(1-D_{\text{ST}})}\mp I_{L2}\frac{1-D_P}{1-D_{\text{ST}}}. \tag{15}$$

From (15), it can be observed that the I_{L1} currents depends on the value of the L_2 inductor current (I_{L2}). To eliminate the coupling between I_{L1} and I_{L2}, output of the voltage controller i'_{L1_ref} is processed through the decoupler block (i.e., $\pm\frac{1-D_P}{1-D_{ST}}I_{L2}$) and subtracted from i'_{L1_ref}. Furthermore, by introducing the decoupling term, the plant can be treated as a boost converter with a plant transfer given by the following:

$$G_{P_m}=\frac{\widetilde{v_{\text{out}}}}{\widetilde{i_{L1}}}=\frac{\frac{(1-D_{\text{ST}})V_{\text{out}}}{L_1C}-\frac{sI_{L1}}{C}}{\left(s+\frac{1}{R_LC}\right)\frac{V_{\text{out}}}{L_1}+\frac{(1-D_{\text{ST}})I_{L1}}{L_1C}}. \tag{16}$$

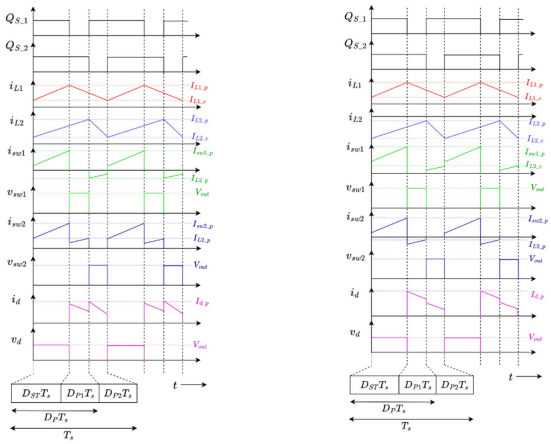
C. Open-Loop Gain of the Converter

Using the average model equations the gain of the converter can be evaluated without considering the nonidealities. The gain of the converter can be expressed in terms of multiple sources or single switches with their associate duty ratios are given by the following:

$$V_{\text{out}}=\frac{V_1+V_2}{1-D_{\text{ST}}}=\frac{V_2}{1-D_P}. \tag{17}$$

D. Mode-0 Operation

Apart from three modes of the converter which are explained earlier, there is another mode of operation in which both the switches of the converters operate simultaneously. The converters operate as conventional boost converters (Mode-0 operation).



(a) (b)

Fig. 10. Waveform of switch and diode currents, and voltages along with the inductor currents and duty pulses (a) when L_2 inductor current is positive and (b) when L_2 inductor current is negative.

In this mode, the I_{L2} current is uncontrolled but the I_{L1} current is controlled. The average voltage across the inductor in this condition is given by (18), which shows the average voltage across the L_2 inductor is negative for all cases. However, in this mode of operation negative current through the inductors is not allowed, for which the I_{L2} current remains in DCM

$$V_{L2} = V_2 D_{\text{ST}} + (V_2 - V_{\text{out}})(1 - D_{\text{ST}}) = -ve. \tag{18}$$

During the start-up process, the converter is operated in this mode, and after reaching the desired output voltage I_{L2} current control is implemented and the converter shifts to the Mode-I, II, or III as per the controller action.

E. Selection of the Switches

The switch of the IDIC are selected based on the power rating of the converter and the peak current of the inductor current considering the maximum allowable current through the inductor. The current through and the voltage across the switches for Mode-I and Mode-II is shown in Fig. 10. The average value of the L_1 inductor current is given by

$$I_{L1(\text{avg})} = \frac{1}{T_s}\left\{ \int_0^{D_{\text{ST}}T_s} \left(I_{L_{1\_c}} + \frac{I_{L_{1\_p}} - I_{L_{1\_c}}}{D_{\text{ST}}T_s} t \right) dt + \int_0^{(1-D_{\text{ST}})T_s} \left(I_{L_{1\_p}} - \frac{I_{L_{1\_p}} - I_{L_{1\_c}}}{(1-D_{\text{ST}})T_s} t \right) dt \right\}. \tag{19}$$

The average value of the L_2 inductor current is given by

$$I_{L2(\text{avg})} = \frac{1}{T_s}\left\{ \int_0^{D_P T_s} \left(I_{L_{2\_c}} + \frac{I_{L_{2\_p}} - I_{L_{2\_c}}}{D_P T_s} t \right) dt + \int_0^{(1-D_P)T_s} \left(I_{L_{2\_p}} - \frac{I_{L_{2\_p}} - I_{L_{2\_c}}}{(1-D_P)T_s} t \right) dt \right\}. \tag{20}$$

The peak value of the L_1 inductor current is given by

$$I_{L1\_p} = I_{L1(\text{avg})} + \frac{V_1 + V_2}{2L_1 f_s} D_{\text{ST}}. \tag{21}$$

The peak value of the L_2 inductor current is given by

$$I_{L2\_p} = I_{L2(\text{avg})} + \frac{V_2}{2L_2 f_s} D_P. \tag{22}$$

The peak value of the S_1 switch for both Mode-I and Mode-II is given by

$$I_{\text{sw1\_p}} = I_{L1(\text{avg})} + \frac{V_1 + V_2}{2L_1 f_s} D_{\text{ST}}. \tag{23}$$

The peak current expression for the L_2 inductor current for Mode-I and Mode-II and is given by

$$I_{\text{sw2\_p}} = \begin{cases} I_{L1\_p} + \left\{ I_{L2\_c} + \frac{V_2}{L_2 f_s} D_{\text{ST}} \right\} : \text{Mode-I} \\ I_{L1\_p} - \left\{ I_{L2\_c} + \frac{V_2}{L_2 f_s} D_{\text{ST}} \right\} : \text{Mode-II}. \end{cases} \tag{24}$$

The peak value of the diode current for Mode-I and Mode-II is given by

$$I_{D\_p} = \begin{cases} I_{L1\_p} - \frac{V_1 + V_2 - V_{\text{out}}}{L_1 f_s} D_{P1} + I_{L2\_p} : \text{Mode-I} \\ I_{L1\_p} : \text{Mode-II}. \end{cases} \tag{25}$$

As the L_1 inductor current should be in CCM for seamless operation, the maximum average value of the L_2 inductor current considering the L_1 inductor current is in boundary condition is given by

$$I_{L2} < \frac{I_P}{1 - D_P} \left\{ \frac{f_s L_1}{R_L D_{\text{ST}}(1 - D_{\text{ST}})} - \frac{1 - D_{\text{ST}}}{2} \right\} \tag{26}$$

where I_P is peak current of L_1 inductor during boundary condition. The DCM condition of I_{L1} will only happen if the I_{L2} current is positive and the value is more than the value given by (26). Moreover, the I_{L1} inductor current will always be in CCM condition when I_{L2} current is negative, hence (26) does not have a negative boundary, however, it is limited by the switch ratings.

Furthermore, there is no as such limitation of the upper value of the L_1 inductor current. However, the upper value of the inductor current cannot be increased indefinitely, the upper limit of the L_1 inductor current is defined by the power rating of the converter and the maximum current limit set by the user. Hence, the S_1 is selected based on the maximum value of the L_1 inductor current. The S_2 is selected depending upon the maximum allowable value of L_1 inductor current or maximum value of the L_2 [(26)] inductor current whichever is higher. Additionally, safety factors can also be considered during the selection of the switches. The flowchart of switch selection is shown in Fig. 11.

F. Selection of Switching Frequency

The switching frequency of the converter depends on the permissible value of the inductor current ripple and the DCM condition of the L_1 inductor current. The expression of ripple content of the L_1 and L_2 inductor currents are given by

$$\Delta i_{L1} = \frac{V_1 + V_2}{f_s L_1} D_{\text{ST}}; \Delta i_{L2} = \frac{V_2 - V_{\text{out}}}{f_s L_2} D_{P2}. \tag{27}$$

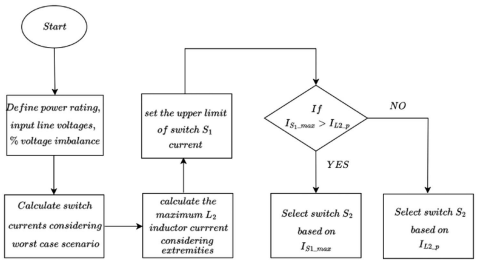


Fig. 11. Flowchart to select current ratings of the switches.

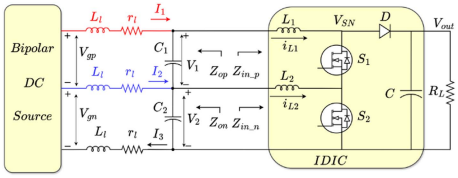


Fig. 12. Connection of IDIC with source and load.

However, as mentioned before for seamless operation the L_1 inductor current should be in CCM and to maintain this the minimum switching frequency of the converter is given by

$$f_s > \frac{R_L T_s D_{\rm ST}(1-D_{\rm ST})}{L_1}\left\{\frac{1-D_{\rm ST}}{2}+\frac{(1-D_P)I_{L2}}{I_P}\right\}. \tag{28}$$

Hence, the maximum switching frequency of the converter can be defined by the user as per the defined ripple content in the inductor currents, the value of the inductances (i.e., L_1 and L_2) and the maximum switching frequency of the switches. However, the minimum switching frequency is restricted by converter operation and given by (28).

IV. Control Strategy of IDIC

The control structure for IDIC consists of an outer voltage loop to regulate the output voltage. Each of the inductor currents is regulated using current-programmed control. The control methodology, current controller and voltage controller are as follows.

A. Control Methodology

Fig. 12 shows the connection of IDIC with the source or the bipolar line which represents the converter highlighted in Fig. 1. The impedance grouping of the source side and the load side has been done as per [34]. The input side terminal voltages of the converter are measured and the current references can be determined to achieve power flow management and the desired converter input impedance. The input power depends on the voltage level of the sources and the inductor current, and the expression of the power is given by (29). Here, P_p represents the amount of power drawn when L_2 inductor current is positive, hence, I_2 is positive. Under this scenario, the maximum power drawn from the negative line is limited by (26). P_n in (29) represents the power drawn when I_2 current is negative and in this condition, the maximum power drawn from the positive line is limited by the switch current limits of the converter

$$\left.\begin{aligned} P_p &= V_1 \times I_1 + V_2 \times (I_1 + I_2) \\ P_n &= V_1 \times I_1 + V_2 \times (I_1 - I_2) \end{aligned}\right\}. \tag{29}$$

The current drawn from the bipolar dc source with respect to the positive and negative line are I_1 and $I_1 \pm I_2$, respectively. The input current to the converter I_1 and I_2 are the same as the L_1 and L_2 inductor current, respectively. Hence, power flow management is done by controlling the respective inductor currents. Based on the voltage imbalance of the line when more power needs to be drawn from the negative line (i.e., $V_2 > V_1$), the L_2 inductor current reference $i_{L2\_\rm ref}$ is set to a positive value. Similarly, if the positive line has more stability margin (i.e., $V_1 > V_2$) the L_2 inductor current reference $i_{L2\_\rm ref}$ is set negative. For balanced conditions, the L_2 inductor current reference $i_{L2\_\rm ref}$ is set to zero or slightly positive or negative as per the deviation of the line voltage. Furthermore, the positive line impedance ($Z_{\rm in\_}p$) and negative line input impedances ($Z_{\rm in\_}n$) of the converter is expressed by (30) and (31), respectively

$$Z_{\rm in\_}p = \frac{V_{\rm out}^2}{P}(1-D_{\rm ST})^2\left\{1 \pm \frac{I_{L2}(1-D_P)}{I_{L1}(1-D_{\rm ST})}\right\}\frac{V_1}{V_1+V_2} \tag{30}$$

$$Z_{\rm in\_}n = \frac{V_{\rm out}^2}{P}(1-D_P)^2 \left\{\frac{I_{L1}(1-D_{\rm ST})}{(I_{L1}\pm I_{L2})(1-D_{\rm ST})} \pm \frac{I_{L2}}{I_{L1}\pm I_{L2}}\right\}. \tag{31}$$

An illustrative diagram is shown in Fig. 12, where IDIC is feeding a CPL while connected to a bipolar dc grid. The grid side voltages for the positive and negative lines are V_{gp} and V_{gn}, respectively. It is assumed that the positive line is more loaded than the negative line, and due to this, the converter side voltage V_1 is less than V_2. Hence, $Z_{\rm in\_}P$ is less than $Z_{\rm in\_}n$ if the same amount of current is drawn from both of the lines ($I_{L2} = 0$). The power contributed by the positive line and negative line when I_{L2} is zero is P_1 and P_2, respectively. The maximum and minimum impedance of the converter is specified for stable operation and the I_{L2} current is varied as per the (32), where $K = (V_1/V_2)^{1/2}$. As the negative line is less loaded, more current can be drawn from this line and the new power shared by the line is P_2'. Similarly, the load on the positive line can be minimized and the new power drawn from the positive line is P_1'. This is achieved by setting the I_{L2} current to a positive value, hence, the $Z_{\rm in\_}p$ will increase, and $Z_{\rm in\_}n$ will decrease based on the voltage levels and current shared by the lines. The power sharing between two lines and the operating points are shown in Fig. 13

$$I_{L2} = (I_1 - KI_3)/(1+K). \tag{32}$$

For better understanding, a load of 120 W is connected with IDIC, and the line input voltages to the converter are $V_1 = 10$ V and $V_2 = 12$ V (i.e., $V_1 < V_2$). The line inductance and resistance were 0.97 mH and 0.121 mΩ, respectively. The value of the decoupling capacitors are 200 μF. Based on the voltage magnitude the negative line is healthier than the positive line and more power can be drawn from the negative line with I_{L2} current control. Fig. 14 shows the comparative analysis of the

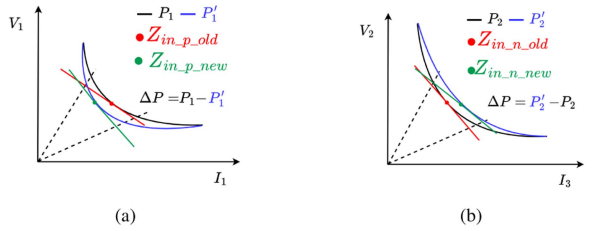


Fig. 13. Input impedance of the converter (a) for positive line and (b) for negative line.

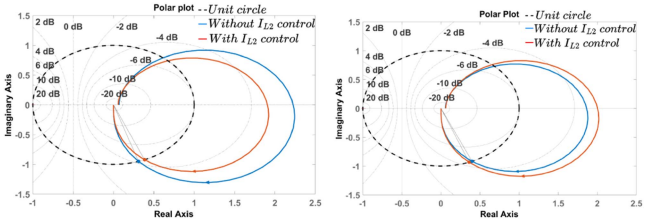


Fig. 14. Polar plot of $\frac{|Z_o|}{|Z_{\text{in}}|}$. (a) For positive line. (b) For negative line.

stability margin of the positive and negative line by using polar plots with and without I_{L2} current control. From Fig. 14(a), it is observed that the PM of $\frac{|Z_{\text{op}}|}{|Z_{\text{in\_}p}|}$ increases by 8° due to I_{L2} current control. Whereas, from Fig. 14(b) it is observed that the PM of $\frac{|Z_{\text{on}}|}{|Z_{\text{in\_}n}|}$ reduces by 2°. In other words, the positive line loading has been reduced by 9.14% (I_1 reduces from 5.454 to 4.955 A), whereas the negative line loading increased by 7.08% (I_3 increases from 5.454 to 5.87 A). Therefore, while powering a CPL using IDIC, the weaker line (i.e., positive line) is less affected than the healthier line (i.e., negative line). Furthermore, the reduction in the stability margin of the negative (healthier) line is less significant compared to the improvement in the stability margin of the positive line. However, the I_{L2} current can not be increased indefinitely, for proper converter operation I_{L1} current should be continuous and the limit of I_{L2} current is given by (26).

Nevertheless, as per the PM criterion, keeping the PM above 60° for stable operation is recommended. Hence, $|Z_{\text{in}}|$ of the converter for any input port can not be reduced indefinitely as a decrease in $|Z_{\text{in}}|$ reduces the PM of that line associated with the input port. The PM of the impedance ratio of the negative line $\frac{|Z_o|}{|Z_{\text{in}}|}$ should be above 70° by introducing a safety factor of 10°.

B. Relationship Between Inductor Currents With Variation in Voltage Unbalance

The relationship between inductor currents with the unbalance in the pole voltages is derived using (32) and (33) expressed by (34)

$$I_3 = I_{L1} + I_{L2}; I_{L1} = I_1 \tag{33}$$

$$\frac{I_{L2}}{I_{L1}} = 1 - \sqrt{\frac{V_1}{V_2}}. \tag{34}$$

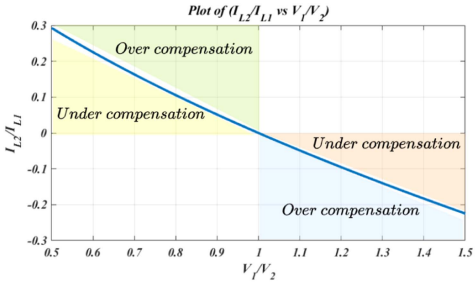


Fig. 15. Plot of change in $\frac{I_{l2}}{I_{L1}}$ with respect to change in $\frac{V_1}{V_2}$.

TABLE I
VOLTAGE UNBALANCE AND PERCENTAGE CHANGE IN LOADING DUE TO I_{L2} CURRENT CONTROL

	V_1	V_2	$\%UB$	$\%VUF$	I_1	I_3	I_{L2}/I_{L1}	I_{1_c}	I_{3_c}	$\%I_1$	$\%I_3$
Variation in V_1	9	12	25.00	28.57	5.714	5.714	0.1340	5.308	6.019	-7.11	5.33
	10	12	16.67	18.18	5.455	5.455	0.0871	5.207	5.661	-4.54	3.78
	11	12	8.33	8.70	5.217	5.217	0.0426	5.104	5.321	-2.17	1.99
	12	12	0.00	0.00	5.000	5.000	0.0000	5.000	5.000	0.00	0.00
	13	12	-8.33	8.00	4.800	4.800	-0.0408	4.896	4.696	2.00	-2.17
	14	12	-16.67	15.38	4.615	4.615	-0.0801	4.793	4.409	3.84	-4.48
	15	12	-25.00	22.22	4.444	4.444	-0.1180	4.691	4.137	5.54	-6.92
Variation in V_2	12	9	-33.33	28.57	5.714	5.714	-0.1547	6.120	5.173	7.10	-9.47
	12	10	-20.00	18.18	5.455	5.455	-0.0954	5.702	5.158	4.54	-5.44
	12	11	-9.09	8.70	5.217	5.217	-0.0445	5.331	5.094	2.17	-2.37
	12	12	0.00	0.00	5.000	5.000	0.0000	5.000	5.000	0.00	0.00
	12	13	7.69	8.00	4.800	4.800	0.0392	4.704	4.889	-2.00	1.85
	12	14	14.29	15.38	4.615	4.615	0.0742	4.438	4.767	-3.84	3.29
	12	15	20.00	22.22	4.444	4.444	0.1056	4.198	4.641	-5.54	4.43
Considering extremities	9	15	40.00	50.00	5.000	5.000	0.2254	4.383	5.370	-12.35	7.41
	15	9	-66.67	50.00	5.000	5.000	-0.2910	5.612	3.979	12.25	-20.41

Fig. 15 shows the variation in the ratio of $\frac{I_{l2}}{I_{L1}}$ with respect to the change in ratio of $\frac{V_1}{V_2}$. From this figure, it can be said that when the V_2 voltage is less compared to V_1 the I_{L2} current will be negative and I_{L2} current is positive when V_1 is more than V_2. The blue line shows the operating line in which the overall input impedance of the converter is maximum. The zones are also mentioned for overcompensation and undercompensation. Table I shows the imbalance in the voltage and the corresponding change in the I_1 (positive line current) and I_3 negative line current, load power considered is 120 W. $\%UB$ is the percentage unbalance in the voltage with respect to the V_2 voltage. In the table, I_1 and I_3 show the line currents if the load is connected to a conventional two-port converter, and I_{1_C} and I_{2_C} show the line current after connecting the load using IDIC. Through this current control methodology, the stress on the weaker line (low voltage line) is reduced in cost of increased stress on the healthier line (voltage is more). Furthermore, from Table I, it is also evident that the percentage reduction in load in the weaker line is more than the increase in stress in the healthier line. In the extreme conditions, it is shown that the reduction in stress in the low voltage line is 20.41%, whereas the increase in stress in the high voltage line is 12.25%. Furthermore, the converter can also be used in under or overcompensating region if further reduction of stress in the lines are required.

C. Voltage Tolerance Level of the Converter

The converter specifications are: $L_1, L_2 = 100\ \mu H$, $f_s = 50$ kHz, Load power = 120 W, $V_1, V_2 = 12$ V (nominal voltage), $V_{\text{out}} = 48$ V and switch current limit 20 A.

1) Case 1: When $(V_1 > V_2)$*:* Under this scenario, the minimum value of the negative line voltage is limited by the maximum duty ratio (D_P) of the converter that is 0.9. Hence, the minimum permissible value of the V_2 voltage is $48 \times (1 - 0.9) = 4.8$ V. Considering the diode voltage drop of 0.7 V, inductor resistance drop and switch drop, the value of V_2 voltage is 5.65 V. Hence, the converter can not tolerate the negative voltage below 5.65 V for seamless operation. Now considering $V_1 = 6$ V and $V_2 = 5.65$ V ($V_1 > V_2$), the maximum current through the switch is 13.38 A. Hence, the considered switch rating is higher than the maximum switch current and the converter can tolerate this condition.

2) Case 2: When $(V_2 > V_1)$*:* When the positive line voltage (V_1) is less than the negative line voltage (V_2), the tolerance limit is set by the maximum allowable L_2 inductor current [as per (26)] and switch ratings. Keeping the negative line voltage (V_2) fixed to its minimum value of 5.65 V and reducing the positive pole voltage V_1 to 2.9 V the maximum current through switch S_2 is 19.48 A. Hence, further reduction in the V_1 voltage will result in a higher current through the switches and may hit the maximum limit of switch current ratings. Therefore, the minimum tolerable value of the positive pole voltage is $2.9 \approx 3$ V.

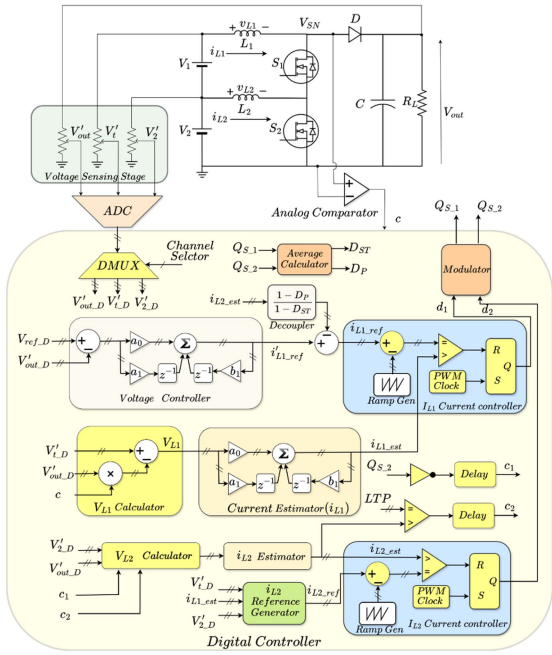


Fig. 16. Detailed diagram of the control scheme implementation using a digital controller.

D. Voltage and Current Controller

The outer voltage loop of the converter is implemented using a PI controller. The output voltage of the converter is compared with the reference voltage to generate the error signal. The error signal is processed by the PI controller to generate the current reference for L_1 inductor current. Peak current mode control is considered for the current controller. Ramp compensation is used to overcome the subharmonic instability in the inductor current. The slope of the L_1 and L_2 inductor currents for different states of operation are given as follows:

$$m_{L1} = \begin{cases} \frac{V_1+V_2}{L_1} & : \text{State-I} \\ \frac{V_1+V_2-V_{out}}{L_1} & : \text{State-II} \\ \frac{V_1+V_2-V_{out}}{L_1} & : \text{State-III} \end{cases}; \quad m_{L2} = \begin{cases} \frac{V_2}{L_2} & : \text{State-I} \\ \frac{V_2}{L_2} & : \text{State-II} \\ \frac{V_2-V_{out}}{L_2} & : \text{State-III.} \end{cases} \tag{35}$$

The L_1 inductor current rises during State-I and falls during State-II and State-III. In case of L_2 inductor current, it rises during State-I and State-II and falls during State-III. Based on the falling slope of the inductor current the slope of the ramp (m_c) is calculated and subtracted from the generated current reference from the voltage controller. In this control approach, the inductor currents are estimated internally using the same digital controller used to control the converter.

E. Inductor Current Estimation

The proposed IDIC is operated using the digital peak current mode control technique. Hence, the inductor current feedback is very crucial for seamless operation of the converter. However, in this case, instead of sensing the inductor currents, they are estimated within the same processor used to control the converter. The current estimation scheme presented in [36] is implemented to estimate both the inductor currents. The detailed control scheme is represented in Fig. 16.

The continuous domain transfer function of the current estimator block is given by

$$G_{\text{est}} = \frac{i_{L\_\text{est}}}{v_L} = \frac{1}{sL + r_L} \tag{36}$$

where i_{L_est}, v_L, L, and r_L are the estimated inductor current, voltage across the inductor, inductance, and inductor resistance, respectively.

In (36), the transfer function is known, hence, the inductor current is estimated by using the voltage across the inductor (v_L) in different switching intervals. The voltage across the inductors can not be measured directly (due to its switching nature), hence it is indirectly calculated in different switching intervals using the terminal voltages and the switch status (i.e., ON/OFF). The ON/OFF status of the combination of S_1 and S_2 switch is detected using an analog comparator see Fig. 16). As per the converter operation, the current through the L_1 inductor current is continuous in nature. Hence, the voltage across L_1 inductor (v_{L1}) can be calculated using the analog comparator signal (c) and the terminal voltages of the converter. When both the switches (S_1 and S_2) are ON, the output of the comparator signal (c) is low (zero) and when any of the switches are OFF, c is high (one). The corresponding voltages (v_{L1}) across the inductor L_1 in different switching intervals are provided in Table II.

In the case of L_2 inductor, The PWM signal (Q_{S_2}) is used to generate an internal comparator signal c_1. However, due to

TABLE II
VOLTAGE ACROSS THE INDUCTOR AND COMPARATOR SIGNALS IN DIFFERENT STATES OF THE IDIC

v_{L1}		v_{L2}				
CCM		CCM		DCM		
c	v_{L1}	c_1	v_{L2}	c_1	c_2	v_{L2}
0	$v_1 + v_2$	0	v_2	0	0	v_2
1	$v_1 + v_2 - v_{out}$	1	$v_2 - v_{out}$	0	1	0
				1	0	$v_2 - v_{out}$
				1	1	0

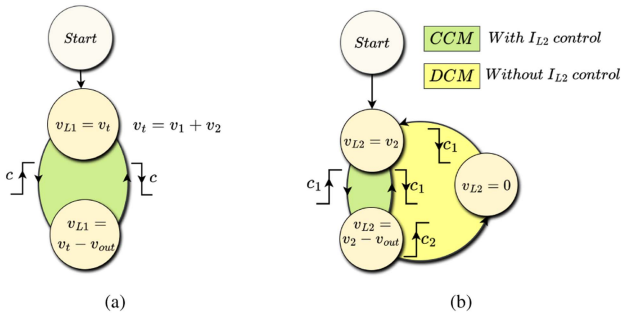


Fig. 17. State machine based inductor voltage calculation. (a) L_1 inductor voltage (v_{L1}). (b) L_2 inductor voltage (v_{L2}).

the startup process of the converter, L_2 inductor current will have discontinuous conduction mode (DCM) (Mode-0). Hence, to detect the DCM another internal digital comparator c_2 is introduced. However, when I_{L2} current is controlled the L_2 inductor current operates in continuous conduction mode (CCM) and the c_2 comparator signal is neglected under this condition. The voltages (v_{L2}) across the inductor L_2 in different switching intervals for both CCM and DCM conditions are provided in Table II. The state machine-based transition of inductor voltage in different switching intervals is depicted in Fig. 17 where the state-to-state transition is triggered by the comparator signals. Moreover, the analog comparator aids in the protection of the converter as it is also used to detect the fault of the switches.

To estimate the inductors' current digitally the continuous domain transfer function (36) of the current estimator is discretized using the bilinear transformation. The digital equivalent equation of the current estimation is represented by the following:

$$i_{L\_\text{est}}[n] = \frac{T_s}{2L + r_L T_s} \cdot v_L[n] + \frac{T_s}{2L + r_L T_s} \cdot v_L[n-1] + \frac{2L - r_L T_s}{2L + r_L T_s} \cdot i_{L\_\text{est}}[n-1]$$
$$i_{L\_\text{est}}[n] = a_0 \cdot v_L[n] + a_1 \cdot v_L[n-1] + b_1 \cdot i_{L\_\text{est}}[n-1]. \quad (37)$$

Here, a_0, a_1, and b_1 are the coefficients of the discrete equation. These coefficient values depend on the inductor parameter (r_L and L) and the sampling time (T_s) of the processor. This digital equation can be realized using different formats. In this work, it is implemented as an IIR filter to get the estimate of the inductor current.

V. IMPLEMENTATION AND VALIDATION OF IDIC OPERATION

A. Design and Implementation of the System

The controller is implemented using the Artix-7-based Basys-3 board. It has a 4-channel, 1 MSPS ADC within the board. The detailed digital implementation of the control scheme is shown in Fig. 16. The terminal voltages of the converter are sensed using a resistive divider circuit and then sensed with a 4-channel ADC with a maximum sample rate of 1-MSPS. The voltage controller for the outer voltage loop is implemented using a digital PI controller. The digital value of the sensed output voltage of the converter ($V'_{\text{out\_}D}$) is subtracted from the reference output voltage ($V_{\text{ref\_}D}$) and the error signal is processed through the PI controller to generate the L_1 inductor current reference signal i'_{L1_ref}. A feedforward term [as per (15)] is introduced and subtracted from the i'_{L1_ref} to decouple the L_1 inductor current reference from the effect L_2 inductor current. The new L_1 inductor current reference i_{L1_ref} is fed to the I_{L1} current controller block. In the current controller block, a compensating ramp signal is generated [as per (35)] and subtracted from i_{L1_ref}, then the resultant is compared with the estimated L_1 inductor current i_{L1_est} and the output of the comparator is the input to the reset (R) terminal of the SR latch. The set (S) terminal of the latch is triggered using a PWM clk signal of 50 kHz. The output of the SR latch is d_1 which is fed to the modulator block as an input signal. The voltage across the L_1 inductor (V_{L1}) is calculated as per Table II using the digital value of the sensed terminal voltages of the converter (V'_{t_D} and $V'_{\text{out\_}D}$) and the comparator signal (c). The calculated voltage is processed through the current estimator block to generate the estimated value of the L_1 inductor current i_{L1_est}. In the case of L_2 inductor current the voltage across it (V_{L2}) is calculated as per the Table II using V'_{2_D} and $V'_{\text{out\_}D}$ voltages and the internally generated comparator signal c_1 and c_2. The calculated value of V_{L2} is processed through the current estimator block to estimate i_{L2_est}. The estimated value of the L_2 inductor current is fed to I_{L2} current controller block where it is compared with the L_2 inductor current reference (i_{L2_ref}) which is generated using V'_{t_D}, V'_{2_D}, and i_{L1_est} as per (34). The working principle of the L_2 inductor current controller is the same as the L_1 current controller except the compensating ramp signal which is generated based on the L_2 inductor current falling slope. The output of the I_{L2} current controller is d_2 which is fed to the modulator as an input. Using the d_1 and d_2 signal the switching signal for S_1 and S_2 switch is generated (i.e., Q_{S_1} and Q_{S_2}) by the modulator.

B. Hardware Verification of IDIC

The proposed IDIC is validated using a laboratory-scale hardware prototype (see Fig. 18). The system specification of the system is given in Table III. Two dc sources are connected in series to realize a bipolar dc microgrid system. The converter is operated in the aforementioned modes and the practical results are shown in this article. Fig. 19 shows the steady-state operation of the converter when I_{L2} current is uncontrolled, and it is in DCM (Mode-0) condition. The output voltage of the converter is maintained at 48 V, and the load power is 120 watts. Fig. 20(a)

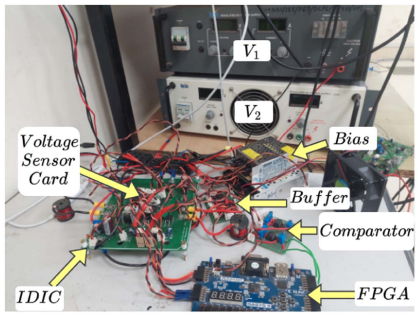
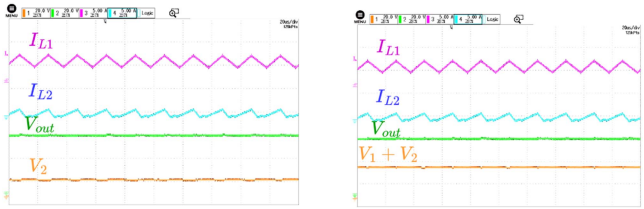


Fig. 18. Testbed of the proposed converter.

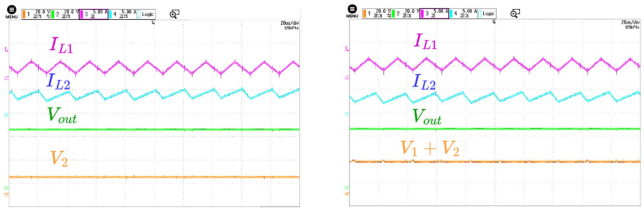
TABLE III
SYSTEM SPECIFICATION OF LABORATORY TESTBED

System Parameters	Specification	System Parameters	Specification
Voltage Source(V_1)	12 V	Output Voltage(V_{out})	48 V
Voltage Source(V_2)	11–17 V	Switching frequency	50 kHz
Inductor(L_1, L_2)	100 μH, 0.032 Ohm	Digital Controller	Artix-7
Capacitor(C)	200 μF, 60 V	Power rating	120–200 W
MOSFETs(S_1, S_2)	FDB52N20TM	Diode(D)	MUR1520



(a) (b)

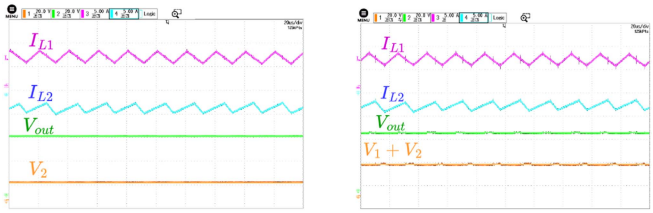
Fig. 19. Steady-state condition in Mode-0 (without I_{L2} current control). (a) V_2 terminal voltage. (b) $V_1 + V_2$ voltage.



(a) (b)

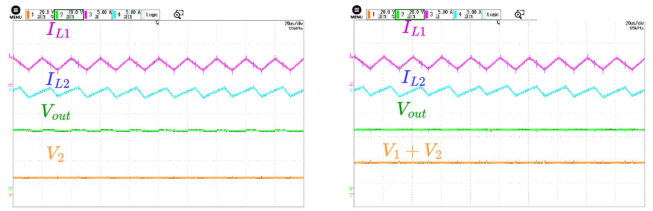
Fig. 20. Steady-state waveform of IDIC in Mode-I with positive L_2 inductor current. (a) V_2 terminal voltage and (b) $V_1 + V_2$ voltage.

and (b) shows the converter performance when I_{L2} is set to a positive value (Mode-I). The average value of I_{L2} is 4.5 A and the average value of I_{L1} current is 2 A. Fig. 21(a) and (b) shows the operating mode of the converter with a negative value of the I_{L2} current (Mode-II). The average value of the I_{L2} current is -4.5A and the average value of the I_{L1} current is 6.5 A. Fig. 22(a) and (b) shows the converter operation with the I_{L2} current control, the average current is close to zero and current is both positive and negative within the switching interval (Mode-III). The average current through the inductors in this mode of operation is $I_{L1} = 4.5$ A and $I_{L2} = -0.5$ A. In each of these results, the terminal voltages of the converters



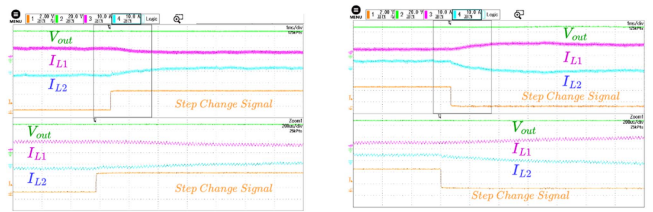
(a) (b)

Fig. 21. Steady-state waveform of IDIC in Mode-II with negative L_2 inductor current. (a) V_2 terminal voltage and (b) $V_1 + V_2$ voltage.



(a) (b)

Fig. 22. Steady-state waveform of IDIC in Mode-III with both positive and negative L_2 inductor current. (a) V_2 terminal voltage and (b) $V_1 + V_2$ voltage.



(a) (b)

Fig. 23. Performance of the converter with (a) step-up change in i_{L2} current and (b) step-down change in i_{L2} current.

are captured. Figs. 20(a), 21(a), and 22(a) show the V_2 terminal voltage, whereas Figs. 20(b), 21(b), and 22(b) show the $V_1 + V_2$ voltage of the converter, respectively. From these results, it can be said that IDIC operation is satisfactory with different modes of operations.

The performance of the proposed converter is also verified with step changes in the operating conditions. An internal MUX is used to change the reference of the L_2 inductor current (I_{L2}) from -3 A to 3 A, the zoomed version of the different parameters are also shown in the captured results [see Fig. 23(a)]. Fig. 23(b) shows the step-down change in the L_2 inductor current when the reference inductor current (I_{L2}) is changed from -4 to 4 A. The experimental results show the dynamic behavior of the converter with different operating points. It can be observed that the converter is capable of drawing different amounts of current from the individual lines. This property of the converter can be used to share the power demand of the load between the positive and negative lines.

The dynamic behavior of the converter is verified during unbalanced pole voltage conditions. The V_2 voltage is varied manually using the regulating knob of the dc voltage source to create a voltage imbalance condition in a bipolar dc microgrid

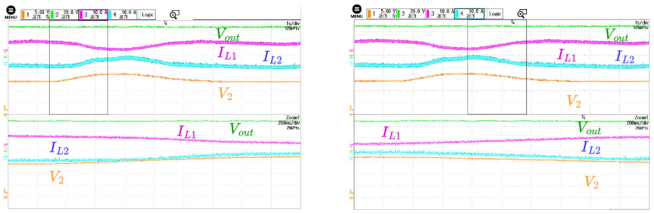


Fig. 24. Variation of L_2 inductor current with variation in V_2 voltage, (a) increase in V_2 voltage, and (b) decrease in V_2 voltage.

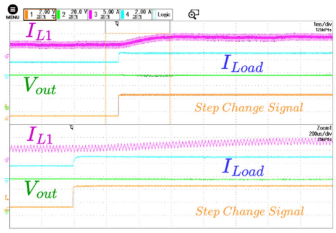


Fig. 25. Performance of the converter with a step change in load current.

system. The V_2 voltage is varied from 11 to 17 V and then back to 11 V. Fig. 24(a) shows the zoomed-in version when I_{L2} current increases due to the increase in V_2 voltage. The increase in I_{L2} current reduces the loading of the positive line as I_{L1} current reduces. Similarly, Fig. 24(b) shows the zoomed-in version when I_{L2} current reduces due to the reduction in V_2 voltage. During this condition, I_{L1} current gradually increases to reduce the loading of the negative line. Hence, as voltage changes the line currents adjust accordingly to minimize the loading effect. The converter is also tested with a step change in the load current. A semiconductor switch with a resistive load is connected in parallel to the output of the converter. Fig. 25 shows the converter performance with a step change in the load current from 2 to 3.6 A (i.e., 80% step change in load). It can be observed from the results that the converter can regulate its output voltage satisfactorily when there is a sudden change in the load.

C. Efficiency Analysis

The efficiency of the converter is obtained in different operating conditions. The losses that are taken into account are the inductor loss, switch conduction loss, switching loss, diode loss, and capacitor loss. The dc resistance of the inductor mentioned in the datasheet is 0.032 Ω. The switch loss of the converter is divided into two categories: the ON-state conduction loss and the switching loss. The ON-state resistance of the switches is 0.041 Ω. In case of S_1, the turn ON switching loss is not present due to the ZVS turn ON by virtue of the PWM control of the converter. The losses in the diode are mainly the conduction losses, which are due to the ON-state resistance loss and diode ON-state voltage drop. The diode voltage drop is 0.7 V and the ON-state resistance is 0.017 Ω. The ohmic losses in the output capacitor is due to the equivalent series resistance (ESR) of the

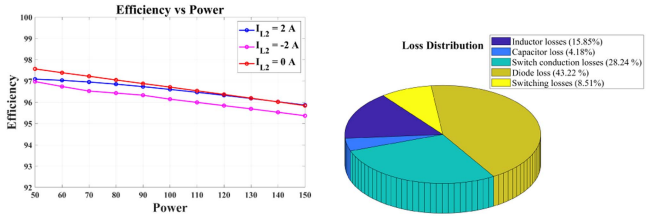


Fig. 26. (a) Efficiency plot of the IDIC converter for different load conditions. (b) Loss distribution of the converter at 120 W load.

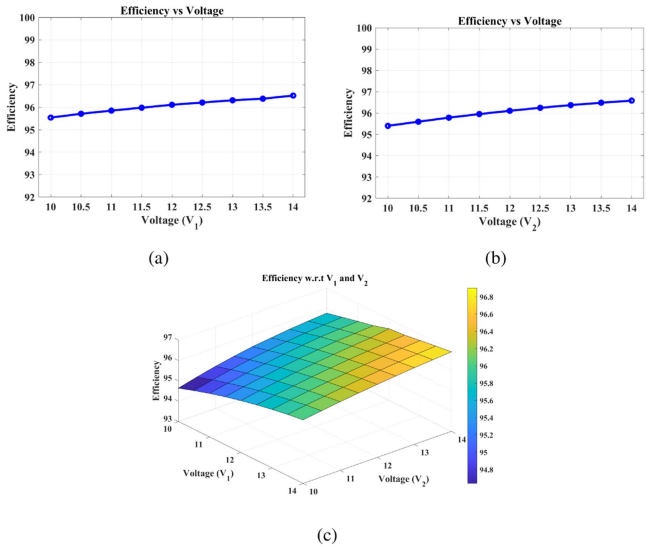


Fig. 27. Efficiency plot of the IDIC converter for different voltage conditions. (a) Fixed V_2 voltage, (b) fixed V_1 voltage, and (c) both V_1 and V_2 varying.

capacitor and the value is 0.054 Ω. Fig. 26(a) shows the efficiency of the converter for different load conditions where the current I_{L2} is varied. Fig. 26(b) shows the percentage break up of the losses in the converter at a load power of 120 W when $I_{L2} = 2$ A.

The efficiency of the converter is evaluated for different values of the line voltages. Fig. 27(a) shows the efficiency plot when the V_2 line voltage is kept constant at 12 V and the V_1 line voltage is varied. Fig. 27(b) similarly shows the efficiency plot when the V_1 line voltage is kept constant at 12 V and the $V21$ line voltage is varied. In each of the cases, the variable voltage is varied from 10–14 V. Fig. 27(c) shows the 3-D surface plot of the converter efficiency when both V_1 and V_2 line voltage is varied. From these results, it can be said that converter efficiency is low (94.6%) when the terminal voltages are low (10 V) and the efficiency increases, and the maximum efficiency achieved is 96.9% when both the terminal voltages are 14 V (the nominal voltage is 12 V).

D. Comparative Analysis With IDIC With Other Bipolar Converters

Dual-input dc–dc converters for a load-side solution to voltage unbalance in bipolar dc distribution systems are reported in [19], [20], [21], [22], [23], [24], and [25]. In [19] and [21],

TABLE IV
COMPARISON OF IDIC WITH OTHER BIPOLAR CONVERTERS IN LITERATURE

Topology	No. of inductors	No. of capacitors	No. of switches	No. of diodes	Output voltage regulation	Voltage unbalance considered	Control Scheme
[19]	1	3	4	Nil	No	12.5 %	Variable resonance frequency and phase shifted control.
[21]	2	4	2	2	No	14 %	DC spring control to divert load to lossy elements.
[22]	1	3	4	Nil	Yes	8.75 %	Coordinated control associated with grid connected converter.
[23]	2	3	4	2	Yes	10 %	Voltage unbalanced based droop control.
[24]	1	2	8	4	Yes	Not mentioned	Phase shifted PWM control to maintain voltage balance.
[25]	2	3	4	Nil	Yes	10% power unbalance in lines was considered	Cascaded phase shifted control to mitigate voltage unbalance through circulating inductor current.
IDIC	2	3	2	1	Yes	40 %	Current mode control based converter input impedance variation during voltage imbalance.

the proposed converter does not regulate the output voltage. The proposed converters in [20], [22], [23], [24], and [25] consist of a higher number of switches. The proposed converter in [21] uses a lossy method to mitigate the voltage unbalance. The proposed converter in [22] requires communication-based control for operation. Tavakoli et al. [23] presented an improved version of the converter presented in [22] by adding an extra inductor. However, due to DCM operation inductor current, the switches experience more stress than the prior one. The converter proposed in [25] consists of a higher number of control loops. The comparison between the converters used in bipolar dc distribution systems as a load-side solution is provided in Table IV.

VI. CONCLUSION

This work presents a three-port dc–dc converter coined as IDIC that can act as an interfacing converter or a front-end converter to a CPL connected to a bipolar dc microgrid. The proposed converter provides a load-side solution to the unbalanced pole voltages and overloading issues associated with bipolar dc microgrids. This article presents the analysis and design of the IDIC and its control methodology to reduce line overloading and to compensate the unbalanced voltages. The converter is capable of processing power from the individual lines seamlessly based on their voltage profile. Moreover, the proposed IDIC utilizes a reduced number of switches as compared to the existing topologies. The operational mechanism of the proposed converter is validated using a laboratory testbed with a switching frequency of 50 kHz and a power rating of 120 W. The designed IDIC can tolerate 53% and 75% reduction in negative and positive line voltages, respectively. Furthermore, results also show that during a 40% unbalanced condition, the overloading of the weaker line can be reduced by 12.35% by increasing the loading of the healthier line by 7.41%. The practical results show a close correlation between the theoretical and practical behavior of the converter. Comparative analysis presented in Section V-D demonstrates the superiority of the proposed IDIC over the existing topologies. The proposed converter can be used for series connected dc sources with different voltage and power levels.

APPENDIX

Losses in Passive Elements: The inductor losses are the ohmic losses due to the inductor dc resistances. The losses in the inductor can be expressed by (38). The loss due to ESR of the capacitor can be expressed by (39)

$$P_{\text{ind}} = \sum_{n=1}^{2} I_{Ln(\text{rms})}^2 r_L \tag{38}$$

$$P_{\text{cap}} = I_{\text{cap(rms)}}^2 r_C. \tag{39}$$

Switch Loss: The switch conduction loss and the switching loss can be expressed by the following:

$$P_S = \sum_{n=1}^{2} I_{swn(\text{rms})} r_{dson} \tag{40}$$

$$P_{\text{Sw\_on}} = \frac{V_{\text{sw}} I_{\text{sw}}}{6} t_{\text{on}} f_s; P_{\text{Sw\_off}} = \frac{V_{\text{sw}} I_{\text{sw}}}{6} t_{\text{off}} f_s. \tag{41}$$

The loss in the diode is expressed by the following:

$$P_D = V_{D(\text{avg})} I_{D(\text{avg})} + I_{D(\text{rms})}^2 r_D. \tag{42}$$

The rms current through the switches are given by

$$I_{\text{sw1(rms)}}^2 = \frac{1}{T_s}\left\{\int_0^{D_{\text{ST}}T_s}\left(I_{L_{1\_c}} + \frac{I_{L_{1\_p}} - I_{L_{1\_c}}}{D_{\text{ST}}T_s}t\right)^2 dt + \int_0^{D_{P2}T_s}\left(I_{L_{2\_p}} - \frac{I_{L_{2\_p}} - I_{L_{2\_c}}}{D_{P2}T_s}t\right)^2 dt\right\} \tag{43}$$

$$I_{\text{sw2(rms)}}^2 = \frac{1}{T_s}\left\{\int_0^{D_{\text{ST}}T_s}\left(I_{L_{1\_c}} + \frac{I_{L_{1\_p}} - I_{L_{1\_c}}}{D_{\text{ST}}T_s}t\right)^2 dt + \int_0^{D_P T_s}\left(I_{L_{2\_c}} + \frac{I_{L_{2\_p}} - I_{L_{2\_c}}}{D_P T_s}t\right)^2 dt\right\}. \tag{44}$$

REFERENCES

[1] V. A. K. Prabhala, B. P. Baddipadiga, and M. Ferdowsi, "DC distribution systems — an overview," in *Proc. Int. Conf. Renewable Energy Res. Appl.*, 2014, pp. 307–312.

[2] K. Strunz, E. Abbasi, and D. N. Huu, "DC microgrid for wind and solar power integration," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 2, no. 1, pp. 115–126, Mar. 2014.

[3] P. A. Madduri, J. Poon, J. Rosa, M. Podolsky, E. A. Brewer, and S. R. Sanders, "Scalable DC microgrids for rural electrification in emerging regions," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 4, pp. 1195–1205, Dec. 2016.

[4] R. Panigrahi, S. K. Mishra, S. C. Srivastava, and P. Enjeti, "Microgrid integration in smart low-voltage distribution systems," *IEEE Power Electron. Mag.*, vol. 9, no. 2, pp. 61–66, Jun. 2022.

[5] S. Rivera, R. L. F, S. Kouro, T. Dragičević, and B. Wu, "Bipolar DC power conversion: State-of-the-art and emerging technologies," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 2, pp. 1192–1204, Apr. 2021.

[6] L. Li, K.-J. Li, K. Sun, Z. Liu, and W.-J. Lee, "A comparative study on voltage level standard for DC residential power systems," *IEEE Trans. Ind. Appl.*, vol. 58, no. 2, pp. 1446–1455, Mar./Apr. 2022.

[7] *IEEE Standard for DC Microgrids for Rural and Remote Electricity Access Applications*, IEEE Standard 2030.10-2021, pp. 1–47, 2021.

[8] Y. Li, K. Sun, Y. Sun, K.-J. Li, J. Lou, and Y. Pang, "A comparative study on power quality standards and interaction analysis for LVDC systems," in *Proc. IEEE Ind. Appl. Soc. Annu. Meeting*, 2022, pp. 1–8.
[9] A. Emadi, A. Khaligh, C. Rivetta, and G. Williamson, "Constant power loads and negative impedance instability in automotive systems: Definition, modeling, stability, and control of power electronic converters and motor drives," *IEEE Trans. Veh. Technol.*, vol. 55, no. 4, pp. 1112–1125, Jul. 2006.
[10] W. Xie, M. Han, W. Yan, and C. Wang, "Stability control strategy for DC micro-grid considering constant power load," in *Proc. IEEE 3rd Int. Conf. DC Microgrids*, 2019, pp. 1–6.
[11] T.-H. Jung, G.-H. Gwon, C.-H. Kim, J. Han, Y.-S. Oh, and C.-H. Noh, "Voltage regulation method for voltage drop compensation and unbalance reduction in bipolar low-voltage DC distribution system," *IEEE Trans. Power Del.*, vol. 33, no. 1, pp. 141–149, Feb. 2018.
[12] F. Wang, Z. Lei, X. Xu, and X. Shu, "Topology deduction and analysis of voltage balancers for DC microgrid," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 2, pp. 672–680, Jun. 2017.
[13] X. Zhang and C. Gong, "Dual-buck half-bridge voltage balancer," *IEEE Trans. Ind. Electron.*, vol. 60, no. 8, pp. 3157–3164, Aug. 2013.
[14] P. Prabhakaran and V. Agarwal, "Novel four-port DC–DC converter for interfacing solar PV-fuel cell hybrid sources with low-voltage bipolar DC microgrids," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 2, pp. 1330–1340, Jun. 2020.
[15] Y. Lin, F. Zhou, G. Xu, W. Xiong, and G. Ning, "Bipolar current-fed DC–DC converter with automatic voltage balance and full range ZVS for bipolar DC system," *IEEE Trans. Power Electron.*, vol. 39, no. 4, pp. 4248–4259, Apr. 2024.
[16] L. Sun, F. Zhuo, F. Wang, and T. Zhu, "A nonisolated bidirectional soft-switching power-unit-based DC–DC converter with unipolar and bipolar structure for DC networks interconnection," *IEEE Trans. Ind. Appl.*, vol. 54, no. 3, pp. 2677–2689, May/Jun. 2018.
[17] S. D. Tavakoli, M. Mahdavyfakhr, M. Hamzeh, K. Sheshyekani, and E. Afjei, "A unified control strategy for power sharing and voltage balancing in bipolar DC microgrids," *Sustain. Energy, Grids Netw.*, vol. 11, pp. 58–68, 2017.
[18] G.-H. Gwon, C.-H. Kim, Y.-S. Oh, C.-H. Noh, T.-H. Jung, and J. Han, "Mitigation of voltage unbalance by using static load transfer switch in bipolar low voltage DC distribution system," *Int. J. Elect. Power Energy Syst.*, vol. 90, pp. 158–167, 2017.
[19] S. Yadav, P. Bauer, and Z. Qin, "Simplified operation and control of a series resonant balancing converter for bipolar DC grids," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 12, no. 4, pp. 4015–4024, Aug. 2024.
[20] H.-J. Byun, S.-H. Kim, S.-H. Kim, J. Yi, and C.-Y. Won, "Input-series-output-parallel DAB converter on energy storage system for voltage balancing strategy in bipolar DC microgrid," in *Proc. 24th Int. Conf. Elect. Mach. Syst.*, 2021, pp. 818–823.
[21] J. Liao, N. Zhou, Y. Huang, and Q. Wang, "Decoupling control for DC electric spring-based unbalanced voltage suppression in a bipolar DC distribution system," *IEEE Trans. Ind. Electron.*, vol. 68, no. 4, pp. 3239–3250, Apr. 2021.
[22] L. Tan, B. Wu, V. Yaramasu, S. Rivera, and X. Guo, "Effective voltage balance control for bipolar-DC-bus-fed EV charging station with three-level DC–DC fast charger," *IEEE Trans. Ind. Electron.*, vol. 63, no. 7, pp. 4031–4041, Jul. 2016.
[23] S. D. Tavakoli, J. Khajesalehi, M. Hamzeh, and K. Sheshyekani, "Decentralised voltage balancing in bipolar DC microgrids equipped with trans-z-source interlinking converter," *IET Renewable Power Gener.*, vol. 10, no. 5, pp. 703–712, 2016.
[24] G. V. d. Broeck, J. Beerten, M. D. Vecchia, S. Ravyts, and J. Driesen, "Operation of the full-bridge three-level DC–DC converter in unbalanced bipolar DC microgrids," *IET Power Electron.*, vol. 12, no. 9, pp. 2256–2265, 2019.
[25] S. Kim, H. Cha, and H.-G. Kim, "High-efficiency voltage balancer having DC–DC converter function for EV charging station," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 1, pp. 812–821, Feb. 2021.
[26] R. Roy, V. I. Kumar, and S. Kapat, "Ripple voltage injection to mitigate limit cycle in digitally controlled intermediate bus architectures," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 3127–3138, Mar. 2020.
[27] Q. Xu, W. Jiang, F. Blaabjerg, C. Zhang, X. Zhang, and T. Fernando, "Backstepping control for large signal stability of high boost ratio interleaved converter interfaced DC microgrids with constant power loads," *IEEE Trans. Power Electron.*, vol. 35, no. 5, pp. 5397–5407, May 2020.
[28] S. Arora, P. Balsara, and D. Bhatia, "Input–output linearization of a boost converter with mixed load (constant voltage load and constant power load)," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 815–825, Jan. 2019.
[29] A. v. Jouanne and B. Banerjee, "Assessment of voltage unbalance," *IEEE Trans. Power Del.*, vol. 16, no. 4, pp. 782–790, Oct. 2001.
[30] H. Kakigano, Y. Miura, and T. Ise, "Low-voltage bipolar-type DC microgrid for super high quality distribution," *IEEE Trans. Power Electron.*, vol. 25, no. 12, pp. 3066–3075, Dec. 2010.
[31] R. D. Middlebrook, "Input filter considerations in design and application of switching regulators," in *Proc. IEEE Power Electron. Specialists Conf.*, 1976.
[32] C. Wildrick, F. Lee, B. Cho, and B. Choi, "A method of defining the load impedance specification for a stable distributed power system," *IEEE Trans. Power Electron.*, vol. 10, no. 3, pp. 280–285, May 1995.
[33] X. Wang, R. Yao, and F. Rao, "Three-step impedance criterion for small-signal stability analysis in two-stage DC distributed power systems," *IEEE Power Electron. Lett.*, vol. 1, no. 3, pp. 83–87, Sep. 2003.
[34] A. Riccobono and E. Santi, "Comprehensive review of stability criteria for DC power distribution systems," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3525–3535, Sep./Oct. 2014.
[35] X. Feng, J. Liu, and F. Lee, "Impedance specifications for stable DC distributed power systems," *IEEE Trans. Power Electron.*, vol. 17, no. 2, pp. 157–162, Mar. 2002.
[36] K. Biswas and O. Ray, "A nonintrusive digital current sensing method for DC–DC converters with wide load range," *IEEE Sens. Lett.*, vol. 7, no. 6, pp. 1–4, Jun. 2023.

Kausik Biswas (Graduate Student Member, IEEE) received the B.Tech. degree from the Government College of Engineering and Textile Technology Berhampore, Berhampore, India, in 2019, and the M.Tech. degree from the Indian Institute of Technology Bhubaneswar, Khordha, India, in 2022, both in electrical engineering. He is currently working toward the Ph.D. degree in electrical engineering with the PMRF fellowship with the School of Electrical and Computer Sciences, Indian Institute of Technology Bhubaneswar.

His research interests include current estimation techniques for nonisolated dc–dc and ac–dc converters, converter parameter estimation, modeling of dc–dc converters, digital control of dc–dc converters, and bipolar dc microgrids.

Chandrashekhar N. Bhende (Senior Member, IEEE) received the Ph.D. degree in power quality from the Indian Institute of Technology Delhi, New Delhi, in 2008.

In 2008, he went to University of Wollongong, Australia for a Postdoctoral Research and in December 2008, he joined as Assistant Professor with the Indian Institute of Technology Guwahati, India. In 2010, he moved to School of Electrical Sciences, Indian Institute of Technology Bhubaneswar, Khordha, India, and is presently serving as a Professor. His research interests include energy management in microgrids, power quality issues, condition monitoring, and application of artificial intelligent techniques.

Dr. Bhende has been honoured with Innovative Ph.D. Thesis Award in 2009 by the Indian National Academy of Engineering. He was the recipient of Indo-Australia Science and Technology Visiting Fellowship in 2013 and BASE Fellowship in 2018. Presently, he is serving as Member of "Policy Advocacy and Vision Group" for implementation of Odisha Renewable Energy Policy, Government of Odisha.

Olive Ray (Member, IEEE) received the B.E.E. degree from Jadavpur University, Kolkata, India, in 2009, the M.Tech. and Ph.D. degrees from the Indian Institute of Technology Kanpur, Kanpur, India, in 2011 and 2016, respectively, all in electrical engineering.

He worked as a Research Engineer with GE Global Research Bangalore till 2018. He is currently an Assistant Professor with the School of Electrical and Computer Sciences, Indian Institute of Technology Bhubaneswar, Khordha, India. His research interests include dc–dc power converters, digital control systems, and electric vehicle subsystems.