Switching Frequency Control Strategy of Inverter for Multifrequency Multiload WPT System Based on Hysteresis Current Control

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***Abstract*—Due to the complexity of current variation of the multifrequency and multiload (MFML) wireless power transfer (WPT) system based on hysteresis current (HC) control, resulting in a wide range of switching frequency variation, high frequency, and high switching losses of the inverter. This article proposes a blocking delay switching frequency control strategy. Based on the design of blocking delay module, the time division blocking delay and full-time fixed frequency blocking delay control modes are investigated, which can reduce the inverter switching frequency fluctuation range and fix the inverter switching frequency respectively. First, the structure and working principle of the MFML WPT system based on HC control containing passive compensation network are analyzed. Second, the system switching frequency characteristics are analyzed. Third, for different system switching frequency limitation requirements, time division blocking delay control mode and full-time fixed-frequency blocking delay control mode are proposed. Finally, an experimental platform is built to verify the proposed control strategy, the experimental results show that the system switching frequency of different parameters is reduced to within 200 kHz and 180 kHz in the time division blocking delay control, and the system switching frequency is fixed to 150 kHz and 250 kHz in the full-time fixed-frequency blocking delay control.**

***Index Terms*—Blocking delay control, fixed switching frequency, hysteresis current control, low switching frequency, multifrequency and multiload (MFML), wireless power transfer (WPT).**

I. Introduction

COMPARED with the traditional wired power transfer method, wireless power transfer (WPT) technology does not require physical contact or wired connection, which has the advantage of being more flexible and convenient [1], [2]. WPT technology has been gradually penetrated into the fields of electric vehicles [3], rail transportation [4], and high-performance medical devices [5], and has a wide range of application prospects.

With the development of WPT technology, the research and application of WPT system operating modes have been gradually extended to the multifrequency and multiload (MFML) synchronous transmission modes [6]. MFML power synchronous transmission modes can be generally classified into four modes: 1) multiple primary-side inverters operating in parallel [7], [8], [9], 2) fundamental-harmonic parallel utilization mode [10], [11], 3) multifrequency load power supply in time slots [12], and 4) multifrequency power superposition output mode [13], [14], [15], [16].

In the previous work, the authors of this article proposed a MFML WPT system based on hysteresis current (HC) control [17]. This system achieves independent stable and efficient power transmission for each load by designing command current directly according to each load frequency and power demand. At the same time, it offers advantages of simple system structure, flexible control, and fast response speed compared with other multifrequency power superposition utilization methods. However, as loads with different frequency and power demand are added, the switching frequency of inverter is high, with a wide and complex variation range. This places high demands on the design of the high-frequency inverter, and concurrently affects the efficient and stable operation of the MFML WPT system based on HC control. Therefore, in order to comply with the development trend of high-frequency and miniaturization of inverters, as well as to meet the wide and efficient application of the MFML WPT system based on HC control, it is urgent to study the switching frequency control strategy of its inverters.

Currently, the research on the switching frequency control strategy of HC controlled inverters mainly includes digital variable loop width fixed frequency control, resonant soft switch design, and so on. For example, Zhu et al. [18] set a fixed switching frequency for H-bridge cascade type inverter, calculates the relationship between switching frequency and loop width through digital control, and dynamically adjusts the loop width to achieve a fixed switching frequency. Wang and Zhang [19] proposed a fixed frequency control method based on double triangular carriers, which achieves the fixing of switching frequency for the HC control of grid-connected inverters by superimposing double triangular carriers as a new loop width band on the traditional fixed loop width.

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In summary, it is found that the current research for digital variable loop width fixed frequency control in the command current frequency is low and only contains a fundamental frequency. But in the MFML WPT system based on HC control, command current change law is no longer sinusoidal, while each subcommand current frequency is relatively high. So subject to the command current change speed and the calculation module computing speed, through the digital control dynamically adjust the loop width to achieve real-time fixed switching frequency is more difficult to achieve. Similarly, due to the complexity of the multifrequency resonant soft-switch circuit design, the system resonant soft-switch design will be more difficult to achieve.

Since the high-frequency inverter will only produce large switching losses during the periods of higher switching frequencies or larger currents in the switching process. Furthermore, achieving a fixed switching frequency of the system will facilitate the filter design. Therefore, it is of great significance to investigate the inverter switching frequency control strategy for the special characteristics of the MFML WPT system based on HC control.

In this article, the switching frequency control strategy of the MFML WPT system based on HC control is investigated. First, the system structure and working principle are analyzed, and the inverter switching frequency characteristic model is established and analyzed. Then, a blocking delay switching frequency control strategy is proposed, and the time division blocking delay control mode and the full-time fixed-frequency blocking delay mode are investigated, which effectively achieve the reduction of the inverter switching frequency fluctuation range and the fixed switching frequency, respectively. Compared with other fixed-frequency control strategies, the blocking delay switching frequency control strategy can effectively reduce the inverter switching frequency for multifrequency systems with different parameters and under different working conditions, which is flexible and universal. Then, the parameter design process is proposed for the two operating modes, which can optimally reduce the inverter switching frequency and fix the switching frequency under the premise of guaranteeing the power quality received by the load. Finally, the correctness of the blocking delay switching frequency control strategy is experimentally verified.

II. Structure and Working Principle of MFML WPT System Based on HC Control Containing Passive Compensation Network

The structure of the MFML WPT system based on HC control containing passive compensation network is shown in Fig. 1.

As shown in Fig. 1, the system structure specifically includes a primary-side dc power supply U_d, switching devices S_1–S_4, and diodes D_1–D_4 to form a high-frequency full-bridge inverter. The WPT system has a single transmitter and multiple receiver structure. L_P is the inductance of transmitting coil. R_P is the equivalent internal resistance of L_P. L_{S1}, L_{S2}, …, L_{Sn}(n is the number of loads at different operating frequencies) are the inductance of multiple receiving coils on the secondary side. M_{PSi} is the mutual inductance between the receiving coil and

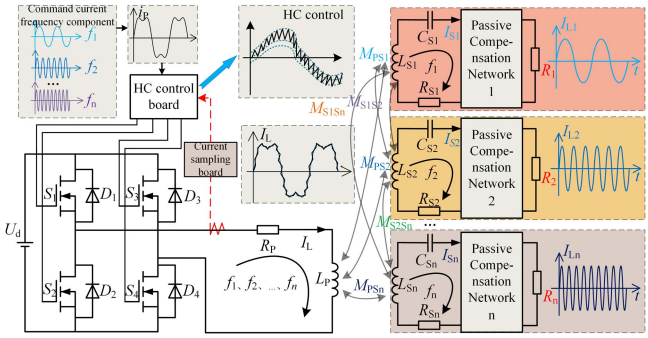

Fig. 1. Structure diagram of MFML WPT system based on HC control containing passive compensation network.

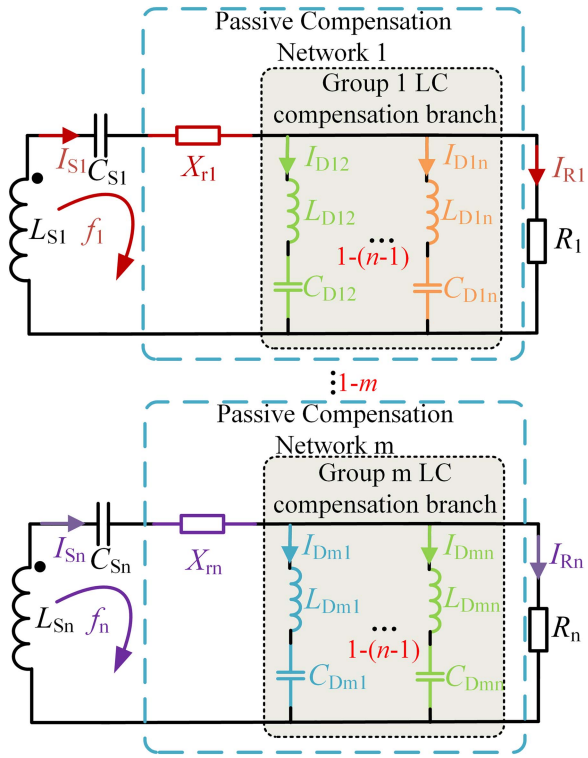

Fig. 2. Schematic diagram of secondary side passive compensation network.

the transmitting coil of the $i(i = 1, 2, \ldots, n.)$ secondary loop. M_{SiSj} is the cross mutual inductance between the receiving coil of the i secondary loop and the receiving coil of the j ($j = 1, 2, \ldots, n.$ $i \neq j$) secondary loop. R_{Si} is the internal resistance of the receiving coil of the i secondary loop. R_i is the load of the i secondary loop. C_{Si} is the compensation capacitance of the i secondary loop. f_i is the operating frequency of the i secondary loop. The secondary side also includes n passive compensation networks with different resonant frequencies.

The structure of the secondary passive compensation network is shown in Fig. 2.

As shown in Fig. 2, the passive compensation network consists of several LC passive compensation branches at frequencies other than their own resonant frequencies, which are connected in parallel to the loads. X_{r1}, X_{r2},…,X_{rn} are the dynamic compensation reactance of the n receiver circuits. L_{Dm1},

$L_{Dm2},\ldots,L_{Dmn}(m\neq n)$ are the inductances of the n-1 LC passively compensated branches of the receiver circuit m that are not at their own resonant frequencies. $C_{Dm1}, C_{Dm2},\ldots,C_{Dmn}(m\neq n)$ are the capacitances of the n-1 LC passively compensated branches of the receiver circuit m that are not at their own resonant frequency.

A bipolar fixed bandwidth current modulation mode is used to control the high-frequency full-bridge inverter switching tubes S_1–S_4, in which S_1 and S_4 is a group and S_2 and S_3 is a group, with the same control signals for each group of switching tubes, and the two groups of control signals conduct complementarily. First, the frequency of the load side and the power level requirement are determined. Then, the subcommand current amplitude-phase parameter is set by establishing the mapping relationship between each subcommand current function and the corresponding load received power. Finally, the design of the command current i_P is given in the following equation:

$$\begin{aligned} i_P &= i_P^{(1)} + i_P^{(2)} + i_P^{(3)} + \cdots + i_P^{(n)} \\ &= a_1 \sin(2\pi f_1 t + \varphi_1) + \cdots + a_n \sin(2\pi f_n t + \varphi_n) \\ &= \sum_{i=1}^{n} a_i \sin(2\pi f_i + \varphi_i) \end{aligned} \tag{1}$$

where $i_P{}^{(1)}$, $i_P{}^{(2)}$, …, $i_P{}^{(n)}$ are the subcommand currents at each frequency component f_i, a_1, a_2,…,a_n are the amplitude of each subcommand current component, respectively, φ_1, φ_2,…,φ_n are the initial phases of each subcommand current component, respectively.

First, the designed i_P is inputted. Then, i_P is compared with the primary side transmitter coil inductance current I_L to generate an error current $\Delta i = i_P$-I_L to be fed into the hysteresis loop comparator. When Δi reaches the upper loop width of hysteresis band, indicating that the commanded current size i_P is larger than the inductance current I_L, control switch tubes S_1, S_4 turn ON, while S_2, S_3 turn OFF. This results in the rise of inductance current I_L, reducing Δi. Until it reaches the hysteresis loop comparison lower loop width, i_P is smaller than the inductor current I_L, control switch tubes S_2, S_3 turn ON, while S_1, S_4 turn OFF. This causes I_L to decreases. When Δi is in the range between the loop widths of $+h$ and $-h$, the switching mode of the system stays unchanged. As a result, I_L will follow the command current i_P in the form of a sawtooth wave. Therefore, it is considered that the high frequency inverter output current waveform is the command current waveform, which contains multiple frequency components of electrical energy.

The command current HC control operating waveform and the driving signal U_{S1} of the inverter switching tube S_1 are shown in Fig. 3.

The secondary receiver circuit needs to filter out the rest of the power other than the frequency component required by the load to ensure that the load receives power quality. Therefore, the secondary side satisfies the following resonance conditions:

$$(2\pi f_i)^2 L_{Si} C_{Si} = 1. \tag{2}$$

For the MFML WPT system based on HC control, the higher the switching frequency, the better the current tracking effect and the higher the power quality received by the load. However, reducing the switching frequency will inevitably cause the actual inductor current harmonic distortion rate to increase. In order to minimize the effect of the increase in the harmonic distortion rate of the inductor current on the quality of the power received at the secondary side, the passive compensation network of each receiver circuit should further filter out the rest of the power in addition to the frequency components required by the load, so that the n-1 LC passive compensation branches in each receiver circuit are required to filter out the n-1 frequency components of the power in addition to their own resonance frequencies, which should be satisfied by the LC passive compensation branches of each receiver circuit

$$\begin{cases} (2\pi f_2)^2 L_{D12} C_{D12} = 1 \\ \quad\vdots \qquad\qquad (m, i = 1, 2, \ldots n; m \neq i). \\ (2\pi f_i)^2 L_{Dmi} C_{Dmi} = 1 \end{cases} \tag{3}$$

After adding the LC passive compensation branch, in order to make the equivalent impedance of each receiver circuit still present pure resistive under its own resonant frequency, and tends to infinity under the nonself-resonant frequency, so the passive compensation network needs to contain dynamic compensation reactance X_{rn}. When the LC passive compensation branch presents inductance under its own resonant frequency, it should make dynamic compensation reactance present capacitive under its own resonant frequency, and it should be made to present inductance conversely.

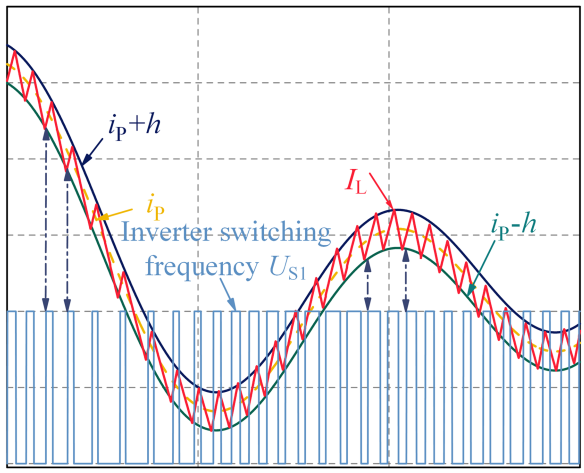

Fig. 3. Command current HC control operation waveform and drive signal U_{S1} waveform.

III. Modeling and Analysis of MFML WPT System Based on HC Control Containing Passive Compensation Network

A. System Model Analysis

The MFML WPT system based on HC control containing passive compensation network is modeled and analyzed as an example of a dual-frequency dual-load WPT system. According to the analysis of the HC control principle in Section II, under the condition that the I_L can track the i_P and only the load operating

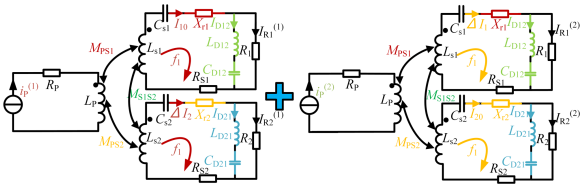

Fig. 4. Equivalent models of circuits with current sources of different operating frequencies acting alone.

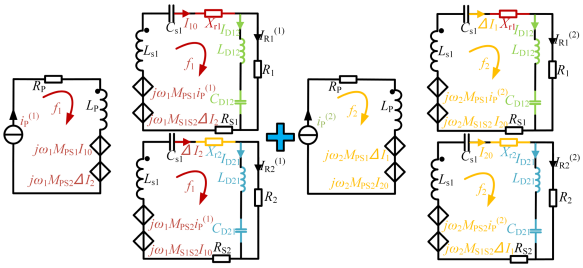

Fig. 5. Decoupling equivalent circuit diagram.

frequency power component is considered, it is considered that the output current of the inverter is i_{P}. Since the command current function is determined by the demand of each load, it is independent of the external circuit structure. Therefore, the system complies with the current source characteristics [20], [21], it can be assumed that the inverter is a current-source inverter. According to the theorem of superposition of the circuits, the system shown in Fig. 1 is transformed into an equivalent model of circuits under the action of current sources of different frequencies, respectively, as shown in Fig. 4.

Where I_{10} is the current in receiver circuit 1 when the current source with operating frequency f_1 is acting alone, I_{20} is the current in receiver circuit 2 when the current source with operating frequency f_2 is acting alone, ΔI_1 is the current in receiver circuit 1 when the current source with operating frequency f_2 is acting alone, and ΔI_2 is the current in receiver circuit 2 when the current source with operating frequency f_1 is acting alone. I_{Dm1}, I_{Dm2} are the current values of the two *LC* passive compensation branches of the receiver circuit 12 that are not at their own resonant frequencies, respectively, and I_{R1}, I_{R2} are the load R_1, R_2 values of load currents.

The decoupling equivalent circuit of Fig. 4 is shown in Fig. 5.

According to Fig. 5, the KVL equations are written for each vice-side receiver circuit and primary-side loop under the separate action of the current source at f_1 and f_2 frequencies, respectively, and the voltage-current relationship matrices are obtained at two frequencies f_1 and f_2

$$\begin{cases} \begin{bmatrix} U_{\mathrm{in}}^{(1)} \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} Z_{\mathrm{P}}^{(1)} & -j\omega_1 M_{\mathrm{PS1}} & -j\omega_1 M_{\mathrm{PS2}} \\ -j\omega_1 M_{\mathrm{PS1}} & Z_{\mathrm{S1}}^{(1)} & j\omega_1 M_{\mathrm{S1S2}} \\ -j\omega_1 M_{\mathrm{PS2}} & j\omega_1 M_{\mathrm{S1S2}} & Z_{\mathrm{S2}}^{(1)} \end{bmatrix} \begin{bmatrix} i_{\mathrm{P}}^{(1)} \\ I_{10} \\ \Delta I_2 \end{bmatrix} \\ \begin{bmatrix} U_{\mathrm{in}}^{(2)} \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} Z_{\mathrm{P}}^{(2)} & -j\omega_2 M_{\mathrm{PS1}} & -j\omega_2 M_{\mathrm{PS2}} \\ -j\omega_2 M_{\mathrm{PS1}} & Z_{\mathrm{S1}}^{(2)} & j\omega_2 M_{\mathrm{S1S2}} \\ -j\omega_2 M_{\mathrm{PS2}} & j\omega_2 M_{\mathrm{S1S2}} & Z_{\mathrm{S2}}^{(2)} \end{bmatrix} \begin{bmatrix} i_{\mathrm{P}}^{(2)} \\ \Delta I_1 \\ I_{20} \end{bmatrix} \end{cases} \tag{4}$$

where $Z_{\mathrm{P}}{}^{(1)}$ and $Z_{\mathrm{P}}{}^{(2)}$ are the equivalent impedances at the transmitter side at the operating frequencies f_1, f_2, respectively, $Z_{\mathrm{S1}}{}^{(1)}$ and $Z_{\mathrm{S1}}{}^{(2)}$ are the equivalent impedances at the receiver side of the secondary receiver circuit 1 at the operating frequencies f_1, f_2, respectively, $Z_{\mathrm{S2}}{}^{(1)}$ and $Z_{\mathrm{S2}}{}^{(2)}$ are the equivalent impedances at the receiver side of the secondary receiver circuit 2 at the operating frequencies f_1, f_2, respectively, $U_{\mathrm{in}}{}^{(1)}$ and $U_{\mathrm{in}}{}^{(2)}$ are the sinusoidal fundamental components of two frequencies of the square wave voltage obtained after inversion of U_{d}, respectively. Due to the addition of passive compensation network, while limiting the transmission of nonresonant power, it should be ensured that the receiving coil is still overall in resonance at its own resonant frequency. The equivalent impedance of each receiver circuit at different frequencies is

$$\begin{cases} Z_{\mathrm{S1}}^{(1)} = \frac{R_1 (X_{\mathrm{D12}}^{(1)})^2 + jR_1^2 (X_{\mathrm{D12}}^{(1)})}{R_1^2 + (X_{\mathrm{D12}}^{(1)})^2} + jX_{\mathrm{r1}}^{(1)} + R_{\mathrm{S1}} \\ Z_{\mathrm{S1}}^{(2)} = \frac{R_1 (X_{\mathrm{D12}}^{(2)})^2 + jR_1^2 (X_{\mathrm{D12}}^{(2)})}{R_1^2 + (X_{\mathrm{D12}}^{(2)})^2} + j\omega_2 L_{\mathrm{S1}} - j\frac{1}{\omega_2 C_{\mathrm{S1}}} \\ \qquad + jX_{\mathrm{r1}}^{(2)} + R_{\mathrm{S1}} \\ Z_{\mathrm{S2}}^{(1)} = \frac{R_2 (X_{\mathrm{D21}}^{(1)})^2 + jR_2^2 (X_{\mathrm{D21}}^{(1)})}{R_2^2 + (X_{\mathrm{D21}}^{(1)})^2} + j\omega_1 L_{\mathrm{S2}} - j\frac{1}{\omega_1 C_{\mathrm{S2}}} \\ \qquad + jX_{\mathrm{r2}}^{(1)} + R_{\mathrm{S2}} \\ Z_{\mathrm{S2}}^{(2)} = \frac{R_2 (X_{\mathrm{D21}}^{(2)})^2 + jR_2^2 (X_{\mathrm{D21}}^{(2)})}{R_2^2 + (X_{\mathrm{D21}}^{(2)})^2} + jX_{\mathrm{r2}}^{(2)} + R_{\mathrm{S2}} \\ Z_{\mathrm{P}}^{(1)} = j\omega_1 L_{\mathrm{P}} + R_{\mathrm{P}}, Z_{\mathrm{P}}^{(2)} = j\omega_2 L_{\mathrm{P}} + R_{\mathrm{P}} \\ X_{\mathrm{D12}}^{(1)} = \omega_1 L_{\mathrm{D12}} - \frac{1}{\omega_1 C_{\mathrm{D12}}}, X_{\mathrm{D12}}^{(2)} = \omega_2 L_{\mathrm{D12}} - \frac{1}{\omega_2 C_{\mathrm{D12}}} \\ X_{\mathrm{D21}}^{(1)} = \omega_1 L_{\mathrm{D21}} - \frac{1}{\omega_1 C_{\mathrm{D21}}}, X_{\mathrm{D21}}^{(2)} = \omega_2 L_{\mathrm{D21}} - \frac{1}{\omega_2 C_{\mathrm{D21}}} \end{cases} \tag{5}$$

where $X_{\mathrm{Dmn}}{}^{(i)}$ is the equivalent impedance of the n-1 *LC* passive compensation network of the receiver circuit m at frequency f_{i}.

From (4) and (5), it can be obtained that the currents in each receiver circuit are shown in (6) when the current sources of different frequencies act alone

$$\begin{cases} I_{10} = \frac{Z_{\mathrm{S2}}^{(1)}(j\omega_1 M_{\mathrm{PS1}}) + (j\omega_1 M_{\mathrm{PS2}})(j\omega_1 M_{\mathrm{S1S2}})}{Z_{\mathrm{S1}}^{(1)} Z_{\mathrm{S2}}^{(1)} - (j\omega_1 M_{\mathrm{S1S2}})(j\omega_1 M_{\mathrm{S1S2}})} i_{\mathrm{P}}^{(1)} \\ \Delta I_1 = \frac{Z_{\mathrm{S2}}^{(2)}(j\omega_2 M_{\mathrm{PS1}}) + (j\omega_2 M_{\mathrm{PS2}})(j\omega_2 M_{\mathrm{S1S2}})}{Z_{\mathrm{S1}}^{(2)} Z_{\mathrm{S2}}^{(2)} - (j\omega_2 M_{\mathrm{S1S2}})(j\omega_2 M_{\mathrm{S1S2}})} i_{\mathrm{P}}^{(2)} \\ I_{20} = \frac{Z_{\mathrm{S1}}^{(2)}(j\omega_2 M_{\mathrm{PS2}}) + (j\omega_2 M_{\mathrm{PS1}})(j\omega_2 M_{\mathrm{S1S2}})}{Z_{\mathrm{S1}}^{(2)} Z_{\mathrm{S2}}^{(2)} - (j\omega_2 M_{\mathrm{S1S2}})(j\omega_2 M_{\mathrm{S1S2}})} i_{\mathrm{P}}^{(2)} \\ \Delta I_2 = \frac{Z_{\mathrm{S1}}^{(1)}(j\omega_1 M_{\mathrm{PS2}}) + (j\omega_1 M_{\mathrm{PS1}})(j\omega_1 M_{\mathrm{S1S2}})}{Z_{\mathrm{S1}}^{(1)} Z_{\mathrm{S2}}^{(1)} - (j\omega_1 M_{\mathrm{S1S2}})(j\omega_1 M_{\mathrm{S1S2}})} i_{\mathrm{P}}^{(1)}. \end{cases} \tag{6}$$

The *LC* passive compensation branch current in the secondary receiver circuit is

$$\begin{cases} I_{\mathrm{D12}}^{(1)} = I_{10} \frac{R_1}{R_1 + jX_{\mathrm{D12}}^{(1)}}, I_{\mathrm{D21}}^{(1)} = \Delta I_2 \frac{R_2}{R_2 + jX_{\mathrm{D21}}^{(1)}} \\ I_{\mathrm{D12}}^{(2)} = \Delta I_1 \frac{R_1}{R_1 + jX_{\mathrm{D12}}^{(2)}}, I_{\mathrm{D21}}^{(2)} = I_{20} \frac{R_2}{R_2 + jX_{\mathrm{D21}}^{(2)}} \\ I_{\mathrm{R1}}^{(1)} = I_{10} \frac{jX_{\mathrm{D12}}^{(1)}}{R_1 + jX_{\mathrm{D12}}^{(1)}}, I_{\mathrm{R2}}^{(1)} = \Delta I_2 \frac{jX_{\mathrm{D21}}^{(1)}}{R_2 + jX_{\mathrm{D21}}^{(1)}} \\ I_{\mathrm{R1}}^{(2)} = \Delta I_1 \frac{jX_{\mathrm{D12}}^{(2)}}{R_1 + jX_{\mathrm{D12}}^{(2)}}, I_{\mathrm{R2}}^{(2)} = I_{20} \frac{jX_{\mathrm{D21}}^{(2)}}{R_2 + jX_{\mathrm{D21}}^{(2)}}. \end{cases} \tag{7}$$

From (5), (6), and (7), taking the receiver circuit 1 as an example, due to the high impedance characteristic of the *LC* passive compensation branch at frequency f_1, all the current I_{10} flows to the load R_1. Similarly, due to the resonance state of the *LC* passive compensation branch at frequency f_2, all the

TABLE I
PARAMETERS OF THE SECONDARY SIDE SYSTEM

Parameter	Value	Parameter	Value
L_{S1}	233.5 μH	C_{D12}(50 kHz)	43.43 nF
L_{S2}	233.28 μH	C_{D12}(90 kHz)	13.41 nF
L_{D12}	233.28 μH	C_{D21}(5 kHz)	4.33 μF
L_{D21}	233.5 μH	C_{D21}(20 kHz)	271.2 nF
C_{S1}(5 kHz)	4.33 μF	X_{r1}(5 kHz,15 kHz)	542.76 nH
C_{S1}(20 kHz)	271.2 nF	X_{r2}(5 kHz,15 kHz)	208.1 μF
C_{S2}(15 kHz)	482.59 nF	X_{r1}(5 kHz,25 kHz)	180.97 nH
C_{S2}(25 kHz)	173.57 nF	X_{r2}(5 kHz,25 kHz)	224.34 μF
C_{S2}(30 kHz)	120.65 nF	X_{r1}(20 kHz,30 kHz)	217 nH
C_{S2}(50 kHz)	43.43 nF	X_{r2}(20 kHz,30 kHz)	129.94 μF
C_{S2}(90 kHz)	13.41 nF	X_{r1}(20 kHz,50 kHz)	51.704 nH
C_{D12}(15 kHz)	482.59 nF	X_{r2}(20 kHz,50 kHz)	196.19 μF
C_{D12}(25 kHz)	173.57 nF	X_{r1}(20 kHz,90 kHz)	14.102 nH
C_{D12}(30 kHz)	120.65 nF	X_{r2}(20 kHz,90 kHz)	221.98 μF

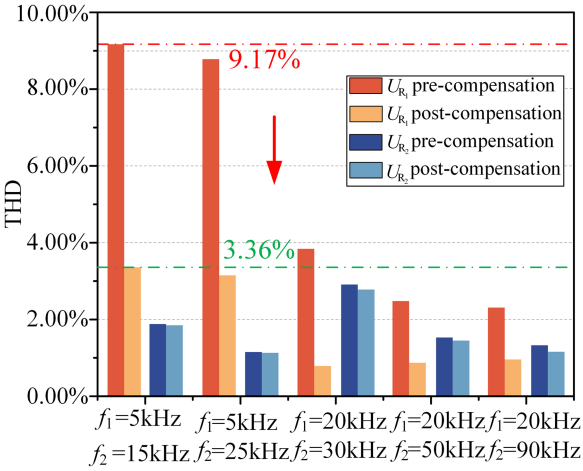

Fig. 6. Harmonic distortion rate of load voltage before and after compensation.

current ΔI_1 is absorbed by the LC passive compensation branch, which reduces the harmonic content in the load R_1, and further improves the receiving power quality of the load R_1. Meanwhile, the output power of R_1 is mainly provided by the frequency f_1 component power. And after adding the passive compensation network, $X_{D12}{}^{(1)}$ is much larger than R_1 and $Z_{S1}{}^{(1)}$ basically keeps R_1 unchanged, so $I_{R1}{}^{(1)}$ is still equal to I_{10}. Therefore, adding the passive compensation network will not affect the output power and efficiency of the system. Receiver circuit 2 is similar with receiver circuit 1, passive compensation network also further improves the quality of power received by load R_2.

To analyze the effect of the passive compensation network, the parameters of the secondary system are set, as shown in Table I.

Based on Simulink, the harmonic distortion rate of load terminal voltage before and after adding passive compensation network under different command current frequencies is obtained, as shown in Fig. 6.

As shown in Fig. 6, for the MFML WPT system based on HC control, the addition of passive compensation network in the receiver circuit can reduce the harmonic distortion rate of the received power at the load side, which lays the foundation for the switching frequency reduction.

Since the mutual inductance between the load receiving coil is much smaller than that between the transmitting coil and

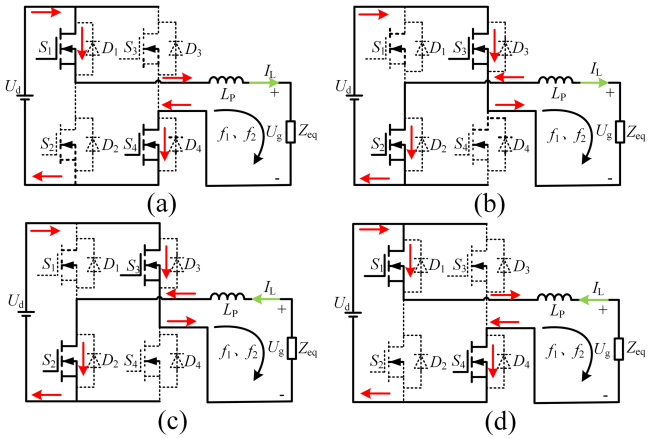

Fig. 7. State diagram of the high-frequency inverter circuit. (a) Circuit state 1. (b) Circuit state 2. (c) Circuit state 3. (d) Circuit state 4.

receiving coil, it can be ignored. Therefore, according to (5), the equivalent impedance of each receiver circuit is converted to the primary side, and the equivalent impedance of the primary side can be obtained as

$$\begin{cases} Z_{\mathrm{eq}}^{(1)} = \dfrac{(\omega_1 M_{\mathrm{PS1}})^2}{Z_{\mathrm{S1}}^{(1)}} + \dfrac{(\omega_1 M_{\mathrm{PS2}})^2}{Z_{\mathrm{S2}}^{(1)}} \\ Z_{\mathrm{eq}}^{(2)} = \dfrac{(\omega_2 M_{\mathrm{PS1}})^2}{Z_{\mathrm{S1}}^{(2)}} + \dfrac{(\omega_2 M_{\mathrm{PS2}})^2}{Z_{\mathrm{S2}}^{(2)}}. \end{cases} \tag{8}$$

From (8), the system secondary side is converted to the primary side equivalent voltage U_{g} as

$$\begin{aligned} U_{\mathrm{g}} &= U_{\mathrm{g}}^{(1)} + U_{\mathrm{g}}^{(2)} = i_{\mathrm{P}}^{(1)} Z_{\mathrm{eq}}^{(1)} + i_{\mathrm{P}}^{(2)} Z_{\mathrm{eq}}^{(2)} \\ &= E_1 \sin(\omega_1 t + \theta_1) + E_2 \sin(\omega_2 t + \theta_2) \end{aligned} \tag{9}$$

where $U_{\mathrm{g}}{}^{(1)}$ and $U_{\mathrm{g}}{}^{(2)}$ are the equivalent voltages of the secondary side of the system converted to the primary side at an operating frequency of f_1, f_2, respectively. E_1 and E_2 are the electromotive forces of U_{g} of the different frequency components. θ_1 and θ_2 are the initial phases of U_{g} of the different frequency components, respectively.

B. Inverter Switching Frequency Characteristics Analysis

Due to the high and variable inverter switching frequency of the MFML WPT system based on HC control, it is necessary to analyze the high frequency inverter switching frequency characteristics in this system. The operating state of the high-frequency inverter circuit based on HC control is shown in Fig. 7.

Circuit state 1: Switch tubes S_1 and S_4 conduct, the inverter output current is in the same direction as the current in the circuit, and the current increases positively.

The KVL voltage equation is written according to the current circuit state, as shown in

$$\begin{cases} L_{\mathrm{P}} \dfrac{\mathrm{d}I_{\mathrm{L}}}{\mathrm{d}t} = U_{\mathrm{d}} - U_{\mathrm{g}} \\ \dfrac{\mathrm{d}I_{\mathrm{L}}}{\mathrm{d}t} t_1 - \dfrac{\mathrm{d}i_{\mathrm{P}}}{\mathrm{d}t} t_1 = 2h. \end{cases} \tag{10}$$

Circuit state 2: Switch tubes S_2 and S_3 conduct, the inverter output current is opposite to the direction of the current in the circuit, and the current decreases positively.

The KVL voltage equation is written according to the current circuit state, as shown in

$$\begin{cases} L_{\mathrm{P}}\frac{\mathrm{d}I_{\mathrm{L}}}{\mathrm{d}t} = -U_{\mathrm{d}} - U_{\mathrm{g}} \\ \frac{\mathrm{d}I_{\mathrm{L}}}{\mathrm{d}t}t_2 - \frac{\mathrm{d}i_{\mathrm{P}}}{\mathrm{d}t}t_2 = -2h \end{cases} \tag{11}$$

where t_1 is the time period when I_{L} is in the rising phase and t_2 is the time period when I_{L} is in the falling phase. h is the HC control loop width. $+h$ is the upper loop width. $-h$ is the lower loop width.

Circuit state 3: Switch tubes S_2 and S_3 conduct, the inverter output current is in the same direction as the current in the circuit, the current increases in the reverse direction, and its KVL voltage equation is the same as that of circuit state 2.

Circuit state 4: Switch tubes S_1 and S_4 conduct, the inverter output current is opposite to the direction of the current in the circuit, the current decreases in the reverse direction, and the KVL voltage equation is the same as that of circuit state 1.

From (10) and (11), the high frequency inverter switching frequency f_{s} can be introduced as

$$f_{\mathrm{s}} = \frac{1}{t_1 + t_2} = \frac{U_{\mathrm{d}}^2 - \left(U_{\mathrm{g}} + L_{\mathrm{p}}\frac{\mathrm{d}i_{\mathrm{P}}}{\mathrm{d}t}\right)^2}{4L_{\mathrm{P}}hU_{\mathrm{d}}}. \tag{12}$$

Assuming that the switching frequency change is much higher than the command current change frequency, so it is considered that the command current remains unchanged during the switching frequency change cycle, combining with (9), the high-frequency inverter switching frequency f_{s} can be obtained as

$$f_{\mathrm{s}} = \underbrace{\frac{U_{\mathrm{d}}}{4L_{\mathrm{P}}h} - \frac{E_1^2 + E_2^2}{8hL_{\mathrm{P}}U_{\mathrm{d}}}}_{\text{Average switching frequency } f_{\mathrm{sav}}} \underbrace{\begin{array}{l} + \frac{E_1^2\cos(2\omega_1 t + 2\theta_1) + E_2^2\cos(2\omega_2 t + 2\theta_2)}{8L_{\mathrm{P}}U_{\mathrm{d}}h} \\ - \frac{E_1E_2\sin(\omega_1 t + \theta_1)\sin(\omega_2 t + \theta_2)}{2L_{\mathrm{P}}U_{\mathrm{d}}h} \end{array}}_{\text{Wave switching frequency}} \tag{13}$$

where f_{sav} is the average switching frequency.

The maximum switching frequency is

$$f_{\mathrm{s\,max}} = \frac{U_{\mathrm{d}}}{4L_{\mathrm{P}}h}. \tag{14}$$

From (14), the maximum switching frequency of the system is only related to U_{d}, h, and L_{P}. Based on the above analysis, the relationship between the average switching frequency and the dual-frequency composite command current amplitude, frequency, and coupling coefficient of the receiving coil is plotted, respectively, as shown in Figs. 8 –10. The maximum switching frequencies of the system for the selected parameters in Figs. 8–10 are 859 kHz, 1.37 MHz, and 723 kHz, respectively.

As shown in Figs. 8 and 9, when the dual-frequency composite command current amplitude and frequency are lower, the average switching frequency is closer to the maximum switching frequency, and the switching frequency fluctuation range is small. When the dual-frequency composite command current amplitude and frequency are higher, the average switching frequency differs greatly from the maximum switching frequency,

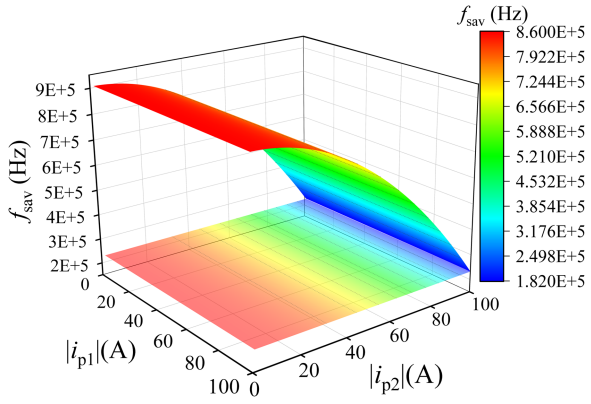

Fig. 8. Plot of the relationship between the average switching frequency and the amplitude of the dual-frequency composite command current.

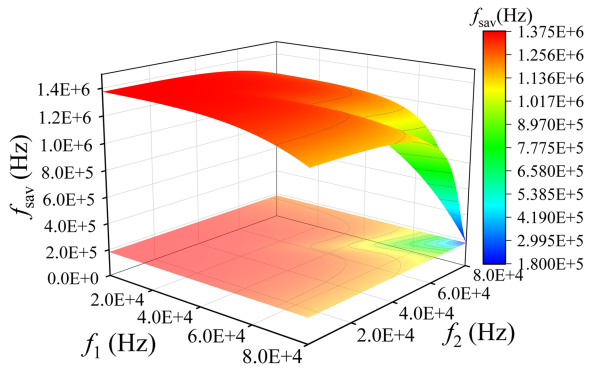

Fig. 9. Plot of the relationship between the average switching frequency and the frequency of the dual-frequency composite command current.

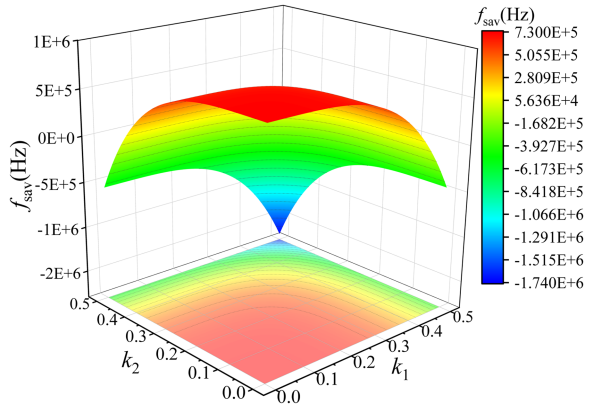

Fig. 10. Plot of the relationship between the average switching frequency and the coupling coefficient of the receiving coil.

and the switching frequency fluctuation range is large. As shown in Fig. 10, the fluctuation range of inverter switching frequency is inversely proportional to the coupling coefficient. The negative average switching frequency of the inverter does not indicate that the actual switching frequency is negative, but is a theoretical indication that the out-of-step phenomenon is occurring. As shown in Fig. 11, at this time, Δi fluctuation range will exceed h.

The main reason for the out-of-step phenomenon is that U_{d} is less than U_{g}, and I_{L} cannot track i_{P}. In order to ensure that I_{L}

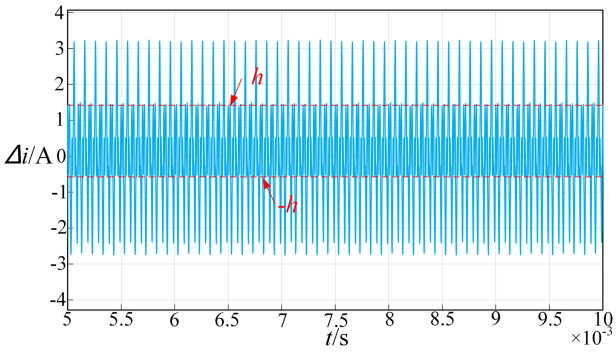

Fig. 11. Error current Δi waveform diagram when the out-of-step phenomenon occurs.

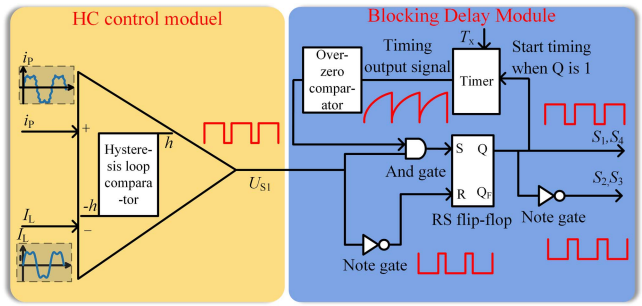

Fig. 12. Blocking delay module design structure diagram.

can track i_{P}, it is necessary to meet

$$U_{\mathrm{d}} > |U_{\mathrm{g}}|_{\max} \tag{15}$$

where $|U_{\mathrm{g}}|_{\max}$ is the maximum value of the secondary equivalent voltage.

From the above analysis, for the MFML WPT system based on HC control, the variation of parameters such as command current frequency, amplitude, load size, mutual inductance between transmitter and receiver coils, and loop width can cause large fluctuations in the switching frequency.

IV. Blocking Delay Switching Frequency Control Strategy

For the MFML WPT system based on HC control, the tracking effect is mainly affected by the switching frequency. The higher the switching frequency, the better the effect of tracking command current. However, it will also produce large switching loss, which affects the efficient and stable operation of the system. In order to reduce the high-frequency inverter switching loss in the MFML WPT system based on HC control as much as possible, and comply with the development trend of inverter high frequency, miniaturization, and low loss. At the same time, in order to adapt to the special change rule of switching frequency due to the special characteristics of tracking multifrequency composite command current in this system, and to consider the requirements of the system to receive power quality and flexibility, a blocking delay switching frequency control strategy is proposed to reduce the switching frequency of the inverter.

A. Blocking Delay Module Design

In order to meet the above blocking delay switching frequency control strategy function, a blocking delay module is proposed. The module is mainly composed of RS flip-flop, timer, and logic gate circuit, as shown in Fig. 12.

The specific working principle of the blocking delay module is as follows. It is assumed that the analysis starts when Δi reaches h. The HC control module outputs a turn-ON signal, and the Q terminal of the RS flip-flop outputs a high level, which serves as the input signal for the timer and at the same time makes the switching tubes S_1 and S_4 conductive. I_{L} gradually increases. At the same time, the timer detects the arrival of the rising edge input signal and starts timing for the period T_{x} corresponding to the switching frequency to which it is desired to reduce. During the timer timing period, the timing value continuously records the current timing period. The timing output of the timer is connected to the negative input of the overzero comparator, and the positive input of the overzero comparator is connected to the zero level. The timing output of the timer is always greater than the zero level before the timing is completed, so the overzero comparator outputs a low level, and one of the inputs of the and gate is always held low, and the and gate outputs a low level. Therefore, the input S of the RS flip-flop changes from high to low immediately after the timing starts, blocking the arrival of the output drive signal of the HC control module in the next cycle. Until the timer timing is completed, the blocking limit of the gate is contacted. At this time, the turn-ON signal of the next cycle is allowed to arrive, and the drive signals are reapplied to the switching tubes S_1 and S_4. The cycle repeats, the switching frequency is forced down to $1/T_{\mathrm{x}}$ due to the forced blocking of the arrival of the turn-ON signal for the next switching cycle.

During the blocking delay period, when the hysteresis loop comparator outputs a high level, the RS flip-flop input is two low levels, which keep the previous output state unchanged. I_{L} continues to rise. When the hysteresis loop comparator outputs a low level, the RS flip-flop outputs a low level. I_{L} continues to fall. As a result, after the timer starts timing, the blocking delay module only blocks the arrival of the turn-ON signal in the next cycle, so its essence is a variable loop width control in which $+h$ remains unchanged and $-h$ changes.

In this blocking delay module design, if the timer has ended, but the next cycle turn-ON signal does not come, it means that at this time the theoretical switching frequency is lower than the blocking delay switching frequency, and the inverter loss is lower. Thus, the blocking delay is invalidated and the switching period is unchanged. From the above analysis, the blocking delay waveform at lower switching frequency and higher switching frequency is shown in Fig. 13.

With the development trend of inverter high frequency, miniaturization, and low loss, reducing the inverter switching frequency fluctuation range can achieve the goal of inverter low loss. Furthermore, fixing the switching frequency is conducive to the design of subsequent inverter filters. Based on the requirements of high-frequency inverter withstanding characteristics and the requirements of actual engineering application scenarios, the two working modes of the blocking delay control strategy

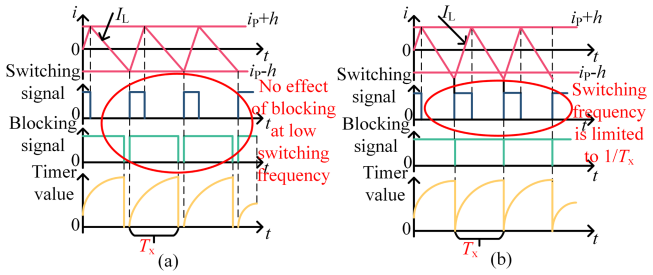

Fig. 13. Waveforms of blocking delay control strategy. (a) Low switching frequency. (b) High switching frequency.

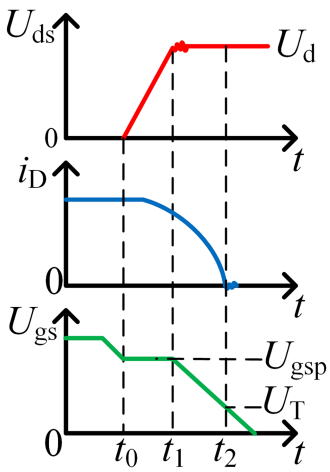

Fig. 14. Switching tube turn-OFF waveform.

are proposed – the time division blocking delay control mode and the full-time fixed-frequency blocking delay control mode.

B. Time Division Blocking Delay Control Mode

The blocking delay control strategy essentially further reduces $-h$. It can further increase the time period in which the inverter meets the controlled-type soft switching within one command current cycle and further reduce the inverter turn-ON losses [22]. This article analyses the inverter switching losses using the inverter turn-OFF process as an example. The inverter turn-ON process is similar to the turn-OFF process. The switching tube turn-OFF waveform is shown in Fig. 14.

The switching tube turns OFF when the gate voltage U_{gs} falls to U_{gsp}. During the t_0-t_1 phase, the drain voltage U_{ds} rises linearly, the drain current i_D remains essentially unchanged, and the gate voltage U_{gs} is maintained at U_{gsp}. Until the moment t_1, the switching tube drain voltage U_{ds} rises to U_{in}, the gate voltage U_{gs} falls. Until $U_{gs}<U_T$, the channel disappears, i_D falls to 0, and the switching tube is completely turned OFF.

According to Fig. 14, in order to simplify the analysis, the change process of both drain voltage U_{ds} are regarded as linear changes, then the inverter turn-OFF loss is

$$E_{off} = \int_{t_0}^{t_2} i_D(t) \cdot U_{ds}(t) dt = 0.5 U_d I_L \cdot (t_1 - t_0) + 0.5 I_D(\theta) U_d (t_2 - t_1). \quad (16)$$

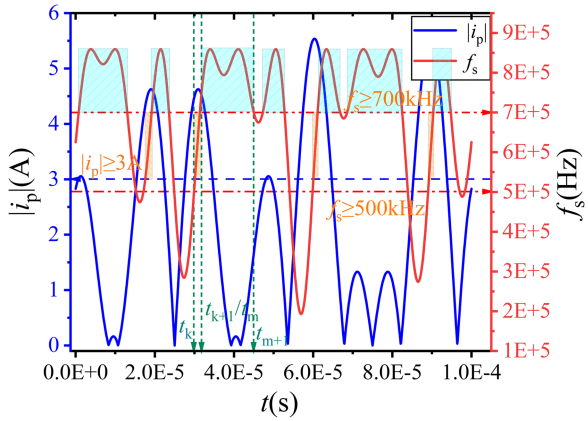

Fig. 15. Schematic diagram for selecting the moment of the time division blocking delay.

In which, the size of U_{ds} is related to U_d, and I_D represents the switching tube drain current. Since the inverter adopts the HC control, the switching tube drain current I_D is the same current as I_L, and, therefore, its value is related to the size of the multi-frequency compound i_P. Therefore, when the inverter switching frequency is higher, the switching action of the switching tube in one command current cycle is more, the switching loss must increase. Similarly, when i_P is larger, the drain current I_D flowing through the inverter during the shutdown process is larger, the shutdown loss generated in the primary switching tube shutdown process is larger, and the switching loss must increase.

From the above analysis, in order to reduce the inverter switching loss in the MFML WPT system based on HC control as much as possible, and at the same time, and to consider the requirements of the system load to receive the power quality requirements and the flexibility requirements, the time division blocking delay conditions are proposed as follows.

Time division blocking delay condition I: when the instantaneous theoretical switching frequency f_s is higher than the first preset frequency f_{x1}, the blocking delay module is intervened, and the delay time is set to T_{x1} ($T_{x1} \geq 1/f_{x1}$).

Time division blocking delay condition II: when the instantaneous theoretical switching frequency f_s is higher than the second preset frequency f_{x2} and the current modulus of I_L is greater than the preset current I_x, the blocking delay module is intervened, and the delay time is set to T_{x2} ($T_{x2} \geq 1/f_{x2}$, $f_{x1} \geq f_{x2}$).

Time division blocking delay condition III: when the time intersection of time division blocking delay condition I and time division blocking delay condition II occurs in one cycle, time division blocking delay condition I prevails.

A schematic diagram of the time division blocking delay moment selection within one command current cycle is shown in Fig. 15.

Where t_m-t_{m+1} is the time period in which the theoretical switching frequency $f_s(t)$ is higher than f_{x1} in a command current cycle, all of which satisfy the time division blocking delay condition I. t_k-t_{k+1} is the time period in which the theoretical switching frequency $f_s(t)$ is higher than f_{x2} in a command current

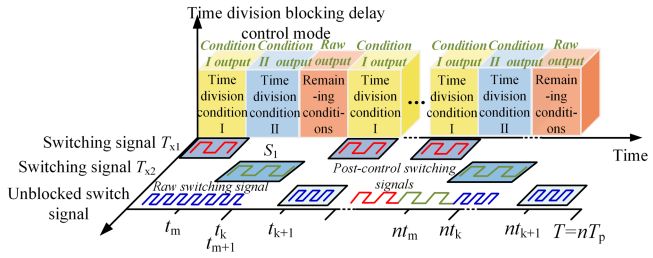

Fig. 16. Timing diagram for time division blocking delay control.

cycle, and the current modulus value of I_L is greater than I_x, all of which satisfy the time-split blocking delay condition II.

In a command current cycle, the original switching signal output from the hysteresis loop comparator is partially reduced to the corresponding frequency of the blocking delay in the time division blocking delay control mode according to different segmentation conditions. The switching signal after the time division blocking delay control will realize the local frequency fixing effect, and the maximum switching frequency is limited. The time period without blocking delay control in the command current cycle will maintain the original switching frequency in the original fixed loop width mode. The method reduces the range of inverter switching frequency fluctuation, and reduces the impact of the increase in harmonic distortion of the tracking current due to the reduction of the switching frequency as much as possible. The control timing is shown in Fig. 16.

In the traditional HC control, the switching frequency of the inverter is generally increased or decreased by adjusting h empirically. However, from the above analysis, the time division blocking delay control mode only reduces the switching frequency of the inverter at high frequency, and reduces the fluctuation range of the switching frequency of the inverter. Compared with the overall reduction of the switching frequency of inverter by adjusting h directly, it further reduces the increase of harmonic distortion of tracking current caused by the decrease of switching frequency at the low switching frequency of inverter. Therefore, when the maximum switching frequency of the inverter is limited to the same switching frequency level, the time division blocking delay control mode has lower current harmonic distortion and better receiving power quality.

C. Full-Time Fixed-Frequency Blocking Delay Control Mode

For the MFML WPT system based on HC control, when the frequency fixing requirement is put forward for the high-frequency inverter of the system, the switching frequency of the high-frequency inverter can be fixed by adopting the blocking delay control strategy with the same time for the whole period, and the switching frequency of the whole period will be reduced to the frequency f_x corresponding to the time-delayed time. Then, the switching frequency of the high-frequency inverter can be fixed. Since the blocking delay strategy only reduces the switching frequency where the theoretical switching frequency is higher than the blocking delay frequency, the prerequisite for the use of this control mode is that the minimum value of the theoretical switching frequency should be greater than the blocking delay frequency

$$f_x < f_{smin}. \tag{17}$$

From the analysis of the switching frequency characteristics in Section III, the maximum value of the theoretical switching frequency is related to U_d and preset h, and the fluctuating switching frequency is not related to U_d and preset h. Therefore, when the desired switching frequency f_x to be fixed is determined, the fixing of the switching frequency can be optimally achieved by dynamically adjusting U_d and the preset h with the objective of the power quality received by the load.

D. Parameter Relationship Studies

Blocking delay control is essentially an adaptive variable loop width control in which $+h$ remains constant and $-h$ changes dynamically with different rates of inductor current change. Since it has no control effect at low switching frequencies, there may be a resulting error. In the time division blocking delay control mode, the variable parameters include a first preset frequency f_{x1}, a first delay time T_{x1}, a second preset frequency f_{x2}, a second delay time T_{x2}, and a preset current I_x. Parameter constraints to avoid errors are discussed below.

E. Inherent Limitations on Parameter Selection

When f_{x1}, f_{x2}, and I_x are determined, in a command current cycle, it can be determined that a total of $2M$ moments satisfy the time-delay condition I, corresponding to the time period t_m-t_{m+1}, and a total of $2N$ moments satisfy the time-delay condition II, corresponding to the time period t_k-t_{k+1}. In order to ensure that it has at least one complete switching cycle in each time period, T_{x1} and T_{x2} need to satisfy the following equation:

$$\begin{cases} T_{x1} < t_{m+1} - t_m \\ T_{x2} < t_{k+1} - t_k \end{cases} (m, k = 1, 3 \cdots 2M(N) - 1). \tag{18}$$

F. Parameter Selection Switching Limit

In taking the time division blocking delay, the delay time selection T_x has an upper limit value. First, since the more the system switching frequency is reduced, the more THD increases. Second, when switching from not taking a blocking delay to taking a blocking delay, assume that I_L rise and fall rate is kept constant. When T_x is larger, for the previous switching cycle, due to the role of blocking delay, I_L falls when the loop width exceeds $-h$. Assume that Δi reaches $-h'$ at this time. For the next switching cycle, I_L no longer rises from $-h$, so the actual single switching cycle time is slightly larger than the theoretical calculation value. If the switching cycle time of this cycle is greater than the blocking delay time T_x, resulting in the blocking delay is invalid. The switching frequency of this cycle is lower than $1/T_x$, and time division frequency fixing cannot be realized. However, this does not increase the switching frequency any further. In order to avoid this situation as much as possible, it is necessary to limit the two segmented delay time selection T_x. Taking U_g larger than 0 as an example to analyze. The principle of the inability to time division frequency fixing is shown in Fig. 17.

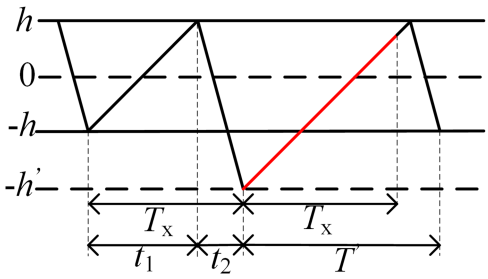

Fig. 17. Schematic diagram of the inability to time division frequency fixing.

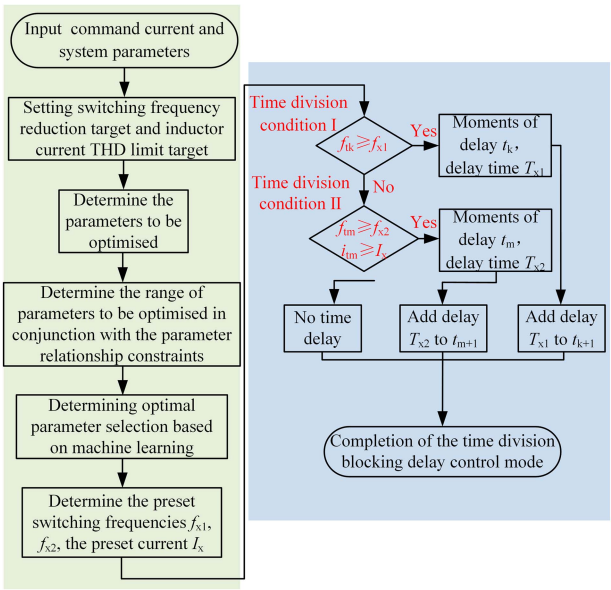

Fig. 18. Flowchart for the design of time division blocking delay control mode.

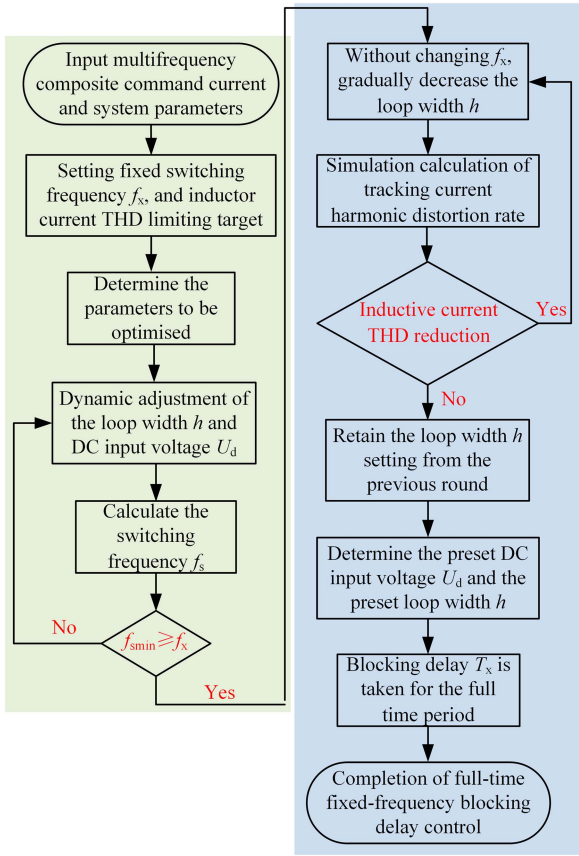

Fig. 19. Flowchart for the design of full-time fixed-frequency blocking delay control mode.

According to Fig. 17

$$\begin{cases} t_1 = \frac{2hL_P}{U_d - U_g} \\ h + h' = t_2 \frac{dI_L}{dt} = (T_x - t_1)\frac{U_d + U_g}{L_P} \\ T' = \frac{(h+h')L_P}{U_d - U_g} + \frac{2hL_P}{U_d + U_g}. \end{cases} \tag{19}$$

In order to avoid a situation where the blocking delay is not valid, it needs to be satisfied

$$T_x > T'. \tag{20}$$

Since $U_d > |U_g|_{max}$, then

$$\begin{cases} T_x < \min\left(\frac{2hL_P}{U_g(U_d+U_g)}\right), U_g \geq 0 \\ T_x > \max\left(\frac{2hL_P}{U_g(U_d+U_g)}\right), U_g < 0. \end{cases} \tag{21}$$

From (21), when U_g is less than 0, because at this time I_L rising rate is greater than the rate of decline, it is easy to know, at this time, the next switching cycle time must be less than the delay time T_x, so this error will not occur again.

In summary, when f_{x1}, f_{x2}, I_x and other parameters of the system have been determined, the selection ranges of delay times T_{x1}, T_{x2} can be obtained based on (18), (21). The overall design flow of the MFML WPT system based on HC control with time division blocking delay control is shown in Fig. 18.

For the time division blocking delay control mode, it can effectively reduce the switching frequency fluctuation range of the inverter. However, the tracking effect of I_L and the quality of received power at the load end will be affected to some extent by the decrease of inverter switching frequency. Therefore, due to the load receiving power quality has a certain limit, so the inverter switching frequency fluctuation reduction range has a limit. Then, combined with the above parameter design process, a nonlinear relationship model between time-division blocking delay control parameters and the receiving power quality of the secondary side can be established. It is possible to optimally select the time division blocking delay mode control parameters for any system parameter to achieve the most reduction in switching frequency under the premise that the power received at the load side meets the requirements.

For the full-time fixed-frequency blocking delay mode, since there is no blocking delay switching process, the starting moment of the blocking delay control for each cycle is not the original -h. Rather, for each switching cycle, Δi are over -h, and thus, there is no error due to parameter selection switching, as described above. The parameter design flow is shown in Fig. 19.

However, since I_L change rate is not a linear process. For the full-time fixed-frequency blocking delay mode, after determining the required frequency fixing rate in this system, the system parameters corresponding to the minimum tracking current harmonic distortion rate are selected by dynamically

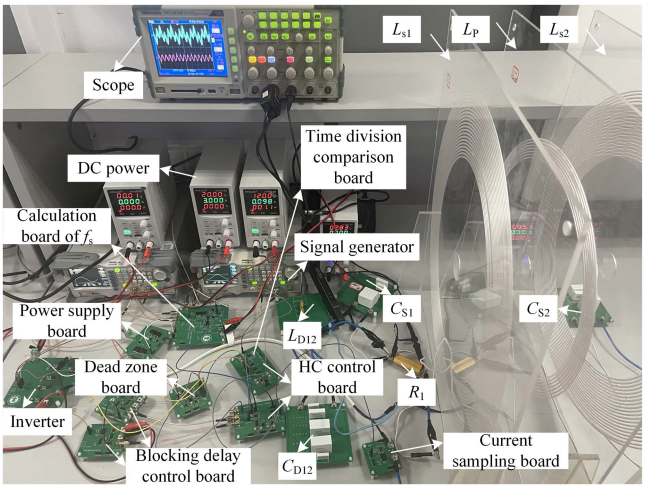

Fig. 20. Experimental setup diagram.

TABLE II
SYSTEM PARAMETERS

Parameter	Value	Parameter	Value
L_P	34.58 μH	R_{S1}	0.2 Ω
R_P	0.092 Ω	L_{S2}	0.2 Ω
L_{S1}	233.5 μH	R_{S2}	0.24 Ω
M_{P1S1}	18.019 μH	M_{P1S2}	11.52 μH
R_1	1 Ω	R_2	1 Ω

adjusting U_d and h under the conditions shown in (17). The system parameter design is completed.

V. EXPERIMENTAL VERIFICATION

In order to verify the correctness of the designed control strategy, an experimental setup was designed, as shown in Fig. 20.

An inverter designed based on GAN devices is used, which can withstand high switching frequency with low switching losses. The control module includes calculation circuit of f_s, time division comparison circuit, HC control circuit, blocking delay control circuit, dead zone circuit, and current sampling circuit. All control modules are built using analogue circuits, which do not require real-time computation and make the overall computational resources difficulty less. Meanwhile, common analogue chips are used in the circuits, which are cheap. Therefore, the overall cost increments of this control strategy are less. The parameters in the circuit are selected, as shown in Table II, and the parameters of the secondary system are the same as Table I.

A. Functional Verification of Blocking Delay Control Module

Set the delay frequency of the blocking delay control module to 500 kHz and input 1 MHz square wave to get the blocking delay module output, as shown in Fig. 21(a). The timer output capacitor voltage and the blocking delay module output are shown in Fig. 21(b).

Where U_{in} is the blocking delay module input raw signal, U_{S1} is the blocking delay module output signal, which is also the inverter switching tube S_1 drive signal. After being controlled by the dead zone circuit, it will be converted into the inverter's four drive signals. U_c is the timer output capacitor voltage.

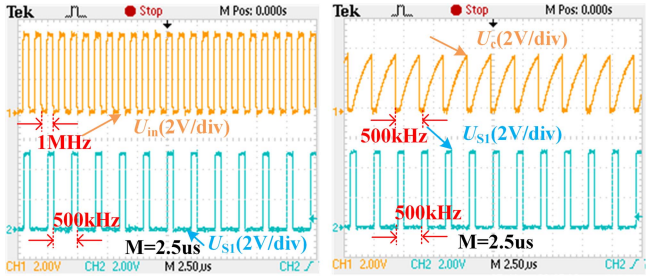

Fig. 21. Waveforms of the blocking delay module at high switching frequency. (a) Input and output signal waveforms of the blocking delay module. (b) Timer capacitor voltage and output waveform of the blocking delay module.

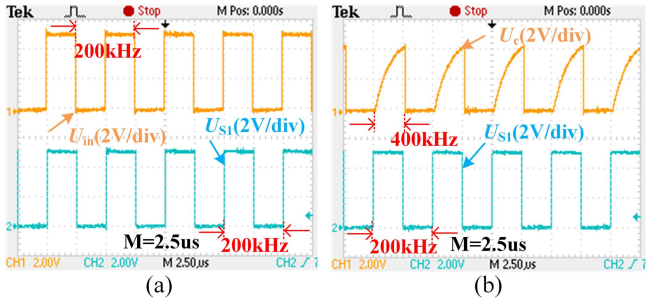

Fig. 22. Waveforms of the blocking delay module at low switching frequency. (a) Input and output signal waveforms of the blocking delay module. (b) Timer capacitor voltage and output waveform of the blocking delay module.

As shown in Fig. 21, after being controlled by the blocking delay module, the original switching frequency is reduced to the delay frequency set by the blocking delay module. Changing the input signal to 200 kHz square wave, the delay frequency of the blocking delay module is set to 400 kHz, and the output of the blocking delay module is shown in Fig. 22(a). The timer output capacitor voltage and the blocking delay module output are shown in Fig. 22(b).

As shown in Fig. 22, for switching frequencies below the blocking delay frequency, the blocking delay module will maintain the original switching signal output.

B. Validation of Time Division Blocking Delay Control Model

Due to the limitations of the sampling chip sampling rate and other hardware conditions, the command current is selected as $i_P = \sqrt{2}\sin(5000t) + \sqrt{2}\sin(25000t + \pi/2)$, U_d is set to be 20 V, and h is set to be 0.5. Before the time division blocking delay control strategy is adopted, I_L waveforms and the spectral analysis are, as shown in Fig. 23.

As shown in Fig. 23, the inverter switching frequency fluctuates from 90 kHz to 300 kHz before the time division blocking delay control strategy is adopted. The parameters of the time division blocking delay control mode are set to $f_{x1} = 196$ kHz, $f_{x2} = 180$ kHz, $I_x = 1.48$ A, $T_{x1} = 6.7$ μs, $T_{x2} = 8.3$ μs. After the time division blocking delay control, I_L waveform and spectrum analysis are shown in Fig. 24.

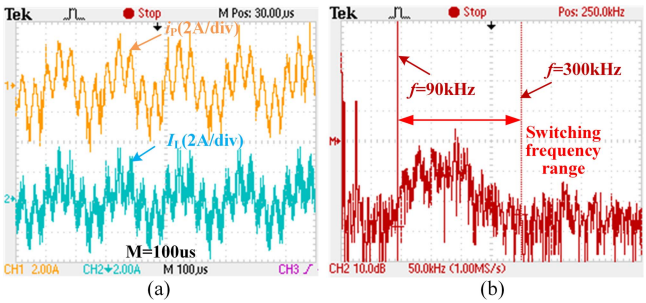

Fig. 23. (a) Dual-frequency composite command current and I_L waveforms. (b) I_L spectral analysis plot.

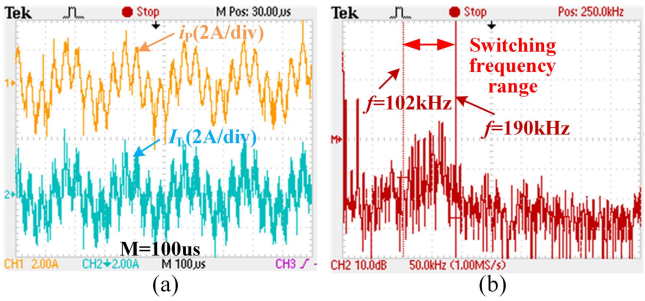

Fig. 24. (a) Dual-frequency composite command current and I_L waveforms. (b) I_L spectral analysis plot.

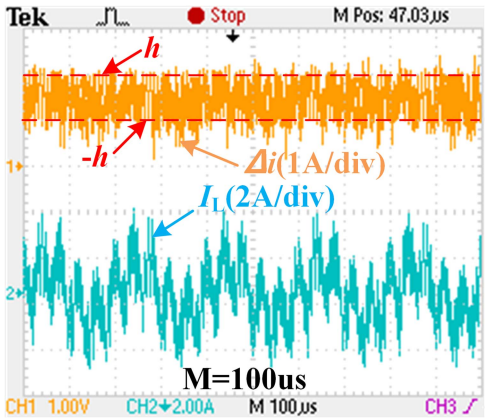

Fig. 25. Error current Δi and actual current I_L waveforms.

As shown in Fig. 24, after the time division blocking delay control, the inverter switching frequency is significantly reduced to within 200 kHz, and the part of the original switching frequency lower than the blocking delay frequency still maintains the original switching frequency unchanged. Compared to the original switching frequency fluctuation change is reduced, and the inverter switching frequency is mainly concentrated in the 120 kHz–150 kHz. At this time, Δi t waveform is shown in Fig. 25. Δi waveform is shown in Fig. 25.

As shown in Fig. 25, the blocking delay control strategy is essentially a part of $+h$ is unchanged, and -h is changed by the variable loop width control. In the time division blocking delay control mode, Δi will exceed -h in a switching cycle in the part of ΔI, which is taken to be controlled by the blocking delay, and the part of ΔI, which is not taken to be controlled by the blocking delay will remain unchanged by -h. The load voltage waveform is shown in Fig. 26.

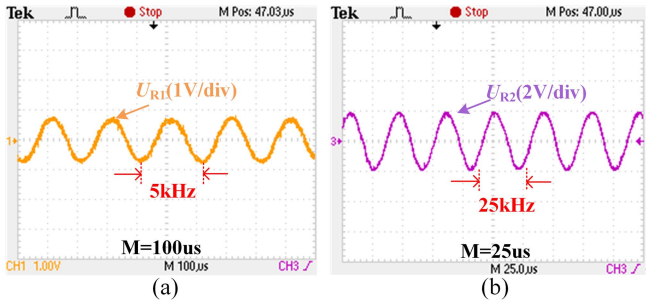

Fig. 26. Load voltage waveform. (a) Load R_1 voltage waveform. (b) Load R_2 voltage waveform.

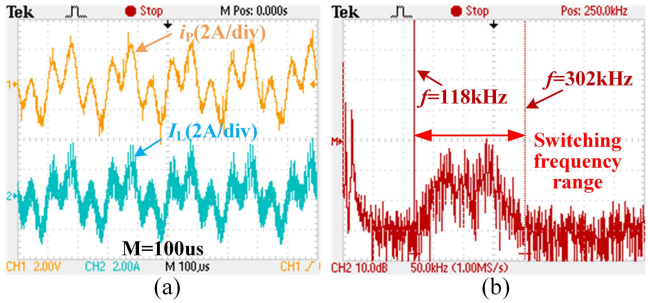

Fig. 27. (a) Dual-frequency composite command current and I_L waveforms. (b) I_L spectral analysis plot.

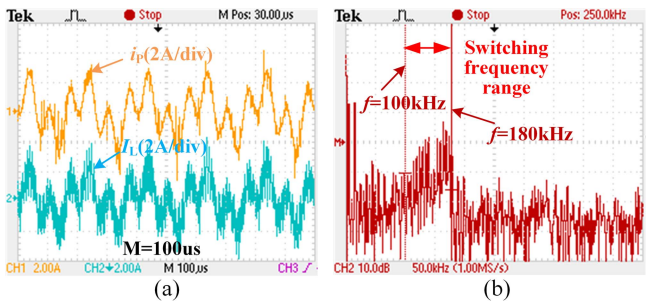

Fig. 28. (a) Dual-frequency composite command current and I_L waveforms. (b) I_L spectral analysis plot.

As shown in Fig. 26, the two loads receive power as 5 kHz and 25 kHz sinusoidal waveforms, respectively, which meets the power quality requirements of the loads.

The command current is changed to $i_P = \sqrt{2}\sin(5000t) + \sqrt{2}\sin(15000t + \pi/2)$, U_d is set to 20 V, and h is set to 0.5. Before adopting the time division blocking delay control strategy, I_L waveforms and spectral analysis are shown in Fig. 27.

As shown in Fig. 27, the inverter switching frequency fluctuates from 118 kHz to 300 kHz before the time division blocking delay control strategy is adopted. The parameters of the time division blocking delay control mode are set to $f_{x1} = 180$ kHz, $f_{x2} = 134$ kHz, $I_x = 0.91$ A, $T_{x1} = 6.4\ \mu$s, $T_{x2} = 9.7\ \mu$s. After the time division blocking delay control, I_L waveform and spectrum analysis are shown in Fig. 28.

As shown in Fig. 28, the inverter switching frequency is significantly reduced to less than 180 kHz after the time division

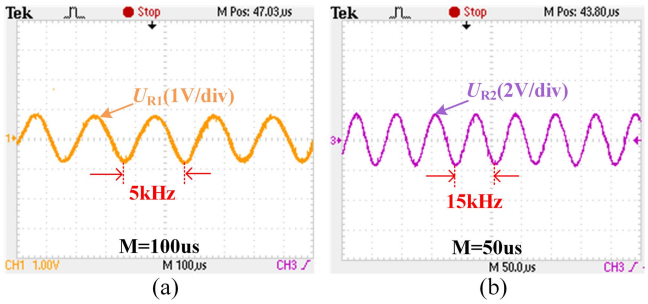

Fig. 29. Load voltage waveform. (a) Load R_1 voltage waveform. (b) Load R_2 voltage waveform.

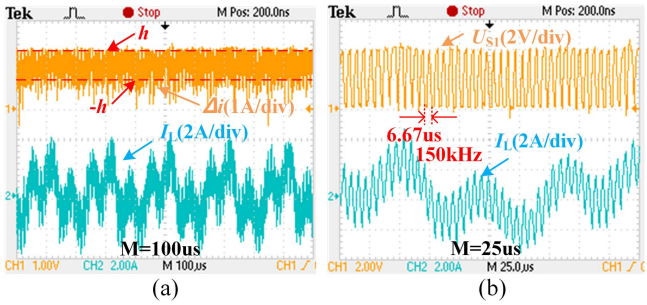

Fig. 30. (a) Dual-frequency composite command current and I_L waveforms. (b) I_L waveforms and switching tube drive signal waveforms.

blocking delay control, and the part of the original switching frequency lower than the blocking delay frequency remains unchanged from the original switching frequency. Compared with the original switching frequency fluctuation change reduction, the inverter switching frequency is mainly concentrated in 100 kHz–156 kHz. The load voltage waveform is shown in Fig. 29.

As shown in Fig. 29, the two loads receive power as 5 kHz and 15 kHz sinusoidal waveforms, respectively, which meets the power quality requirements of the loads.

C. Validation of Full-Time Fixed-Frequency Blocking Delay Control Mode

The command current is changed to $i_P = \sqrt{2}\sin(5000t) + \sqrt{2}\sin(15000t+\pi/2)$, U_d is set to 25 V, h is set to 0.5, and the rest of the parameters are the same as Tables I and II to validate the full-time fixed-frequency blocking delay control mode.

As shown in Fig. 27, the system switching frequency fluctuates from 118 kHz to 300 kHz before the full-time fixed-frequency blocking delay control strategy is adopted. First, the switching frequency is fixed to 150 kHz by adopting the full-time fixed-frequency blocking delay control. I_L waveforms, the error current waveforms, and the switching tube driving signal waveforms are shown in Fig. 30.

I_L spectrum is analyzed, as shown in Fig. 31.

As shown in Fig. 31(a) and (b), for the full-time fixed-frequency blocking delay control mode, the essence is still variable loop width control. However, since the blocking delay module has the effect of lowering the switching frequency for the whole time period, Δi will not be within h. As shown in

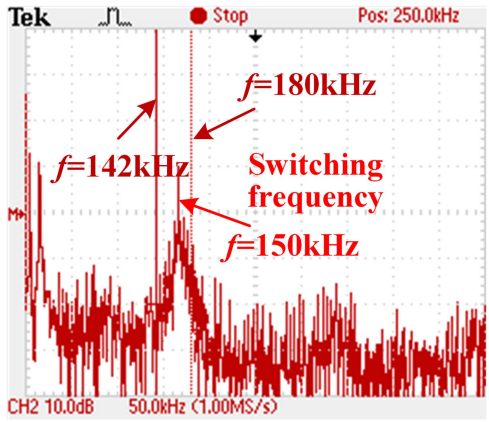

Fig. 31. I_L spectral analysis plot.

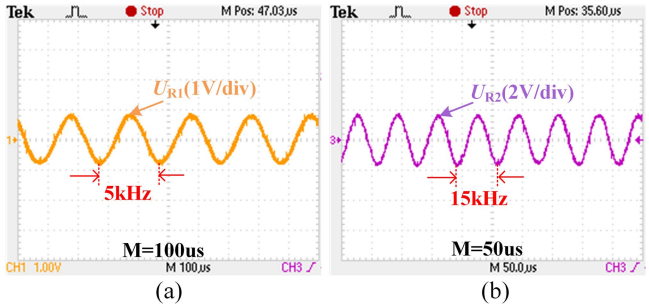

Fig. 32. Load voltage waveform. (a) Load R_1 voltage waveform. (b) Load R_2 voltage waveform.

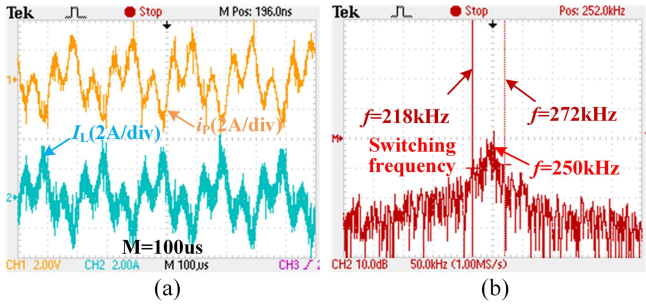

Fig. 33. (a) Dual-frequency composite command current and I_L waveforms. (b) I_L spectral analysis plot.

Fig. 31(c), the inverter switching frequency is fixed to 150 kHz. The load voltage waveform is shown in Fig. 32.

As shown in Fig. 32, the two loads receive power as 5 kHz and 15 kHz sinusoidal waveforms, respectively, which meets the power quality requirements of the loads.

Furthermore, based on the design flow of the full-time fixed-frequency blocking delay control strategy, and the switching frequency is fixed to 250 kHz. I_L waveform and spectrum analysis are shown in Fig. 33.

As shown in Fig. 33, the inverter switching frequency is fixed to 250 kHz. The load voltage waveform is shown in Fig. 34.

As shown in Fig. 34, the two loads receive power as 5 kHz and 15 kHz sinusoidal waveforms, respectively, which meets the power quality requirements of the loads. In summary, the experiments verified the correctness of the time division blocking delay

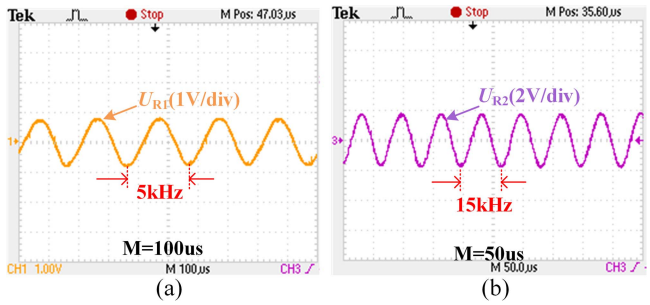

Fig. 34. Load voltage waveform. (a) Load R_1 voltage waveform. (b) Load R_2 voltage waveform.

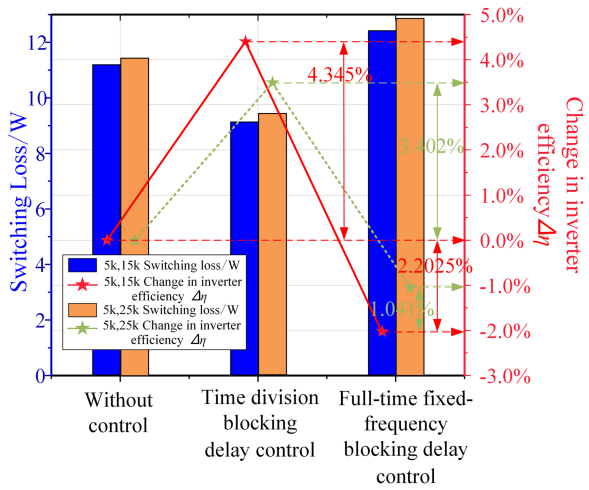

Fig. 35. Inverter switching loss and the change in inverter efficiency diagram under different control modes.

control mode and the full-time fixed-frequency blocking delay control mode, respectively.

D. Analysis of Inverter Switching Loss and Inverter Efficiency Under Different Control Modes

From the analysis of the coil transfer efficiency in [17], after the system adopts the switching frequency control strategy, i_P is unchanged, and the magnitude of the electric energy component in I_L at the load operating frequency is basically unchanged under the premise that I_L can track i_P. Meanwhile, the structural parameters of the receiving end are unchanged, so the coil transmission efficiency is basically unchanged. Therefore, this article mainly calculates the inverter switching loss and inverter efficiency. As shown in Fig. 35, the curves of switching loss and the change in inverter efficiency under different control modes are plotted.

As shown in Fig. 35, when the command current frequency is 5 kHz and 15 kHz, in the time division block delay control mode, the switching loss of the inverter is reduced by 2.452 W, and the inverter efficiency is increased by 4.345%. In the full-time fixed-frequency blocking delay control mode, the switching loss of the inverter increases by 0.996 W, and the inverter efficiency decreases by only 2.203%. When the command current frequency is 5 kHz and 25 kHz, in the time division block delay control mode, the switching loss of the inverter is reduced by 1.915 W, and the inverter efficiency is increased by 3.402%. In the full-time fixed-frequency blocking delay control mode, the switching loss of the inverter increases by 1.62 W, and the inverter efficiency decreases by only 1.041%.

After the time division blocking delay control, the switching frequency and switching times of the inverter are reduced in one command current cycle. Therefore, the switching loss of the inverter is reduced, and the inverter efficiency is improved significantly.

After the full-time fixed-frequency blocking delay control, fixing the switching frequency to 250 kHz makes part of the inverter switching frequency to be raised. Therefore, the switching loss of the inverter is slightly increased, but it is within an acceptable range. What is more worth explaining is that in the full-time fixed-frequency blocking delay control mode, the inverter switching loss is mainly related to the fixed frequency, the fixed frequency is low, the switching loss will be reduced. However, its main advantage is to achieve a fixed inverter switching frequency within the range of acceptable inverter switching loss changes, rather than reducing the inverter switching loss. The realization of fixed switching frequency of inverter under HC control is conducive to the subsequent filter design, the reduction of the output high-frequency switching harmonics, and the long-term application of the system. The significance of these functions is far greater than the impact of the reduced efficiency of the inverter currently.

E. Comparative Analysis of Existing Switching Frequency Control Technologies

At present, due to the MFML WPT system based on HC control has just been proposed, there are few inverter control strategies in this system. Therefore, several switching frequency control technologies under HC control are selected for comparative analysis in this article.

As can be seen from Table III, Zhu et al. [18] and Wang and Zhang [19] used digital variable loop width and double triangular carrier control, respectively, to achieve the fixed switching frequency of the H-bridge inverter and the single-phase grid-connected inverter by calculating the loop width in real time through digital control. However, it does not consider the effect of the command current change rate on the inverter switching frequency, which reduces the accuracy of the control. Meanwhile, the application area is only single-frequency system, and the command current frequency and inverter switching frequency are low. Xu and Liu [23] used a variable loop wide quasi-constant frequency control, which considers the change rate of the command current and improves the accuracy of the control. However, it is unable to completely fix the inverter switching frequency to 30 kHz, and there is a certain range of fluctuation. In contrast, the control strategy in this article has a good effect of fixing the frequency without obvious range fluctuations. [24] used variable discourse domain fuzzy control to fix inverter switching frequency, which improves the inverter fixed frequency rating to a certain extent, but the inverter switching frequency rating is still lower compared to that in the MFML WPT system. Xu and Zhang [25] used hybrid boundary current control. The hybrid h is

TABLE III
COMPARISON OF DIFFERENT SWITCHING FREQUENCY CONTROL TECHNOLOGIES

	Switching frequency control mode	Applicable scene	Switching frequency f_s and i_P frequency level f	Implementation method and difficulty	Consider the i_P change rate	Control effect
[18]	Digital variable loop width control	Single frequency system	f=50 Hz, f_s is tens of kHz	Digital control real-time calculation/ More difficult	NO	Fixed frequency 10 kHz
[19]	Double triangular carrier control	Single frequency system	f=50 Hz, f_s is tens of kHz	Digital control real-time calculation/ More difficult	NO	Fixed frequency 100 Hz
[23]	Variable loop width quasi-constant frequency control	Single frequency system	f is a few hundred Hz, and f_s is less than 20 kHz	Digital control real-time calculation/ More difficult	YES	Fixed frequency 30 kHz
[24]	Variable discourse domain fuzzy control	Single frequency system	f=50 Hz, f_s is tens of kHz	Variable domain fuzzy controller adjusts the loop width in real time/ More difficult	NO	Fixed frequency tens of kHz
[25]	Hybrid boundary current control	Single frequency system	f=50 Hz, f_s is tens of kHz	Digital control real-time calculation/ More difficult	NO	Reduced switching frequency fluctuation range
Proposed	Blocking delay control	MFML WPT system	f is more than 1 kHz, f_s is several hundred kHz to several MHz	Analog circuit adaptive control, without real-time calculation/ Easier	YES	Both reduce the range of switching frequency fluctuations and fix the switching frequency / Fixed frequency 250kHz

designed to reduce the inverter switching frequency fluctuation range by mixing the boundary characteristics of multiple current modulation modes. However, it is unable to fix the inverter switching frequency.

Based on the above analyses, the existing switching frequency control strategies are only for single-frequency systems, and both the command current frequency and the inverter switching frequency are low. And its essence all need to use digital control to calculate h in real time. However, in the MFML WPT system, there are multiple command current frequencies, which are usually above 1 kHz. Therefore, the inverter switching frequency can reach hundreds of kHz to several MHz. However, the control strategy proposed in this article does not require real-time calculation and is simple to control. At the same time, it can adaptively reduce the inverter switching frequency, which is still applicable in high-frequency systems. In addition, this article also considers the effect of the command current change rate on the inverter switching frequency, which improves the accuracy of control. Finally, the two working modes proposed in this article can not only reduce the fluctuation range of inverter switching frequency, but also fix the inverter switching frequency, which can be flexibly applied to different working conditions.

VI. CONCLUSION

In this article, a blocking delay switching frequency control strategy is proposed for the MFML WPT system based on HC control, and the time division blocking delay mode and the full-time fixed-frequency blocking delay mode are investigated. The time division blocking delay mode can limit the maximum switching frequency of the inverter, reduce the fluctuation range of the inverter switching frequency, and reduce the inverter switching loss. The full-time fixed-frequency blocking delay mode can fix the inverter switching frequency, which is conducive to the subsequent filter design. In addition, this article also proposes a passive compensation network design method to further ensure the power quality of the load receiving when the inverter switching frequency is reduced.

REFERENCES

[1] H. Guo, X. Zhang, and Q. Yang, "Overview of research and application of space omnidirectional wireless energy transmission technology," *Chin. Soc. Elect. Eng.*, vol. 42, no. 24, pp. 9006–9022, 2022.

[2] Y. Li, S. Shi, and X. Liu, "Review of magnetic field coupled wireless energy transmission coupling mechanism," *Trans. China Electrotechnical Soc.*, vol. 36, no. S2, pp. 389–403, 2021.

[3] P. Zhang, M. Saeedifard, O. C. Onar, Q. Yang, and C. Cai, "A field enhancement integration design featuring misalignment tolerance for wireless EV charging using LCL topology," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 3852–3867, Apr. 2021.

[4] Y. Geng, Z. Yang, and F. Lin, "Design and control for catenary charged light rail vehicle based on wireless power transfer and hybrid energy storage system," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 7894–7903, Aug. 2020.

[5] J. Wang et al., "A 403 MHz wireless power transfer system with tuned split-ring loops for implantable medical devices," *IEEE Trans. Antennas Propag.*, vol. 70, no. 2, pp. 1355–1366, Feb. 2022.

[6] S. Sun, B. Zhang, and J. Li, "Topological development and analysis of multiload magnetically coupled wireless energy transmission systems," *Trans. China Electrotechnical Soc.*, vol. 37, no. 8, pp. 1885–1903, 2022.

[7] F. Liu, Y. Yang, Z. Ding, X. Chen, and R. M. Kennel, "A multifrequency superposition methodology to achieve high efficiency and targeted power distribution for a multiload MCR WPT system," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 9005–9016, Oct. 2018.

[8] D. Ahn and P. P. Mercier, "Wireless power transfer with concurrent 200-kHz and 6.78-MHz operation in a single-transmitter device," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 5018–5029, Jul. 2016.

[9] X. Zhang, F. Liu, and T. Mei, "Multifrequency phase-shifted control for multiphase multiload MCR WPT system to achieve targeted power distribution and high misalignment tolerance," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 991–1003, Jan. 2021.

[10] C. Zhao and D. Costinett, "GaN-based dual-mode wireless power transfer using multifrequency programmed pulse width modulation," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9165–9176, Nov. 2017.

[11] C. Xia, S. Ren, N. Ma, Y. Hou, Y. Sun, and J. Chen, "Fundamental-harmonic dual pathway parallel inductively coupled power transmission system," *Automat. Electric Power Syst.*, vol. 41, no. 7, pp. 93–100, 2017.

[12] Y.-J. Kim, D. Ha, W. J. Chappell, and P. P. Irazoqui, "Selective wireless power transfer for smart power distribution in a miniature-sized multiple-receiver system," *IEEE Trans. Ind. Electron.*, vol. 63, no. 3, pp. 1853–1862, Mar. 2016.

[13] C. Xia, N. Wei, H. Zhang, S. Zhao, Z. Li, and Z. Liao, "Multifrequency and multiload MCR-WPT system using hybrid modulation waves SPWM control method," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 12400–12412, Nov. 2021.

[14] J. Wu, L. Bie, W. Kong, P. Gao, and Y. Wang, "Multifrequency multi-amplitude superposition modulation method with phase shift optimization for single inverter of wireless power transfer system," *IEEE Trans. Circuits Syst. I, Regular Papers*, vol. 68, no. 5, pp. 2271–2279, May 2021.

[15] D. Thenathayalan and J.-H. Park, "Individually regulated multiple-output WPT system with a single PWM and single transformer," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 4, pp. 3542–3557, Dec. 2020.
[16] D. Thenathayalan and J.-H. Park, "An independently controlled single-PWM multiple-output narrow-band resonant converter," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5042–5061, Jun. 2018.
[17] A. Sun et al., "Multifrequency and multiload MCR-WPT system based on hysteresis current control," *IEEE Trans. Power Electron.*, vol. 39, no. 8, pp. 10532–10545, Aug. 2024, doi: 10.1109/TPEL.2024.3393003.
[18] S. Zhu, H. Ouyang, and D. Liu, "A novel modulation method for H-bridge cascaded inverter based on current hysteresis loop control," *Trans. China Electrotechnical Soc.*, vol. 28, pp. 212–218, 2013.
[19] W. Wang and D. Zhang, "Dual-delta carrier-based inverter control strategy," *Power Electron.*, vol. 55, no. 5, pp. 117–119, 2021.
[20] C. Anyapo, N. Teerakawanich, C. Mitsantisuk, and K. Ohishi, "Development of wireless power transfer with primary-side current mode control capability using virtual-current source resonant inverter," in *Proc. 44th Annu. Conf. IEEE Ind. Electron. Soc.*, 2018, pp. 4805–4809.
[21] S. Samanta and A. K. Rathore, "Wireless power transfer technology using full-bridge current-fed topology for medium power applications," *IET Power Electron.*, vol. 9, no. 9, pp. 1903–1913, Jul. 2016.
[22] Y. Gu, S. Chen, and Z. Lv, "Implementation strategy of controlled-type soft switching converter," *Chin. Soc. Elect. Eng.*, vol. 25, no. 6, pp. 58–62, 2005.
[23] Y. Xu and X. Liu, "Variable-loop wide quasi-constant-frequency current hysteresis loop control method considering command current," *Trans. China Electrotechnical Soc.*, vol. 27, no. 6, pp. 90–95, 2012.
[24] M. Dai, H. Chen, and F. Zhen, "Improved hysteresis loop current control strategy for microgrid grid-connected inverters," *Power Electron.*, vol. 52, no. 4, pp. 24–26, 2018.
[25] J. Xu and D. Zhang, "A novel hybrid soft-switching current control strategy for single-phase inverters," *Electric Eng.*, vol. 40, no. 5, pp. 8–12, 2019.

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