Switch Open-Circuit Fault Diagnosis Method Using Bridge Arm Midpoint Voltage Integral for LLC Resonant Converter

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***Abstract*—The *LLC* resonant converter offers several advantages, including compact size, low losses, and high efficiency. These attributes make it an ideal choice for use in seafloor observation networks where space is limited and efficient heat dissipation is crucial. However, the reliability of the *LLC* converter is compromised due to the susceptibility of the primary switch to failure. In response to this issue, this article proposes a precise open-circuit fault diagnosis (OCFD) method for phase-shifted *LLC* resonant converters using the integral of the bridge arm midpoint voltage, aiming to identify the fault location and facilitate maintenance. First, the characteristics of the primary-side switch fault in the *LLC* resonant converter are analyzed in detail, and the characteristic quantity required for fault diagnosis is selected. Subsequently, the OCFD method is introduced, which exclusively depends on the integral value of the voltage at the midpoint of the primary-side switching bridge arm. Following this, a diagnostic circuit is designed to process the bridge-arm midpoint voltage and precisely pinpoint the faulty switch. Finally, the experimental verification is performed on the *LLC* resonant converter prototype. The results demonstrate that the proposed method can swiftly detect and locate faults within two switching cycles when the *LLC* converter operates at 100 kHz.**

***Index Terms*—Bridge arm midpoint voltage, fault diagnosis, *LLC* resonant converter, open circuit.**

I. Introduction

At present, isolated dc–dc converters are extensively employed in a wide range of dc power conversion applications. Among the various circuit topologies available for isolated dc–dc converters, the *LLC* resonant converter has gained prominence due to its utilization of high-frequency soft switching technology. This technology offers several advantages, including high power density, low losses, and high efficiency [1], [2], [3]. Consequently, *LLC* resonant converters are particularly well-suited for specialized scenarios that demand exceptional volume and heat dissipation performance, such as seafloor observation and aerospace applications. However, in these scenarios, it becomes imperative to enhance the reliability of *LLC* resonant converters [4], [5], [6].

Switch faults of the primary-side semiconductor power account for approximately half of all faults encountered in *LLC* converters [7], [8], [9]. They can generally be categorized into short circuit faults (SCF) and open circuit faults (OCF) [7]. SCF is usually caused by gate oxide shortening or shorting of the gate and source metals [10]. For SCF, most drive circuits have integrated short-circuit protection functions [11]. OCF can be attributed to lifted bond wires, faults in the gate driver circuit, or cracking resulting from SCF [10], [12]. OCF characteristic will not trigger the converter protection, resulting in long-term operation under an open-circuit fault. This would cause damage to healthy components [14], [15], OCF tends to occur more frequently [13], and lacks accurate guidelines for protection design [18]. The requirements for the open-circuit fault diagnosis (OCFD) scheme mainly include three points. One is to reduce system power outage time. At present, OCFD is mostly done through offline detection, which requires a long time for maintenance. Second, to reduce the number of component replacements. Most existing solutions locate and replace the entire bridge arm. The third is to reduce costs. Currently, OCFD requires additional testing equipment and labor [8], [9].

Regarding open circuit faults in dc–dc converters, various researchers have conducted relevant studies. The traditional approach to OCF is to select semiconductor devices with excessive redundant power during the design and manufacturing of converter equipment [16]. However, this method is not cost-effective and may result in increased volume. Pei et al. [17] proposed an OCF diagnosis method using the dc-link voltage and the average value of the transformer primary voltage as diagnostic criteria. This method needs to add an additional auxiliary winding on the transformer primary side, which may not be suitable for the converters already in production. In [18], an FPGA-based fast switching fault diagnosis method is presented for nonisolated dc–dc converters, utilizing the inductor current. However, this method may involve complex algorithms and expensive detection costs. Zheng et al. [19] used the average value of the bridge-arm midpoint voltage as a means to quickly identify

Manuscript received 31 December 2023; revised 31 May 2024; accepted 1 July 2024. Date of publication 12 July 2024; date of current version 4 September 2024. This work was supported in part by the National Natural Science Foundation of China under Grant 52125705, in part by the Key Research and Development Program of Hunan Province, China, under Grant 2023GK2010, and in part by the National Natural Science Foundation of China under Grant 52207203. Recommended for publication by Associate Editor T. Mishima. *(Corresponding authors: Yang Li; Zhikang Shuai.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3427134.

Digital Object Identifier 10.1109/TPEL.2024.3427134

faults. This approach may be prone to fault diagnosis errors due to sampling errors. In [20] and [21], a fault diagnosis method for dc–dc converters using the magnetic near-field as a diagnostic criterion is proposed. This method employs a ring magnetic near-field probe to capture the magnetic near-field of the converter. However, it may be susceptible to interference from the diagnosis location and the external environment, making it less suitable for engineering applications. Pei et al. [22] proposed a solution to achieve primary winding voltage waveform distortion using active phase shift control, but this method requires additional auxiliary windings and magnetic probes, which is costly. Zhuo et al. [23] introduced a real-time diagnosis method for switch faults based on the Luenberger observer. This method utilizes the inductor current as a diagnostic variable, reducing the need for additional sensors.

Sun et al. [24] proposed a novel fault diagnostic method for the single-ended primary-inductor converter based on the crow search algorithm and deep belief network. Dhumale and Lokhande [25] proposed an ANN fault diagnostic strategy combined with Park's vector transform and discrete wavelet transform to identify both single and multiple open switch faults when the voltage source inverters operate under variable load conditions. Han et al. [26] proposed an initial fault diagnosis method for dc–dc converters, utilizing multidimensional feature fusion. This method incorporates a feature selection technique based on Mahalanobis distance to identify sensitive features and achieve feature fusion. However, those methods require a large amount of training data and computing resources, and its computing efficiency needs improvement. Fan et al. [27] proposed a hybrid fault diagnosis method based on a cascaded H-bridge multilevel converter open-circuit fault disturbance estimation convolutional network, which combines model-based and data-driven multilevel converter diagnosis methods. Chai et al. [28] proposed a predictive control multilevel converter fault diagnosis method based on a finite control set model. Model predictive control fault detection methods were also proposed for modular multilevel converters [29] and matrix converters [30]. This type of method can detect single or multiple open-circuit switch faults without additional voltage or current sensors by comparing the converter current predicted by the model predictive controller with the actual measurement value. However, those methods are susceptible to measurement noise and model uncertainty, resulting in misdiagnosis.

In summary, the aforementioned methods cannot simultaneously meet the criteria of simple control and topology, fast and accurate diagnosis, low cost, and compatibility with existing hardware devices. This article proposes a switch open-circuit fault diagnosis method using bridge arm midpoint voltage integral for *LLC* resonant converter with phase-shift control. The main contributions of this article are as follows.

1) The proposed OCF diagnosis principle relies solely on the integral value of the primary-side bridge arm midpoint voltage to quickly detect and locate the fault. Compared to existing methods that employ average values, this method is less susceptible to sampling errors and interference, thereby enhancing diagnostic accuracy.
2) A simple hardware circuit for diagnosing open circuit faults is designed, requiring only a minimal number of operational amplifiers, comparators, and logic chips. The structure of the circuit is uncomplicated, low cost, easy to install and configure.
3) The OCFD method proposed in this article is an online detection method that can monitor and determine device OCF in real time. Accurately locating the faulty switch position can shorten maintenance time and reduce components replacement.

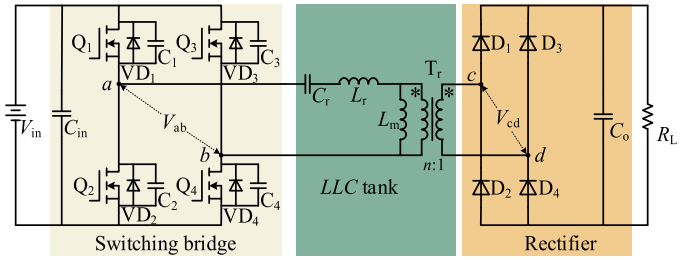

Fig. 1. Typical topology of *LLC* full bridge resonant converter.

The rest of this article is organized as follows. Section II introduces the *LLC* resonant converters topology. Section III analyzes the open-circuit fault characteristics in detail. Then, an OCF diagnosis strategy is proposed and diagnostic circuit is designed in Section IV. Section V carries out experimental verification. Finally, Section VI concludes this article.

II. Topology of *LLC* Resonant Converter

A typical *LLC* converter topology is shown in Fig. 1, which adopts phase-shift control. It mainly consists of three parts: primary-side full bridge, *LLC* resonant tank, and secondary-side uncontrolled rectifier bridge. The primary-side full bridge consists of 4 silicon carbide metal–oxide–semiconductor field-effect transistors (SiC MOSFETs), which can easily work at 100 kHz frequency. SiC MOSFETs typically consist of a power transistor, parasitic capacitors C_1–C_4 and body antiparallel diodes VD_1 – VD_4. The resonant tank includes inductors L_r, L_m and capacitor C_r, where L_r and C_r are resonant inductor and resonant capacitor, respectively, and L_m can be replaced by transformer excitation inductor. The uncontrolled rectifier bridge on the secondary-side is composed of 4 Schottky diodes.

III. Open Circuit Fault Analysis

Open-circuit faults of different semiconductor switches on the primary-side in the *LLC* resonant converter may occur at different moments. Therefore, the process is more complicated. The Q_2 and Q_4 are taken as examples to analyze the OCF characteristics in this article, which belong to different bridge arms. Among them, V_{in}, V_{ab} V_{Cr}, $V_{Qn\text{-}ON}$, and V_{VDn} represent the input voltage, the voltage at the midpoint of the primary-side switching bridge arm, the resonant capacitor voltage, the SiC MOSFET ON-state voltage, and the body antiparallel diode VD_n conduction voltage drop ($n = 1, 2, 3,$ and 4). Finally, the midpoint voltage value of the primary side bridge arm in one cycle after all the switch tubes are turned ON simultaneously when the Q_2 and Q_4 tubes are turned ON is summarized.

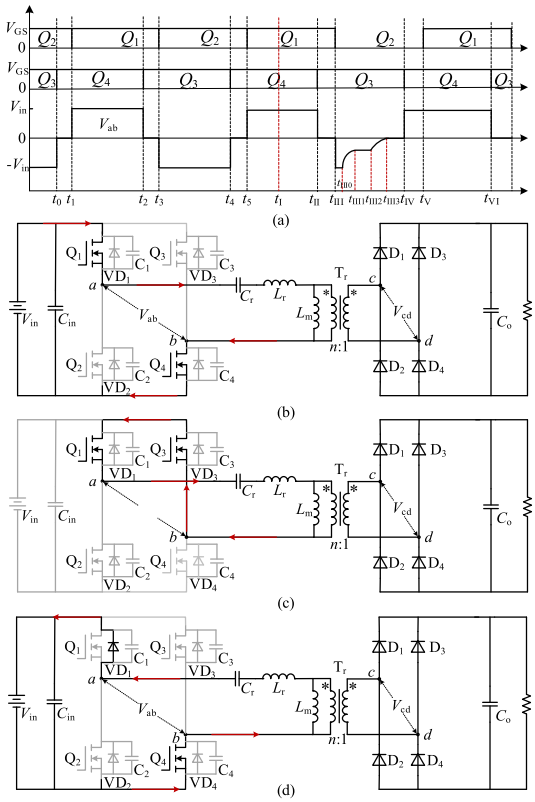

Fig. 2. Transient processes and key waveforms under Q_2 OCF. (a) Key waveforms. (b) Mode 1 and mode 5. (c) Mode 2. (d) Mode 4.

A. Analysis of the Open Circuit Fault on Q_2

The fault characteristics of the *LLC* resonant converter in Q_2 OCF occurs are analyzed when Q_1 and Q_4 are turned ON, which is main divided five modes. Some transient waveforms are shown in Fig. 2(a).

Mode 1 ($t_I \sim t_{II}$)*:* Q_1 and Q_4 are turned ON at the same time, and OCF occurs in Q_2 tube at t_I. Since the disconnection of Q_2 will not affect the original working state of Q_1 and Q_4, the circuit is shown in Fig. 2(b). At the moment, V_{ab} can be expressed as

$$V_{ab} = V_{in} - V_{Q1\text{-}on} - V_{Q4\text{-}on} \approx V_{in}. \tag{1}$$

Mode 2 ($t_{II} \sim t_{III}$)*:* At t_{II}, Q_4 is turned OFF, Q_3 is turned ON. That is, Q_1 and Q_3 are turned ON, forming a freewheeling circuit, as shown in Fig. 2(c), then there is

$$V_{ab} = -(V_{Q1\text{-}on} + V_{Q3\text{-}on}) \approx 0. \tag{2}$$

Mode 3 ($t_{III} \sim t_{IV}$)*:* At t_{III}, Q_1 is OFF and Q_2 should be ON. However, due to an open-circuit fault in Q_2, it remains OFF, causing the current in the resonant cavity to automatically seek the most suitable flow path. Owing to the presence of switched parallel capacitors and diodes, both the magnitude and path of the current are altered. The analysis becomes more complex, being divided into five microtransient processes as follows.

1) When Q_1 is turned OFF, the resonant inductor current, which cannot change abruptly, rapidly charges capacitor C_1. Consequently, the voltage at point a of the front bridge arm swiftly drops from V_{in} to 0. Given the small value of the parasitic capacitance C_1, the duration of this process is extremely brief, typically on the order of nanoseconds. Simultaneously, the voltage at the bridge arm midpoint *ab* rapidly shifts from 0 to -V_{in}. As the voltage at point *a* falls to 0 and the current direction remains unchanged, the reverse diode VD_2 of Q_2 is compelled to conduct, forming a new current loop as depicted in Fig. 3(a). Applying the Kirchhoff's voltage law, the voltage at the midpoint ab of the bridge arm during this process can be calculated as

$$V_{ab} = -V_{in} + V_{Q3\text{-}on} + V_{VD2} \approx -V_{in}. \tag{3}$$

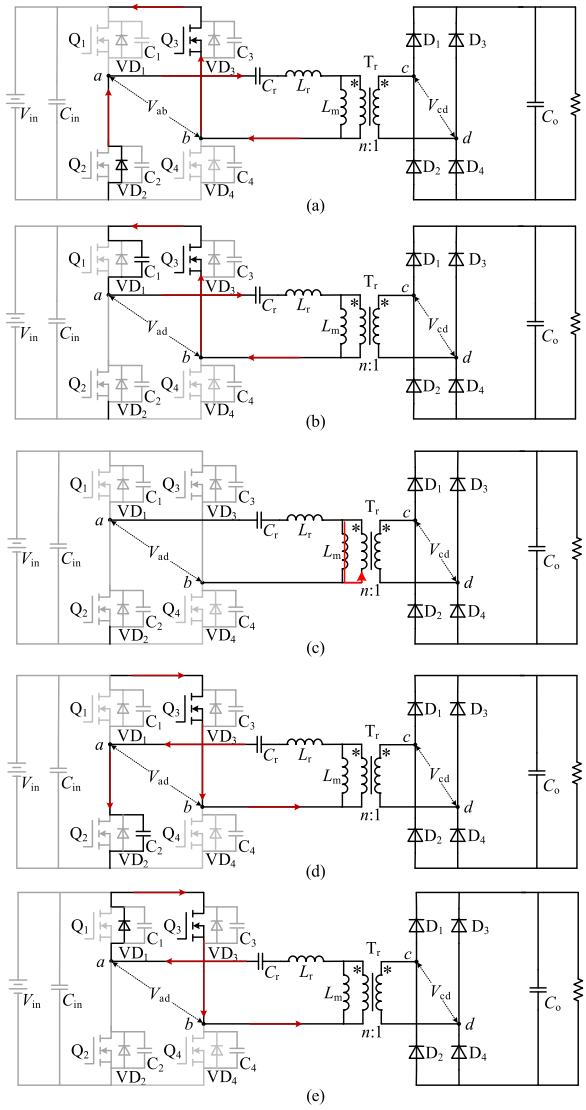

Fig. 3. Transient processes of open circuit fault device Q_2 participating in working mode 3. (a) At t_{III}. (b) At t_{III0}. (c) At t_{III1}. (d) At t_{III2}. (e) At t_{III3}.

2) As the resonant inductor current decreases, the resonant capacitor C_r charges further, causing a continuous increase in the voltage at point a. This can be considered the voltage discharge process of the parallel capacitor C_1 associated with Q_1, as illustrated in Fig. 3(b). Consequently, the voltage V_{ab} at the midpoint of the primary side bridge

arm decreases

$$V_{\mathrm{ab}} = (-V_{\mathrm{in}} + V_{\mathrm{Q3\text{-}on}} + V_{\mathrm{VD2}})e^{-\sqrt{\frac{C_1}{(C_1+C_r)L_r}}(t-t_{\mathrm{III0}})} > -V_{\mathrm{in}}. \quad (4)$$

3) At t_{III1}, the current in the resonant circuit reduces to zero, the voltage V_{Cr} across the resonant capacitor C_{r} remains constant, and the voltage across inductor L_{r} approaches zero. All residual energy in inductor L_{m} is transferred to the secondary side, as depicted in Fig. 3(c). At this process, the bridge arm midpoint voltage V_{ab} can be expressed as

$$V_{\mathrm{ab}} = -V_{\mathrm{in}} + V_{\mathrm{Cr}} > -V_{\mathrm{in}}. \quad (5)$$

4) At t_{III2}, influenced by the voltage of the resonant capacitor C_{r}, the resonant inductor current reverses direction, and the parallel parasitic capacitance C_2 of Q_2 charges via the activated Q_3, creating a current loop, as depicted in Fig. 3(d). Throughout this process, the voltage at point a on the front bridge arm progressively increases until the antiparallel diode VD_1 of the Q_1 starts conducting. Subsequently, the bridge arm midpoint voltage V_{ab} can be articulated as

$$V_{\mathrm{ab}} = (-V_{\mathrm{in}} + V_{\mathrm{cr}})e^{-\sqrt{\frac{C_2}{(C_2+C_r)(L_r+L_m)}}(t-t_{\mathrm{III2}})} > -V_{\mathrm{in}}. \quad (6)$$

5) At t_{III3}, following the activation of the Q_1 antiparallel diode VD_1, a freewheeling loop is formed with the Q_3 tube and the resonant cavity, as illustrated in Fig. 3(e). During this process, the bridge arm midpoint voltage V_{ab} diminishes to nearly zero

$$V_{\mathrm{ab}} = V_{\mathrm{Q3\text{-}on}} + V_{\mathrm{VD1}} \approx 0. \quad (7)$$

Mode 4 ($t_{\mathrm{IV}} \sim t_{\mathrm{V}}$)*:* Upon completion of mode 3, at moment t_{IV}, the Q_3 turns OFF while the Q_4 begins to turn ON. Given that the inductor current remains constant, the voltage across Q_3 parallel capacitor C_3 rapidly escalates from 0 to V_{in}, while the voltage at point b of the rear bridge arm falls to zero. Following the turn-ON of the Q4, current flow is impeded as the Q_2 remains disconnected. As the magnitude and direction of the resonant inductor current cannot abruptly alter, the Q_4 and the Q_1 antiparallel diode VD_1 establish a freewheeling loop, as depicted in Fig. 2(d). Consequently, the bridge arm midpoint voltage V_{ab} undergoes another change, described as

$$V_{\mathrm{ab}} = V_{\mathrm{in}} + V_{\mathrm{Q4\text{-}on}} + V_{\mathrm{VD1}} \approx V_{\mathrm{in}}. \quad (8)$$

Mode 5 ($t_{\mathrm{V}} \sim t_{\mathrm{VI}}$)*:* Q_2 is turned OFF, Q_1 is turned ON at t_{V}. Q_1, Q_4 and the resonant tank forming a forward charging circuit for the resonant capacitor, as shown in Fig. 2(b). Then, there is

$$V_{\mathrm{ab}} = V_{\mathrm{in}} - V_{\mathrm{T1\text{-}on}} - V_{\mathrm{T4\text{-}on}} \approx V_{\mathrm{in}}. \quad (9)$$

B. Analysis of the Open Circuit Fault on Q_4

Similarly, assuming that OCF occurs in Q_4 when Q_1 and Q_4 are turned ON, the transient characteristics of the *LLC* resonant converter are analyzed ignoring the dead time with one cycle. It can be mainly divided into five modes, and the transient waveforms are shown in Fig. 4(a).

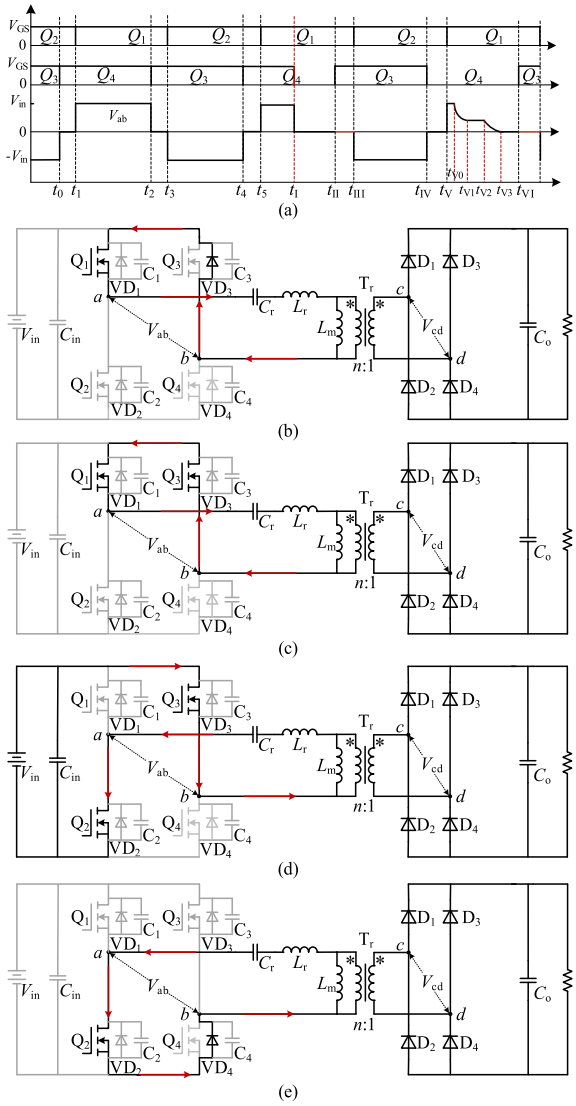

Fig. 4. Transient processes and key waveforms under Q_4 OCF. (a) Key waveforms. (b) Mode1. (c) Mode 2. (d) Mode 3. (e) Mode 4.

Mode 1 ($t_{\mathrm{I}} \sim t_{\mathrm{II}}$)*:* During the operation of the *LLC* converter, when transistors Q_1 and Q_4 are simultaneously ON-state, an OCF in Q_4 at t_{I} abruptly interrupts the original conduction path. As the resonant inductor current cannot change instantaneously, capacitor C_4 rapidly charges until its voltage equals V_{in}. Consequently, the voltage at midpoint b of the rear bridge arm enables the forward conduction of the Q_3 antiparallel diode VD_3, leading to the formation of a freewheeling circuit comprising Q_1, VD_3, and the resonant circuit, as illustrated in Fig. 4(b). During the freewheeling phase, the midpoint voltage V_{ab} of the primary side bridge arm is expressed as

$$V_{\mathrm{ab}} = -(V_{\mathrm{VD3}} + V_{\mathrm{Q1\text{-}on}}) \approx 0. \quad (10)$$

Mode 2 ($t_{\mathrm{II}} \sim t_{\mathrm{III}}$)*:* At t_{II}, Q_4 is turned OFF and Q_3 is turned ON. Q_1, Q_3 and the resonant tank form a freewheeling circuit, as shown in Fig. 4(c), then there is

$$V_{\mathrm{ab}} = -(V_{\mathrm{Q1\text{-}on}} + V_{\mathrm{Q3\text{-}on}}) \approx 0. \quad (11)$$

Mode 3 ($t_{\mathrm{III}} \sim t_{\mathrm{IV}}$)*:* At t_{III}, Q_1 is turned OFF, and Q_2 is turned ON. Q_2 and Q_3 form a reverse charging circuit for the resonant capacitor C_{r}, as shown in Fig. 4(d). In this mode, V_{ab} can be calculated as

$$V_{\mathrm{ab}} = -V_{\mathrm{in}} + V_{\mathrm{Q2\text{-}on}} + V_{\mathrm{Q3\text{-}on}} \approx -V_{\mathrm{in}}. \tag{12}$$

Mode 4 ($t_{\mathrm{IV}} \sim t_{\mathrm{V}}$)*:* At t_{IV}, in accordance with the steady-state operation rules of the *LLC* converter, the Q_3 turns OFF while the Q_4 begins to turn ON. The capacitor C_4 commences rapid discharge, with the voltage across C_4 swiftly falling from V_{in} to zero. Concurrently, the potential at midpoint *b* of the rear bridge arm also diminishes to zero. Due to an open circuit fault, the Q_4 remains disconnected. This condition forces the current to flow through the Q_4 antiparallel diode VD_4. The Q_4 antiparallel diode VD_4, along with Q_2 and the resonant circuit, establishes a freewheeling circuit, as depicted in Fig. 4(f). Throughout this period, the expression for the midpoint voltage V_{ab} of the primary side bridge arm is calculated as

$$V_{\mathrm{ab}} = V_{\mathrm{Q2\text{-}on}} + V_{\mathrm{VD4}} \approx 0. \tag{13}$$

Mode 5 ($t_{\mathrm{V}} \sim t_{\mathrm{VI}}$)*:* At t_{V}, Q_2 turns OFF, while Q_1 starts to turn ON, entering the positive half-cycle conduction phase of Q_1 and Q_4. However, due to an open circuit fault, Q_4 cannot conduct normally and remains disconnected. Consequently, only Q_1 is ON-state during this phase. Owing to the presence of switched parallel capacitors and diodes, both the magnitude and path of the current are altered. The analysis mode is more complicated, mainly divided into five microtransient processes as follows.

1) Following the deactivation of Q_2, its parallel capacitor C_2 charges rapidly, with the voltage across C_2 escalating from zero to V_{in}. Concurrently, the voltage at point *a* of the front bridge arm attains V_{in}. Given that the direction of the current in the resonant inductor cannot change abruptly, the current forms a conduction loop via the antiparallel diodes of Q_1 and Q_4, as depicted in Fig. 5(a). At this moment, the bridge arm midpoint voltage V_{ab} is calculated as follows:

$$V_{\mathrm{ab}} = V_{\mathrm{in}} + V_{\mathrm{Q1\text{-}on}} + V_{\mathrm{VD4}} \approx V_{\mathrm{in}}. \tag{14}$$

2) As the resonant inductor current progressively diminishes, the resonant capacitor C_{r} continues to charge, resulting in a sustained increase in the voltage at point *b*. This phenomenon can be interpreted as the voltage discharge process of the parallel capacitor C_3 of Q_3, as illustrated in Fig. 5(b). Consequently, the voltage V_{ab} at the midpoint of the bridge arm on the primary side begins to decrease

$$V_{\mathrm{ab}} = (V_{\mathrm{in}} + V_{\mathrm{Q1\text{-}on}} + V_{\mathrm{VD4}}) e^{-\sqrt{\frac{C_3}{(C_3+C_{\mathrm{r}})L_{\mathrm{r}}}}(t-t_{\mathrm{V0}})} < V_{\mathrm{in}}. \tag{15}$$

3) At t_{V1}, the current in the resonant circuit diminishes to zero, the voltage V_{Cr} across the resonant capacitor C_{r} remains constant, and the voltage across the inductor L_{r} approaches zero. All residual energy in the inductor L_{m} is transferred to the secondary side, as depicted in Fig. 5(c). At this moment, the bridge arm midpoint voltage V_{ab} can be articulated as

$$V_{\mathrm{ab}} = V_{\mathrm{in}} - V_{\mathrm{cr}} < V_{\mathrm{in}}. \tag{16}$$

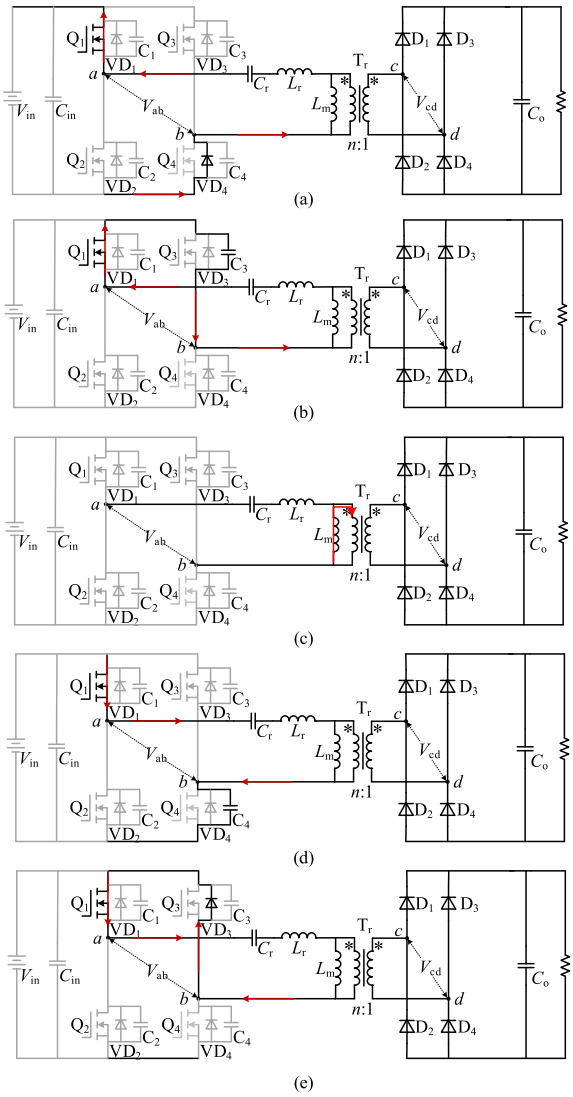

Fig. 5. Transient processes of open circuit fault device Q_4 participating in working mode 5. (a) At t_{V}. (b) At t_{V0}. (c) At t_{V1}. (d) At t_{V2}. (e) At t_{V3}.

4) At t_{V2}, influenced by the voltage of the resonant capacitor C_{r}, the current through the resonant inductor begins to reverse. Concurrently, the parallel parasitic capacitance C_4 of Q_4 charges via the activated Q_1, establishing a current loop, as depicted in Fig. 5(d). Throughout this process, the voltage at point *b* on the front bridge arm progressively increases until the antiparallel diode VD_3 of Q3 commences conduction. Subsequently, the bridge arm midpoint voltage V_{ab} can be articulated as

$$V_{\mathrm{ab}} = (V_{\mathrm{in}} - V_{\mathrm{Cr}}) e^{-\sqrt{\frac{C_4}{(C_4+C_{\mathrm{r}})(L_{\mathrm{r}}+L_m)}}(t-t_{\mathrm{V2}})} < V_{\mathrm{in}}. \tag{17}$$

5) At t_{V3}, following the activation of the Q_3 antiparallel diode VD_3, a freewheeling loop is established with the Q_3 and the resonant cavity, as depicted in Fig. 5(e). Throughout this process, the bridge arm midpoint voltage V_{ab} diminishes nearly to zero

$$V_{\mathrm{ab}} = -(V_{\mathrm{Q1\text{-}on}} + V_{\mathrm{VD3}}) \approx 0. \tag{18}$$

TABLE I
PRIMARY-SIDE ARM MIDPOINT VOLTAGE AT OPEN CIRCUIT FAULT

Mode	Primary side bridge arm midpoint voltage V_{ab}			
	Q_1 OCF	Q_2 OCF	Q_3 OCF	Q_4 OCF
Mode 1	0	V_{in}	V_{in}	0
Mode 2	$-V_{in}$	0	0	0
Mode 3	$-V_{in}$	$-V_{in}$, $-V_1$, $-V_2$, $-V_3$, 0	$-V_{in}$, $-V_1$, $-V_2$, $-V_3$, 0	$-V_{in}$
Mode 4	0	V_{in}	0	0
Mode 5	V_{in}, V_1, V_2, V_3, 0	V_{in}	V_{in}	V_{in}, V_1, V_2, V_3, 0

Similarly, the Q_1 and Q_3 open-circuit faults are analyzed. In a fault cycle, the change of the midpoint voltage of the primary side bridge arm is shown in Table I. It can be seen that after an open-circuit fault, the midpoint voltage of the primary side bridge arm will always change in some modes compared with normal operation. This provides a certain theoretical basis for the subsequent fault diagnosis of this article.

To demonstrate the bridge arm midpoint voltage V_{ab} of each modal in Table I, assuming primary-side semiconductor switches have the same parasitic parameters. The conduction voltage drops $V_{Q1\text{-}ON}$, $V_{Q2\text{-}ON}$, $V_{Q3\text{-}ON}$, and $V_{Q4\text{-}ON}$ for Q_1, Q_2, Q_3, and Q_4 are equal, respectively. Similarly, the forward voltage drops V_{VD1}, V_{VD2}, V_{VD3}, and V_{VD4} of the parallel diodes are considered equal. The parasitic capacitances C_1, C_2, C_3, and C_4 are likewise equal. Therefore, V_1, V_2, and V_3 are used to represent the bridge arm midpoint voltage V_{ab} at mode3 and mode5 in Table I, such as

$$\begin{aligned} V_1 &= (V_{in} + V_{Q4\text{-on}} + V_{VD1})e^{-\sqrt{\frac{C_2}{(C_2+C_r)L_r}}(t-t_{V0})} \\ &= (V_{in} + V_{Q3\text{-on}} + V_{VD2})e^{-\sqrt{\frac{C_1}{(C_1+C_r)L_r}}(t-t_{III0})} \\ &= (V_{in} + V_{Q2\text{-on}} + V_{VD3})e^{-\sqrt{\frac{C_4}{(C_4+C_r)L_r}}(t-t_{III0})} \\ &= (V_{in} + V_{Q1\text{-on}} + V_{VD4})e^{-\sqrt{\frac{C_3}{(C_3+C_r)L_r}}(t-t_{V0})} \end{aligned} \tag{19}$$

$$V_2 = V_{in} - V_{Cr} \tag{20}$$

$$\begin{aligned} V_3 &= (V_{in} - V_{Cr})e^{-\sqrt{\frac{C_1}{(C_1+C_r)(L_r+L_m)}}(t-t_{V2})} \\ &= (V_{in} - V_{Cr})e^{-\sqrt{\frac{C_2}{(C_2+C_r)(L_r+L_m)}}(t-t_{III2})}. \\ &= (V_{in} - V_{Cr})e^{-\sqrt{\frac{C_3}{(C_3+C_r)(L_r+L_m)}}(t-t_{III2})} \\ &= (V_{in} - V_{Cr})e^{-\sqrt{\frac{C4}{(C_4+C_r)(L_r+L_m)}}(t-t_{V2})} \end{aligned} \tag{21}$$

IV. OPEN CIRCUIT FAULT DIAGNOSIS

A. Diagnostic Strategy of the Open Circuit Fault

Based on the aforementioned analysis, the corresponding fault diagnostic strategy is proposed by using the midpoint voltage of the primary-side semiconductor switch fault bridge arm. Traditional diagnostic methods that relay on the average value of the midpoint voltage has the problem of detection error, leading to misjudgments. Under an open circuit fault, the midpoint voltage only changes in two modes in one cycle, making average value detection methods particularly ineffective. Therefore, this article proposes a fault diagnosis strategy based on the integral value of the primary side bridge arm midpoint voltage. This method comparing the integral value of the midpoint voltage for each half-cycle with the integral value during normal operation to identify open circuit faults and locate faulty devices.

When the phase-shift control *LLC* resonant converter operates normally, the primary side bridge arm voltage V_{ab} is integrated in the positive. Assuming that V_{ab} is detected to change from 0 to V_{in} at t_1, after $T/2$-T_{ps} (T_{ps} is phase shift time), the voltage V_{ab} changes to 0 again. In this half-cycle, the bridge arm midpoint voltage integral value S_+ in the positive half-cycle can be calculated as in

$$S_+ = \int_{t_1}^{t_1+T/2-T_{ps}} V_{ab}dt = V_{in}(T/2 - T_{ps}). \tag{22}$$

Similarly, in the negative half-cycle, the bridge arm midpoint voltage V_{ab} is integrated to obtain S_-

$$S_- = \int_{t_3}^{t_3+T/2-T_{ps}} |V_{ab}|\, dt = V_{in}(T/2 - T_{ps}). \tag{23}$$

After an open-circuit fault occurs in the *LLC* resonant converter, according to the above analysis, the bridge arm midpoint voltage V_{ab} changes, which will lead to a change in its integral value. Fig. 6 shows the integrated value of the corresponding bridge arm midpoint voltage when the semiconductor switch has open-circuit faults. S_+ and S- are, respectively, integral value of primary-side bridge arms midpoint voltage in the positive and negative half-cycle when the *LLC* is working normally; S_{f+} and S_{f-} are, respectively, the integral value of the primary-side bridge arms midpoint voltage in the first positive and negative half-cycle after *LLC* open circuit fault.

When OCF occurs in Q_1 or Q_4, due to the effects of switch parasitic capacitor and body antiparallel diodes, the resonant tank current will continue to flow through them, but it will cause the bridge arm midpoint voltage V_{ab} to decrease. Therefore, the integral value of V_{ab} in the positive half-cycle is S_{f+}, which is smaller than the integral value S_+ during normal operation. Considering the sampling accuracy error and voltage fluctuation, the coefficient α is introduced. Generally, the allowable fluctuation range of the dc bus voltage is $\pm 10\%$ [31]. Meanwhile, according to the device datasheet, the sampling and integration accuracy of the designed diagnostic circuit ranges between 7.01% and 7.36%. Therefore, the value of α in this article is set to 10%, which can reduce the impact of input voltage fluctuation and sampling error

$$S_{f+} = \int_{t_5}^{t_5+T/2-T_{ps}} V_{ab}dt < (1-\alpha)S_+. \tag{24}$$

Similarly, when OCF occurs in Q_2 or Q_3, the integral value of V_{ab} in the negative half-cycle is S_{f-}, which is smaller than the

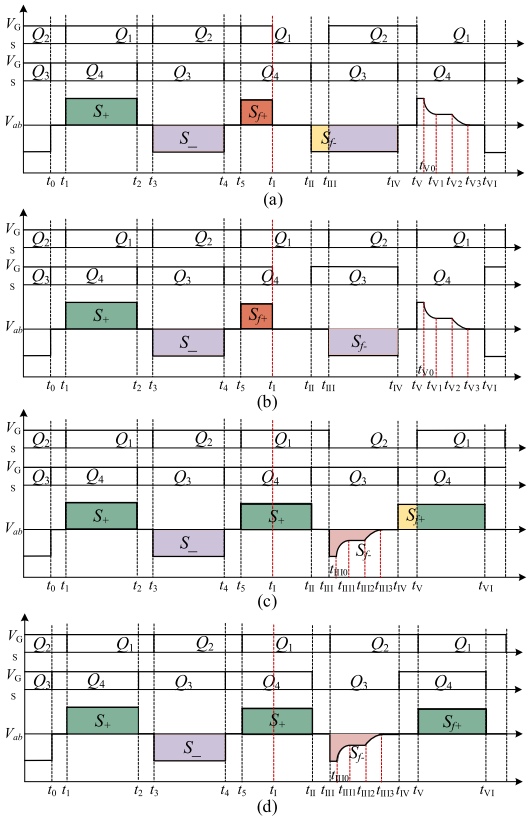

Fig. 6. Integral values of the bridge arm midpoint voltage during open circuit fault. (a) Q_1 OCF. (b) Q_4 OCF. (c) Q_2 OCF. (d) Q_3 OCF.

integral value S_- during normal operation

$$S_{f-} = \int_{t_{\rm III}}^{t_{\rm III}+T/2-T_{ps}} |V_{ab}|\, dt < (1-\alpha)S_-. \tag{25}$$

After detecting OCF fault, it is necessary to accurately locate the position of the faulty switch. When Q_1 or Q_4 fault is detected, the integrated value S_{f-} of the primary-side bridge arm midpoint voltage is calculated in the next negative half-cycle

$$\begin{aligned} &\mathrm{Q_1OCF}: S_{f-} = \int_{t_{\rm II}}^{t_{\rm IV}} |V_{ab}|\, dt > (1+\alpha)S_- \\ &\mathrm{Q_4OCF}: (1-\alpha)S_- \le S_{f-} = \int_{t_{\rm II}}^{t_{\rm IV}} |V_{ab}|\, dt \le (1+\alpha)S_-. \end{aligned} \tag{26}$$

Similarly, when the Q_2 or Q_3 open-circuit fault is detected, the integral value of the bridge arm midpoint voltage is S_{f+} in the next positive half cycle

$$\begin{aligned} &\mathrm{Q_2OCF}: S_{f+} = \int_{t_{\rm IV}}^{t_{\rm VI}} V_{ab}dt > (1+\alpha)S_+ \\ &\mathrm{Q_3OCF}: (1-\alpha)S_+ \le S_{f+} = \int_{t_{\rm IV}}^{t_{\rm VI}} V_{ab}dt \le (1+\alpha)S_+. \end{aligned} \tag{27}$$

Table II summarizes the comparison of the integrated value of the bridge arm midpoint voltage when the semiconductor switch has an open circuit fault and operates normally. Based on the above theoretical analysis, this article uses the integral value of the primary-side bridge arm midpoint voltage to identify and locate the open circuit fault.

TABLE II
PRINCIPLE OF OPEN CIRCUIT FAULT DIAGNOSIS

OCF Location	Principle of Fault Diagnosis	F_{Q1}	F_{Q2}	F_{Q3}	F_{Q4}
Q_1 OCF	$S_{f+} < 0.9S_+$ and $S_{f-} > 1.1S_-$	1	0	0	0
Q_2 OCF	$S_{f+} > 1.1S_+$ and $S_{f-} < 0.9S_-$	0	1	0	0
Q_3 OCF	$0.9S_+ \leqslant S_{f+} \leqslant 1.1S_+$ and $S_{f-} < 0.9S_-$	0	0	1	0
Q_4 OCF	$S_{f+} < 0.9S_+$ and $0.9S_- \leqslant S_{f-} \leqslant 1.1S_-$	0	0	0	1

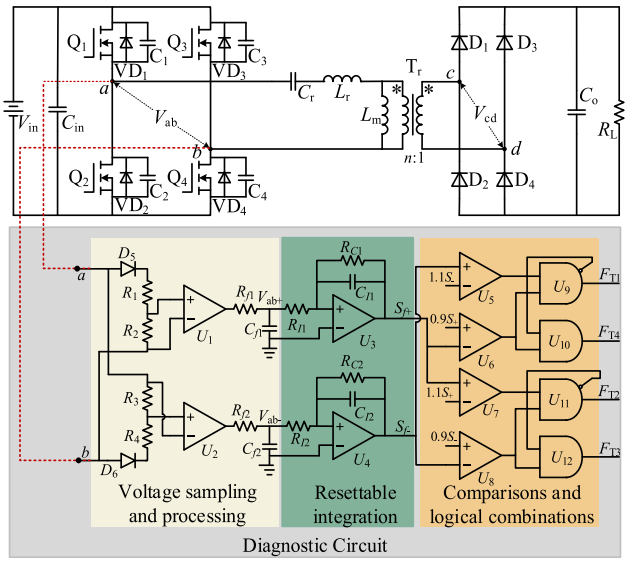

Fig. 7. OCF diagnostic circuit topology for *LLC* converter.

B. Diagnostic Circuit of the Open Circuit Fault

Analog circuits exhibit higher reliability compared to digital MCUs. The real-time processing speed of analog circuits is at the nanosecond level, whereas the processing speed of MCUs is contingent upon the complexity of the algorithm, generally exceeding the microsecond level. Furthermore, analog circuits employing straightforward fault diagnostic logic possess a volumetric advantage over MCUs [32]. Consequently, the selection of analog circuits for designing fault diagnosis circuits in the described *LLC* converters is motivated by the special operating environments, e.g., seafloor, for high reliability, real-time performance, and compactness. Based on the proposed open-circuit fault diagnosis strategy suitable for *LLC* resonant converters, a simple and effective diagnostic hardware circuit is designed. The fault diagnostic circuit discussed in this article is purely analog. The circuit modifies the voltage at the midpoints of the bridge arms to achieve real-time, online fault localization. As illustrated in Fig. 7, the topology of the diagnostic circuit

primarily consists of voltage sampling and processing, resettable integration, comparison, and logical combinations. Building upon the topology of the circuit, a diagnostic circuit board is developed, as depicted in Fig. 6.

Voltage sampling and processing is mainly used to collect the bridge arm midpoint voltage V_{ab} on the primary side of the *LLC* converter in real time. Conveniently, the input ports *a* and *b* of the diagnostic circuit are directly electrically connected to the converter bridge arm midpoint. Ultrafast recovery diodes D_5, D_6, and separate voltage sampling resistors R_1, R_2, R_3, R_4 are strategically integrated into the fault diagnosis circuit. This configuration allows for discrete sampling of the node voltage V_{ab} at the midpoint of the bridge arm during both positive and negative half-cycles, facilitating precise voltage measurement at subsequent nodes. U_1 and U_2, standard differential amplifiers, convert the differential voltage at the bridge arm nodes into a single-ended output. This conversion helps suppress common-mode noise and enhances the strength and clarity of the sampling voltage signals. The output from the differential amplifiers is filtered through a simple passive filter, consisting of R_{f} and C_{f} to enhance signal noise immunity. The outputs, positive half-cycle sampling voltage $V_{\mathrm{ab}+}$ and negative half-cycle sampling voltage $V_{\mathrm{ab}\text{-}}$, are obtained from the midpoint of the bridge arm, disregarding the diode's forward voltage drop, as detailed in (28). Additionally, a simple delay circuit synchronizes the positive and negative half-cycle sampling voltages, ensuring accurate timing for subsequent comparisons and logical operations

$$\begin{cases} V_{\mathrm{ab}+} = V_{\mathrm{ab}p} \times \frac{R_2}{R_1} \times G_{U1} \\ V_{\mathrm{ab}-} = |V_{\mathrm{ab}n}| \times \frac{R_3}{R_4} \times G_{U2} \end{cases} \tag{28}$$

where $V_{\mathrm{ab}p}$ and $V_{\mathrm{ab}n}$ represent the bridge-arm midpoint voltage of the positive half-cycle and negative half-cycle, respectively, $V_{\mathrm{ab}p} = \text{-}V_{\mathrm{ab}n} = V_{\mathrm{in}}$. G_{U1} and G_{U2} are the differential-amplifier gains, respectively.

The resettable integrator comprises operational amplifiers U_3, U_4, resistors R_{I}, R_{C}, and capacitor C_{I}, designed to integrate the midpoint voltage of the bridge arm during both positive and negative half-cycles. When the midpoint sampling voltages $V_{\mathrm{ab}+}$ and $V_{\mathrm{ab}\text{-}}$ of the bridge arm reach high levels, R_{I} and C_{I} initiate integration. This integration process calculates the integral values $S_{\mathrm{f}+}$ and $S_{\mathrm{f}\text{-}}$, for each half-cycle, as defined in (29). During low level stages, C_{I} discharges through *RC*, resetting the integrator to zero in preparation for the next high-level cycle. A high-speed peak detection circuit is integrated at the integrator's output to capture the peak values. The circuit's output voltage tracks and maintains the peak of the input signal. This enhances the precision of fault diagnosis in subsequent comparative circuit analyses

$$\begin{cases} S_{f+} = \frac{1}{R_{I1} \times C_{I1}} \int_{t_p}^{t_p+T/2} V_{ab+} d(t) \\ S_{f-} = \frac{1}{R_{I2} \times C_{I2}} \int_{t_n}^{t_n+T/2} V_{ab-} d(t) \end{cases} \tag{29}$$

where t_{p} and t_{n} represent the positive and negative half-cycle times, respectively. *T* represents the converter switching period.

The comparisons and logical combinations consist of comparators U_5, U_6, U_7, U_8, and logic chips U_9, U_{10}, U_{11}, U_{12}. The input reference voltage values $1.1S_{\text{-}}$, $0.9S_{\text{-}}$, $1.1S_{+}$, and $0.9S_{+}$ for the comparators are derived by dividing the voltage through resistors, utilizing a straightforward reference voltage source. The values and ratios of the voltage-dividing resistors are determined using (22) and (23). The output values from the resettable integrator circuit are compared against the preset reference values using comparators U_5, U_6, U_7, and U_8. Specifically, the comparator circuit compares the integrated midpoint voltages $S_{\mathrm{f}+}$ and $S_{\mathrm{f}\text{-}}$ of the bridge arm, under open-circuit conditions of the switching tube, with the reference voltages $1.1S_{\text{-}}$, $0.9S_{\text{-}}$, $1.1S_{+}$, and $0.9S_{+}$. Following the open switch tube fault diagnosis principles for the *LLC* converter module outlined in Table II, the comparator outputs are processed through a logic combination circuit, comprising AND and NAND gates, to generate the corresponding fault status signals. Ultimately, this fault status signal is relayed to the controller, which identifies the location of the faulty device and implements corrective measures.

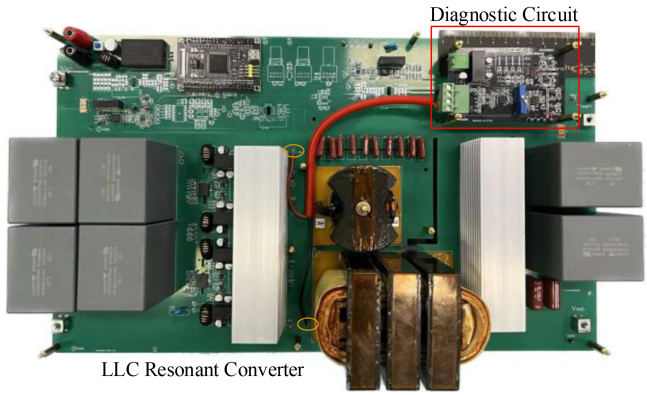

Fig. 8. Experimental prototype.

V. Experiment and Results

To validate the effectiveness of the proposed fault diagnosis strategy, an isolated *LLC* full bridge converter prototype with phase-shift control method has been implemented, as shown in Fig. 8. The diagnostic circuit board, measuring approximately 9 cm × 5.6 cm in size, is connected to the *LLC* converter bridge arm midpoint using a pair of wires. The key parameters of *LLC* full bridge converter are provided in Table III. To test the proposed method, efficient simulation of open-circuit faults is required. This experiment is conducted by programming the STM32 software to set the gate driver signal to 0, simulating the occurrence of open-circuit faults.

Fig. 9 shows the experimental results when OCF occurs in different primary-side switches of the *LLC* converter with phase-shift control. The *LLC* converter works normally until t_{OCF}, when the primary-side switch suddenly experiences an open-circuit fault (the gate drive signal S_{T} of the corresponding switch is set to zero). At t_{OCF}, the left side is the normal operating state and the right side is the open circuit fault state. Fig. 9 shows the measured output voltage V_{out}, resonant current I_{Cr}, bridge arm midpoint voltage V_{ab}, and switch drive signal S_{T} before and after the open circuit fault occurs. It can be seen from the Fig. 9

TABLE III
PARAMETERS OF *LLC* FULL BRIDGE CONVERTER

Parameters	Value
Input voltage V_{in}	90V–120 V
Output voltage V_{out}	37.5 V
Output power P_{out}	100 W
Transformer turns ratio n	100/38
Switching frequency f	100 kHz
Q_1, Q_2, Q_3, Q_4	G3R45MT17K
D_1, D_2, D_3, D_4	UJ3D06560KSD
L_r	52 μH
L_m	364 μH
C_r	43.9 nF

that in the first few cycles after the open circuit fault occurs, the output voltage $V_{\rm out}$ is almost unchanged, which means that the phase shift control angle of the *LLC* converter has not changed during this period. The resonant current $I_{\rm Cr}$ suddenly becomes smaller under different primary-side switch faults. Therefore, an open-circuit fault will not cause overcurrent impact to the equipment in a short period of time, but will cause it to work in an unhealthy state. Moreover, the variation pattern of the resonant current is not very different, making it difficult to use it as a standard for open circuit fault diagnosis.

The changing pattern of the primary-side bridge arm midpoint voltage $V_{\rm ab}$ has certain differences under different primary-side switch open-circuit faults, which can be used for fault diagnosis. It can be seen from Fig. 9(a) and (b) that under Q_1 or Q_4 open-circuit faults, the change of $V_{\rm ab}$ in the positive half-cycle is particularly large, and meanwhile, the area enclosed by the time axis is greatly reduced. Similarly, in Fig. 9(c) and (d), $V_{\rm ab}$ shows the above changing pattern in the negative half-cycle. Therefore, this can be used as a criterion to distinguish Q_1, Q_4 and Q_2, Q_3 open circuit faults, as shown in (24) and (25). Furthermore, in Fig. 9(a), the negative half-cycle time after the Q_1 open-circuit fault is about 2 μs, which is the same as the time in the normal state. However, in Fig. 9(b), this time increases to 2.8 μs after the Q_4 open-circuit fault. Thence, the area enclosed by the negative half-cycle $V_{\rm ab}$ and the time axis is used to distinguish Q_1 and Q_4 open circuit faults, as shown in (26). Likewise, in Fig. 9(c) and (d), Q_2 and Q_3 open circuit faults can also be distinguished using (27). The experimental results verify the correctness of open-circuit fault theoretical analysis and the rationality of diagnostic method.

In the fault diagnosis process, when an open-circuit fault occurs in the Q_4 tube, the output waveform shown in Fig. 10 illustrates the behavior. During this fault, the positive half-cycle voltage at the midpoint of the bridge arm decreases, while the negative half-cycle voltage remains unchanged. The voltage processing and resettable integration shown in Fig. 7 are applied to these waveforms. As a result of this processing, the integral value of the positive half-cycle voltage, denoted as S_{f+}, decreases,

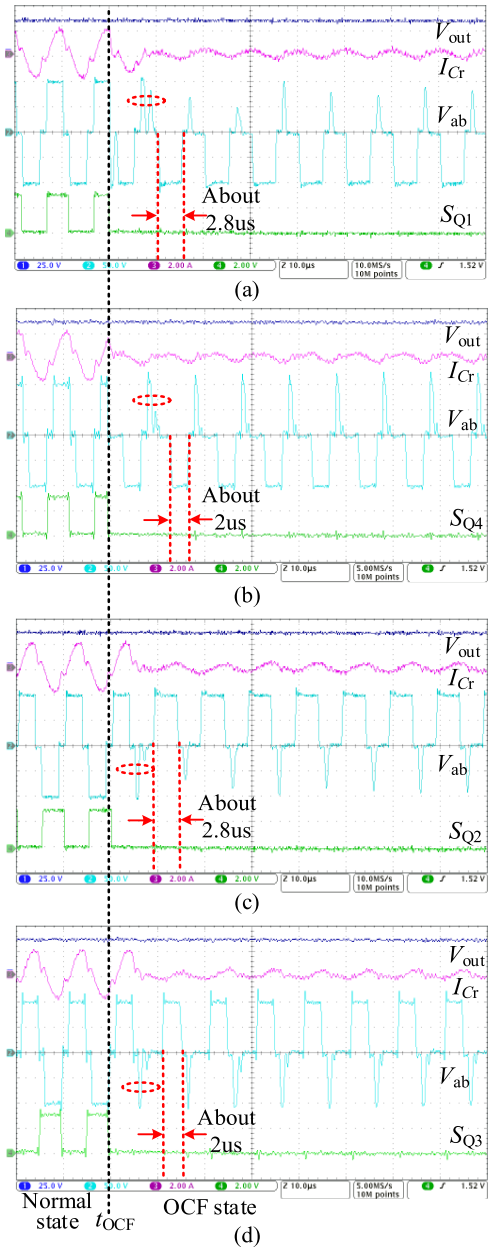

Fig. 9. Experimental waveforms when OCF happen on different primary-side switch in *LLC* converter with phase-shift control. (a) Q_1 OCF. (b) Q_4 OCF. (c) Q_2 OCF. (d) Q_3 OCF.

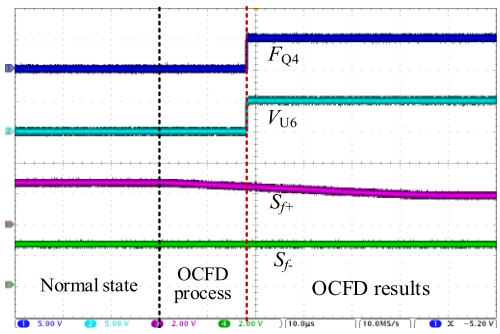

Fig. 10. Q_4 OCF diagnosis circuit waveform.

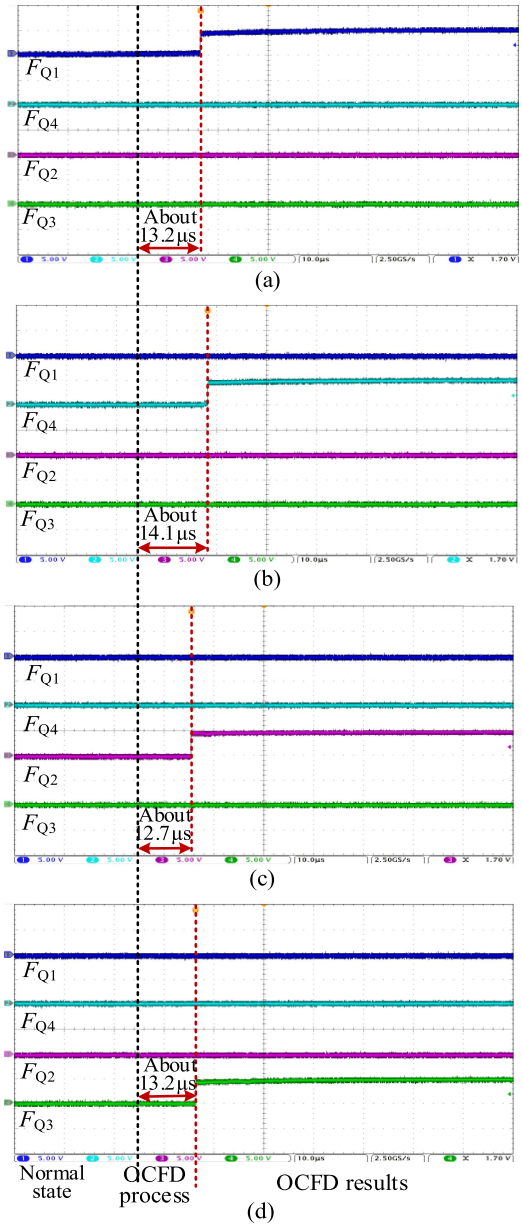

Fig. 11. OCFD by the proposed diagnostic circuit in *LLC* converter with phase-shift control. (a) Q_1 OCF. (b) Q_4 OCF. (c) Q_2 OCF. (d) Q_3 OCF.

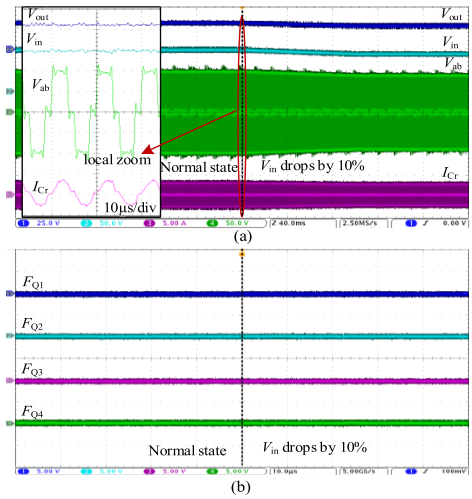

Fig. 12. Critical waveforms for a 10% drop in *LLC* input voltage. (a) *LLC* waveforms. (b) Diagnosis results.

while the integral value of the negative half-cycle voltage, denoted as S_{f-}, remains nearly unchanged. This behavior aligns with the waveform depicted in Fig. 10. When the integrated value S_{f+} drops to the reference value of $0.9S_{+}$, the output level V_{U6} of comparator U_6 in Fig. 7 transitions from low to high. Through logical combination, the fault signal F_{Q4}, corresponding to the Q_4 tube, also changes from low to high. This change in the fault signal indicates the presence of an open circuit failure in the Q4 tube.

The fault diagnosis process for other switching tubes follows a similar pattern as described above. Fig. 11 illustrates the output waveforms of the diagnostic circuit for open circuit faults in different switches. The corresponding diagnosis times for Q_1, Q_4, Q_2, and Q_3 are approximately 13.2 μs, 14.1 μs, 12.7 μs, and 13.2 μs, respectively. These results indicate that the faulty device can be accurately located within two switching cycles. This fast and precise fault diagnosis enables subsequent redundant fault-tolerant control or prompt replacement of faulty components by operators. As a result, the reliability of the *LLC* is improved to a certain extent.

The proposed circuit accomplishes accurate fault diagnosis under fixed input voltage conditions, and also adapts to input voltage dips or load jumps without misdiagnosis. In addition, accurate fault localization can be accomplished under different input voltage and load conditions. Fig. 12(a) shows that the input voltage V_{in} to the *LLC* converter drops by 10% from 100 V to 90 V. The *LLC* converter still maintains normal operation. The primary side bridge arm midpoint voltage V_{ab} amplitude will also be 90 V, but the integral values of its positive and negative half-cycles are still equal. This will not trigger the fault diagnostic circuitry, and the fault signals for all switches will remain low, as shown in Fig. 12(b). Fig. 13(a) shows that the load of the *LLC* converter is cut in half. The output voltage V_{out} fluctuates slightly at the moment of removal, but the input voltage remains nearly unchanged. Similarly, the process does not trigger the fault diagnostic circuit, and the fault signals of all switches remain low as shown in Fig. 13(b). Therefore, the proposed method in this article is still valid when subjected to input voltage steps and load jumps.

Fig. 14 shows the waveform of Q_2 undergoing an open-circuit fault when the *LLC* converter is operating at a nonrated input voltage (100 V dips to 90 V). After an open-circuit fault occurs in Q_2, the bridge-arm midpoint voltage integral value decreases in the negative half-cycle and increases in the positive half-cycle. The fault diagnostic circuit is triggered, and after about 12.1 μs, the Q_2 fault signal changes from a low level to a high level, locating open-circuit fault switch.

Fig. 15 shows the waveform of an open-circuit fault occurring in Q_2 when the *LLC* converter is operating at half-load conditions. Similarly, after an open-circuit fault occurs in Q_2,

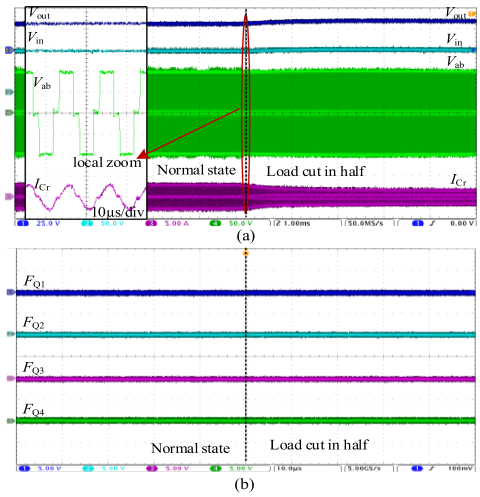

Fig. 13. Critical waveforms when the *LLC* load is cut in half. (a) *LLC* waveforms. (b) Diagnosis results.

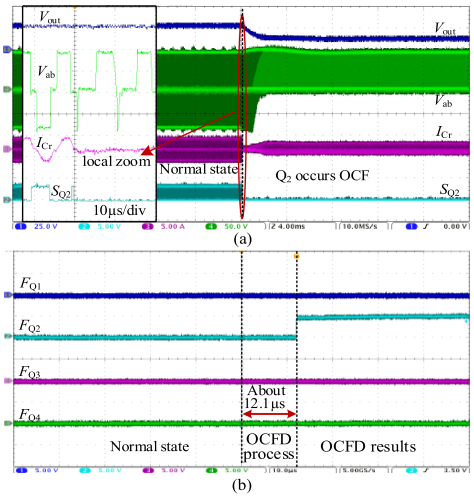

Fig. 14. Q_2 open-circuit fault waveforms during input voltage drop operation. (a) *LLC* waveforms. (b) Diagnosis results.

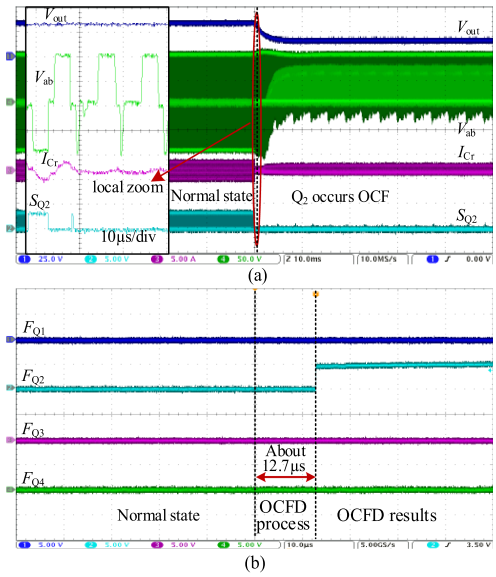

Fig. 15. Q_2 open-circuit fault waveforms during half-load operation. (a) *LLC* waveforms. (b) Diagnosis results.

TABLE IV
THE COMPREHENSIVE COMPARISON RESULTS OF THE PROPOSED METHOD WITH [17] AND [19]

	Proposed method	Ref. [17]	Ref. [19]
Control method	Phase shift	Phase shift	Extended phase shift
Fault type	Single switch OCF on primary side	Single switch OCF on primary side	Single switch OCF on primary and secondary side
Diagnostic response speed	About 14 μs	About 1 ms	More than 20 μs
Complexity	Simple	Slightly complex	Slightly complex
Additional sensors	No	Auxiliary winding	current sensor
Diagnostic circuit volume	Small	Medium	Medium

after about 12.7 μs, the Q_2 fault signal changes from low level to high level. Therefore, the fault diagnosis circuit proposed in this article can accurately complete the fault diagnosis process under the conditions of input voltage or load change, with a certain degree of adaptive.

Similar works on open circuit fault diagnosis in [17] and [19] that are mentioned in the introduction is compared with the method proposed in this article, in terms of control method, diagnostic fault type, diagnostic response speed, method complexity, additional sensors, and diagnostic circuit volume. The comprehensive comparison results are presented in Table IV. It can be seen that the fault diagnosis method proposed in this article has low complexity and fast response time compared to the same type of diagnosis methods. In addition, the method proposed in this article does not require additional sensors and the diagnostic circuit is more compact.

VI. CONCLUSION

This article proposes an accurate and fast fault diagnosis method suitable for phase-shifted *LLC* full bridge converter using the integral of the primary-side bridge arm midpoint voltage. Furthermore, based on this method, a simple and cost-effective diagnostic circuit is designed. The main conclusions are as follows.

1) The proposed method uses the integral value of the midpoint voltage as the diagnostic criterion. Compared with the instantaneous value or average value, the diagnostic results are more accurate and reliable. Moreover, this method also considers the need of rapid diagnosis, and experimental results show that the fault diagnosis can be completed in two switching cycles.
2) The designed diagnostic circuit uses relatively conventional devices in small quantities, hence keeping the cost

minimal. In addition, the circuit only needs electrical connection to the bridge arm midpoint, making it easily expandable to operational *LLC* equipment.

3) This diagnostic method is an online detection method, which can monitor the switch operating status in real time and detect the occurrence of open circuit faults in time. This can reduce maintenance costs and downtime. Combined with the proposed diagnostic method, continuous fault handling can be achieved, further improving the reliable operation capability of the converter.

The proposed method is designed to diagnose single-switch OCF of the *LLC* converter. However, in some extreme circumstances, multiple-switch faults may occur during a short time. The proposed diagnosis method has some limitations for such scenarios and needs improvement. In addition, due to the use of the bridge-arm midpoint voltage as the diagnostic basis, there could be a certain limitation under other control methods such as variable frequency or variable duty cycle. Future work will explore a more comprehensive *LLC* converter fault diagnosis method by combining variables such as resonant current or drive signal.

REFERENCES

[1] J. Zeng, G. Zhang, S. S. Yu, B. Zhang, and Y. Zhang, "LLC resonant converter topologies and industrial applications — A review," *Chin. J. Elect. Eng.*, vol. 6, no. 3, pp. 73–84, Sep. 2020.

[2] C.-E. Kim, J.-I. Baek, and J.-B. Lee, "High-efficiency single-stage LLC resonant converter for wide-input-voltage range," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7832–7840, Sep. 2018.

[3] C. Fei, F. C. Lee, and Q. Li, "High-efficiency high-power-density LLC converter with an integrated planar matrix transformer for high-output current applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9072–9082, Nov. 2017.

[4] Y. Song and B. Wang, "Survey on reliability of power electronic systems," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 591–604, Jan. 2013.

[5] S. Peyghami, F. Blaabjerg, and P. Palensky, "Incorporating power electronic converters reliability into modern power system reliability analysis," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 2, pp. 1668–1681, Apr. 2021.

[6] A. Khosroshahi, M. Abapour, and M. Sabahi, "Reliability evaluation of conventional and interleaved DC–DC boost converters," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5821–5828, Oct. 2015.

[7] L. F. Costa and M. Liserre, "Failure analysis of the DC-DC converter: A comprehensive survey of faults and solutions for improving reliability," *IEEE Power Electron. Mag.*, vol. 5, no. 4, pp. 42–51, Dec. 2018.

[8] W. Zhang, D. Xu, P. N. Enjeti, H. Li, J. T. Hawke, and H. S. Krishnamoorthy, "Survey on fault-tolerant techniques for power electronic converters," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6319–6331, Dec. 2014.

[9] F. Bento and A. J. M. Cardoso, "A comprehensive survey on fault diagnosis and fault tolerance of DC-DC converters," *Chin. J. Elect. Eng.*, vol. 4, no. 3, pp. 1–12, Sep. 2018.

[10] V. Mulpuri, "Failure signature of electrical overstress on power MOSFETs," M.S. thesis, Univ. of Akron, Akron, OH, USA, 2017.

[11] K. Sun, J. Wang, R. Burgos, and D. Boroyevich, "Design, analysis, and discussion of short circuit and overload gate-driver dual-protection scheme for 1.2-kV, 400-A SiC MOSFET modules," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 3054–3068, Mar. 2020.

[12] T. Li and L. Parsa, "Design, control, and analysis of a fault-tolerant soft-switching DC–DC converter for high-power high-voltage applications," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1094–1104, Feb. 2018, doi: 10.1109/TPEL.2017.2684832.

[13] H. Wang, X. Pei, Y. Wu, Y. Xiang, and Y. Kang, "Switch fault diagnosis method for series–parallel forward DC–DC converter system," *IEEE Trans. Ind. Electron.*, vol. 66, no. 6, pp. 4684–4695, Jun. 2019.

[14] E. Pazouki, Y. Sozer, and J. A. De Abreu-Garcia, "Fault diagnosis and fault-tolerant control operation of nonisolated DC–DC converters," *IEEE Trans. Ind. Appl.*, vol. 54, no. 1, pp. 310–320, Jan./Feb. 2018.

[15] E. Farjah, H. Givi, and T. Ghanbari, "Application of an efficient rogowski coil sensor for switch fault diagnosis and capacitor ESR monitoring in non-isolated single-switch DC–DC converters," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1442–1456, Feb. 2017.

[16] P. Hofer-Noser and N. Karrer, "Monitoring of paralleled IGBT/diode modules," *IEEE Trans. Power Electron.*, vol. 14, no. 3, pp. 438–444, May 1999.

[17] X. Pei, S. Nie, Y. Chen, and Y. Kang, "Open-circuit fault diagnosis and fault-tolerant strategies for full-bridge DC–DC converters," *IEEE Trans. Power Electron.*, vol. 27, no. 5, pp. 2550–2565, May 2012.

[18] M. Shahbazi, E. Jamshidpour, P. Poure, S. Saadate, and M. R. Zolghadri, "Open- and short-circuit switch fault diagnosis for nonisolated DC–DC converters using field programmable gate array," *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 4136–4146, Sep. 2013.

[19] M. Zheng, H. Wen, H. Shi, Y. Hu, Y. Yang, and Y. Wang, "Open-circuit fault diagnosis of dual active bridge DC-DC converter with extended-phase-shift control," *IEEE Access*, vol. 7, pp. 23752–23765, 2019.

[20] Y. Chen, X. Pei, S. Nie, and Y. Kang, "Monitoring and diagnosis for the DC–DC converter using the magnetic near field waveform," *IEEE Trans. Ind. Electron.*, vol. 58, no. 5, pp. 1634–1647, May 2011.

[21] S. Nie, X. Pei, Y. Chen, and Y. Kang, "Fault diagnosis of PWM DC–DC converters based on magnetic component voltages equation," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4978–4988, Sep. 2014.

[22] X. Pei, S. Nie, Y. Chen, and Y. Kang, "Open-circuit fault diagnosis and fault-tolerant strategies for full-bridge DC–DC converters," *IEEE Trans. Power Electron.*, vol. 27, no. 5, pp. 2550–2565, May 2012.

[23] S. Zhuo, A. Gaillard, L. Xu, C. Liu, D. Paire, and F. Gao, "An observer-based switch open-circuit fault diagnosis of DC–DC converter for fuel cell application," *IEEE Trans. Ind. Appl.*, vol. 56, no. 3, pp. 3159–3167, May/Jun. 2020.

[24] Q. Sun, Y. Wang, and Y. Jiang, "A novel fault diagnostic approach for DC-DC converters based on CSA-DBN," *IEEE Access*, vol. 6, pp. 6273–6285, 2018.

[25] R. B. Dhumale and S. D. Lokhande, "Neural network fault diagnosis of voltage source inverter under variable load conditions at different frequencies," *Measurement*, vol. 91, pp. 565–575, Sep. 2016.

[26] W. Han et al., "Incipient fault diagnosis for DC–DC converter based on multi-dimensional feature fusion," *IEEE Access*, vol. 11, pp. 58822–58834, 2023.

[27] C. Fan, K. Xiahou, L. Wang, and Q. H. Wu, "Hybrid fault diagnosis of multiple open-circuit faults for cascaded H-bridge multilevel converter based on perturbation estimation convolution network," *IEEE Trans. Instrum. Meas.*, vol. 73, 2024, Art. no. 3508812, doi: 10.1109/TIM.2024.3351234.

[28] M. Chai, N. B. Y. Gorla, and S. K. Panda, "Fault detection and localization for cascaded H-bridge multilevel converter with model predictive control," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10109–10120, Oct. 2020.

[29] D. Xie, H. Wang, X. Ge, Q. Deng, B. Gou, and L. Ma, "A voltage-based multiple fault diagnosis approach for cascaded H-bridge multilevel converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 5, pp. 5092–5106, Oct. 2022.

[30] Y. Chen, L. Du, and J. He, "Online diagnosis and ride-through operation for cascaded h-bridge converter based STATCOM with a single open-circuit IGBT," *IEEE Trans. Ind. Electron.*, vol. 69, no. 8, pp. 7549–7559, Aug. 2022.

[31] *IEEE Standard for Interconnection and Interoperability of Distributed Energy Resources with Associated Electric Power Systems Interfaces*, Standard IEEE Std 1547-2018 (Revision of IEEE Std 1547-2003), Apr. 2018.

[32] B. J. LaMeres, "Introduction: Analog vs. digital," in *Introduction to Logic Circuits & Logic Design With VHDL*. Berlin, Germany: Springer, 2017.

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