Phase-Shift and Duty-Ratio Control Optimization of a 6 kW Three-Port Resonant DC–DC Converter for Dual Auxiliary Voltage EV Applications

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***Abstract*—Isolated three-port dc–dc converters (TPCs) facilitate integration of three voltage sources/loads in electric vehicle applications. Three-port resonant converter (TPRC) is an attractive TPC topology as it inherits the advantages of resonant converters. Phase-shift (PS) control applied to TPRCs enables independent power flow control among all ports. Phase-shift and duty-ratio (PSDR) control introduces three additional degrees of freedom providing the potential for improving the converter efficiency compared to PS control. This article presents a generalized harmonic approximation-based steady-state mathematical model for a TPRC with five-variable PSDR control. Mathematical solutions to the steady-state converter bridge voltages and the ac currents under PSDR control are provided. The proposed mathematical model is integrated with a TPRC power loss model and together are used to formulate a control optimization problem for evaluating the optimal control variables at maximum converter efficiency. The optimized five-variable PSDR control is compared against PS control using a 6 kW/100 kHz rated hardware demonstrator, with efficiency improvements as high as 12.4%.**

***Index Terms*—Control variable optimization, electric vehicle (EV), generalized harmonic approximation (GHA), phase-shift and duty-ratio (PSDR) control, three-port resonant converter (TPRC), triple active bridge.**

NOMENCLATURE

C_1, C_2	Resonant capacitors of ports 1 and 2.
$C_{\text{DS},j}$	Drain-source capacitance across a MOSFET of port j.
d_j	Duty-ratio of port j.
$\mathbf{d}$	Vector of duty-ratio $[d_1\ d_2\ d_3]$.
$E_{\text{available}}$	Circulating energy available during the dead time for port j.
$E_{\text{off},j}$	Turn-OFF switching energy map of MOSFETs in port j.
$E_{\text{on},j}$	Turn-ON switching energy map of MOSFETs in port j.
E_{sink}	Energy required to fully discharge the total C_{DS} in port j.
e_{ss}	Steady-state error.
f_s	Switching frequency.
f_r	Resonant frequency.
I_j	DC current of port j.
$I_{Si,\text{off}}$	Turn-OFF current of MOSFET S_i.
$I_{Si,\text{on}}$	Turn-ON current of MOSFET S_i.
$i_{D,i}(t)$	Drain current through MOSFET i.
$i_j(t)$	Instantaneous ac currents of port j.
i'_j	AC currents of port j referred to port 1.
$i_{j(\text{RMS})}$	AC rms current of port j.
$i_{M,i(\text{RMS})}$	Rms current through MOSFET i.
$i_m(t)$	Magnetizing current referred to port 1.
k	Harmonic number.
k_{fe}, α, β	Steinmetz coefficients of the transformer core.
L_1, L_2	Resonant inductance + leakage inductance of ports 1 and 2.
L_3	Leakage inductance of port 3.
L_m	Transformer magnetizing inductance referred to port 1.
$L_{\text{loop},j}$	Averaged commutation loop inductance of port j.
N_2	Transformer turns ratio between ports 1 and 2 (n_1/n_2).
N_3	Transformer turns ratio between ports 1 and 3 (n_1/n_3).
n	Total number of harmonics.
$n_1 : n_2 : n_3$	Transformer turns among ports 1, 2, and 3.
$p_j(t)$	Instantaneous ac power transfer in port j.
$P_{\text{cond}(M),i}$	Conduction loss of MOSFET i.
$P_{\text{cond}(D),i}$	Body diode conduction loss of MOSFET i.
P_{core}	Transformer core loss.
P_{Cu}	Transformer copper (ohmic) loss.
$P_{\text{ESR},j}$	Power loss due to the equivalent series resistance in resonant tank elements of port j.
P_{loss}	Total power loss in the TPRC.

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$P_{\text{loss}(M),i}$	Power loss per MOSFET.
$P_{\text{off},i}$	Turn-OFF switching loss of MOSFET i.
$P_{\text{on},i}$	Turn-ON switching loss of MOSFET i.
P_j	Desired power flow in port j for a given control point.
$P_{j(\text{model})}$	Modeled power flow in port j for a given control point.
$R_{\text{ac},j}$	AC resistance of the transformer winding + busbar of port j.
$R_{\text{DS(on)},i}$	On-state resistance of MOSFET i at $T_{j,i} = 125$ °C.
R_j	Total parasitic resistance of port j.
$R_{\text{th,HS},i}$	Heat sink thermal resistance of MOSFET i.
$R_{\text{th},i}$	Total thermal resistance of MOSFET i.
$R_{\text{th,JC},i}$	Junction to case thermal resistance of MOSFET i.
$R_{\text{th,TIM},i}$	Thermal resistance of the thermal interface material of MOSFET i.
$R_{\text{res},j}$	Total equivalent series resistance in resonant tank elements of port j.
T_{HS}	Heat sink temperature.
$T_{j,i}$	Junction temperature of MOSFET i.
$T_{j,\text{max}}$	Maximum MOSFET junction temperature.
T_s	Switching period.
$t_{d,j}$	Dead time of port j.
V_e	Transformer core volume.
V_j	DC bus voltage of port j.
$V_{\text{on},i}$	Drain to source voltage of MOSFET S_i at turn-ON.
$V_{\text{off},i}$	Drain to source voltage of MOSFET S_i under partial ZVS.
$V_{SD,i}$	Datasheet specified source to drain forward voltage of the body diode of MOSFET i.
$v_j(t)$	Bridge voltage of port j.
$v_{\text{eq},j}(t)$	Thevenin's equivalent voltage referred to port j.
$v_{\text{DS},i}(t)$	Drain to source voltage across MOSFET S_i during switching.
$\mathbf{x}$	Control variable vector $[\varphi_{12}\ \varphi_{13}\ d_1\ d_2\ d_3]$.
$Z_{\text{eq},j}$	Thevenin's equivalent impedance referred to port j.
Z_{ij}	Impedance between ports i and j of the equivalent delta network.
Z_j	Total impedance of port j including parasitic resistance, resonant inductor and capacitor, and leakage inductance.
Z_m	Impedance of magnetizing inductance (L_m).
ΔB	Flux density swing in the transformer core.
η	TPRC efficiency.
φ_{12}	Phase-shift between ports 1 and 2.
φ_{13}	Phase-shift between ports 1 and 3.
ω	Angular switching frequency.

I. Introduction

WITH the global net zero emissions to be reached by 2050, automakers have increased their electrification targets [1], [2]. Power electronics systems play a crucial role in EVs managing the power transfer among high-voltage (HV) and low-voltage (LV) batteries, electric motors, and other medium to LV loads. The demand for efficient and reliable power electronics is increasing as the governments and consumers shift toward electrified transportation to reduce the emissions and fight the climate change [3].

TABLE I
Comparison Among the Fully Isolated TPCs for EV Applications

Ref.	Topology	Control technique	Voltage range/ max current	Peak efficiency
[12] [14]	TPRC + buck converter	FM + PSDR	400 V/ 17.5 A, 250 – 450 V/ 28 A, 10.5 – 15.5 V/ 150 A	93.3% [a] 98.6% [b] 96.1% [c]
[15]	TPRC + current doubler	FM + PS	380 – 700 V/ 10 A, 240 – 420 V/ 10 A, 11 – 14 V/ 30 A	97.61%
[11]	TPRC	FM + PS	400 V/ 16.5 A, 270 – 450 V/ 24 A, 9 – 15 V/ 111 A	97.7%
[16]	TPRC	FM + PS	250 – 500 V/ 12 A 250 – 500 V/ 12 A 10.5 – 15 V/ 200 A	96.5%
[10]	TAB	Optimized PSDR	300 V/ 5 A 42 V/ 24 A 14 V/ 36 A	91.5%
This work	**TPRC**	**Optimized PSDR**	**400 – 800 V/ 15 A 46 – 50 V/ 70 A 10 – 14 V/ 280 A**	**96.34%**

[a] port 2 to 3
[b] port 1 to 2
[c] buck converter operation only

The HV bus in an EV connects the HV energy storage systems (ESSs) (typically 400 or 800 V battery) and the HV loads such as the electric motor. Apart from the LV bus (typically 12 V nominal voltage) connecting the LV battery and the auxiliary power module, the addition of ESSs and loads of medium to HV levels (i.e., 48 to 400 V) to meet the increasing power requirements of EVs is also being discussed [4], [5], [6]. While the general two-port dc–dc converters can interface two sources/loads of different voltage levels, integration of multiple voltage levels requires either multiple two-port converters or multiport converters. However, multiport converters can improve the system efficiency and power density compared to multiple two-port converters.

Three-port dc–dc converters (TPCs) allow power transfer among three voltage levels : either to interface charging/discharging of multiple ESSs or to interface an HV battery with MV and LV buses [7], [8], [9]. A comparison among fully isolated TPC topologies proposed for EVs is given in Table I. Majority of the existing contributions focus on integrating two HV ports with a single LV port and there are limited sources on TPC solutions for dual auxiliary voltage EV applications [10]. Triple active bridge (TAB) converters and three-port resonant converters (TPRCs) are the most common fully isolated TPC topologies and are used as a basis to derive new TPC topologies [9], [10], [11], [12]. The TPRC inherits the advantages of resonant converters, such as reduced peak currents due to sinusoidal nature, reduced filter requirements, and a wide range of zero voltage switching (ZVS) compared to a TAB [13].

The TPC control should be able to facilitate independent power flow among the three ports. Multivariable control in TPCs

use additional degrees of freedom for optimal control. Phase-shift (PS) control, phase-shift and duty-ratio (PSDR) control, and frequency modulation (FM) have been studied for TPRCs. PS control is the simplest control technique to implement, however, PS control alone may lead to increased losses from high switching currents [17]. FM can facilitate zero current switching and improve efficiency, but the implementation is challenging when it comes to independent power flow control among the three ports. In the case of two output ports and one input port of the TPRC, FM would require operation at two different switching frequencies to achieve the respective voltage gains. Hence, researchers have investigated FM in hybrid with PS control in [16], [18], and [19]. The FM-PS hybrid control proposed in Dao et al.'s [18] work for a TPRC has FM to regulate one output port and PS control to regulate the other, however, the decoupled power flow control during the operation of both output ports is unclear. Also, in wide voltage range applications this may widen the range of switching frequencies, making the design of magnetics and closed loop control difficult. A comparison among the control techniques implemented in fully isolated TPCs proposed for EV applications is also included in Table I.

PSDR control is easier to implement than FM and can aid in achieving higher efficiency than PS control due to increased degrees of freedom. The decoupled control for both PS and PSDR control has been discussed in literature based on the first harmonic approximation (FHA) [10]. PSDR control will introduce five control variables: two PS angles for two ports with respect to the third port and duty-ratios for each port. The TPRC can operate at multiple combinations of the five control variables for a single operating point [9]. Hence, the control needs to be optimized to achieve a desired goal.

A sufficiently accurate converter model is required for use in control optimization. Several techniques are used to model and optimize multivariable control in fully isolated TPCs to achieve different objectives. Use of steady-state mathematical models is a popular method of control optimization as discussed in [20] and [21] for TABs and in Mungekar and Mallik's [22] work for a TPRC. Data driven modeling approaches, such as artificial neural networks (ANNs) are also proposed to avoid heavy computational analysis in mathematical models and memory usage for lookup tables (LUTs) as proposed in [23] and [24]. The optimization objective discussed in the aforementioned sources also vary as rms current minimization, semiconductor loss minimization, and reactive power minimization.

The modeling approach should be decided based on the objective of the control optimization. For loss minimization objectives, the control optimization solely based on rms/dc current minimization would not be effective depending on the converter parameters. Setting the objective as efficiency maximization can ensure loss minimization, even though a comprehensive loss model of the system is required. Hence, the control optimization objective for the TPRC discussed in this work is set as efficiency maximization. Derivation of a steady-state mathematical model is selected over data driven modeling approaches to model the TPRC, because, an analytical loss model can be more effective in terms of accuracy and computational burden and a data driven model would require a validated thermal simulation model to train the model.

The mathematical modeling technique depends on the converter control technique. For phase-shifted TPCs, FHA is used to approximate the quasisquare bridge voltages to a sinusoidal waveform [10], [25]. Steady-state model of a TPRC derived by applying the generalized averaged model to FHA-based state–space model is provided in Krishnaswami and Mohan's [25] work. But, FHA-based model is insufficiently accurate to estimate the switching currents of the converter. Time domain analysis is a popular and sufficiently accurate modeling technique for optimizing resonant converters [26]. Discrete time domain analysis is applied to known voltage and current waveforms of the converter by linearizing the time intervals. However, it is challenging to apply time domain analysis to a TPRC due to the numerous combinations of time intervals that can exist with respect to the bridge voltage and ac current waveforms of the three ports, that end up resulting in multiple modes of operations and boundary conditions to the steady-state solutions. A mathematical model based on generalized harmonic analysis (GHA) was presented in Dey et al.'s [27] work for a TAB. In GHA, bridge voltages are modeled as a sum of harmonics, instead of limiting to FHA, which improves the model accuracy. However, a sufficiently accurate steady-state model of the TPRC for utilization in converter design or control optimization has not been proposed in the literature.

This article presents the steady-state mathematical model for a PSDR controlled TPRC. GHA of the equivalent circuit is used to derive the bridge voltages and ac currents. The steady-state model is expanded to evaluate the converter losses and optimize the PSDR control for maximizing efficiency. The optimized PSDR control is compared against PS control for a 6 kW TPRC with three ports rated at 400–800, 46–50, and 10–14 V. The contributions from this article are listed as follows.

1) Derivation of the steady-state mathematical model of the TPRC, which includes the functions of the bridge voltages and the ac currents.
2) Derivation of the ZVS criteria for full, partial, and no ZVS based on the steady-state model. The derivation of the voltage across the switching devices in the case of partial ZVS is provided.
3) Formulation of the converter efficiency as the objective function of the control optimization problem, through loss evaluation of the derived steady-state model.
4) Methodology for PSDR control optimization along with the identification of the constraints to meet the electrical and thermal limits.
5) Validation of the proposed TPRC model and the optimized PSDR control through simulations and experiments.

The rest of this article is organized as follows. Section II presents an overview of the TPRC topology and the PSDR control. The steady-state mathematical model of the TPRC is derived and validated against simulation results in Section III. The methodology of PSDR control optimization along with the development of a loss model as the objective function is provided in Section IV. Section V presents the experimental results to

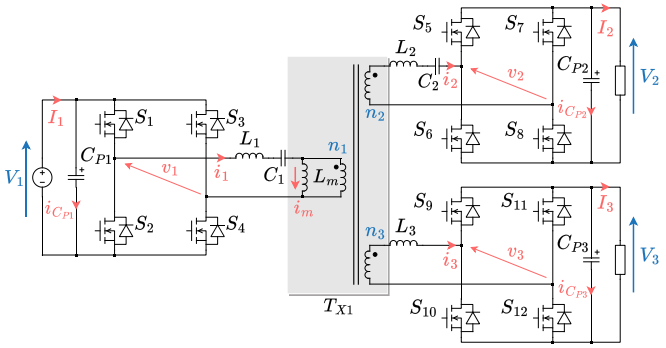


Fig. 1. TPRC topology.

validate the efficiency improvement from the optimized control. Finally, Section VI concludes this article.

II. Three-Port Resonant Converter

The TPRC topology can have resonant tanks in one or more ports, and the configuration of the resonant tank can be either series, parallel, or series–parallel based on the application [17], [28]. This work is based on the fully isolated TPRC seen in Fig. 1 for an application to interface the HV battery (port 1) with two auxiliary load buses in an EV (ports 2 and 3) [9]. The power flow among the three ports is independently controlled through PSDR control.

A. TPRC Overview

The TPRC topology in Fig. 1 has two series resonant tanks in ports 1 and 2, while utilizing the leakage inductance of port 3. The converter operates at a fixed switching frequency under PSDR control. The resonant frequency of both series resonant tanks are chosen to be the same as given in the following [9]:

$$f_r = \frac{1}{2\pi\sqrt{L_1C_1}} = \frac{1}{2\pi\sqrt{L_2C_2}}. \tag{1}$$

The three winding transformer has turns n_1, n_2, and n_3 on ports 1–3. The resonant tank elements and the magnetizing inductance should be selected based on the control technique and the range of operation. The process of determining the resonant tank parameters for the topology in Fig. 1 with PSDR control is explained in Keshmiri et al.'s [9] work. To ensure ZVS and continuous conduction in the output ports while minimizing circulating currents, f_s should be selected such that $f_s > f_r$.

The TPRC topology can allow bidirectional power flow among three ports. The derivations provided in this work are based on the power transfer from port 1 to ports 2 and 3 and are still applicable to bidirectional power flow among the three ports, however, have been omitted for brevity. Port 1 provides power from the HV battery, supporting a wide voltage range of 400–800 V, to supply an auxiliary load bus (port 2) and LV bus/battery (port 3).

Since port 3 is a LV high current port, having a series resonant tank will require high current ratings in its resonant tank components. Hence, a series resonant tank in port 3 is avoided, and the transformer leakage inductance on port 3 (L_3) is considered for circuit analysis due to its effects on power transfer and soft switching.

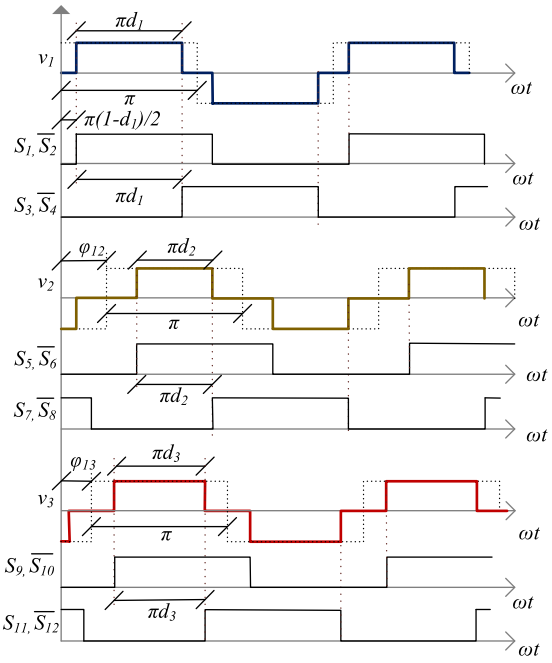


Fig. 2. Bridge voltages and gate signals during port 1 feeding ports 2 and 3.

B. PSDR Control

PS control with two ports phase-shifted with respect to the third port can control the power transfer among the three ports [17]. Under PS control, there exists a single pair of PSs the TPRC can operate with to reach a desired output power level.

With PSDR control, the duty-ratio of the bridge voltage in each port can be controlled to have three additional degrees of freedom for optimizing the TPRC operation [9]. The five control variables in PSDR with respect to bridge voltages are illustrated in Fig. 2. The gate signals for all three ports are also defined in Fig. 2 with respect to the control variables. The dead time (t_{d1}, t_{d2}, and t_{d3}) between the complementary switches is not illustrated in Fig. 2 for clarity. The PS angles are defined for ports 2 and 3 with respect to port 1 such that $-\pi/2 < \varphi_{12}, \varphi_{13} < \pi/2$. In the case of port 1 powering ports 2 and 3, both PSs will be positive, i.e., v_2 and v_3 will be leading v_1. The duty-ratios of each port are defined such that $0 < d_1, d_2, d_3 < 1$. In the case of PSDR, the TPRC can operate at multiple control points $[\varphi_{12}, \varphi_{13}, d_1, d_2, d_3]$ for a singular operating point. Hence, the optimal control point needs to be identified to maximize the converter efficiency.

As seen in Fig. 2, the duty-ratio control is introduced by applying a PS between the gate signals of two legs in each port. Hence, the switching currents in the two legs of each full bridge are different. The top and bottom MOSFETs of each leg switch in a complementary fashion with a dead time. Since each MOSFET switches with approximately 50% duty-ratio (dead time results duty-ratio slightly less than 50%), the switching

currents of the complementary MOSFETs are similar. Hence, the additional degrees of freedom provide the control over switching times, hence managing the converter losses. Even though the optimization of PSDR control can reduce switching and conduction losses, it is important to analyze the effects of unequal temperature distribution in each port and ensure the MOSFET junction temperature (T_j) does not exceed the design limits.

The power transfer among the three ports through PS and PSDR controls is coupled [10]. Hence, during power transfer from port 1 to ports 2 and 3, power transfer between ports 2 and 3 is inevitable. The power transfer can be independently controlled either through hardware or control decoupling [10], [28]. In hardware decoupling control, the impedance in each port is designed such that the power transfer between the two coupled ports (ports 2 and 3 in this work) is limited by increasing the impedance between those two ports (Z_{23}). However, hardware decoupling has limited feasibility in bidirectional wide voltage range applications. Control decoupling through a decoupling network will not affect the range of converter operation and can be implemented as a part of closed loop control. The decoupling network for a TAB is derived based on FHA in Zhao et al.'s [10] work, and the derivation was expanded based on GHA in Dey and Mallik's [29] work. Derivation of the decoupling network based on FHA for a TPRC is given in Keshmiri et al.'s [9] work and is used in this work.

III. Steady-State Converter Model

In order to optimize the PSDR control, an accurate model of the TPRC is necessary. The analytical model should accurately compute the converter ac root-mean-square (rms) currents, MOSFET rms currents, switching currents, soft switching status, and blocking voltage of the MOSFETs to estimate the converter efficiency for a given operating point. The loss parameters of the components can be inputs to the mathematical model based on their respective datasheets. This section provides the converter steady-state model derivations with bridge voltage functions and ac current functions. These functions are used to estimate the TPRC losses and compute overall efficiency. An evaluation of ZVS availability is necessary to accurately predict the converter losses. Hence, the criteria to assess ZVS and the derivations for the voltage across the MOSFET in the case of partial ZVS are also discussed in this section. The model is validated via simulation results.

A. Mathematical Model Development

The quasisquare voltage waveforms of the three bridges are synthesized based on GHA by applying the Fourier transform for n number of harmonics, as given in (2)–(4) [27], [30]. These are functions of the dc voltages observed at each port and the control variables. Due to the half-wave symmetry, only odd harmonics are considered [31].

$$v_1(t) = \sum_{k=1,\text{odd}}^{n} \frac{4V_1}{k\pi} \sin\left(\frac{k\pi d_1}{2}\right) \sin\left(\frac{k\pi}{2}\right) \sin(k\omega t) \tag{2}$$

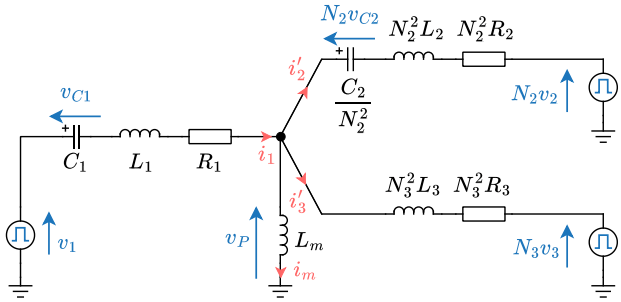


Fig. 3. Equivalent radial circuit of the TPRC referred to port 1.

$$v_2(t) = \sum_{k=1,\text{odd}}^{n} \frac{4V_2}{k\pi} \sin\left(\frac{k\pi d_2}{2}\right) \sin\left(\frac{k\pi}{2}\right) \sin[k(\omega t - \varphi_{12})] \tag{3}$$

$$v_3(t) = \sum_{k=1,\text{odd}}^{n} \frac{4V_3}{k\pi} \sin\left(\frac{k\pi d_3}{2}\right) \sin\left(\frac{k\pi}{2}\right) \sin[k(\omega t - \varphi_{13})]. \tag{4}$$

The equivalent circuit of the TPRC as a radial circuit is given in Fig. 3. All the voltages, currents, and passive elements are referred to port 1. The turns ratio between ports 1 and 2 is defined as $N_2 = \frac{n_1}{n_2}$ and between ports 1 and 3 as $N_3 = \frac{n_1}{n_3}$. Also, $R_j = R_{\text{ac},j} + R_{\text{res},j}$. The state–space equations obtained by applying Kirchhoff's voltage and current laws for the equivalent radial circuit considering kth harmonic are given in the following:

$$v_{1,k}(t) = R_1 i_{1,k}(t) + L_1 \frac{\mathrm{d}i_{1,k}(t)}{\mathrm{d}t} + v_{C_1,k}(t) + v_{P,k}(t) \tag{5}$$

$$N_2 v_{2,k}(t) = -N_2^2 R_2 i'_{2,k}(t) - N_2^2 L_2 \frac{\mathrm{d}i'_{2,k}(t)}{\mathrm{d}t} - N_2 v_{C_2,k}(t) + v_{P,k}(t) \tag{6}$$

$$N_3 v_{3,k}(t) = -N_3^2 R_3 i'_{3,k}(t) - N_3^2 L_3 \frac{\mathrm{d}i'_{3,k}(t)}{\mathrm{d}t} + v_{P,k}(t) \tag{7}$$

$$v_{P,k}(t) = L_m \frac{\mathrm{d}i_{m,k}(t)}{\mathrm{d}t} \tag{8}$$

$$i_{1,k}(t) = i'_{2,k}(t) + i'_{3,k}(t) + i_{m,k}(t) \tag{9}$$

$$i_{1,k}(t) = C_1 \frac{\mathrm{d}v_{C_1,k}(t)}{\mathrm{d}t} \tag{10}$$

$$i'_{2,k}(t) = \frac{C_2}{N_2} \frac{\mathrm{d}v'_{C_2,k}(t)}{\mathrm{d}t}. \tag{11}$$

The above-mentioned state–space equations are simplified to formulate (12)–(14)

$$\frac{\mathrm{d}v_{1,k}}{\mathrm{d}t} = (L_1 + L_m)\frac{\mathrm{d}^2 i_{1,k}}{\mathrm{d}t^2} + R_1 \frac{\mathrm{d}i_{1,k}}{\mathrm{d}t} + \frac{i_{1,k}}{C_1} - L_m \frac{\mathrm{d}^2(i'_{2,k} + i'_{3,k})}{\mathrm{d}t^2} \tag{12}$$

$$N_2\frac{\mathrm{d}v_{2,k}}{\mathrm{d}t} = -(N_2^2L_2+L_m)\frac{\mathrm{d}^2i'_{2,k}}{\mathrm{d}t^2} - N_2^2R_2\frac{\mathrm{d}i'_{2,k}}{\mathrm{d}t} - \frac{N_2^2i_{2,k}}{C_2} + L_m\frac{\mathrm{d}^2(i_{1,k}-i'_{3,k})}{\mathrm{d}t^2} \tag{13}$$

$$N_3\frac{\mathrm{d}v_{3,k}}{dt} = -(N_3^2L_3+L_m)\frac{\mathrm{d}^2i'_{3,k}}{\mathrm{d}t^2} - N_3^2R'_3\frac{\mathrm{d}i'_{3,k}}{\mathrm{d}t} + L_m\frac{\mathrm{d}^2(i_{1,k}-i'_{2,k})}{\mathrm{d}t^2}. \tag{14}$$

Finally, the state–space equations are represented in matrix form, as given in (15)–(20). $\underline{v_k}$ is the vector of quasisquare voltage functions of the kth harmonic derived from (2)–(4)

$$\frac{\mathrm{d}\underline{v_k}(t)}{\mathrm{d}t} = [A]\frac{\mathrm{d}^2\underline{i_k}(t)}{\mathrm{d}t^2} + [B]\frac{\mathrm{d}\underline{i_k}(t)}{\mathrm{d}t} + [C]\underline{i_k}(t) \tag{15}$$

$$\underline{v_k} = [v_{1,k};\, N_2v_{2,k};\, N_3v_{3,k}] \tag{16}$$

$$\underline{i_k} = [i_{1,k};\, i'_{2,k};\, i'_{3,k}] \tag{17}$$

$$[A] = \begin{pmatrix} (L_1+L_m) & -L_m & -L_m \\ L_m & -(N_2^2L_2+L_m) & -Lm \\ L_m & -L_m & -(N_3^2L_3+L_m) \end{pmatrix} \tag{18}$$

$$[B] = \begin{pmatrix} R_1 & 0 & 0 \\ 0 & -N_2^2R_2 & 0 \\ 0 & 0 & -N_3^2R_3 \end{pmatrix} \tag{19}$$

$$[C] = \begin{pmatrix} \frac{1}{C_1} & 0 & 0 \\ 0 & -N_2^2/C'_2 & 0 \\ 0 & 0 & 0 \end{pmatrix}. \tag{20}$$

In order to solve the system of equations represented by (15) for $i_{1,k}(t)$, $i_{2,k}(t)$, and $i_{3,k}(t)$, Laplace transformations can be used. The Laplace transform of (15) is given in (21). The Laplace domain functions of currents $I_{1,k}(s)$, $I_{2,k}(s)$, and $I_{3,k}(s)$ are provided in (A.5)–(A.7) in the Appendix.

$$\mathcal{L}\left\{\frac{\mathrm{d}\underline{v_k}}{\mathrm{d}t}\right\} = \left([A]s^2+[B]s+[C]\right)\underline{I_k}(s). \tag{21}$$

The inverse Laplace transforms of (A.5)–(A.7) cannot be solved symbolically due to the algebraic complexity of the Laplace domain functions resulting from the high number of unknown parameters (i.e., TPRC parameters, harmonic number, and control variables). However, the Laplace domain functions can be simplified by reducing the number of unknowns through substitution of numerical values for the converter parameters and finally solved for the inverse Laplace functions using MATLAB or similar numerical computing platforms. The inverse Laplace solutions will carry both the transient and steady-state terms. The transient terms can be identified as the ones with exponential terms and should be neglected [32] from the solution

$$\underline{i_k}(t) = \mathcal{L}^{-1}\left\{\underline{I_k}(s)\right\} \tag{22}$$

$$\underline{i}(t) = \sum_{k=1,\mathrm{odd}}^{n}\underline{i_k}(t). \tag{23}$$

TABLE II
RATINGS AND PARAMETERS OF THE TPRC

Key specifications	V_1 = 400–800 V P_1 = 6 kW L_1 = 87.5 μH C_1 = 35 nF	V_2 = 46–50 V P_2 = 3.2 kW L_2 = 1.8 μH C_2 = 1.7 μF	V_3 = 10–14 V P_3 = 2.8 kW L_3 = 32 nH
MOSFET part number	G3R20MT12K (GeneSiC)	IAUS260N10 —S5N019T (Infineon)	IAUS300N08 —S5N012T (Infineon)
MOSFETs in parallel	1	3	4
Dead time	$t_{d,1}$ = 250 ns	$t_{d,2}$ = 400 ns	$t_{d,3}$ = 600 ns
f_s	100 kHz		
Transformer	$n_1 : n_2 : n_3$ = 48 : 4 : 1 L_m = 1.87 mH		

The ac rms currents and MOSFET rms currents of port j are given in (24) and (25). The power delivered/received from each port can be computed from (26)

$$i_{j(\mathrm{RMS})} = \sqrt{\sum_{k=1,\mathrm{odd}}^{n}\frac{i_{j,k}^2}{T_s}} \tag{24}$$

$$i_{M,j(\mathrm{RMS})} = \frac{1}{\sqrt{2}}i_{j(\mathrm{RMS})} \tag{25}$$

$$P_{j(\mathrm{model})} = v_j(t)i_j(t). \tag{26}$$

B. Model Validation

The solution to the derived mathematical model is validated against the simulation results of a TPRC model in PLECS. The converter ratings are given in Table II .

1) Harmonic Number: Both the bridge voltage and ac current functions of each port are given as a sum of n harmonics. With increasing n, the model accuracy improves although requiring a longer computation time. Hence, the minimum value of n to be used in control optimization is determined using a sensitivity analysis of n on the model accuracy.

The model parameters required for the TPRC loss computation are rms currents and instantaneous switching currents. Based on the simulation results, the modeled rms currents converge to simulated values within a low number of harmonics. Hence, the sensitivity analysis of n is conducted for switching currents in each port. The sensitivity analysis results are presented in Fig. 4 for a boundary operating condition of the TPRC. The boundary is chosen away from the unity conversion ratio of the TPRC to verify its validity. The MOSFETs switching the highest current levels in each port are used in the sensitivity analysis. These correspond to S_3 and S_4 of port 1, S_5 and S_6 of port 2, and S_9 and S_{10} of port 3. The e_{ss} between the modeled and simulated switching currents reaches a constant by $n = 201$, and is used for the model comparisons and control optimization within the rest of this article. The waveforms of bridge voltages and ac currents from PLECS simulation results overlapping those from the mathematical model (at $n = 201$) at the same operating point as the sensitivity analysis are illustrated in Fig. 5. The PLECS simulation model is generated with the same passive element ratings used in the analytical model and

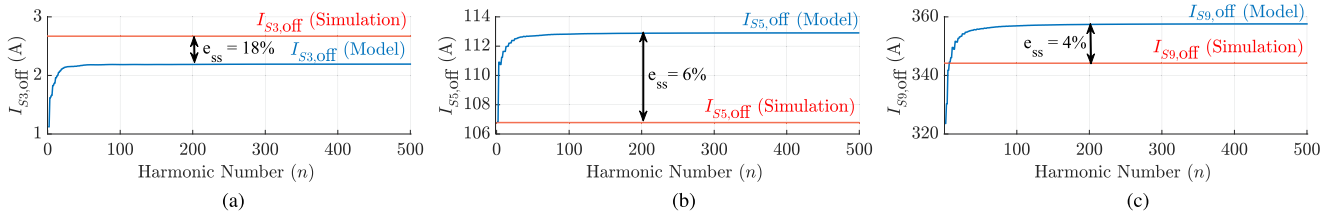


Fig. 4. Sensitivity analysis of the harmonic number at $V_1 = 400$ V, $V_2 = 48$ V, $V_3 = 12$ V, $P_2 = 1.6$ kW, $P_3 = 1.4$ kW. (a) $I_{S3,\text{off}}$ (Port 1). (b) $I_{S_5,\text{off}}$ (Port 2). (c) $I_{S9,\text{off}}$ (Port 3).

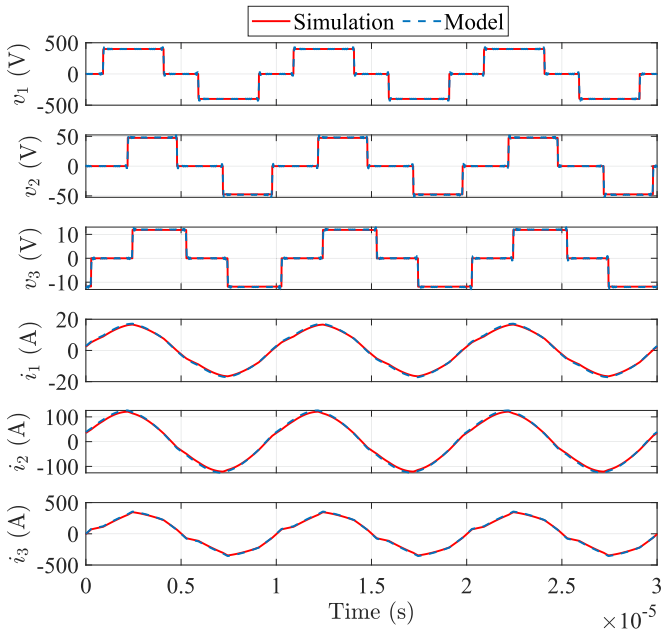


Fig. 5. Comparison of bridge voltage and ac current waveforms between PLECS simulation results and mathematical model $V_1 = 400$ V, $V_2 = 48$ V, $V_3 = 12$ V, $P_2 = 1.6$ kW, $P_3 = 1.4$ kW.

the other nonidealities are not considered. Hence, ideal MOSFET models are used for all three ports. It can be observed that the results from the steady state model can closely follow the simulation results.

2) Comparison Between the Mathematical Model and the Simulation Model: The mathematical model developed previously is compared against the simulation results for $n = 201$ harmonics. The model validation was carried out by comparing rms currents and MOSFET turn-OFF currents of each leg at varying port voltages and power levels. The model comparison plots with varying port 2 power at $V_1 = 600$ V, $V_2 = 50$ V, $V_3 = 12$ V, and $P_3 = 2.8$ kW are given in Fig. 6. It is observed that the mathematical model can closely follow the trend in the simulation results. While the current waveforms are seen to overlap in Fig. 5, errors in rms currents (average error $= 5\%$) and switching currents (average error $= 6\%$) are observed in Fig. 6. The modeling error can be attributed to the different solvers, i.e., the mathematical model uses continuous time and laplace domain functions while PLECS uses piecewise linear functions [33].

TABLE III
DIRECTION OF AC CURRENT TO SATISFY ZVS CONDITION 1 FOR TPRC

Port	MOSFETs	Ac current direction to satisfy ZVS condition 1
Port 1	S_1, S_4	$i_1 < 0$
	S_2, S_3	$i_1 > 0$
Port 2	S_5, S_8	$i_2 > 0$
	S_6, S_7	$i_2 < 0$
Port 3	S_9, S_{12}	$i_3 > 0$
	S_{10}, S_{11}	$i_3 < 0$

C. ZVS Criteria

The TPRC inherits ZVS capability, which should be considered in the development of mathematical loss models for accurate computation of power losses. To achieve ZVS at turn-ON, the voltage across the MOSFET should reach zero by fully discharging the output capacitance across it. Hence, it is important to identify the criteria for ZVS.

The ZVS operation can be explained with respect to port 1 MOSFETs at S_1 turn-OFF and S_2 turn-ON as follows. With reference to Fig. 2, before S_1 turns-OFF, S_1 and S_4 are conducting. At the moment of S_1 turning OFF, if the direction of i_1 is $i_1 > 0$, output capacitance ($C_{\text{DS},1}$) across S_2 starts to discharge while charging that of S_1. If there is sufficient circulating energy during dead time to fully discharge $C_{\text{DS},1}$ of S_2, S_2 can have full ZVS at turn-ON. The desired direction of ac currents to discharge $C_{\text{DS},j}$ across each MOSFET of the three ports is given in Table III. The two conditions required to achieve ZVS at turn-ON as given in [34] are as follows.

1) The direction of current flow in each port during the dead time before turning on should be according to Table III. This direction of current flow will ensure $C_{\text{DS},j}$ charges/discharges appropriately.
2) The circulating energy during the dead time ($E_{\text{available}}$) should be sufficient to charge/discharge the MOSFET output capacitance fully.

The ZVS criteria should be evaluated at the turn-ON of each MOSFET (S_1 to S_{12}). To evaluate the ZVS criteria based on the above-mentioned conditions, energy required to fully discharge the total $C_{\text{DS},j}$ (E_{sink}) under different switching states should be considered. ZVS criteria for a TAB with a similar control technique is defined in Dey et al.'s [27] work, where the authors have presented E_{sink} under six switching states for each of the ports. TPRC with PSDR control can also be analyzed under the same six states with a similarly derived Thevenin equivalent

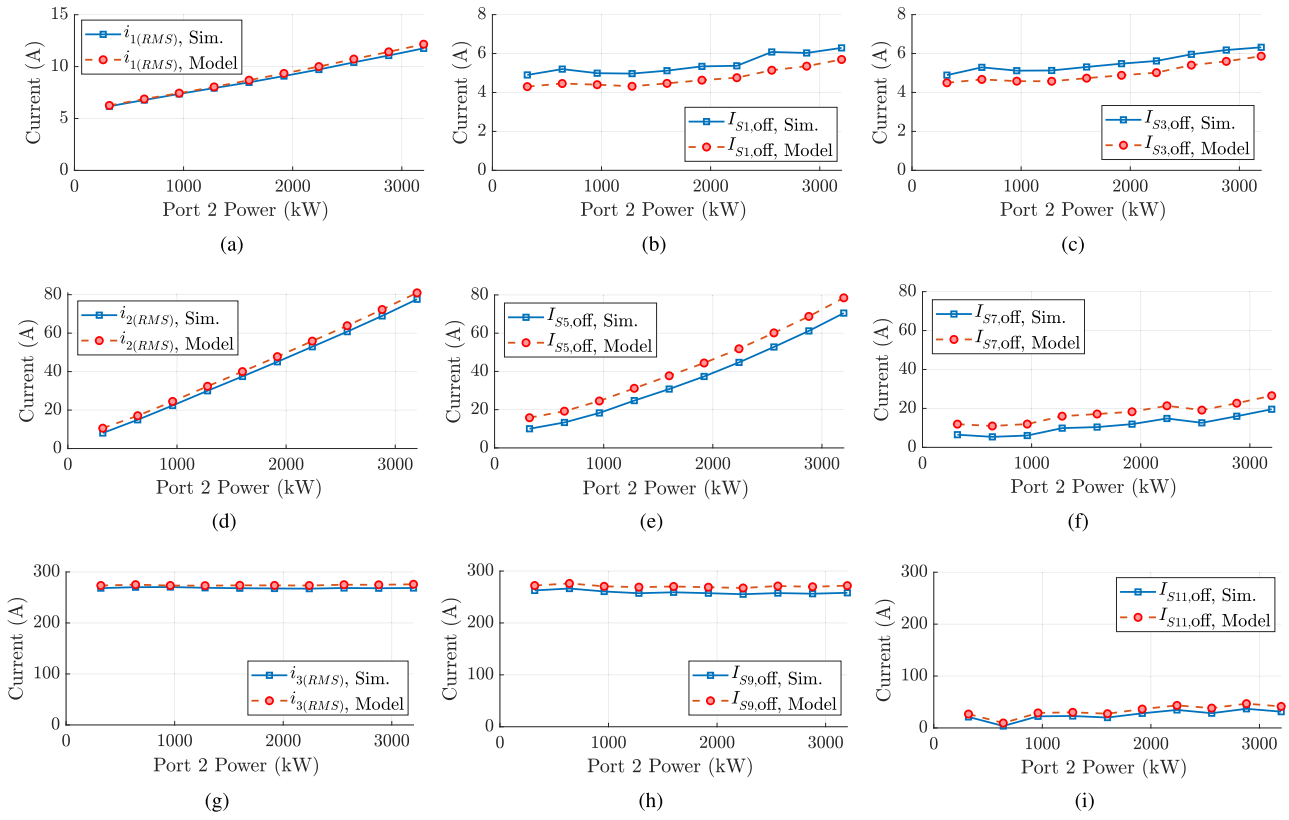


Fig. 6. (a)–(i): Simulated and mathematically modeled currents of the TPRC; $V_1 = 600$ V, $V_2 = 50$ V, $V_3 = 12$ V, $P_2 = 0.32 - 3.2$ kW, $P_3 = 2.8$ kW.

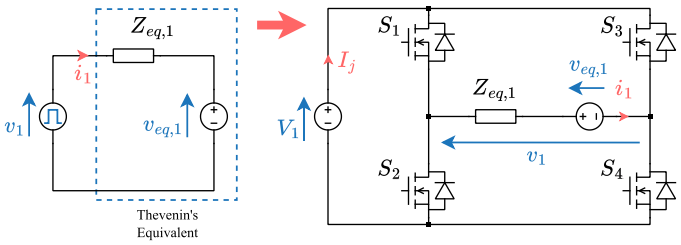


Fig. 7. Thevenin's equivalent circuit referred to port 1.

TABLE IV
FUNCTIONS FOR E_{SINK}

MOSFET turning ON	E_{sink}
$S_{4(j-1)+2}$ and $S_{4(j-1)+3}$	$2C_{\text{DS},j}V_j v_{\text{eq},j}(t)$
$S_{4(j-1)+1}$ and $S_{4(j-1)+4}$	$-2C_{\text{DS},j}V_j v_{\text{eq},j}(t)$
$S_{4(j-1)+1}$	$-2C_{\text{DS},j}V_j v_{\text{eq},j}(t) - C_{\text{DS},j}V_j^2$
$S_{4(j-1)+2}$	$2C_{\text{DS},j}V_j v_{\text{eq},j}(t) - C_{\text{DS},j}V_j^2$
$S_{4(j-1)+3}$	$2C_{\text{DS},j}V_j v_{\text{eq},j}(t) + C_{\text{DS},j}V_j^2$
$S_{4(j-1)+4}$	$-2C_{\text{DS},j}V_j v_{\text{eq},j}(t) + C_{\text{DS},j}V_j^2$

circuit for each port. Thevenin's equivalent circuit referred to port 1 is shown in Fig. 7 and Thevenin's equivalent impedance ($Z_{\text{eq},1}$) and equivalent voltage ($v_{\text{eq},1}$) are given in (27) and (28), respectively. Thevenin's equivalent circuit, impedance, and voltage can be derived similarly for ports 2 and 3. Z_{12}, Z_{13}, and Z_{23} are impedances of the equivalent delta network, whose derivations are given in (A.2)–(A.4) of the Appendix. The functions of E_{sink} for the six switching states of port j are given in Table IV. The first two states are valid for $d_j = 1$ and the rest for $0 < d_j < 1$.

$$Z_{\text{eq},1} = \frac{Z_{12}Z_{13}}{Z_{12} + Z_{13}} \tag{27}$$

$$v_{\text{eq},1} = v_2 \frac{Z_{\text{eq},1}}{Z_{12}} + v_3 \frac{Z_{\text{eq},1}}{Z_{13}}. \tag{28}$$

The $E_{\text{available}}$ for ZVS of a MOSFET in port j is evaluated as the energy in $Z_{\text{eq},j}$ at the turn-OFFof its complementary MOSFET (t_{off,S_c}), as given in (29). The turn-ON and turn-OFFtimes of each MOSFET based on the modulation criteria shown in Fig. 2 are given in Table VII in the Appendix.

$$E_{\text{available}} = \int_{t_{\text{off},S_c}}^{t_{\text{off},S_c}+t_{d,j}} (v_j - v_{\text{eq},j}) i_j \, \text{d}t. \tag{29}$$

If only the first condition for ZVS is met and $E_{\text{available}} < E_{\text{sink}}$, partial ZVS occurs. It is important to analyze partial ZVS to calculate the turn-ON switching losses accurately. During partial ZVS, the voltage across the MOSFET turning-ON will be between 0 and the port dc voltage. This voltage is calculated based on the $E_{\text{available}}/E_{\text{sink}}$ ratio and is validated for one of the switching states considered for ZVS analysis in port 1 as follows.

Consider the case where $0 < d_1 < 1$ and $i_1 > 0$ for the ZVS of S_2 in port 1. MOSFET S_1 will turn-OFF and after the dead time

TABLE V
TPRC POWER LOSS FUNCTIONS

Component	Loss symbol	Power loss (W)
S_i	$P_{\text{cond}\,(M),i}$	$i^2_{M,j(\text{RMS})} R_{\text{DS}\,(\text{on}\,),i}$
	$P_{\text{on},i}$	$f_s E_{\text{on}\,,j}$
	$P_{\text{off},i}$	$f_s E_{\text{off}\,,j}$
	$P_{\text{cond}\,(D),i}$	$f_s t_{d,i} V_{\text{SD}\,,i} \text{abs}(I_{Si,\text{off}})$
Transformer	P_{Cu}	$\sum_{j=1}^{3} i^2_{j,(\text{RMS})} R_{\text{ac},j}$
	P_{core}	$k_{fe} f_s^{\alpha} \Delta B^{\beta} V_e$
Resonant tank	$P_{\text{ESR}\,,j}$	$i^2_{j(\text{RMS})} R_{\text{res}\,,j}$

$t_{d,1}$, S_2 will turn-ON. In the meantime, S_3 is OFFand S_4 is ON. During the dead time voltage across S_1 charges from 0 V and voltage across S_2 discharges from V_1. Suppose S_2 cannot fully discharge the voltage from V_1 to 0 V; partial ZVS occurs with the voltage across the MOSFET at $V_{\text{on},2}$, where $0 < V_{\text{on},2} < V_1$. Based on the Thevenin equivalent circuit in Fig. 7, the energy available to partially charge/discharge $C_{\text{DS},1}$ can be derived as follows:

$$v_{\text{DS},1} + v_{\text{DS},2} = V_1 \tag{30}$$

$$i_{S_1} = C_{\text{DS},1} \frac{\text{d}v_{\text{DS},1}}{\text{d}t} = -C_{\text{DS},1} \frac{\text{d}v_{\text{DS},2}}{\text{d}t} \tag{31}$$

$$i_{S_2} = -C_{\text{DS},1} \frac{\text{d}v_{\text{DS},2}}{\text{d}t} \tag{32}$$

$$\begin{aligned} E_{\text{available}} &= \int_{t_{\text{off},S_1}}^{t_{\text{off},S_1}+t_{d,1}} (v_{\text{eq},1} i_1 - V_1 I_1) \text{d}t \\ &= \int_{t_{\text{off},S_1}}^{t_{\text{off},S_1}+t_{d,1}} \left(-2 v_{\text{eq},1} C_{\text{DS},1} \frac{\text{d}v_{\text{DS},2}}{\text{d}t} + V_1 C_{\text{DS},1} \frac{\text{d}v_{\text{DS},2}}{\text{d}t} \right) \text{d}t \\ &= \int_{V_1}^{V_{\text{on},2}} (-2 v_{\text{eq},1} C_{\text{DS},1} + V_1 C_{\text{DS},1}) \text{d}v_{\text{DS},2} \\ &= (2 v_{\text{eq},1} C_{\text{DS},1} + V_1 C_{\text{DS},1})(V_1 - V_{\text{on},2}). \end{aligned} \tag{33}$$

The E_{sink} to fully charge/discharge $C_{\text{DS},1}$ can be obtained from (33) when $V_{\text{on},2} = 0$, as given in the following:

$$E_{\text{sink}} = (2 v_{\text{eq},1} + V_1) C_{\text{DS},1} V_1. \tag{34}$$

Based on the above-mentioned equation, the voltage across S_2 at turn-ON can be derived as in the following:

$$V_{\text{on},2} = \left(1 - \frac{E_{\text{available}}}{E_{\text{sink}}} \right) V_1. \tag{35}$$

Therefore, in the event of incomplete discharge, the voltage across any turning-ON MOSFET of the TPRC can be calculated similarly based on the $E_{\text{available}}/E_{\text{sink}}$ ratio of the respective port and used in switching loss calculations.

Based on the conditions discussed previously, ZVS can be defined as an array of 12 elements corresponding to the voltage across the 12 MOSFETs in the TPRC before turning ON ($0 \leq V_{\text{on},i} \leq V_j$).

IV. CONTROL OPTIMIZATION

Once the TPRC currents and voltages are formulated, as discussed in Section III, they are used to derive the TPRC power loss model. This can be used to formulate the objective function for the control optimization. This section outlines the derivation of the power loss model and the methodology of control optimization.

A. Power Loss Model

The solution to the steady-state currents, ac rms currents, and MOSFET rms currents are evaluated for a set of control variables **x**, port voltages, and power levels. This information is used to estimate the power losses through numerical computation.

The generic power loss formulas of the components in the TPRC are defined in Table V. The MOSFET's ON-state resistance ($R_{\text{DS(on)},i}$) at $T_j = 125$ °C is used to estimate worst-case conduction losses. $E_{\text{on},j}$ is the turn-ON energy map as a function of $V_{\text{on},i}$ and $I_{Si,\text{on}}$. $V_{\text{on},i}$ is determined based on the full/partial/no ZVS availability at the control point being evaluated. $E_{\text{off},j}$ is the turn-OFFenergy map as a function of $V_{\text{off},i}$ (equal to V_j) and $I_{Si,\text{off}}$. The $P_{\text{cond}(D),i}$ is only evaluated if there is full ZVS based on the explanation in Section III-C; otherwise, its evaluation is omitted.

Fig. 8(a) shows the double pulse test (DPT) of port 1's MOSFET at 600 V. Fig. 8(b) and 8(c) shows the switching energy measurement during the turn-ON and turn-OFF intervals, respectively. For the port 2 and port 3 MOSFETs, their switching energies cannot be measured due to the inability to measure currents through the surface-mount devices; instead, they are estimated by consecutive measurements of voltage spike amplitude (VSA) and co-simulation with SPICE [35].

Due to the high-current requirements of ports 2 and 3 of the TPRC, the transformer interconnection with the port printed circuit boards (PCBs) is bulky and a major contributor to ohmic losses within the converter. Using the dc resistance of the busbar and winding for loss calculations will provide an inaccurate estimation of losses at higher power levels and switching frequencies, due to skin and proximity effects. Hence, ac resistance of the transformer, including the interconnecting busbar between the power PCBs and the transformer along with the winding resistance is measured. The measured ac resistance values using a Keysight E4990 A impedance analyzer are $R_{\text{ac},2} = 40.16$ mΩ and $R_{\text{ac},3} = 2.53$ mΩ. The transformer core loss is calculated for four ER51 cores used to construct the transformer [36]. The ohmic losses due to the equivalent series resistance (ESR) of resonant tank elements are also calculated based on the manufacturer provided data of each component.

T_j of each MOSFET is computed based on the total power loss and thermal resistance per MOSFET as given in (36)–(38). The MOSFETs are in contact with the heat sink through a thermal interface material (TIM), and the thermal resistances from MOSFET junction to heat sink are used to compute total thermal resistance, as given in (37). The values for $R_{\text{th,TIM},i}$ and $R_{\text{th,JC},i}$ are obtained from the datasheets of the TIM and MOSFETs, respectively. $R_{\text{th,JC},i}$ is evaluated through finite element analysis

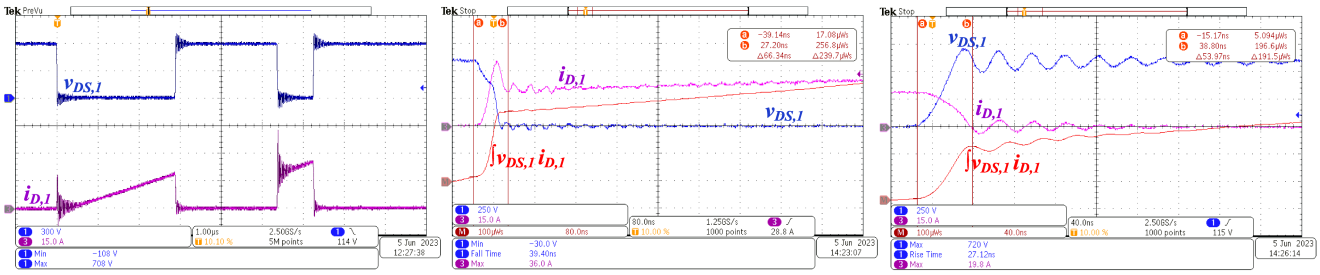


Fig. 8. Switching energy measurement of G3R20MT12 K. (a) DPT. (b) Turn-ON interval. (c) Turn-OFF interval.

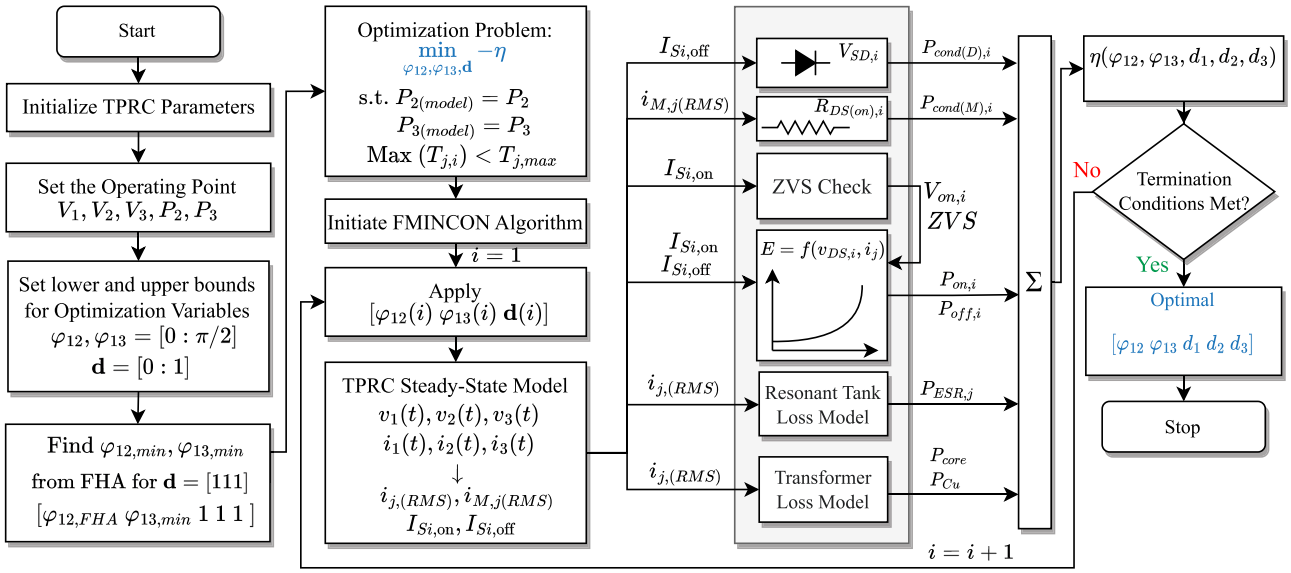


Fig. 9. PSDR control optimization procedure for TPRC.

of the cooling design

$$P_{\text{loss}(M),i} = P_{\text{cond}(M),i} + P_{\text{on},i} + P_{\text{off},i} + P_{\text{cond}(D),i} \quad (36)$$

$$R_{\text{th},i} = R_{\text{th,JC},i} + R_{\text{th,TIM},i} + R_{\text{th,HS},i} \quad (37)$$

$$T_{j,i} = P_{\text{loss}(M),i} R_{\text{th},i} + T_{\text{HS}}. \quad (38)$$

The solution of the steady-state equations defined in Section III are used to determine the aforementioned power losses. The switching instance details for the MOSFETs are given in Table VII of the Appendix.

B. Optimization Procedure

The control optimization procedure is illustrated in Fig. 9. This procedure is iterated through each operating point defined by V_1, V_2, V_3, P_2, and P_3 to evaluate the optimal control variables. TPRC efficiency is formulated from the power loss model discussed previously and used as the objective function of the optimization problem. The upper and lower bounds for PSs and duty-ratios are set to the extreme feasible values for the power transfer from port 1 to ports 2 and 3. The optimization algorithm runs based on the defined bounds, initial point, and the constraints. The termination criteria are defined based on the tolerances for constraints, optimization variable step size, and objective function [37].

C. Formulation of the Optimization Problem

The optimization problem for efficiency maximization is defined in (39). The objective function is represented by η and the optimization variables are the control variables [φ_{12}, φ_{13}, d_1, d_2, d_3]. Since the optimization problems are generally defined as minimization problems, and to maximize efficiency, minimization of $-\eta$ is considered

$$\begin{aligned} \min_{\varphi_{12},\varphi_{13},\mathbf{d}} \quad & -\eta \\ \text{s.t.} \quad & P_{2(\text{model})} = P_2 \\ & P_{3(\text{model})} = P_3 \\ & \max_{i=1 \text{ to } 12} (T_{j,i}) < T_{j,\max}. \end{aligned} \quad (39)$$

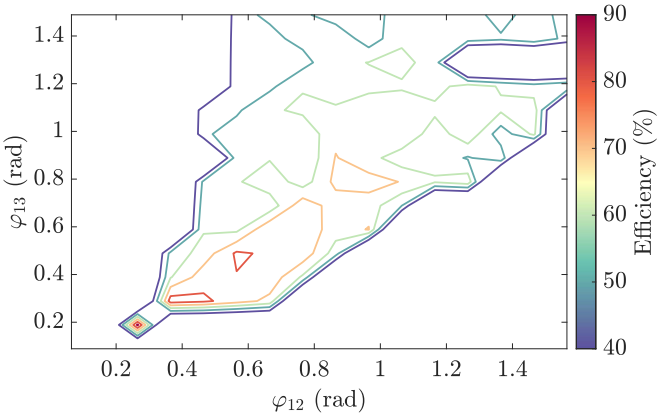


Fig. 10. Contour plot of the efficiency function at nominal voltages (600/48/12 V) with $P_2 = 1772$ W (55% of FL) and $P_3 = 1152$ W (40% of FL).

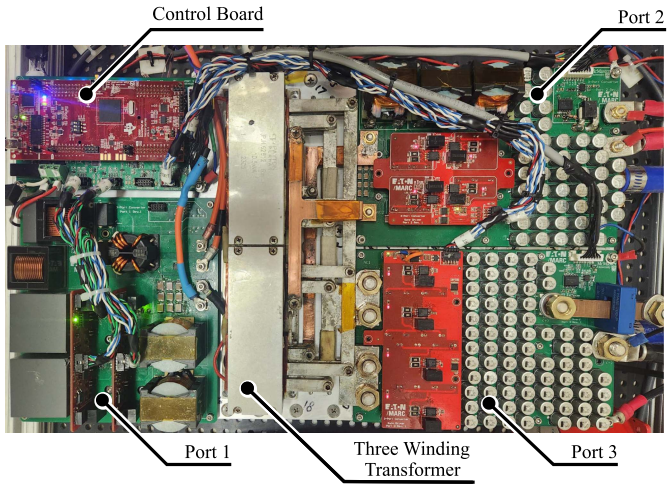


Fig. 11. 6 kW hardware demonstrator of the TPRC.

The converter efficiency is formulated as a function of losses from the loss model, as given in the following:

$$P_{\text{loss}} = \sum (P_{\text{cond}(M),i} + P_{\text{on},i} + P_{\text{off},i} + P_{\text{cond}(D),i} + P_{\text{Cu}} + P_{\text{core}} + P_{\text{ESR},j}) \tag{40}$$

$$\eta = \frac{P_2 + P_3}{P_{\text{loss}} + P_2 + P_3}. \tag{41}$$

1) Optimization Algorithm: The optimization algorithm for efficiency maximization should be determined based on the trajectory of the objective function as a function of optimization variables. A local optimization algorithm can be used for a minimization problem if the objective function has only one minimum (i.e., local minimum = global minimum). However, if the objective function has several local minima, the global minimum should be evaluated either by using a global optimization algorithm or multiple iterations of a local optimization algorithm with different starting points.

The MATLAB optimization toolbox offers methods, such as FMINCON, pattern search, and genetic algorithm (GA) for optimization problems with nonlinear objective functions and constraints [38]. GA is the only global optimization algorithm; the rest are local optimization algorithms. However, the parameters of GA concerning populations must be carefully selected to avoid convergence to an incorrect solution. FMINCON, a gradient-based optimization algorithm, is identified as the most efficient among the local optimization algorithms [39]. In the case of multiple local minima, FMINCON converges to the local minimum near the initial point.

The contour plot of η as a function of φ_{12} and φ_{13} is provided in Fig. 10. It can be observed that there exist several local minima; however, the global minimum lies in the vicinity of the minimum PSs. The power transfer equations derived by applying the FHA to the quasisquare voltages in the equivalent delta network are given in (42)–(46) [9]. It is observed that the PSs are minimum when $\mathbf{d} = 1$

$$P_{12} = \frac{8}{\pi^2}\frac{V_1 V_2'}{Z_{12}} \sin\left(\frac{\pi}{2}d_1\right) \sin\left(\frac{\pi}{2}d_2\right) \sin(\varphi_{12}) \tag{42}$$

$$P_{13} = \frac{8}{\pi^2}\frac{V_1 V_3'}{Z_{13}} \sin\left(\frac{\pi}{2}d_1\right) \sin\left(\frac{\pi}{2}d_3\right) \sin(\varphi_{13}) \tag{43}$$

$$P_{23} = \frac{8}{\pi^2}\frac{V_2' V_3'}{Z_{23}} \sin\left(\frac{\pi}{2}d_2\right) \sin\left(\frac{\pi}{2}d_3\right) \sin(\varphi_{13} - \varphi_{12}) \tag{44}$$

$$P_2 = P_{12} - P_{23} \tag{45}$$

$$P_3 = P_{13} + P_{23}. \tag{46}$$

The analysis of the objective function makes it possible to minimize multiple iterations of the local optimization algorithm by properly selecting the initial point. Since the global minimum lies in the vicinity of the minimum PSs when $\mathbf{d} = 1$, a gradient-based local optimization algorithm can be used with the initial point set to $\mathbf{x} = [\varphi_{12,\min}\ \varphi_{13,\min}\ 1\ 1\ 1]$ instead of using GA with a high computation time. Hence, to solve this optimization problem, FMINCON is used with the initial point approximated using FHA at $\mathbf{d} = 1$.

2) Optimization Constraints: The optimization constraints are listed in the problem definition given in (39). Since the voltage functions in the mathematical model are derived assuming desired voltages V_2 and V_3 in ports 2 and 3, respectively, the desired power levels (P_2 and P_3) are used in equality constraints to determine whether the set point is reached. An inequality constraint on maximum T_j is used to maintain the junction temperature of the MOSFETs less than the design-limited value, which is set to 125 °C.

V. Experimental Validation

The proposed control optimization is validated using a 6 kW/100 kHz hardware demonstrator with liquid cooling, as seen in Fig. 11. Closed loop control is implemented to test the PS and optimized PSDR control. The experiments are carried out for wide power and voltage ranges. The efficiency, power losses, rms, and switching currents of the TPRC are compared between PS and optimized PSDR control from the experimental results. Thermal run tests are also conducted to analyze the MOSFET case temperature rise and temperature gradient in each port.

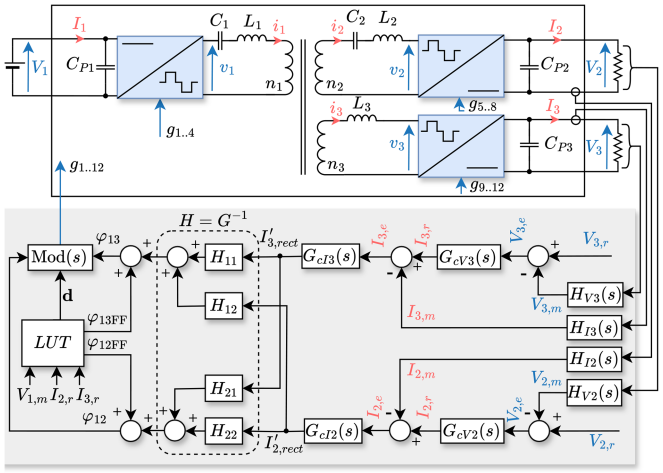


Fig. 12. Control loop of the TPRC.

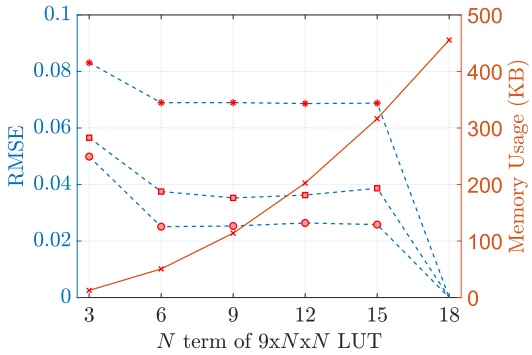


Fig. 13. RMSE compared to 9×18×18 LUTs and memory usage for varying LUT sizes.

A. Closed Loop Control and Feedforwarding Mechanism

An EV with dual auxiliary ports requires two separate control loops for the regulation of load voltages in the TPRC. A closed loop control scheme for the presented TPRC has been initially defined in [9] and [40] and is used in this work as a basis. Fig. 12 depicts a simplified version of the control structure. Utilizing power transfer equations from (42)–(44), rectifier output currents $I_{2,\text{rect}}$ and $I_{3,\text{rect}}$ are obtained as follows:

$$I_{2,\text{rect}} = \frac{8}{\pi^2}\frac{n_1}{n_2}\frac{V_1}{Z_{12}}\sin\left(\frac{\pi}{2}d_1\right)\sin\left(\frac{\pi}{2}d_2\right)\sin(\varphi_{12}) - \frac{8}{\pi^2}\frac{n_1^2}{n_2 n_3}\frac{V_3}{Z_{23}}\sin\left(\frac{\pi}{2}d_2\right)\sin\left(\frac{\pi}{2}d_3\right)\sin(\varphi_{13}-\varphi_{12}) \quad (47)$$

$$I_{3,\text{rect}} = \frac{8}{\pi^2}\frac{n_1}{n_3}\frac{V_1}{Z_{13}}\sin\left(\frac{\pi}{2}d_1\right)\sin\left(\frac{\pi}{2}d_3\right)\sin(\varphi_{13}) + \frac{8}{\pi^2}\frac{n_1^2}{n_2 n_3}\frac{V_2}{Z_{23}}\sin\left(\frac{\pi}{2}d_2\right)\sin\left(\frac{\pi}{2}d_3\right)\sin(\varphi_{13}-\varphi_{12}). \quad (48)$$

The dependence of φ_{12}, φ_{13}, d_1, d_2, and d_3 on $I_{2,\text{rect}}$ and $I_{3,\text{rect}}$ demonstrate the points of control. The rectifier current equations in (47) and (48) can be illustrated in the vector form as $\mathbf{I}_{\text{rect}} = G\boldsymbol{\varphi}$. However, in this form φ_{12} and φ_{13} cannot independently control their respective ports. Thus, a decoupling matrix $H = G^{-1}$ is required [9].

To respond to unpredictable changing auxiliary loads in an EV, the control consists of dual (nested) loops; outer voltage and inner current loops [10]. Output voltages and currents are measured directly and processed in a digital controller implemented via a DSP. Feedback transfer functions $H_{Vj}(s)$ and $H_{Ij}(s)$ are representative of various low-pass filters placed throughout the signal chain and ADC sample and hold (S/H) delays. $\text{Mod}(s)$ corresponds to the gate signal modulator modeled with the computation overhead delays and phase delays due to discretized PWM. The form of voltage ($G_{cVj}(s)$) and current ($G_{cIj}(s)$) compensators with respect to port j are given in the following. Voltage compensators are PI controllers where current compensators have the form of a lead compensator with an additional integrator.

$$G_{cVj}(s) = \frac{K_{Vj}(s+z_{Vj})}{s} \qquad G_{cIj}(s) = \frac{K_{Ij}(s+z_{Ij})}{s(s+p_j)}. \quad (49)$$

The compensators are designed based on the frequency response of the system model in Fig. 12. Further details about the compensators are provided in Kozielski et al.'s [40] work along with a controller design procedure for the TPRC outlining loop gains and delays introduced from a digital implementation, and have been omitted in this article for brevity.

Five LUTs generated based on the optimization procedure discussed in Section IV are utilized to compute the optimum control point for feedforwarding ($\varphi_{12\text{FF}}$, $\varphi_{13\text{FF}}$, d_1, d_2, d_3). Each LUT is defined using $M\times N\times N$ values, where it is referenced from M number of port 1 dc voltage ($V_{1,m}$) terms, N number of port 2 dc current reference ($I_{2,r}$) terms, and N number of port 3 dc current reference ($I_{3,r}$) terms. The exact LUT size ($M\times N\times N$) is determined based on the interpolation accuracy of varying LUT sizes and their memory usage. Considering the use of single core in the TMS320F28379D digital signal processor (DSP) for closed loop control implementation, a maximum of 90% flash memory utilization (460 KB out of 512 KB) is allocated for the LUTs. For V_1 range in steps of 50 V (400 : 50: 800 V) M is selected as 9. Thus, the maximum possible size for each LUT is limitted to 9×18×18. The root-mean-square error (RMSE) of the duty-ratios with linear interpolation of varying LUT sizes ($9\times N\times N$) compared to 9×18×18 LUTs can be calculated as per (50) shown at the bottom of this page. The plot of RMSE and memory usage of each LUT size is given in Fig. 13. It is observed that the RMSE variation is negligible beyond 9×6×6

$$\text{RMSE of LUT}_{9\times N\times N} = \sqrt{\frac{\sum_{I_{2,r}=I_{2,\max}/18}^{I_{2,\max}}\sum_{I_{3,r}=I_{3,\max}/18}^{I_{3,\max}}\left[\text{LUT}_{9\times 18\times 18} - \text{interp}\left(\text{LUT}_{9\times N\times N}\right)\right]^2}{18^2}}. \quad (50)$$

TABLE VI
COMPARISON AMONG STATE-OF-THE-ART CONTROL OPTIMIZATION IMPLEMENTATIONS FOR FULLY ISOLATED TPCS

Reference	Topology	Control variables	Optimization objective	Model	Closed loop control
[20]	TAB	φ_{12}, φ_{13}, d_1, d_2, d_3 [d]	Rms current minimization	GHA based loss model	Cascaded and decoupled voltage - current control with model-independent gradient-descent optimization algorithm
[21]	TAB	φ_{12}, φ_{13}, d_1, d_2, d_3 [e]	Reactive power minimization	Based on power transfer equations	Decoupled power flow control with offline calculated LUTs
[22]	C3L3-TPRC	f_s, φ_{12}, φ_{13}	Semiconductor loss minimization	Improved GHA-based loss model	Decoupled voltage control with offline-online polynomial regression based optimization framework
[23]	TAB	φ_{12}, φ_{13}, d_1, d_2, d_3	Rms current and input dc current minimization	3-D-ripple correlation (RCC)	Online 3D-RCC optimization with decoupled voltage control
[24]	TAB	φ_{12}, φ_{13}, d_1, d_2, d_3	Rms current minimization	ANN	Offline trained ANN with decoupled voltage control
This work	**TPRC**	φ_{12}, φ_{13}, d_1, d_2, d_3	**Efficiency maximization**	**GHA-based loss model**	**Cascaded and decoupled voltage - current control with offline optimized LUTs**

Reference	f_s	**Max. computation time**	**Memory allocation**	**DSP**
[20]	247 kHz (DPS), 195 kHz (TPS), 134 kHz (PPS)	4.05 μs (DPS), 5.13 μs (TPS), 7.48 μs (PPS)	Unspecified	TMS320F28335
[21]	20 kHz	Unspecified	Unspecified	TMS320F28377D
[22]	360 - 500 kHz	1.9 – 4.1 μs	1.4 KB (ROM) [g] unspecified (RAM)	TMS320F28379D
[23]	40 kHz	Unspecified	Unspecified	Imperix L.t.d. B-Box
[24]	40 kHz	ANN: ~127 μs closed-Loop: 25 μs [f]	3.45 KB (ROM) 188 B (RAM)	STM32F334R8
This work	**100 kHz**	**8.2 μs**	**65.05 KB (ROM)**	**TMS320F28379D**

[d] The number of degrees of freedom selected offline as to dual phase-shift (DPS), triple phase-shift (TPS), quadruple phase-shift (QPS), and penta phase-shift (PPS).
[e] At least one of the three bridges has a two-level square waveform, hence only two duty-ratios vary at a time.
[f] Computation time estimated from the rate of closed-loop controller in the manuscript.
[g] Estimated memory solely consumed by 2nd order polynomial solution of 15 coefficients and three variables.

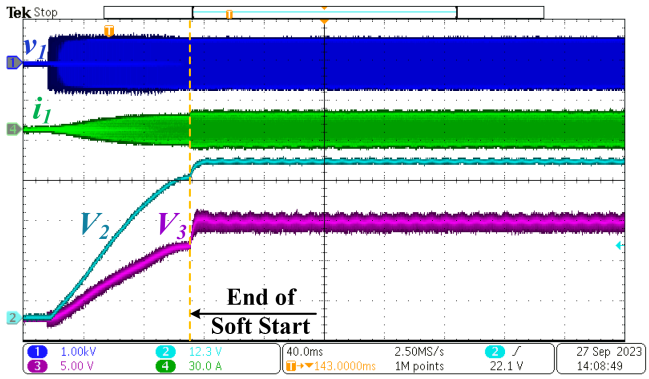


Fig. 14. Closed loop control converging to nominal dc voltages at ports 2 and 3 (48/12 V), $V_1 = 600$ V following soft start.

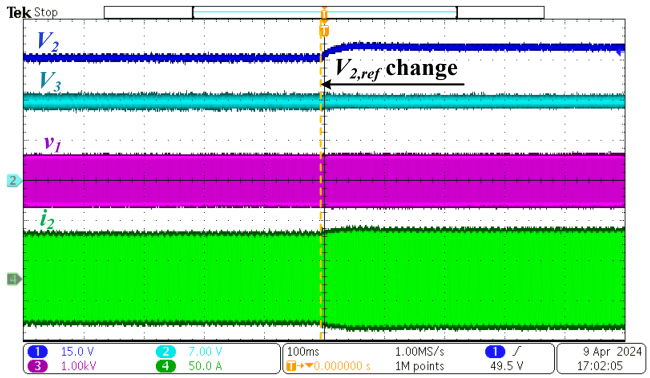


Fig. 15. Port 2 voltage reference change from 46 to 50 V at $V_1 = 600$ V, $P_2 = 1772$ W, and $P_3 = 1152$ W.

LUTs, hence LUT size can be fixed to 9×6×6 to conserve the memory usage (50.625 KB).

The closed loop control and LUT computations are implemented in two separate loops similar to [41]. The closed loop control, whose maximum computation time is 8.2 μs, is executed within a 10 μs interrupt. The optimal control variables from the LUT interpolations are updated every 180 μs, accounting for the worst case computation time of the LUTs. The control implementation in this work is compared against the state-of-the-art implementations of the multivariable control optimization published in the literature as given in Table VI.

The modulator generates gating signals, as defined in Fig. 2, based on the resultant control variables from the LUTs and the compensators. Experimental results for the closed loop control converging to set reference values of ports 2 and 3 dc voltages following the soft-start is seen in Fig. 14. A soft-start strategy to limit the inrush currents at the initial powering of the TPRC is also implemented [40]. The robustness of the voltage regulation under a step change in port 2 voltage reference is given in Fig. 15. It is observed that the LUT interpolation along with the closed loop control can allow stable voltage regulation of both output ports.

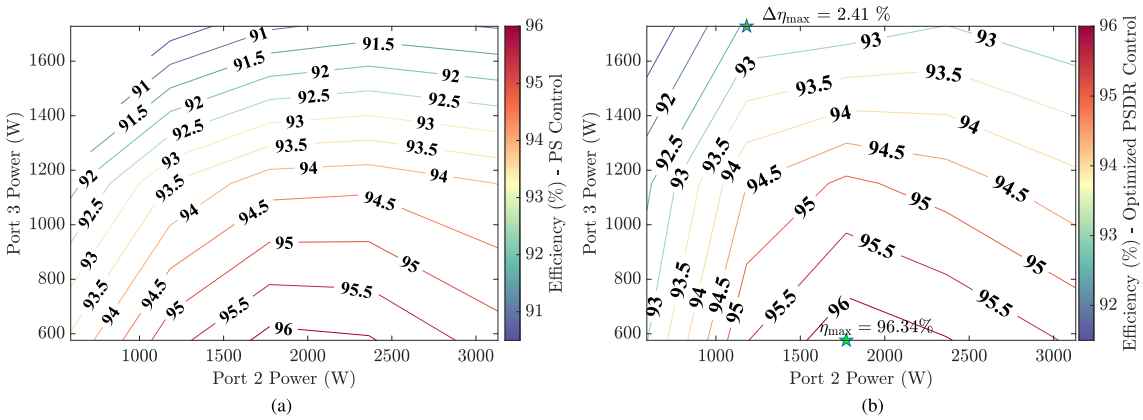


Fig. 16. Efficiency improvement between PS control and optimized PSDR control at nominal voltages (600/48/12 V). (a) PS control. (b) Optimized PSDR control.

B. *Efficiency Improvement With Optimized PSDR Control*

The closed loop control structure discussed previously is used to implement both PS control and optimized PSDR control. When implementing the PS control, there is no feedforwarding of PSs and the duty-ratios are set to 1. The efficiency comparison between optimized PSDR control and PS control is illustrated inFig. 16 at the nominal voltages ($V_1 = 600$ V, $V_2 = 48$ V, and $V_3 = 12$ V) for varying P_2 and P_3. It is observed that the effectiveness of optimized control improves at higher loads. A maximum efficiency improvement of 2.41% is observed at 15% and 60% loads in ports 2 and 3, respectively. The peak efficiency at nominal voltages with optimized PSDR control is 96.34% at medium load in port 2 and light load in port 3.

The oscilloscope waveforms of bridge voltages (v_2 and v_3) and currents (i_2 and i_3) recorded with full load (FL) on port 2 and 60% load on port 3 are given in Fig. 17. Rms current reduction in port 2 by 1.6% and in port 3 by 3.7% is observed under optimized PSDR control. Reduction in switching currents of leg B compared to leg A in ports 2 and 3 is also observed under optimized PSDR control. The efficiency measurements of the hardware demonstrator are obtained using the Zimmer precision power analyzer (LMG 671) and the recorded efficiency values at the same operating point for PS and optimized PSDR control are provided in Fig. 18. A loss reduction of 97 W and an efficiency improvement of 1.65% are observed at this operating point. The comparison of power loss distribution at the same operating point is illustrated in Fig. 19. During optimized PSDR control, two MOSFET legs in each port have different switching losses due to different switching currents. $P_{sw,A}$ and $P_{sw,B}$ represent the switching loss of the two legs of port 3. MOSFET arrays S_9 and S_{10} of port 3 represent leg A and S_{11} and S_{12} represent leg B. Similarly, in port 2, S_5 and $S6$ represent leg A and S_7 and S_8 represent leg B. There is a total loss reduction of 17.3% due to optimized PSDR control. The majority of loss reduction is from port 3, accounting for 34.2% compared to PS control. The power loss in leg A of port 3 is reduced by 7.7% and leg B by 60.7% compared to those with PS control.

The TPRC operates close to unity gain at its nominal voltages. The efficiency improvement from the optimized PSDR control improves when moving to the boost operation. This is evident in

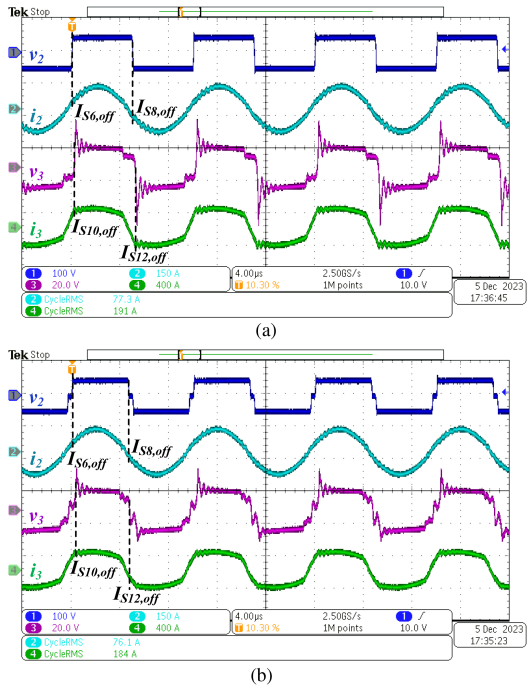
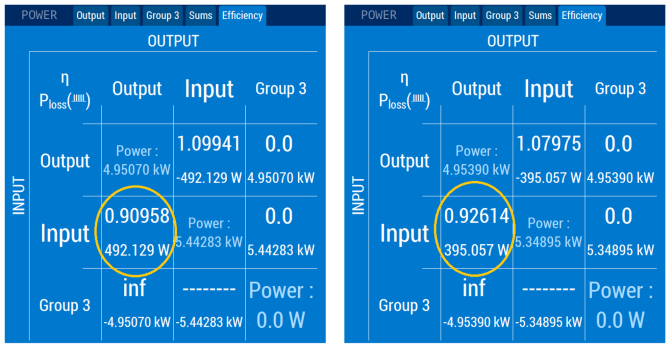


Fig. 17. Bridge voltage and current waveforms of ports 2 and 3 at nominal voltages (600 V/ 48 V/ 12 V) with $P_2 = 3131$ W (FL) and $P_3 = 1728$ W (60% of FL). (a) PS control. (b) Optimized PSDR control.

Fig. 20 at $V_1 = 500$ V through the reduction in ac rms and peak currents after applying the optimized PSDR control. Here, the TPRC is first run in closed loop control under PS control, and then, the optimized PSDR control variables are applied through the LUTs using an external command.

The efficiency comparison for varying port 1 voltage providing both buck and boost operations is given in Fig. 21. It is observed that the effectiveness of the optimized PSDR control improves when moving to the operating boundary of the boost operation. A maximum efficiency improvement of 12.4% (579 W of loss reduction) is observed at $V_1 = 400$ V. The oscilloscope waveforms of bridge voltages and currents recorded at this operating point are given in Fig. 22. RMS current reduction in port 2 by 23% and in port 3 by 12.7% is observed



(a) (b)

Fig. 18. Power analyzer efficiency measurements at nominal voltages (600/48/12 V) with $P_2 = 3131$ W and $P_3 = 1728$ W. (a) PS control. (b) Optimized PSDR control.

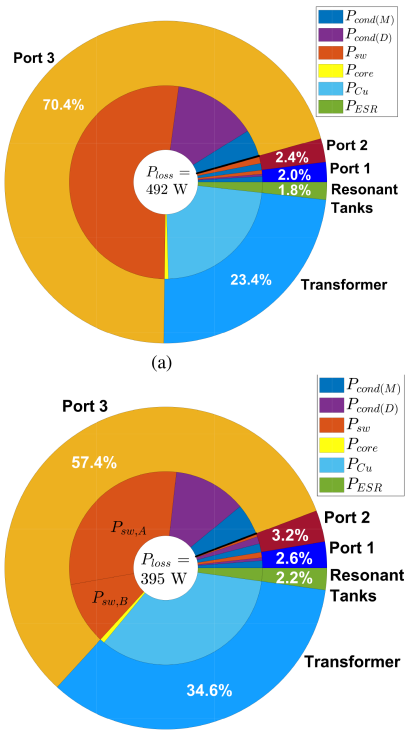


Fig. 19. TPRC loss distribution at nominal voltages (600/48/12 V) with $P_2 = 3131$ W (FL) and $P_3 = 1728$ W. (a) PS control top of subfigure (b) is cropped.

under optimized PSDR control at this operating point. Reduction in switching currents of leg B compared to leg A in ports 2 and 3 is also observed under optimized PSDR control.

The efficiency improvement during optimized PSDR control under boost operation ($V_1 < 600$ V) is clearly seen from Fig. 21. However, the efficiency improvement under buck operation ($V_1 > 600$ V) is not seen. During optimized PSDR control under buck operation, the reduction in rms and switching currents was observed only in port 2 and not in port 3. During the buck operation only d_1 tends to decrease significantly, but d_2 and d_3 remain close to unity. Since the loss contribution from ports 2 and 3 is significantly higher than that of port 1, the change in

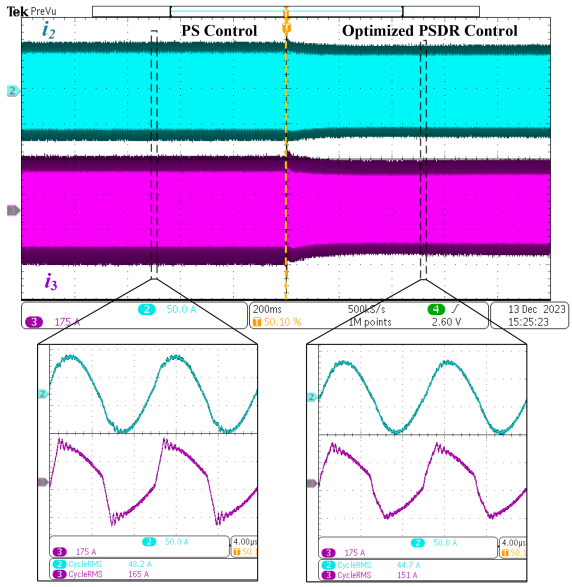


Fig. 20. Current waveforms of ports 2 and 3 during the control switch from PS to optimized PSDR control under boost operation (500/48/12 V) with $P_2 = 1772$ W and $P_3 = 1152$ W.

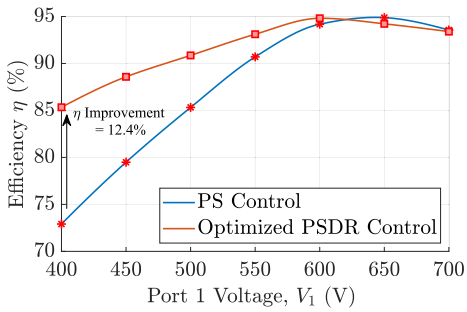


Fig. 21. Efficiency comparison at $P_2 = 1772$ W and $P_3 = 1152$ W for varying V_1.

d_1 alone does not lead to a visible loss reduction with optimized PSDR control.

C. Reduction in Temperature Rise

Liquid cooling for the TPRC hardware demonstrator is provided using a cold plate with a flow rate of 8 L/min and an inlet coolant temperature set at 30 °C. Case temperature readings of the MOSFETs are obtained during thermal run tests with PS control and optimized PSDR control using the thermocouples (OMEGA 5SC-TT-T-36-72) installed in the cold plate as seen in Fig. 23. Fig. 24 illustrates the MOSFET case temperature rise results from the thermal tests under PS control and optimized PSDR control at the same operating point used in Fig. 19.

During PS control, there is equal loss distribution among the MOSFETs in each port, however, the case temperature rise seen in leg B of port 3 is approximately 12 °C higher than that of leg A. This could be due to the heat conduction from the transformer high current busbars, which are in close proximity to the relevant thermocouple (as seen in Fig. 23). As noted previously in Fig. 19,

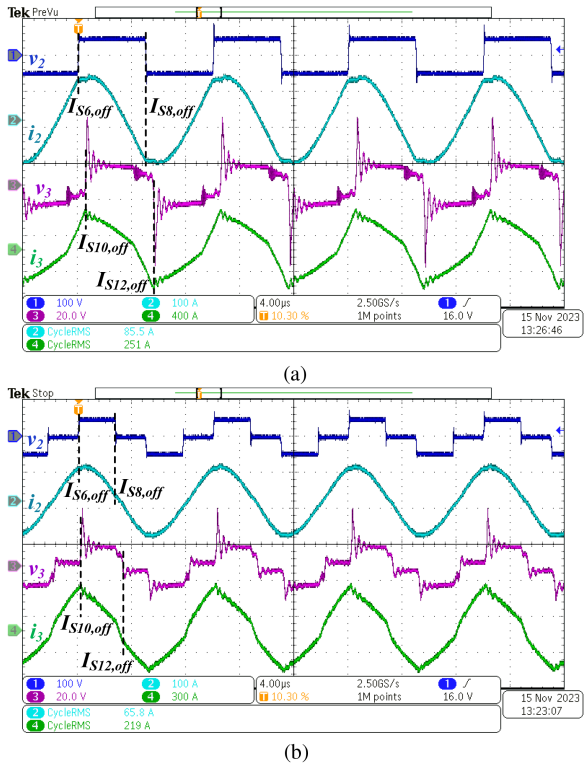


Fig. 22. Bridge voltage and current waveforms of ports 2 and 3 under boost operation (400/48/12 V) with $P_2 = 1772$ W and $P_3 = 1152$ W. (a) PS control. (b) Optimized PSDR control.

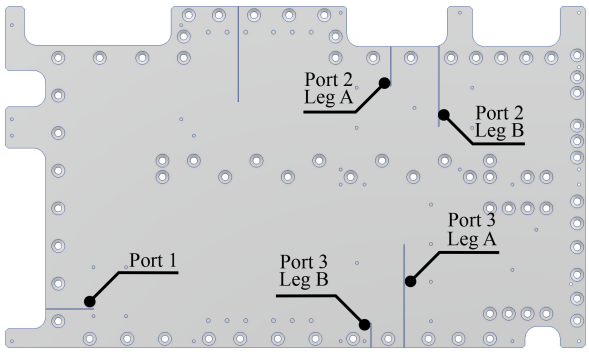


Fig. 23. Position of thermocouples on the cold plate.

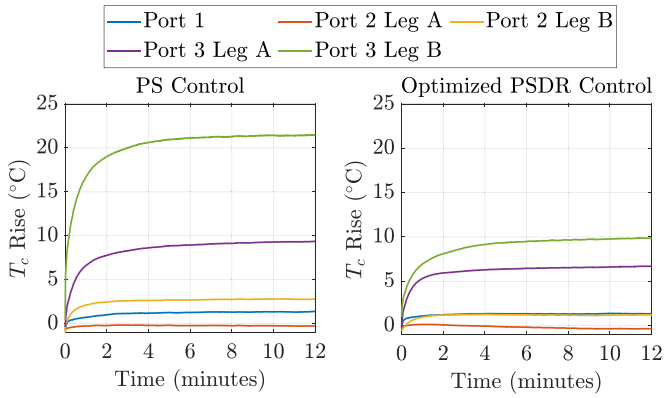


Fig. 24. Case temperature rise measurements at 600/48/12 V with $P_2 = 3131$ W and $P_3 = 1728$ W.

optimized PSDR control provides a loss reduction in port 3 legs A and B by 7.7% and 60.7%, respectively, compared to PS control. This has resulted the T_c reduction seen in Fig. 24, leg A by 2.7 °C and leg B by 11.6 °C. Hence, the optimized PSDR control significantly reduces the temperature rise in the TPRC. This also results in a reduction of temperature gradient in ports 2 and 3 as seen in Fig. 24. The T_c rise difference between legs A and B of port 3 has reduced from 12 °C to 3.2 °C with optimized PSDR control. Therefore, the reduced T_c rise and temperature gradient in each port due to optimized PSDR control can improve the system reliability.

D. System Nonidealities

The TPRC nonidealities which are not considered during model derivation and control implementation, but could impact the model response and accuracy of optimal control point are discussed in this section. The commutation loop inductance and component tolerances are two of the major nonidealities.

1) Effect of Commutation Loop Inductance: The commutation loop inductance (L_{loop}), even though not directly considered in the steady-state analytical model, influence the VSA at switching instances [42]. Hence, voltage spikes are observed in experimental bridge voltages at switching instances, as seen in Figs. 17 and 22, which are not seen in modeled or simulated waveforms. VSA during turn-OFFinstance is formulated, as given in the following:

$$\text{VSA}_j = L_{\text{loop},j} \frac{\text{d}i_j}{\text{d}t}. \tag{51}$$

L_{loop} is a sum of parasitic inductances of the PCB and the component leads. Since high VSAs affect the MOSFET reliability, it is critical to minimize L_{loop} [43]. The highest overshoot is observed in port 3 (12 V), and the further discussion encompasses this port. Based on the port 3 MOSFET switching characteristic and lead inductance (5 nH), there will be a significant VSA of 14 V when switching 100 A [44]. Hence, it is challenging to minimize L_{loop} in high current LV designs. However, the PCB designs for ports 2 and 3 have an estimated L_{loop} of 3.97 and 17.8 nH, respectively, based on ANSYS Q3D simulations. Remedies such as slowing down MOSFET turn-OFF and snubbers are used to manage the VSA. A further optimized PCB layout would help reduced the VSA.

The VSA affects the switching energies of the MOSFETs and has already been accounted for in the power loss model, as discussed in Section IV-A [35]. The impact of the VSA due to the commutation loop inductance has been evaluated based on the fast Fourier transform (FFT) comparison of the modeled and measured instantaneous ac power transfer in port 3. Fig. 25 illustrates a comparison between FFTs of modeled and measured $p_3(t)$ at nominal voltages and medium load. The effect of L_{loop} on the power transfer is evaluated by estimating the power difference at the ringing frequency of 2.8 MHz, and is seen as 2%. Hence, the impact of VSA on the power transfer is negligible, and the disparity can be further bridged by reduction of L_{loop}. It is not introduced in the steady-state mathematical model to simplify the equivalent radial circuit, as given in Fig. 3.

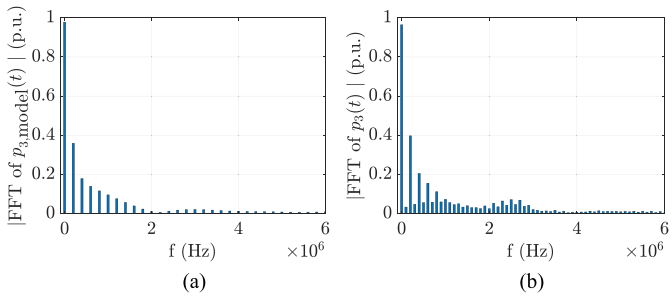


Fig. 25. FFT of the instantaneous ac power transfer at nominal voltages (600/48/12 V) with $P_2 = 1772$ W and $P_3 = 1152$ W. (a) Modeled (power factor = 0.977). (b) Measured (power factor = 0.964).

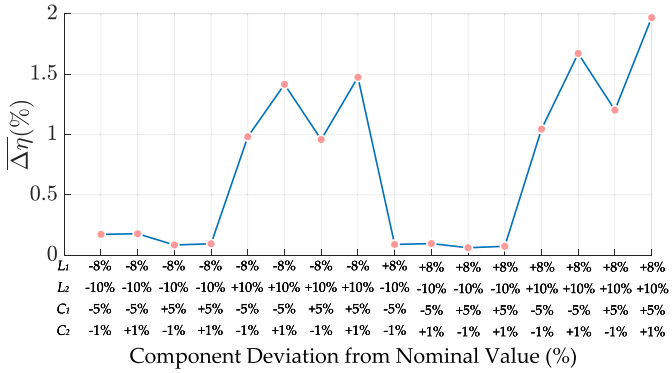


Fig. 26. Mean efficiency error at nominal voltages (600/48/12 V) with varying P_2 and P_3.

2) Effect of Component Tolerances: The LUTs are calculated from the optimization of the steady-state analytical model of the TPRC. The nominal values of the resonant tank components are considered during optimization. However, the resonant tank component values can vary within the manufacturer specified tolerances, which could affect the accuracy of the optimal control points. The manufacturer specified tolerances for the resonant tanks used in the hardware demonstrator are $\pm 8\%$ for L_1, $\pm 10\%$ for L_2, $\pm 5\%$ for C_1, and $\pm 1\%$ for C_2. Therefore, the mean reduction in efficiency ($\overline{\Delta\eta}$) introduced by the variation of the resonant tank parameters at the optimal control points is presented in Fig. 26. The maximum and minimum values for the resonant tank components are considered for the analysis. The mean efficiency error is computed by averaging the efficiency error over 36 operating points ($I_2 = I_{2,\min}$: $I_{2,\max}$ and $I_3 = I_{3,\min}$: $I_{3,\max}$) at nominal voltages. Maximum efficiency error occurs when all the components are at their maximum. It is observed that L_2 value at its maximum results in a significant deviation of the efficiency at the optimal control points. However, these results cannot be generalized as it depends on the range of values of the resonant tank and converter specifications. Nevertheless, it is important to analyze the effect of component tolerances on the accuracy of the optimization results and maintain tight component tolerances based on the analysis. As future work, online implementation of the control optimization to minimize the impact of the deviation in component values can be evaluated to make the control scheme immune from optimal control point variations [22].

VI. Conclusion

This article presents the PS and duty-ratio control optimization of a TPRC for dual auxiliary voltage EV applications. The objective of the control optimization is efficiency maximization and requires a sufficiently accurate model to evaluate the converter losses. Hence, a steady-state mathematical model of the converter is introduced. The steady-state mathematical model of the converter is derived based on GHA. The bridge voltage functions and the Laplace domain functions of the ac currents are provided and validated against the simulation based results in terms of rms and switching currents, which are critical for accurate loss modeling. This model is extended further to evaluate the converter losses through a loss model encompassing the semiconductor, transformer, and resonant tank losses. The developed mathematical model is used to calculate the converter efficiency as the objective function of the optimization problem.

The optimization problem is defined using the aforementioned objective function and constraints on power transfer and MOSFET junction temperature, which are nonlinear in nature. The objective function is analyzed, and the existence of a global minimum is identified. FMINCON, a gradient-based local optimization algorithm available in MATLAB's optimization toolbox, is used with the initial point set in the vicinity of the global minimum to ensure the convergence to the desired control point.

A closed loop control with LUTs of the optimized PSDR control variables is implemented in a 6 kW hardware demonstrator to verify the optimized PSDR control. The experimental results validate the efficiency improvements from PSDR control compared to PS control. The peak efficiency at nominal voltages with optimized PSDR control is observed to be 96.34%. The tests are conducted at buck, boost, and unity gain operation, and a maximum efficiency improvement of 12.4% (579 W of loss reduction) was observed at the extreme voltage levels of boost operation. Lastly, a thermal test is also carried out to ensure a safe temperature rise and gradient within the converter. Maximum case temperature rise was seen in leg B of port 3, which was reduced by 11.6 °C using optimized TPRC control. Therefore, the proposed control optimization methodology is able to improve the efficiency of the TPRC while maintaining the converter temperature distribution within safe limits.

Appendix

A. Switching Times

The turn-ON and OFF times of the MOSFETs under PSDR control with the inclusion of the dead time are given in Table VII.

B. Equivalent Delta Network

The equivalent delta network referred to port 1 for the radial circuit in Fig. 3 is given in Fig. 27 [9]. The derivations for Z_{12}, Z_{13}, and Z_{23} are given in (A.1)–(A.4). The impedances

TABLE VII
TURN-ON AND OFF TIMES OF THE SWITCHES

	Turn-ON time	Turn-OFF time
$S_{1,1}$	$\frac{(1-d_1)}{4f_s}+t_{d1}$	$\frac{(3-d_1)}{4f_s}$
$S_{1,2}$	$\frac{(3-d_1)}{4f_s}+t_{d1}$	$\frac{(1-d_1)}{4f_s}$
$S_{1,3}$	$\frac{(1+d_1)}{4f_s}+t_{d1}$	$\frac{(3+d_1)}{4f_s}$
$S_{1,4}$	$\frac{(3+d_1)}{4f_s}+t_{d1}$	$\frac{(1+d_1)}{4f_s}$
$S_{2,1}$	$\frac{\varphi_{12}}{2\pi f_s}+\frac{(1-d_2)}{4f_s}+t_{d2}$	$\frac{\varphi_{12}}{2\pi f_s}+\frac{(3-d_2)}{4f_s}$
$S_{2,2}$	$\frac{\varphi_{12}}{2\pi f_s}+\frac{(3-d_2)}{4f_s}+t_{d2}$	$\frac{\varphi_{12}}{2\pi f_s}+\frac{(1-d_2)}{4f_s}$
$S_{2,3}$	$\frac{\varphi_{12}}{2\pi f_s}+\frac{(1+d_2)}{4f_s}+t_{d2}$	$\frac{\varphi_{12}}{2\pi f_s}+\frac{(3+d_2)}{4f_s}$
$S_{2,4}$	$\frac{\varphi_{12}}{2\pi f_s}+\frac{(3+d_2)}{4f_s}+t_{d2}$	$\frac{\varphi_{12}}{2\pi f_s}+\frac{(1+d_2)}{4f_s}$
$S_{3,1}$	$\frac{\varphi_{13}}{2\pi f_s}+\frac{(1-d_2)}{4f_s}+t_{d3}$	$\frac{\varphi_{13}}{2\pi f_s}+\frac{(3-d_2)}{4f_s}$
$S_{3,2}$	$\frac{\varphi_{13}}{2\pi f_s}+\frac{(3-d_2)}{4f_s}+t_{d3}$	$\frac{\varphi_{13}}{2\pi f_s}+\frac{(1-d_2)}{4f_s}$
$S_{3,3}$	$\frac{\varphi_{13}}{2\pi f_s}+\frac{(1+d_2)}{4f_s}+t_{d3}$	$\frac{\varphi_{13}}{2\pi f_s}+\frac{(3+d_2)}{4f_s}$
$S_{3,4}$	$\frac{\varphi_{13}}{2\pi f_s}+\frac{(3+d_2)}{4f_s}+t_{d3}$	$\frac{\varphi_{13}}{2\pi f_s}+\frac{(1+d_2)}{4f_s}$

Z_1, Z_2, and Z_3 include parasitic resistances, resonant inductors, resonant capacitors, and leakage inductance of ports 1–3, respectively. Z_m is the impedance due to the magnetizing inductance

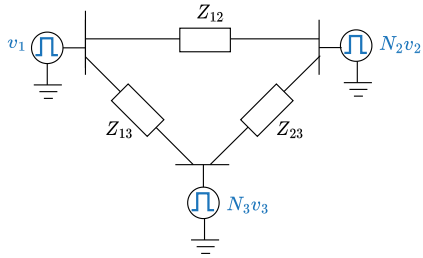


Fig. 27. Equivalent delta network of the TPRC referred to port 1.

$$Z=\frac{1}{Z_1}+\frac{1}{N_2^2Z_2}+\frac{1}{N_3^2Z_3}+\frac{1}{Z_m} \tag{A.1}$$

$$Z_{12}=N_2^2Z_1Z_2Z \tag{A.2}$$

$$Z_{13}=N_3^2Z_1Z_3Z \tag{A.3}$$

$$Z_{23}=N_2^2N_3^2Z_2Z_3Z. \tag{A.4}$$

$$\begin{aligned}I_{1,k}(s)=&\left[4C_1\,s\omega\sin\left(\frac{\pi k}{2}\right)\left\{V_1\sin\left(\frac{\pi d_1\,k}{2}\right)\left[N_2^2(C_2\,s(L_2s+R_2)+1)(N_3^2(L_3s+R_3)+L_ms)\right.\right.\right.\\&+C_2L_mN_3^2\,s^2(L_3s+R_3)\left.\right]+L_mN_2N_3\left[-C_2N_3\,sV_2\sin\left(\frac{\pi d_2\,k}{2}\right)(L_3s+R_3)\Big(s\cos\big(k\varphi_{12}\big)\right.\\&\left.\left.+k\omega\sin\big(k\varphi_{12}\big)\Big)-N_2V_3\sin\left(\frac{\pi d_3\,k}{2}\right)(C_2s(L_2s+R_2)+1)\Big(s\cos\big(k\varphi_{13}\big)+k\omega\sin\big(k\varphi_{13}\big)\Big)\right]\right\}\Bigg]\Bigg/\\&\left[\pi(k^2\omega^2+s^2)\Big\{N_2^2(C_2\,s(L_2s+R_2)+1)(N_3^2(L_3s+R_3)(C_1\,s(s(L_1+L_m)+R_1)+1)\right.\\&\left.+L_ms(C_1\,s(L_1s+R_1)+1))+C_2L_mN_3^2\,s^2(L_3s+R_3)(C_1\,s(L_1s+R_1)+1)\Big\}\right]\end{aligned} \tag{A.5}$$

$$\begin{aligned}I_{2,k}(s)=&-\left[4C_2\omega\sin\left(\frac{\pi k}{2}\right)\left\{-C_1L_mN_3^2\,s^3V_1\sin\left(\frac{\pi d_1\,k}{2}\right)(L_3s+R_3)+N_2V_2\sin\left(\frac{\pi d_2\,k}{2}\right)\right.\right.\\&(s\cos(k\varphi_{12})+k\omega\sin(k\varphi_{12}))\Big(N_3^2(L_3s+R_3)(C_1s(s(L_1+L_m)+R_1)+1)+L_ms(C_1s(L_1s+R_1)+1)\Big)\\&\left.\left.-L_mN_3sV_3\sin\left(\frac{\pi d_3\,k}{2}\right)(C_1s(L_1s+R_1)+1)(s\cos(k\varphi_{13})+k\omega\sin(k\varphi_{13}))\right\}\right]\Bigg/\\&\left[\pi(k^2\omega^2+s^2)\Big\{N_2^2(C_2\,s(L_2s+R_2)+1)(N_3^2(L_3s+R_3)(C_1\,s(s(L_1+L_m)+R_1)+1)\right.\\&\left.+L_ms(C_1\,s(L_1s+R_1)+1))+C_2L_mN_3^2\,s^2(L_3s+R_3)(C_1\,s(L_1s+R_1)+1)\Big\}\right]\end{aligned} \tag{A.6}$$

$$\begin{aligned}I_{3,k}(s)=&\left[2\omega\sin\left(\frac{\pi k}{2}\right)\left\{2L_mN_2\,s^2\left[C_1N_2\,sV_1\sin\left(\frac{\pi d_1\,k}{2}\right)(C_2\,s(L_2s+R_2)+1)+C_2V_2\sin\left(\frac{\pi d_2\,k}{2}\right)\right.\right.\right.\\&(C_1\,s(L_1s+R_1)+1)\Big(s\cos\big(k\varphi_{12}\big)+k\omega\sin\big(k\varphi_{12}\big)\Big)\Big]-2N_3V_3\sin\left(\frac{\pi d_3\,k}{2}\right)\Big(s\cos\big(k\varphi_{13}\big)\\&\left.\left.\left.+k\omega\sin\big(k\varphi_{13}\big)\Big)\Big[N_2^2(C_2\,s(L_2s+R_2)+1)(C_1\,s(s(L_1+L_m)+R_1)+1)+C_2L_ms^2(C_1\,s(L_1s+R_1)+1)\Big]\right\}\right]\Bigg/\\&\left[\pi s(k^2\omega^2+s^2)\Big\{N_2^2(C_2\,s(L_2s+R_2)+1)(N_3^2(L_3s+R_3)(C_1\,s(s(L_1+L_m)+R_1)+1)\right.\\&\left.+L_ms(C_1\,s(L_1s+R_1)+1))+C_2L_mN_3^2\,s^2(L_3s+R_3)(C_1\,s(L_1s+R_1)+1)\Big\}\right].\end{aligned} \tag{A.7}$$

C. Laplace Domain Functions for AC Currents

The Laplace domain functions of the ac currents of the three ports, $I_{1,k}(s)$, $I_{2,k}(s)$, and $I_{3,k}(s)$ are given in (A.5), (A.6), and (A.7) shown at the bottom of the previous page, respectively.

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