Letters

Modular Multilevel Converters With Three-Active-Switch Symmetrical-Half-Bridge Submodules and Parallel Connectivity

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***Abstract*—Modular multilevel converters (MMCs) enjoy growing popularity primarily due to modularity and scalability, but their applications are still constrained by the complexity of hardware and control. MMCs with symmetrical-half-bridge (SHB) submodules can achieve bipolar operation via the simplest structure and reduced cost. However, the imbalance of submodule capacitor voltages remains as a challenge. As a solution, this letter proposes a novel MMC with three-active-switch SHB (3AS-SHB) submodules, which benefits from simple structure and parallel connectivity. Through parallel connection of capacitors among submodules, the proposed MMC allows sensorless voltage balancing, and hence the removal of many voltage sensors, thereby reducing both hardware and control complexity as well as lowering the system cost. Moreover, inherent voltage balancing avoids overmodulation and output waveform distortion. To achieve parallel connectivity, we propose a novel modulation strategy to generate complementary driving signals with adjustable double-edge deadbands. Finally, simulations and experiments validate the effectiveness of the proposed MMC and voltage balance scheme.**

***Index Terms*—Modular multilevel converter (MMC), modulation, sensorless voltage balance, submodule parallelization.**

I. Introduction

COMPARED with two-level converters, multilevel converters offer improved power quality, smaller passive filters, and higher voltage-stress capacity even with low-voltage semiconductors [1]. Among multilevel converters, MMCs stand out owing to their modularity and scalability [2], [3], [4], [5]. However, MMCs still suffer from the complexity associated with both circuit hardware and control software due to the large quantity of active switches and peripheral components, particularly in high-voltage applications where numerous submodules are used. Therefore, the interests of simpler submodules are ongoing, as simpler submodules can translate into lower complexity and cost [6], [7].

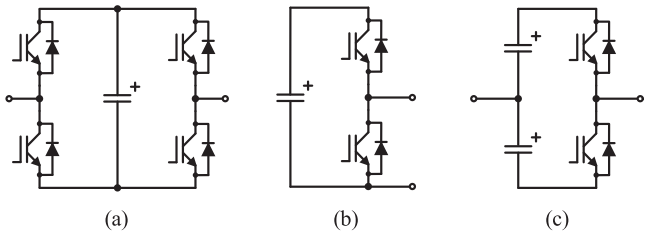

Fig. 1. Schematic diagrams of fundamental MMC submodules, including (a) H-bridge, (b) asymmetrical half-bridge, and (c) symmetrical half-bridge.

As for submodules, two popular options are H-bridge and asymmetrical half-bridge submodules, as shown in Fig. 1(a) and (b), respectively [8]. In contrast, asymmetrical half-bridge submodules enjoy fewer switches, lower costs, and lower conduction losses. Nevertheless, H-bridge submodules benefit from bipolar outputs and better fault performance. Notably, symmetrical-half-bridge (SHB) modules depicted in Fig. 1(c) possess the merit of both simplicity and bipolar outputs, making themselves suitable for four-quadrant operation [9]. Therefore, MMCs with SHB submodules benefit from the simplest structure and reduced cost, but the imbalance of submodule capacitor voltages persists as a challenge [10], [11].

In addition, MMCs with serial and parallel connectivity (MMSPC) have been invented and popular, which introduced switched-capacitor behaviors to conventional MMCs [4]. By submodule parallelization, they can reduce voltage ripples due to the increased equivalent capacitance and equalize submodule capacitor voltages in a sensorless fashion [11]. They allow the removal of voltage sensors and the associated controllers, which can translate into significant improvements in system complexity, cost, and reliability. Notably, almost all existing submodules for MMSPCs are derived from the three aforementioned fundamental submodules. They employ additional active switches and their drivers to implement parallel operation, leading to additional complexity [8].

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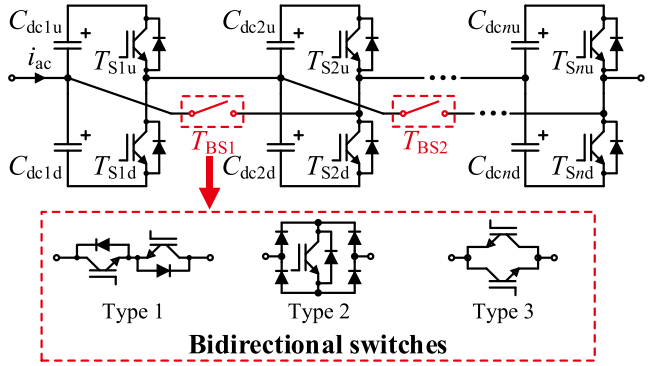

Fig. 2. Schematic diagrams of the proposed MMC with 3AS-SHB submodules and the available types of bidirectional switches.

This letter proposes a novel MMC with three-active-switch SHB (3AS-SHB) submodules, and its benefits are listed as follows.

1) Achieve sensorless voltage balancing among submodules with a simpler structure.
2) Enable parallel connectivity of submodules, which offers a sensorless fashion to balance capacitor voltages with reduced ripples and the removal of almost all voltage sensors.
3) Allow a novel yet straightforward modulation strategy that implements the exclusive OR (XOR) relationship of gate signals with adjustable double-edge deadbands to drive the additional bidirectional switch.

II. Fundamentals of the Proposed MMC With 3AS-SHB Submodules

A. Schematic Diagram

The fundamental properties of MMCs depend on their submodules and module connections. For simplification, the properties associated with the submodules can be evaluated by one arm, which is also a cascaded-bridge converter. Fig. 2 illustrates the schematic diagram of cascaded-bridge converters or MMCs with 3AS-SHB submodules. Each 3AS-SHB submodule is composed of $C_{\mathrm{dc}iu}$, $C_{\mathrm{dc}id}$, $T_{\mathrm{S}iu}$, $T_{\mathrm{S}id}$, and $T_{\mathrm{BS}i}$. We can obtain the 3AS-SHB submodule by adding a bidirectional switch T_{BS} into the conventional SHB submodule. The three commonly used types of bidirectional switches shown in Fig. 2 can be employed in the proposed submodules to enable bidirectional power flow. Notably, $T_{\mathrm{BS}n}$ affiliated with the terminal submodule can be removed for simplification.

B. Operating Modes

As for the proposed MMC with 3AS-SHB submodules, $T_{\mathrm{S}iu}$ and $T_{\mathrm{S}id}$ inherit the operation of the upper and lower switches of conventional SHB submodules, while the switching of $T_{\mathrm{BS}i}$ depends on the operation of its related and subsequent submodules. Taking two adjacent submodules as an example, Fig. 3 details the four operating modes of these switches when the direction of the current is assigned. To simplify the analysis, the ON-state voltage drops of semiconductor switches and equivalent series resistors (ESRs) of capacitors are ignored. As depicted in Fig. 3(a), when both $T_{\mathrm{s}iu}$ and $T_{\mathrm{s}(i+1)\mathrm{u}}$ turn ON, $T_{\mathrm{BS}i}$ must be set to OFF to prevent short circuit and circulating currents. In this Mode 1, $C_{\mathrm{dc}iu}$ and $C_{\mathrm{dc}(i+1)\mathrm{u}}$ are connected in series, and the output voltage across the a and b terminals is the sum of the voltages across the capacitors $C_{\mathrm{dc}iu}$ and $C_{\mathrm{dc}(i+1)\mathrm{u}}$, i.e., $v_{\mathrm{ba}} = v_{\mathrm{dc}iu} + v_{\mathrm{dc}(i+1)\mathrm{u}}$. In Mode 2, we set $T_{\mathrm{BS}i}$ to ON with $T_{\mathrm{s}iu}$ turning ON and $T_{\mathrm{s}(i+1)\mathrm{d}}$ turning ON, resulting in the parallel connection of $C_{\mathrm{dc}iu}$ and $C_{\mathrm{dc}(i+1)\mathrm{d}}$, as demonstrated in Fig. 3(b). This parallelization clears the voltage difference between $v_{\mathrm{dc}iu}$ and $v_{\mathrm{dc}(i+1)\mathrm{d}}$, making $v_{\mathrm{dc}iu} = v_{\mathrm{dc}(i+1)\mathrm{d}}$. Fig. 3(c) shows Mode 3, where both $T_{\mathrm{s}id}$ and $T_{\mathrm{s}(i+1)\mathrm{d}}$ turn ON, then $T_{\mathrm{BS}i}$ turns OFF, resulting in $v_{\mathrm{ba}} = -[v_{\mathrm{dc}id} + v_{\mathrm{dc}(i+1)\mathrm{d}}]$. Mode 4 is characterized by the turning ON of $T_{\mathrm{s}id}$ and turning ON of $T_{\mathrm{s}(i+1)\mathrm{u}}$, where $T_{\mathrm{BS}i}$ should turn ON, resulting in $v_{\mathrm{dc}id} = v_{\mathrm{dc}(i+1)\mathrm{u}}$, as shown in Fig. 3(d). When the direction of the current reverses, the output voltage remains unchanged. Notably, the sudden parallelization of two voltage sources (such as capacitors) with different voltage levels is not allowed according

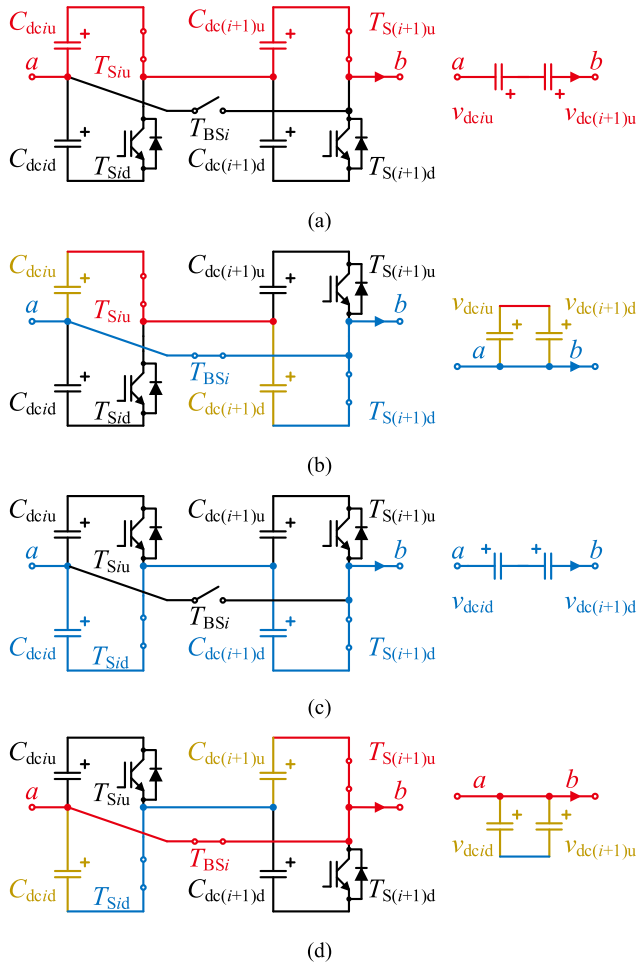

Fig. 3. Operating modes of the proposed MMC with 3AS-SHB submodules, including (a) Mode 1, (b) Mode 2, (c) Mode 3, and (d) Mode 4.

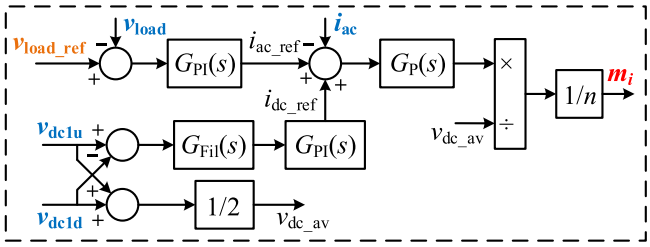

Fig. 4. Control block diagram of the proposed MMC with 3AS-SHB submodules.

to the circuit theory. However, capacitor ESRs, line inductors, and voltage drops of active switches as well as diodes attenuate current spikes in practice [12], [13], [14].

In each switching period, T_{siu} and T_{sid} switch ON and OFF only once, which implies that the four modes mentioned above occur in sequence. Without considering switching ripples, we can derive the following equations through mathematical induction:

$$\begin{aligned} v_{\mathrm{dc1u}} &= v_{\mathrm{dc2d}} = v_{\mathrm{dc3u}} \cdots = v_{\mathrm{dc}(2k+1)\mathrm{u}} = v_{\mathrm{dc}(2k+2)\mathrm{d}} \\ v_{\mathrm{dc1d}} &= v_{\mathrm{dc2u}} = v_{\mathrm{dc3d}} \cdots = v_{\mathrm{dc}(2k+1)\mathrm{d}} = v_{\mathrm{dc}(2k+2)\mathrm{u}}. \end{aligned} \tag{1}$$

From (1), it can be inferred that we only need to ensure the balance of $v_{\mathrm{dc}iu}$ and $v_{\mathrm{dc}id}$, and then the capacitor voltages of the remaining submodules can be equalized, following the domino effect. It is worth noting that the balance of $v_{\mathrm{dc}iu}$ and $v_{\mathrm{dc}id}$ can easily be achieved by injecting a dc component into the ac current reference [15]. Therefore, we can obtain a simple control block diagram of MMCs with 3AS-SHB submodules, as displayed in Fig. 4. $G_{\mathrm{PI}}(s)$, $G_{\mathrm{P}}(s)$, and $G_{\mathrm{Fil}}(s)$ stand for the transfer functions of proportional integral controllers, proportional controller, and notch filter tuned at the fundamental frequency, respectively.

III. Proposed Modulation Strategy for MMCs With 3AS-SHB Submodules

Fig. 5 demonstrates the proposed modulation scheme, where the carrier signals corresponding to two adjacent submodules, i.e., c_i and $c_{(i+1)}$, are shifted by θ_{n} to eliminate switching harmonics, where $\theta_{\mathrm{n}} = 2\pi/n$, and n stands for the number of submodules. The modulation signal m_i comes from the controller in Fig. 4. After being modulated, the gate signal g_i (i.e., $g_{\mathrm{TS}iu}$) drives the corresponding upper switch T_{siu}, while its complimentary signal $g_{\mathrm{TS}id}$ drives the lower switch T_{sid}. To implement the afore-mentioned operating modes, g_{XOR}, the XOR signal of the gate signals from two adjacent submodules (i.e., g_i and $g_{(i+1)}$) drives the bidirectional switch $T_{\mathrm{BS}i}$.

In practice, it is crucial to avoid not only the simultaneous conduction of the upper and lower switches but also the upper/lower switches of adjacent submodules and the additional switch. Hence, deadbands are indispensable.

Normally, we create the deadbands of complimentary signals by delaying the rising edges of the upper and lower signals. However, the creation of XOR signal needs special treatment, which necessitates both a delayed rising edge and an advanced falling edge. Nonetheless, the signal cannot be advanced due

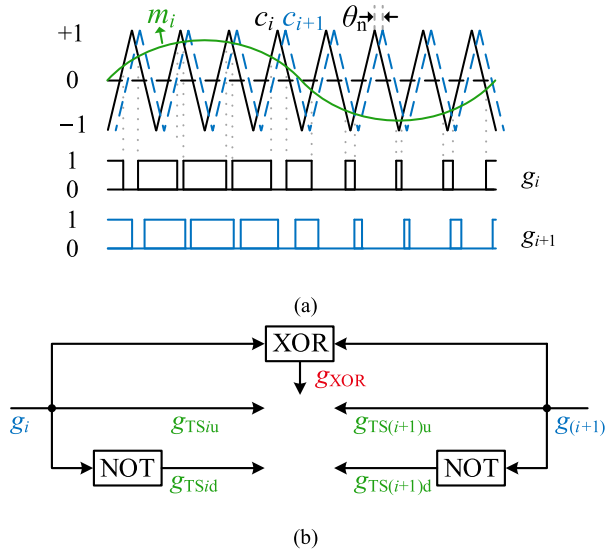

Fig. 5. Proposed modulation waveforms and logics for MMCs with 3AS-SHB submodules with (a) modulation waveforms and (b) modulation logics.

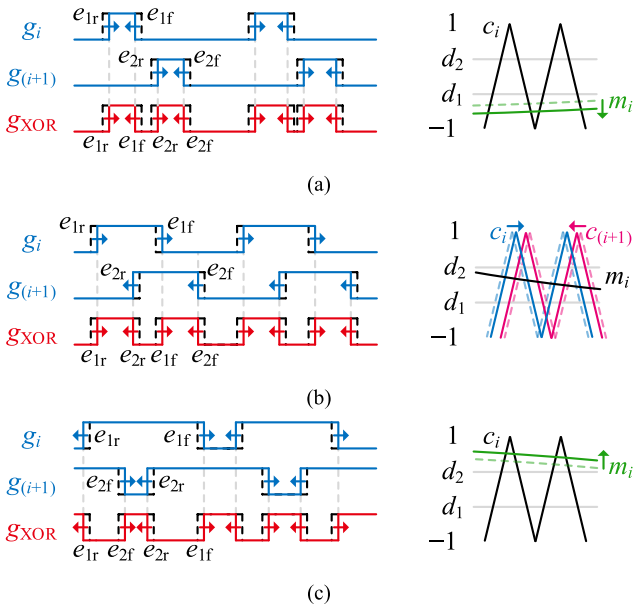

Fig. 6. Schematics of the proposed strategy to generate XOR signals with double-edge deadbands for (a) Case 1, (b) Case 2, and (c) Case 3.

to causality. Therefore, deadbands should be created during the formulation of the g_{XOR} signal. In Fig. 5, g_i, $g_{(i+1)}$, g_{XOR}, c_i, and m_i represent the gate signals of the ith, the $(i+1)$th, the XOR, the carrier, and the modulation signal, respectively.

Referring to Fig. 5, we find that g_i and $g_{(i+1)}$ are identical except for a shifted phase angle θ_{n}. As consequence, g_{XOR} features two pulses in each switching period and can be classified into three cases according to the value of m_i, as shown in Fig. 6 and detailed as follows.

Fig. 6(a) shows Case 1, where $-1 < m_i \le d_1$ and $d_1 = -1 + 2/n$. In this case, the rising and falling edges of the first g_{XOR} pulse are triggered by the rising and falling edges of g_i, i.e., $e_{1\mathrm{r}}$

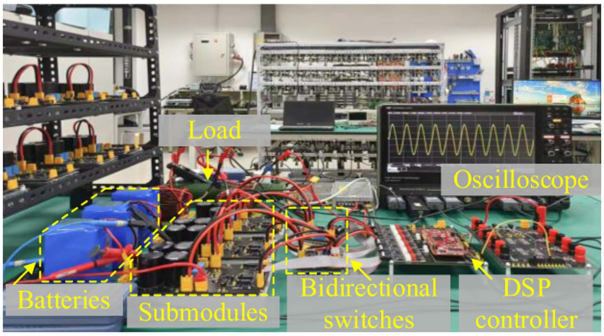

Fig. 7. Photograph of the experimental setup.

and e_{1f}, respectively. In addition, the rising and falling edges of the second g_{XOR} pulse are triggered by the rising and falling edges of $g_{(i+1)}$, i.e., e_{2r} and e_{2f}, respectively. Therefore, we can move m_i downward so that g_i and $g_{(i+1)}$ both get narrower, thus creating the deadbands of g_{XOR}. The concrete value for the downward movement of m_i can be calculated based on the switching period and desired deadbands through similar triangle principle.

Fig. 6(b) presents Case 2, where $d_1 < m_i \leq d_2$ and $d_2 = 1 - 2/n$. In this case, the rising edge of the first g_{XOR} pulse is triggered by the rising edge of g_i, and the falling edge is triggered by the rising edge of $g_{(i+1)}$. The rising edge of the second g_{XOR} pulse is triggered by the falling edge of g_i, and the falling edge is triggered by the falling edge of $g_{(i+1)}$. Therefore, we can delay the phase of c_i and advance the phase of $c_{(i+1)}$ to create the deadbands of g_{XOR}. The concrete values for the operation of c_i and $c_{(i+1)}$ can be calculated based on the switching period and desired deadbands through similar triangle principle.

Fig. 6(c) demonstrates Case 3, where $d_2 < m_i < 1$. In this case, the rising edge of the first g_{XOR} pulse is triggered by the falling edge of $g_{(i+1)}$, and the falling edge is triggered by the rising edge of $g_{(i+1)}$. The rising edge of the second g_{XOR} pulse is triggered by the falling edge of g_i, and the falling edge is triggered by the rising edge of g_i. On the contrary to Case 1, we can move m_i upward so that g_i and $g_{(i+1)}$ both get wider, thereby creating the deadbands of g_{XOR}. The concrete value for the upward movement of m_i can be calculated based on the switching period and desired deadbands through similar triangle principle.

Notably, the proposed modulation strategy generates deadbands from existing signals without additional hardware complexity. Besides, some other existing modulation methods are applicable to the proposed MMC with 3AS-SHB submodules, such as the nearest level modulation.

IV. Simulation and Experimental Results

Fig. 7 visualizes the experimental setup, which includes an oscilloscope (WaveRunner 8000HD: 2 GHz, eight channels), three 3AS-SHB submodules designed as Type 1 with IGBTs (IKW40N120CS6: 1200 V, 40 A) and their drivers (IR2214), batteries (polymer lithium battery, 12 V, 25 Ah), aluminum electrolytic capacitors (ECS2WBW471M: 450 V, 470 μF), and a control board with digital signal processors (DSP TMS320F28379D: 200 MHz) as well as their peripheral digital logic circuits.

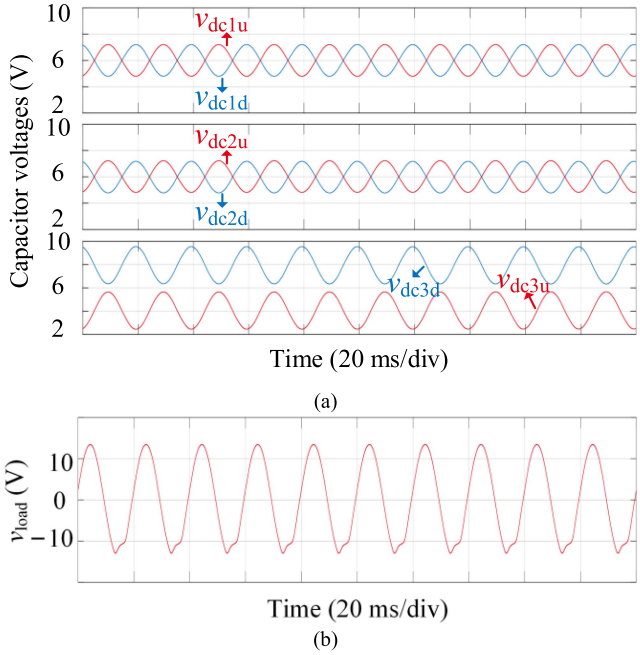

Fig. 8. Steady-state simulation results of the proposed MMC with three 3AS-SHB submodules but without the submodule parallelization strategy for (a) individual capacitor voltages and (b) the load voltage v_{load}.

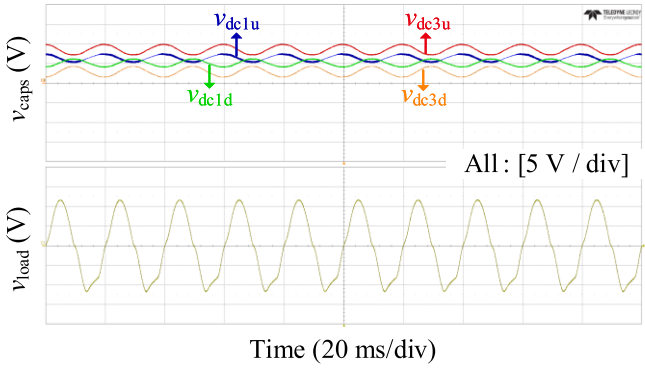

Fig. 9. Steady-state experimental results of the proposed MMC with three 3AS-SHB submodules but without the submodule parallelization strategy.

Figs. 8 and 9 illustrate the steady-state simulation and experimental results of MMCs with 3AS-SHB submodules but without the proposed submodule parallelization strategy, respectively. This case can be regarded as a conventional MMC with SHB submodules. In this case, the capacitance of the upper capacitor in the third submodule is deliberately designed to be halved, i.e., 470 µF, to create an imbalanced condition. As expected, there is a difference between v_{dc3u} and v_{dc3d}. In addition, the imbalance of voltages begets undesirable overmodulation, ultimately resulting in the distortion of the output voltage.

Figs. 10 and 11 present the steady-state simulation and experimental results of the proposed MMC with 3AS-SHB

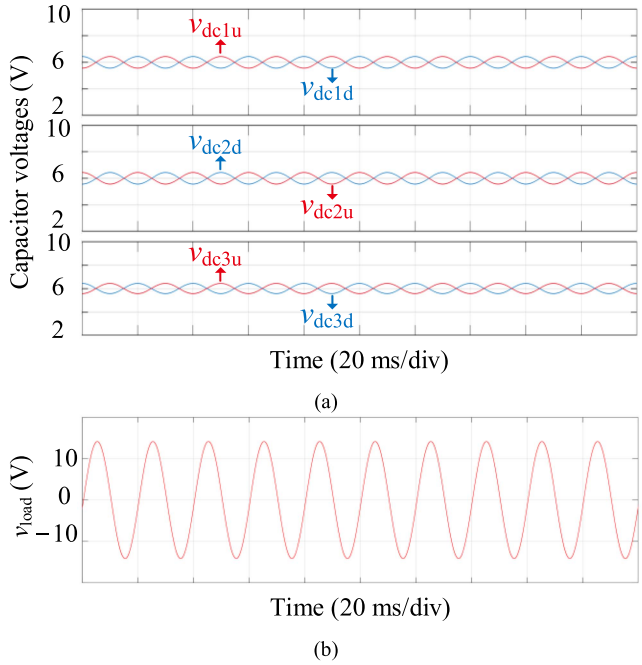

Fig. 10. Steady-state simulation results of the proposed MMC with three 3AS-SHB submodules and the submodule parallelization strategy for (a) individual capacitor voltages and (b) the load voltage v_{load}.

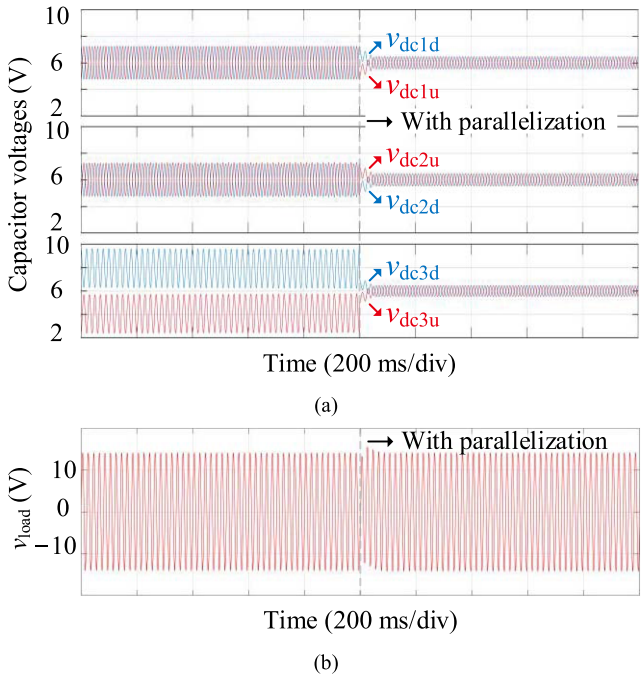

Fig. 12. Dynamic simulation results of the proposed MMC with three 3AS-SHB submodules and the submodule parallelization strategy for (a) individual capacitor voltages and (b) the load voltage v_{load}.

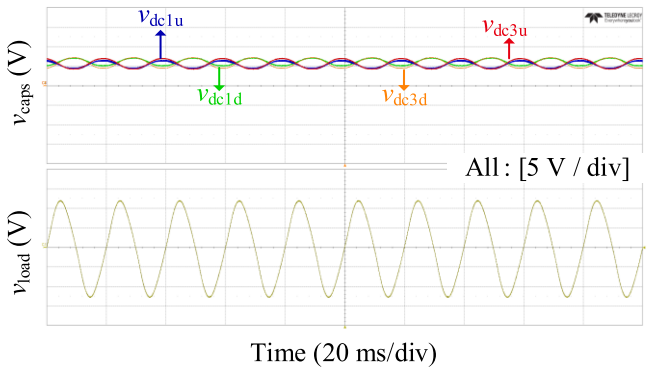

Fig. 11. Steady-state experimental results of the proposed MMC with three 3AS-SHB submodules and the submodule parallelization strategy.

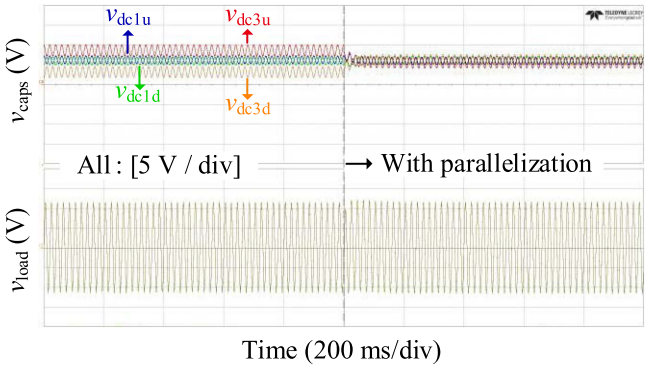

Fig. 13. Dynamic experimental results of the proposed MMC with three 3AS-SHB submodules and the submodule parallelization strategy.

submodules as well as the proposed control and modulation strategy, respectively. The other conditions remain unchanged. Obviously, all the capacitor voltages are balanced with reduced ripples, and the overmodulation issue has been eliminated.

Figs. 12 and 13 present the dynamic behaviors of individual capacitor voltages and the load voltage with the proposed voltage balancing strategy through submodule parallelization, respectively. It is evident that the results regarding the dynamic condition validate the effectiveness of the proposed MMC and voltage balancing scheme as well.

Conclusively, simulation and experimental results agree well with the theoretical analysis.

V. Conclusion

This letter proposes a novel MMC with 3AS-SHB submodules, which features a simple structure and can achieve sensorless balancing of capacitor voltages through a hardware-based strategy of submodule parallelization, leading to a significant reduction of the number of active switches and their peripheral circuits, as well as sensors. In addition, a novel modulation strategy is proposed to implement the XOR relationship of the driving signals of subsequent submodules and generate the driving signal of the additional switch. Simulation and experimental results validate the effectiveness of the proposed MMC and voltage balancing scheme.

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