Load-Independent Class-E Inverter With Dual Quasi-Constant Outputs

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***Abstract*—A novel class-E inverter topology that exhibits load-independent characteristics is presented in this article. Distinguished from the conventional class-E inverter, which is limited to powering a single load, the proposed design boasts dual outputs with only one power switch thanks to its series and parallel resonant cavities. Targeting multioutput systems, the proposed topology reduces the need for multiple power switches and passive components compared to utilizing separate class-E circuits, resulting in a more compact overall design, and enhancing practicality. A comprehensive modeling and analysis process is given, revealing that zero voltage switching, as well as a quasi-constant load current output and a quasi-constant load voltage output, can be achieved simultaneously within a wide operating range through proper resonant parameters design. An experimental prototype is fabricated and tested at the switching frequency of 1 MHz. The measured voltage variation of the quasi-constant voltage output and the measured current variation of the quasi-constant current output remain within 18%. The maximum system efficiency reaches 92.6%.**

***Index Terms*—Class-e inverter, dual outputs, load-independent, quasi-constant current, quasi-constant voltage, zero voltage switching.**

I. Introduction

HIGH operating frequency is advantageous in reducing the size of passive elements in power electronic circuits, making it a continuously pursued research hotspot [1], [2]. However, high switching loss poses a significant challenge that restricts the potential increase in switching frequency. To address this issue and enable higher switching frequencies for power electronic switches, the realization of soft switching techniques become imperative [3].

The class-E inverter can transform a dc power supply into an ac power output with only one power switch ON the low side [4], [5]. Due to the inherent resonant characteristic of the class-E inverter, the shunt capacitance of the power switch undergoes periodical discharge prior to the power switch's activation. Thus, zero voltage switching (ZVS) can be achieved and the switching loss can be greatly reduced. The classical class-E inverter features a choke inductor with a theoretically infinite impedance at the input so that the input current can be treated to have a constant dc value [4]. However, the operating range of the circuit is limited. Deviation from this nominal load leads to system efficiency degradation and output power variation. Consequently, impedance matching networks [6] or additional power converters [7] must be incorporated into the traditional class-E inverter to maintain a stable output, which inevitably complicates the system and introduces additional power losses. Thus, it is not ideally suited for applications like the wireless power transfer (WPT) system [8], where the equivalent load impedance undergoes significant variations during the battery charging process [9].

To address this issue, a load-independent class-E inverter was proposed in [10]. The circuit topology in [10] is exactly the same as the conventional one in [4], with the key difference being the substitution of the input choke inductor with a finite inductor, which participates in the resonant process of the circuit. The output series resonant circuit created a constant voltage (CV) output. ZVS of the metal-oxide-semiconductor field-effect transistor (MOSFET) was analyzed to broaden the operating range. The CV output characteristic of the proposed class-E inverter in [10] eliminated the need for complex closed-loop control to stabilize the output voltage, which greatly enhances its practicability in WPT applications. Subsequently, various load-independent CV inverter topologies emerged, including class-E^{-1} in [11] and class-ϕ_2 in [12], among others. In a WPT system, sometimes the transmitting coil is preferred to be excited with a constant current (CC) power source instead of a CV one. For example, the *LCC* compensation network was used to generate a CC inside the transmitting coil, so that the receiving side can obtain a CV source if compensated with a series-connected capacitor [13] or multiple receivers can be powered simultaneously without affecting each other if neglecting the cross magnetic coupling between the receiving coils [14]. In this case, CV inverters are not suitable anymore, and inverters capable of delivering a CC output are necessary. Currently, there are various load-independent CC inverters such as CC class-E in [15], CC class-E^{-1} in [16], and class-EF in [17]. Some representative single-switch high-frequency load-independent inverters derived from class-E are shown in Table I, which highlights the passive components utilized in each inverter design along

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TABLE I
COMPARISONS OF SINGLE-SWITCH HIGH-FREQUENCY LOAD-INDEPENDENT RESONANT INVERTERS

Research	Topology	Passive Components	Switching Condition	Output
[10]	Class-E	2*L*+2*C*	ZVS	CV
[15]				CC
[11]	Class-E^{-1}	3*L*+2*C*	ZCS	CV
[16]				CC
[18]		3*L*+3*C*	ZVS	CC
[12]	Class-ϕ_2	3*L*+3*C*	ZVS	CV
[17]	Class-EF	3*L*+3*C*	ZVS	CC
This work	Class-E	3*L*+3*C*	ZVS	CC and CV

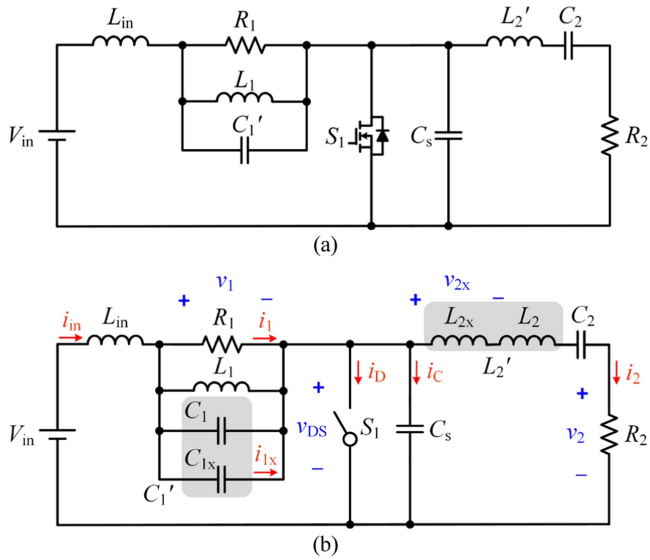

Fig. 1. Circuit diagram of the proposed class-E inverter with dual outputs. (a) Circuit topology. (b) Equivalent circuit for analysis.

with their corresponding switching conditions. The CC class-E in [15], similar to the CV class-E, leverages the second-order resonant characteristics of the class-E circuit to achieve the ZVS of the switch. The only difference between them lies in the design at the output end, while the other parts of the circuit remain identical. The topology of class-E^{-1} in [11] and [16] is the dual form of the class-E topology, exhibiting a mirrored configuration. Due to the need for a dc current source at the input end, an extra choke inductor is typically employed. The topology in [18], based on class-E^{-1}, incorporates a capacitor to facilitate the switching mode transition from zero current switching (ZCS) to ZVS. The topologies in [12] and [17] introduced additional passive components to the class-E structure, offering greater flexibility in circuit design and potentially enabling the achievement of desired operational characteristics. Distinct inverters exhibit unique characteristics, rendering them suitable for a diverse range of applications.

In this article, a novel class-E inverter is proposed, drawing inspiration from both the CC and CV class-E designs. It is distinguished by its dual resonant cavities, consisting of a series resonant cavity and a parallel resonant cavity, with only one power switch. It can be demonstrated that independent operation of the loads in the two resonant cavities can be achieved simultaneously. However, the operational range of the loads is limited. When deviating from this range, there will be mutual interference between the two resonant cavities. The primary challenge in designing such a circuit stems from the interaction between the two resonant cavities. After conducting a thorough analysis, a suitable parameter design method is provided. Then, a quasi-CC can be generated for the parallel resonant output and a quasi-CV can be obtained for the series resonant output while maintaining the ZVS of the MOSFET. The proposed inverter can simultaneously power two loads with different power levels, especially in the WPT application. First, this novel class-E inverter holds great potential in the realm of multiple outputs, seamlessly aligning with the prevailing trend of multiload charging [19], [20]. Second, the inverter's dual-output capabilities, encompassing both CC and CV modes, perfectly fulfill the CC-followed-by-CV charging requirement for batteries, thus presenting significant potential for battery charging applications [21], [22]. Furthermore, this circuit's versatility allows it to be effectively employed in single-output scenarios as well, further enhancing its practicality and applicability.

The rest of this article is organized as follows. In Section II, a comprehensive modeling approach of the proposed load-independent dual-output class-E inverter is presented, serving as a solid foundation for subsequent analysis. Then, the condition to achieve the quasi-CC and CV outputs while maintaining the ZVS of the MOSFET is derived in Section III. The operating range of the proposed class-E inverter is thoroughly analyzed, with a focus on demonstrating the CC and CV properties across varying load variations. Experimental results are presented in Section IV to validate the effectiveness and performance of the proposed load-independent class-E inverter featuring dual outputs. Finally, Section V concludes this article.

II. MODELING OF THE PROPOSED CLASS-E INVERTER

The circuit topology of the proposed class-E inverter with dual quasi-constant outputs is shown in Fig. 1(a), which consists of a dc voltage source V_{in}, three inductors L_{in}, L_1, and L_2', three capacitors C_1', C_s, and C_2, two load resistors R_1 and R_2, and a power MOSFET S_1.

For ease of analysis, the capacitor C_1' can be envisioned as the equivalent of two capacitors (C_1 and C_{1x}) connected in parallel, as depicted in Fig. 1(b). Similarly, the inductor L_2' can be conceptualized as two inductors (L_2 and L_{2x}) connected in series. Different from the existing class-E inverter, the proposed one boasts two outputs, i.e., a parallel resonant output tailored for load R_1 and a series resonant output for load R_2. The current flowing through L_{in} is designated as i_{in}. The voltages across R_1 and R_2 are v_1 and v_2, while the currents flowing through them are i_1 and i_2, respectively. i_{1x} is the current in C_{1x} and v_{2x} is the voltage across L_{2x}. i_D and i_C are the currents flowing through S_1 and C_s. The voltage across S_1 is marked as v_{DS}.

It will be demonstrated later that, through appropriate parameter design, the circuit can attain a quasi-CC for R_1 and a quasi-CV for R_2 within a specified load range while maintaining ZVS for the MOSFET.

A. Assumptions

Before further analysis, some basic assumptions should be made regarding the circuit in Fig. 1(b).

1) The switch is ideal and can be turned ON and OFF instantly. The switching frequency is f, the period is T, and the angular frequency is ω with $\omega = 2\pi f$. The duty cycle of the turning-ON time is D. The switch is ON when $0 \leq \omega t \leq 2\pi D$, and the switch is OFF when $2\pi D \leq \omega t \leq 2\pi$.
2) L_1 and C_1 resonate at the switching frequency f, with the loaded quality factor being defined as

$$Q_1 = \omega C_1 R_1. \tag{1}$$

Q_1 is large enough so that the output voltage v_1 is sinusoidal [15]. Thus, v_1 can be written as

$$v_1(\omega t) = V_1 \sin(\omega t + \alpha) \tag{2}$$

where α is the initial phase of v_1.

3) L_2 and C_2 resonate at the switching frequency f, with the loaded quality factor being defined as

$$Q_2 = \frac{\omega L_2}{R_2}. \tag{3}$$

Q_2 is large enough so that the current i_2 is

$$i_2(\omega t) = I_2 \sin(\omega t + \beta) \tag{4}$$

where β is the initial phase of i_2.

4) Since C_{1x} exhibits capacitive behavior, the current i_{1x} flowing through C_{1x} leads v_1 by 90°, which can be calculated as

$$i_{1x} = I_{1x} \cos(\omega t + \alpha). \tag{5}$$

Similarly, considering L_{2x} is inductive, the voltage v_{2x} across L_{2x} is 90° ahead of i_2, which can be denoted as

$$v_{2x}(\omega t) = V_{2x} \cos(\omega t + \beta). \tag{6}$$

B. Circuit Modeling

Fig. 2 shows the waveforms of the voltages and currents in the circuit shown in Fig. 1(b). When S_1 is ON, the dc voltage source V_{in} charges L_{in}, and the current i_{in} grows. When S_1 is OFF, L_{in} starts releasing energy. In this period, i_D is zero.

Based on assumptions 2) and 3), the parallel resonant cavity is equivalent to a sinusoidal voltage source, and the series resonant cavity can be modeled as a sinusoidal current source, resulting in the equivalent circuit shown in Fig. 3.

According to Kirchhoff's current law, the current i_{in} is

$$i_{in}(\omega t) = i_C(\omega t) + i_D(\omega t) + i_2(\omega t). \tag{7}$$

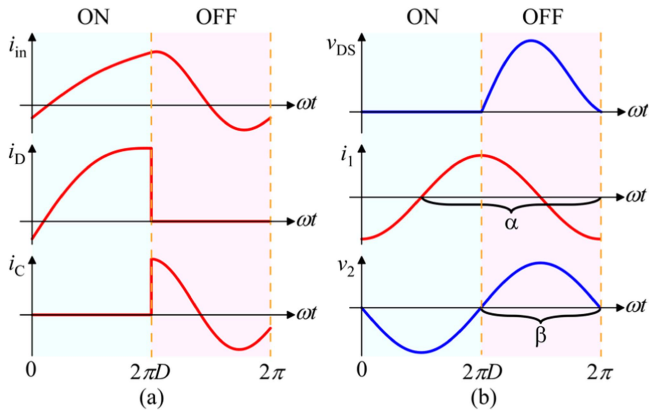

Fig. 2. Current and voltage waveforms of (a) i_{in}, i_D, and i_C. (b) v_{DS}, i_1, and v_2.

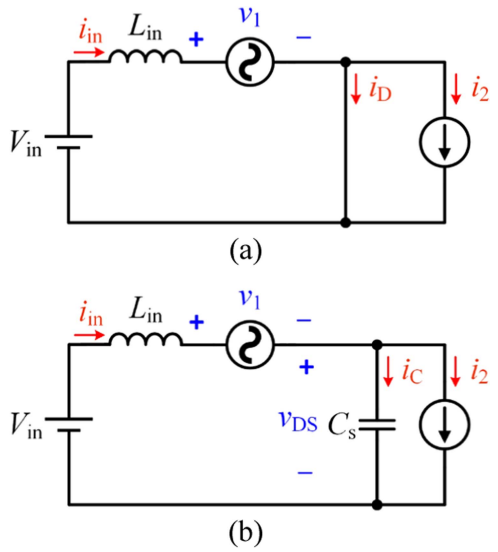

Fig. 3. Equivalent circuit of the proposed class-E inverter under different states. (a) S_1 is ON. (b) S_1 is OFF.

When S_1 is ON, C_s is shorted, so i_C is zero and v_{DS} is zero. The current i_{in} can be calculated as

$$i_{in}(\omega t) = i_{in}(2\pi) + \frac{1}{\omega L_{in}} \int_0^{\omega t} [V_{in} - V_1 \sin(\omega t + \alpha)] d\omega t. \tag{8}$$

When S_1 is OFF, as shown in Fig. 2, the current i_D is zero, the capacitor current i_C is

$$i_C(\omega t) = i_{in}(\omega t) - I_2 \sin(\omega t + \beta). \tag{9}$$

The current i_{in} is

$$i_{in}(\omega t) = i_{in}(2\pi D) + \frac{1}{\omega L_{in}} \int_{2\pi D}^{\omega t} \begin{bmatrix} V_{in} - v_{DS}(\omega t) \\ -V_1 \sin(\omega t + \alpha) \end{bmatrix} d\omega t. \tag{10}$$

The current i_C is also the derivative of v_{DS} as

$$i_C(\omega t) = \omega C_s \frac{dv_{DS}(\omega t)}{d\omega t}. \tag{11}$$

From (9)–(11), (12) is obtained

$$\frac{1}{\omega L_{\text{in}}}\int_{2\pi D}^{\omega t}\left[V_{\text{in}}-v_{\text{DS}}\left(\omega t\right)-V_1\sin\left(\omega t+\alpha\right)\right]d\omega t + i_{\text{in}}\left(2\pi D\right)-I_2\sin\left(\omega t+\beta\right)=\omega C_{\text{s}}\frac{dv_{\text{DS}}\left(\omega t\right)}{d\omega t}. \tag{12}$$

Taking the derivative of both sides of (12) with respect to ωt yields

$$\frac{1}{\omega L_{\text{in}}}\left[V_{\text{in}}-v_{\text{DS}}\left(\omega t\right)-V_1\sin\left(\omega t+\alpha\right)\right] -I_2\cos\left(\omega t+\beta\right)=\omega C_{\text{s}}\frac{d^2v_{\text{DS}}\left(\omega t\right)}{d\left(\omega t\right)^2}. \tag{13}$$

Equation (13) is a second-order linear nonhomogeneous differential equation for v_{DS}, which can be solved to obtain v_{DS} as

$$v_{\text{DS}}\left(\omega t\right)=K_1\cos\left(q\omega t\right)+K_2\sin\left(q\omega t\right)+V_{\text{in}} -\frac{q^2V_1}{q^2-1}\sin\left(\omega t+\alpha\right)-\frac{I_2}{\omega C_{\text{s}}\left(q^2-1\right)}\cos\left(\omega t+\beta\right) \tag{14}$$

where K_1 and K_2 are constants to be determined, and q is defined as

$$q=\frac{1}{\omega\sqrt{L_{\text{in}}C_{\text{s}}}}. \tag{15}$$

To solve K_1 and K_2, two boundary conditions are required. Referring to Fig. 2, v_{DS} is 0 at the instant when S_1 turns OFF

$$v_{\text{DS}}\left(2\pi D\right)=0. \tag{16}$$

Moreover, the average value of v_{DS} is equal to V_{in} because the average voltage across L_{in} must be zero under the steady state

$$V_{\text{in}}=\frac{1}{2\pi}\int_0^{2\pi}v_{\text{DS}}\left(\omega t\right)d\omega t. \tag{17}$$

From (14)–(17), K_1 and K_2 can be obtained, as shown in

$$K_1=\tfrac{1}{2}\csc^2\left[\left(D-1\right)\pi q\right]\left\{\begin{array}{l}\left[\cos\left(2\pi q\right)-\cos\left(2\pi Dq\right)-2\pi Dq\sin\left(2\pi Dq\right)\right]V_{\text{in}}\\ +\frac{q^2\left\{\begin{array}{l}2q\sin\left(\pi D\right)\sin\left(2\pi Dq\right)\sin\left(\pi D+\alpha\right)\\ +\left[\cos\left(2\pi Dq\right)-\cos\left(2\pi q\right)\right]\sin\left(2\pi D+\alpha\right)\end{array}\right\}}{\left(q^2-1\right)}V_1\\ +\frac{\left\{\begin{array}{l}2q\sin\left(\pi D\right)\sin\left(2\pi Dq\right)\cos\left(\pi D+\beta\right)\\ +\left[\cos\left(2\pi Dq\right)-\cos\left(2\pi q\right)\right]\cos\left(2\pi D+\beta\right)\end{array}\right\}}{\omega C_{\text{s}}\left(q^2-1\right)}I_2\end{array}\right\} \tag{18}$$

$$K_2=\tfrac{1}{2}\csc^2\left[\left(D-1\right)\pi q\right]\left\{\begin{array}{l}\left[\sin\left(2\pi q\right)-\sin\left(2\pi Dq\right)+2\pi Dq\cos\left(2\pi Dq\right)\right]V_{\text{in}}\\ -\frac{q^2\left\{\begin{array}{l}2q\sin\left(\pi D\right)\cos\left(2\pi Dq\right)\sin\left(\pi D+\alpha\right)\\ -\left[\sin\left(2\pi Dq\right)-\sin\left(2\pi q\right)\right]\sin\left(2\pi D+\alpha\right)\end{array}\right\}}{\left(q^2-1\right)}V_1\\ -\frac{\left\{\begin{array}{l}2q\sin\left(\pi D\right)\cos\left(2\pi Dq\right)\cos\left(\pi D+\beta\right)\\ +\left[\sin\left(2\pi Dq\right)-\sin\left(2\pi q\right)\right]\cos\left(2\pi D+\beta\right)\end{array}\right\}}{\omega C_{\text{s}}\left(q^2-1\right)}I_2\end{array}\right\}. \tag{19}$$

The expressions for v_{DS} and i_{in} are organized as follows:

$$v_{\text{DS}}\left(\omega t\right)=\left\{\begin{array}{ll}0, & 0\le\omega t\le 2\pi D\\ K_1\cos\left(q\omega t\right)+K_2\sin\left(q\omega t\right) & \\ +V_{\text{in}}-\frac{q^2V_1}{q^2-1}\sin\left(\omega t+\alpha\right)- & 2\pi D\le\omega t\le 2\pi\\ \frac{I_2}{\omega C_{\text{s}}\left(q^2-1\right)}\cos\left(\omega t+\beta\right) & \end{array}\right. \tag{20}$$

$$i_{\text{in}}\left(\omega t\right)=\left\{\begin{array}{ll}\frac{1}{\omega L_{\text{in}}}\left[\begin{array}{l}V_1\cos\left(\omega t+\alpha\right)\\ +V_{\text{in}}\omega t-V_1\cos\alpha\end{array}\right]+i_{\text{in}}\left(2\pi\right), & 0\le\omega t\le 2\pi D\\ \omega C_{\text{s}}\frac{dv_{\text{DS}}\left(\omega t\right)}{d\omega t}+I_2\sin\left(\omega t+\beta\right), & 2\pi D\le\omega t\le 2\pi\end{array}\right. \tag{21}$$

With v_{DS} and i_{in} in (20) and (21), the Fourier decomposition of them can be implemented. The fundamental component of i_{in} can be decomposed into the sine and cosine components, each characterized by a phase angle of α. Similarly, the fundamental component of v_{DS} can be separated into the sine and cosine components with the phase angle of β.

The fundamental sine component of i_{in} is

$$I_1=\frac{1}{\pi}\int_0^{2\pi}i_{\text{in}}\left(\omega t\right)\sin\left(\omega t+\alpha\right)d\omega t=X_1\left(V_1,I_2\right). \tag{22}$$

The fundamental cosine component of i_{in} is

$$I_{1\text{x}}=\frac{1}{\pi}\int_0^{2\pi}i_{\text{in}}\left(\omega t\right)\cos\left(\omega t+\alpha\right)d\omega t=X_2\left(V_1,I_2\right). \tag{23}$$

The fundamental sine component of v_{DS} is

$$V_2=\tfrac{1}{\pi}\textstyle\int_0^{2\pi}v_{\text{DS}}\left(\omega t\right)\sin\left(\omega t+\beta\right)d\omega t=Y_1\left(V_1,I_2\right). \tag{24}$$

The fundamental cosine component of v_{DS} is

$$V_{2\text{x}}=\frac{1}{\pi}\int_0^{2\pi}v_{\text{DS}}\left(\omega t\right)\cos\left(\omega t+\beta\right)d\omega t=Y_2\left(V_1,I_2\right). \tag{25}$$

As can be seen from (22)–(25), I_1, $I_{1\text{x}}$, V_2, and $V_{2\text{x}}$ are all functions of V_1 and I_2. However, their analytical expressions are rather intricate and, therefore, will not be enumerated here due to the paper's length constraint. In this article, since L_1 resonates with C_1 and L_2 resonates with C_2, the sine component of i_{in} flows into R_1 while i_{in}'s cosine component is filtered out by $C_{1\text{x}}$, which will be discussed later. Similarly, the sine component of v_{DS} is designed to be the voltage across R_2, while v_{DS}'s cosine component is located across $L_{2\text{x}}$.

With the above equations, the proposed class-E inverter with dual outputs can be comprehensively characterized. Then, a further analysis of the circuit will be explored in the subsequent section.

III. System Analysis

In a practical application, it is generally preferred to have a constant load output that remains unaffected by the changes in load power, as discussed in Section I. The conditions to achieve the quasi-CC and quasi-CV outputs while ensuring ZVS of the MOSFET are discussed in this section. The working range of the proposed circuit is also derived. Mutual interactions between the two loads are analyzed. Then, an optimal parameter design

approach is introduced to ensure a balanced operating range for both loads.

A. Constant Outputs

ZVS is a crucial issue that should be ensured for the MOSFET since the class-E inverter operates under high frequency. Thus, the following condition should be met:

$$v_{\mathrm{DS}}(2\pi) = 0. \tag{26}$$

By simplifying (20) yields

$$v_{\mathrm{DS}}(2\pi) = l_1 V_{\mathrm{in}} + l_2 V_1 + l_3 I_2 \tag{27}$$

where l_1, l_2, and l_3 are coefficients. It means for any combinations of V_{in}, V_1, and I_2, v_{DS} should be zero at the instant when S_1 turns ON. Thus, the following equation should be satisfied:

$$l_1 = l_2 = l_3 = 0. \tag{28}$$

In the proposed class-E inverter, the design target is to obtain a CC output for R_1 and a CV output for R_2. To obtain a CC output for R_1, I_1 should remain constant for any given V_1 and I_2. Thus, the following conditions should be met:

$$\frac{\partial\left[X_1(V_1, I_2)\right]}{\partial V_1} = 0 \tag{29}$$

$$\frac{\partial\left[X_1(V_1, I_2)\right]}{\partial I_2} = 0. \tag{30}$$

In order to obtain a CV output for R_2, V_2 should remain constant for any given V_1 and I_2. Thus, the following conditions should be met:

$$\frac{\partial\left[Y_1(V_1, I_2)\right]}{\partial V_1} = 0 \tag{31}$$

$$\frac{\partial\left[Y_1(V_1, I_2)\right]}{\partial I_2} = 0. \tag{32}$$

Based on (28)–(32), the parameters q, α, and β can be determined once a fixed duty ratio D_{const} is provided. The detailed solving process is outlined in the appendix, and the results of the solution are summarized as follows:

$$\tan\left[\pi\left(D_{\mathrm{const}} - 1\right)q\right] = \pi D_{\mathrm{const}} q \tag{33}$$

$$\alpha = \left(2 - D_{\mathrm{const}}\right)\pi \tag{34}$$

$$\beta = \left(\frac{3}{2} - D_{\mathrm{const}}\right)\pi. \tag{35}$$

The value of q can be obtained by solving (33), the variation of which concerning D_{const} has been drawn in Fig. 4. It can be seen from Fig. 4 that q increases dramatically when D_{const} is greater than 0.7. In this article, D_{const} is designed as 0.5 to achieve a maximum power output capacity $c_{\mathrm{p\cdot max}}$, as discussed in [23]. In this case, q is 1.2915.

Substituting (33)–(35) into (22)–(25) and simplifying yields

$$I_{1\_\mathrm{const}} = mq^2\omega C_{\mathrm{s}} V_{\mathrm{in}} \tag{36}$$

$$I_{1\mathrm{x}\_\mathrm{const}} = (n+1)\,q^2\omega C_{\mathrm{s}} V_{1\_\mathrm{const}} + nI_{2\_\mathrm{const}} \tag{37}$$

$$V_{2\_\mathrm{const}} = mV_{\mathrm{in}} \tag{38}$$

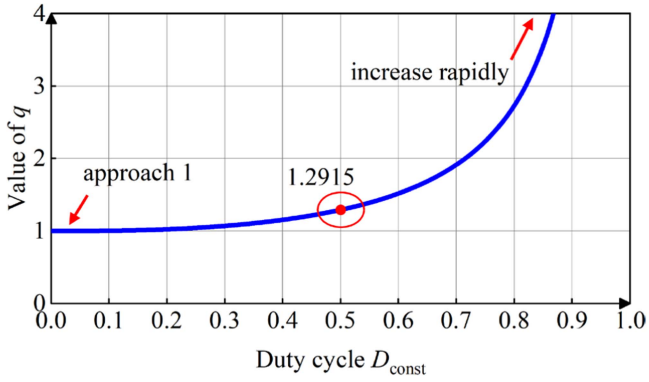

Fig. 4. Solution of q with changes in D_{const}.

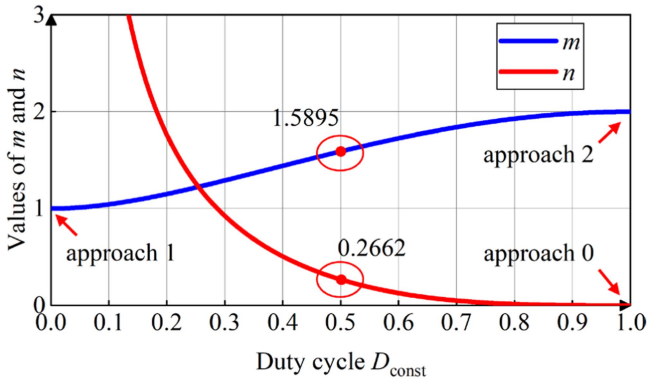

Fig. 5. Variations of m and n with the increasing D_{const}.

$$V_{2\mathrm{x}\_\mathrm{const}} = n\omega L_{\mathrm{in}} I_{2\_\mathrm{const}} + nV_{1\_\mathrm{const}} \tag{39}$$

where the subscript "const" denotes the variables when (33)–(35) are satisfied. For instance, $I_{1\cdot\,\mathrm{const}}$ represents the value of I_1 when the conditions in (33)–(35) are fulfilled.

The parameters m and n in (36)–(39) are functions of D_{const} and q, and their expressions are as follows:

$$m = \frac{2}{\pi}\sin\left(\pi D_{\mathrm{const}}\right) + \frac{2qD_{\mathrm{const}}}{q^2-1}\left\{\begin{array}{l}\sin\left(\pi D_{\mathrm{const}}\right)\cot\left[\pi q\left(D_{\mathrm{const}}-1\right)\right] \\ -q\cos\left(\pi D_{\mathrm{const}}\right)\end{array}\right\} \tag{40}$$

$$n = \frac{q^2\left(D_{\mathrm{const}}-1\right)}{q^2-1} + \frac{q^2}{2\pi\left(q^2-1\right)^2}\left\{\begin{array}{l}4q\cot\left[\pi q\left(D_{\mathrm{const}}-1\right)\right]\sin^2\left(\pi D_{\mathrm{const}}\right) \\ -\left(q^2+1\right)\sin\left(2\pi D_{\mathrm{const}}\right)\end{array}\right\}. \tag{41}$$

When the duty cycle D_{const} is given, the values of m and n can be determined. Fig. 5 shows the curves of m and n changing with D_{const}. As can be seen from Fig. 5, m increases from 1 when D_{const} grows, while n drops rapidly. When D_{const} approaches 1, m approaches 2 and n approaches 0. When D_{const} is 0.5, m equals 1.5895 while n equals 0.2662.

As shown in (36) and (38), I_1 and V_2 are independent of R_1 and R_2. Moreover, based on (37) and (39) the following equations can be obtained:

$$C_{1\mathrm{x}} = \frac{I_{1\mathrm{x}\_\mathrm{const}}}{\omega V_1} = (n+1)\,q^2 C_{\mathrm{s}} + \frac{mnL_{\mathrm{in}}}{R_1 R_2} \tag{42}$$

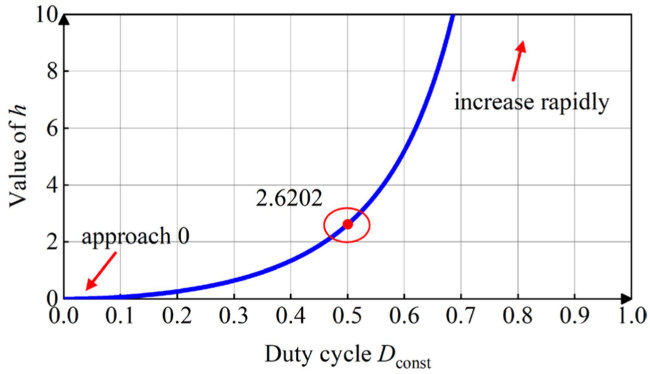

Fig. 6. Curve of h versus the increasing D_{const}.

$$L_{2x} = \frac{V_{2x\_const}}{\omega I_2} = nL_{in} + \frac{nR_1R_2}{\omega L_{in}}. \tag{43}$$

Based on (42) and (43), C_{1x} and L_{2x} can be designed using the following equations:

$$C_{1x} = (n+1)\, q^2 C_s + \frac{mnL_{in}}{k_R} \tag{44}$$

$$L_{2x} = nL_{in} + \frac{nk_R}{\omega L_{in}}. \tag{45}$$

Once a k_R is given, C_{1x} and L_{2x} can be obtained using (44) and (45). However, it can be observed that only when the product of R_1 and R_2 equals the given k_R, the strict load-independent constant outputs can be observed. Any deviation from this optimal load resistance will result in corresponding variations in the output current and voltage. Varying values of k_R exert diverse influences on the system's output. More discussions on the choice of k_R will be given in Section III-B.

According to the above analysis, a solution that satisfies the constant output and ZVS conditions can be obtained. Considering that MOSFET can only withstand unidirectional voltage, as discussed in [24], the circuit needs to meet

$$\left.\frac{dv_{DS}(\omega t)}{d\omega t}\right|_{\omega t = 2\pi} \le 0. \tag{46}$$

Then, (46) can be obtained as

$$m^2 q^2 \omega C_s R_1 + \frac{m^2}{q^2 \omega C_s}\frac{1}{R_2} \le h, \tag{47}$$

where h is the function of D_{const} and q

$$h = 2\pi q^2 {D_{\text{const}}}^2. \tag{48}$$

Fig. 6 depicts the curve of h changing with D_{const}. When D_{const} is 0, h also approaches 0. As D_{const} increases, h monotonically rises. When D_{const} approaches 1, h approaches infinity. Notably, when D_{const} is 0.5, h equals 2.6202.

Based on (47), it can be seen that R_1 has a maximum value $R_{1\max}$ and R_2 has a minimum value $R_{2\min}$. Taking the $R_{1\max}$ and $R_{2\min}$ as the base values, R_1 and R_2 can be normalized as R_{1n} and R_{2n}. Then, (44) and (45) can be rewritten as

$$C_{1x} = \left(\frac{n}{k_{Rn}} + n + 1\right) q^2 C_s \tag{49}$$

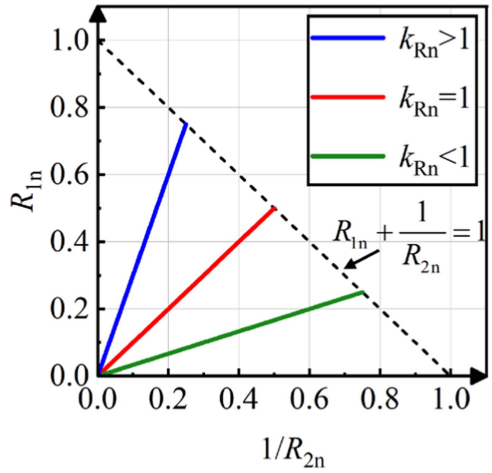

Fig. 7. Load area for ZVS and constant outputs.

$$L_{2x} = nL_{in}\,(k_{Rn} + 1) \tag{50}$$

where

$$k_{Rn} = \frac{k_R}{\omega^2 C_s^2}. \tag{51}$$

If $k_R = R_1R_2$, k_{Rn} is equal to $R_{1n}R_{2n}$. The load resistance needs to meet the two conditions as follows:

$$R_{1n} + \frac{1}{R_{2n}} \le 1 \tag{52}$$

$$R_{1n}R_{2n} = k_{Rn}. \tag{53}$$

The working area that meets (52) and (53) is shown in Fig. 7. The work area also undergoes variations as k_{Rn} changes. The load area for the strict constant output operation is relatively limited. However, the circuit remains capable of achieving ZVS and quasi-constant output when the load varies within a specific range, as discussed below.

B. Discussions of Load Variations

As previously mentioned, the stringent requirements of ZVS, CV, and CC conditions can only be simultaneously fulfilled with the implemented D_{const} when the circuit adheres to conditions (52) and (53). This section delves into the circuit's properties when the load deviates from the constant load area, and explores the practical operating range when the duty cycle D_{const} remains fixed.

When load resistances vary, the ZVS capability of the MOSFET may be compromised, as illustrated in Fig. 8, which depicts four possible scenarios. When v_{DS} reaches zero, the corresponding critical duty cycle is marked as D_{crit} and the switch is ON when $0 \le \omega t \le 2\pi D_{\text{crit}}$ and OFF when $2\pi D_{\text{crit}} \le \omega t \le 2\pi$ theoretically. It is worth noting that D_{crit} represents the duty cycle required to achieve ZVS with varying load resistances, whereas D_{const} denotes the actual duty cycle generated by the controller for the MOSFET to obtain a constant output. Then, the actual turning-ON time of the MOSFET is $\omega t = 2\pi(D_{\text{crit}}\text{-}D_{\text{const}})$. If $D_{\text{crit}} > D_{\text{const}}$, before the switch driver signal arrives, v_{DS} drops to 0, and the body diode of the MOSFET conducts. In this instance, the circuit

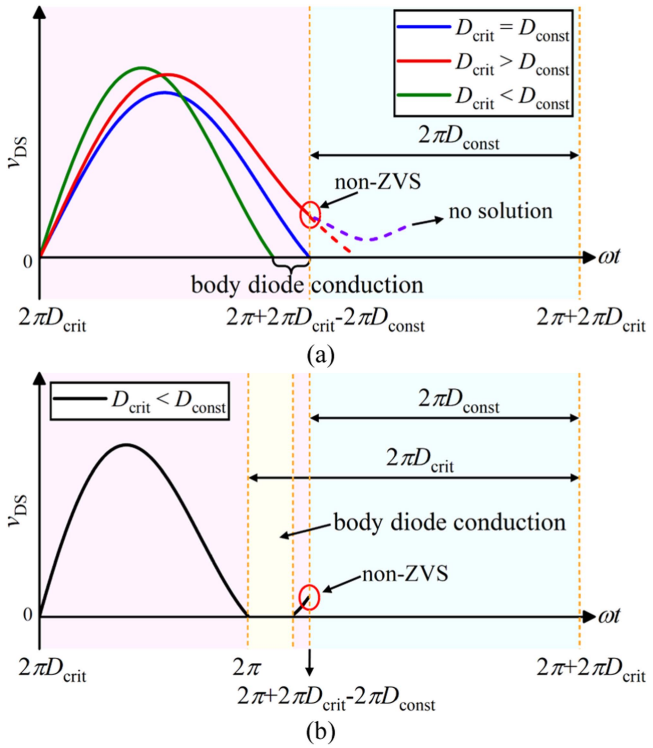

Fig. 8. Illustration of the ZVS condition. (a) Different v_{DS} waveforms during load deviation. (b) Special situation when $D_{crit} > D_{const}$.

can be deemed to approximately meet the ZVS condition. If $D_{crit} = D_{const}$, the circuit precisely achieves ZVS, according to the analysis in Section III-A. If no solution for D_{crit} exists, it implies that the voltage of v_{DS} will never drop to 0, thus rendering ZVS unattainable. If $D_{crit} < D_{const}$, when the switch turns ON, v_{DS} cannot reach 0, resulting in non-ZVS. So D_{crit} should be equal to or larger than D_{const} to ensure ZVS. Otherwise, v_{DS} will retain a nonzero value upon the MOSFET's turn-ON, resulting in the generation of switching.

Notably, as shown in Fig. 8(b), when $D_{crit} > D_{const}$, after v_{DS} drops to zero, the body diode of S_1 begins to conduct. Before S_1 is turned ON, however, the capacitor C_s may be charged again, causing v_{DS} to rise. In order to prevent this scenario, it is necessary to satisfy the following condition:

$$i_D\,[2\pi(D_{crit} - D_{const})] \le 0. \tag{54}$$

Based on (22) through (26) along with (54), the output current I_1, the output voltage V_2 and the critical duty cycle D_{crit} required to achieve ZVS can be determined. I_{1_const} and V_{2_const} in (36) and (38) are selected as the base values of the current and voltage. Then, the normalized load voltage V_{2n} and current I_{1n} can be derived for varying load resistances as follows:

$$I_{1n} = \frac{I_1}{I_{1\_const}} \tag{55}$$

$$V_{2n} = \frac{V_2}{V_{2\_const}}. \tag{56}$$

TABLE II
CIRCUIT PARAMETERS

Parameters	Values	Parameters	Values
V_{in}	24 V	k_{Rn}	1
f	1 MHz	L_{in}	3.04 μH
D_{const}	0.5	C_s	5.00 nF
P_{max}	39.6 W	L_1	0.53 μH
c_{p_max}	0.102	C_1	48.27 nF
I_{1_const}	2 A	C_{1x}	12.79 nF
V_{2_const}	38.2 V	C_1'	61.03 nF
Q_{1max}	6	L_2	29.27 μH
Q_{2max}	10	L_{2x}	1.62 μH
R_{1max}	19.8 Ω	L_2'	30.89μH
R_{2min}	18.4 Ω	C_2	0.87 nF

Taking $D_{const} = 0.5$ to achieve a maximum power output capacity, the values for q, m, n, and h can be obtained from (33), (40), (41), and (48). Subsequently, the solutions for I_{1n}, V_{2n}, and D_{crit} are sorely dependent on R_{1n}, R_{2n}, and k_{Rn}. For different k_{Rn}, the solutions are shown in Fig. 9. When the value of $R_{1n}R_{2n}$ is equal to k_{Rn}, $D_{crit} = D_{const} = 0.5$, $I_{1n} = 1$, $V_{2n} = 1$, which is consistent with the analysis in Section III-A. The larger the discrepancy between $R_{1n}R_{2n}$ and k_{Rn}, the more significant the variations in D_{crit}, I_{1n}, and V_{2n}. As k_{Rn} increases, the range of R_{1n} widens, whereas a decrease in k_{Rn} results in a broader range of R_{2n}. In this article, $k_{Rn} = 1$ is selected to get a balanced load range of both outputs.

IV. CIRCUIT EXPERIMENTAL RESULTS AND DISCUSSION

A. Parameter Design Steps and System Setup

Fig. 10 illustrates the parameter design process for the proposed inverter. In the figure, P_{max} represents the maximum output power of the circuit, which can be determined using (47), as demonstrated in (57). L_{in} can be calculated through

$$P_{max} = \frac{h{V_{in}}^2}{2\omega L_{in}}. \tag{57}$$

Q_{1max} and Q_{2max} in Fig. 10 denote the maximum values of Q_1 and Q_2, respectively. According to (1) and (3), Q_1 and Q_2 vary with R_1 and R_2. Specifically, when R_1 is at its maximum value, Q_1 reaches its maximum value, whereas when R_2 is at its minimum value, Q_2 reaches its maximum value.

By specifying the necessary parameters according to specific scenarios and adhering to the flowchart, the values of all passive components can be solved step by step.

For prototype verifying, parameters V_{in}, f, D_{const}, P_{max}, Q_{1max}, Q_{2max}, and k_{Rn} are given, and then, following the steps shown in Fig. 10, the other parameters are determined. The specific values of all parameters are shown in Table II. As discussed in Section IV-B, k_{Rn} is chosen as 1 in this article.

An experimental prototype of the proposed class-E inverter with dual outputs is fabricated, as shown in Fig. 11. The Si

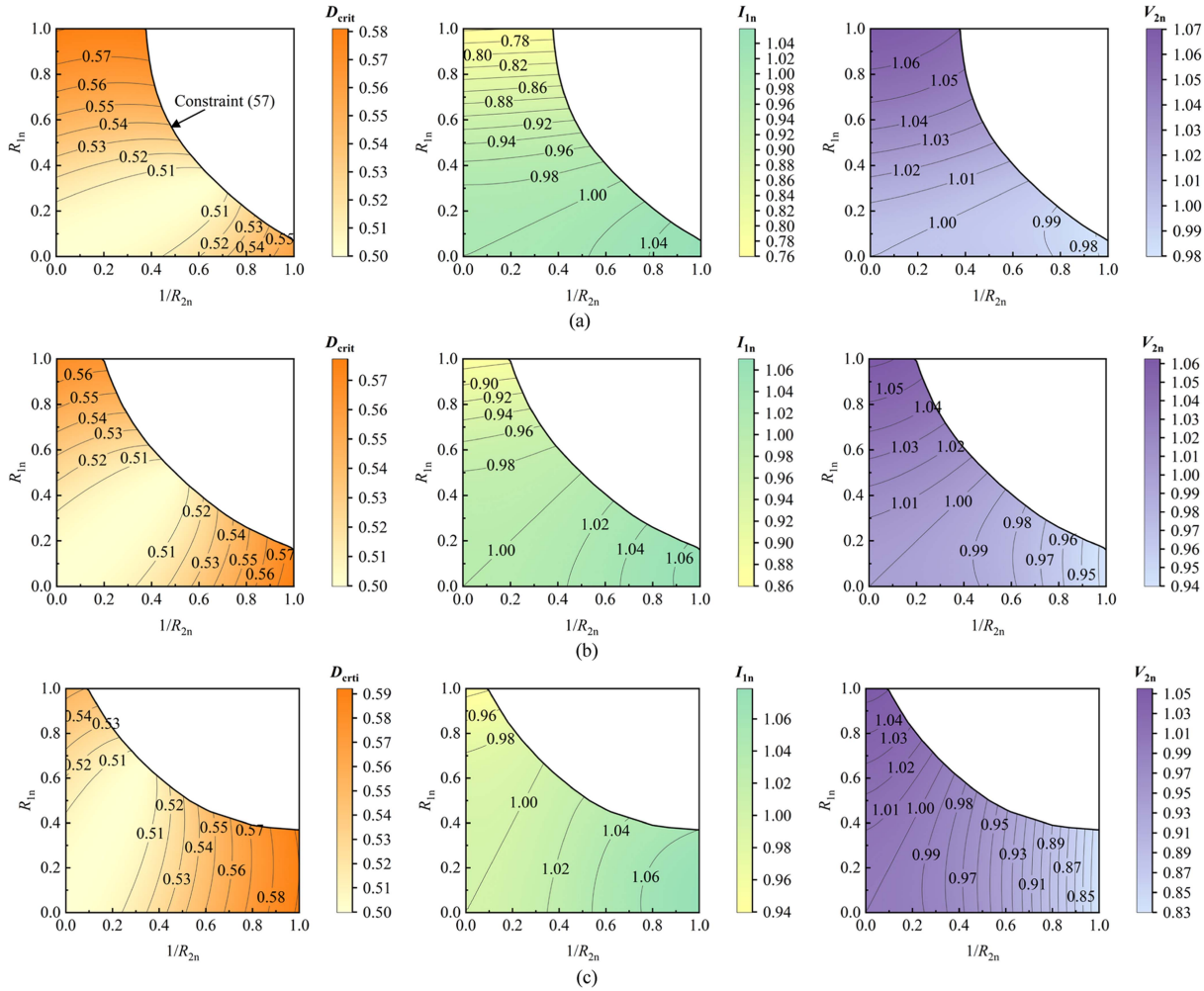

Fig. 9. I_{1n}, V_{2n}, and D_{crit} with different R_{1n}, R_{2n}, and k_{Rn}. (a) $k_{Rn} = 0.5$. (b) $k_{Rn} = 1$. (c) $k_{Rn} = 2$.

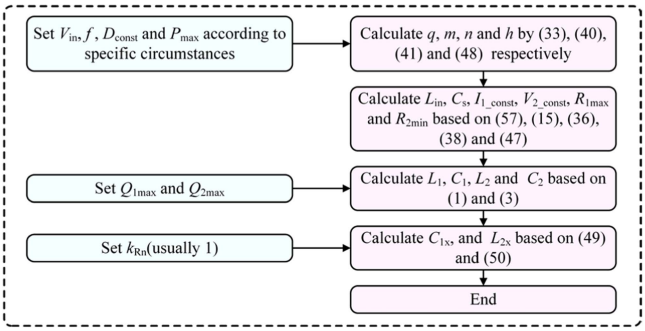

Fig. 10. Design procedures for the proposed inverter.

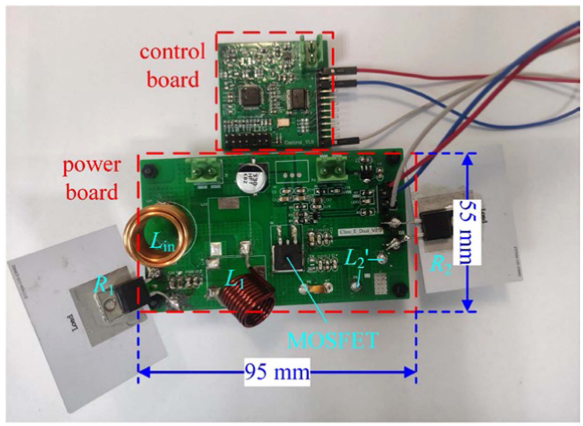

Fig. 11. Experimental prototype and the size of the proposed inverter.

MOSFET IPB320N20N3G from Infineon is chosen as the power switch due to its low conduction resistance of 32 mΩ. The gate drive signal is generated by a control board based on TI's MCU of TMS320F280025. The resonant capacitors utilize the multi-layer ceramic capacitors because they have good high-frequency performances. Air core inductors are selected for L_{in}, L_1, and L_2' in the circuit to reduce loss at high frequencies. Resistors having small parasitic inductances are used as the loads.

B. Measurement Results

Fig. 12 shows the experimental waveforms of the gate driving signal v_{GS}, the switch voltage v_{DS}, and the load voltages v_1 and v_2. Due to the difficulty in measuring i_1, the voltage v_1 was measured. Then, i_1 can be obtained by dividing it by R_1.

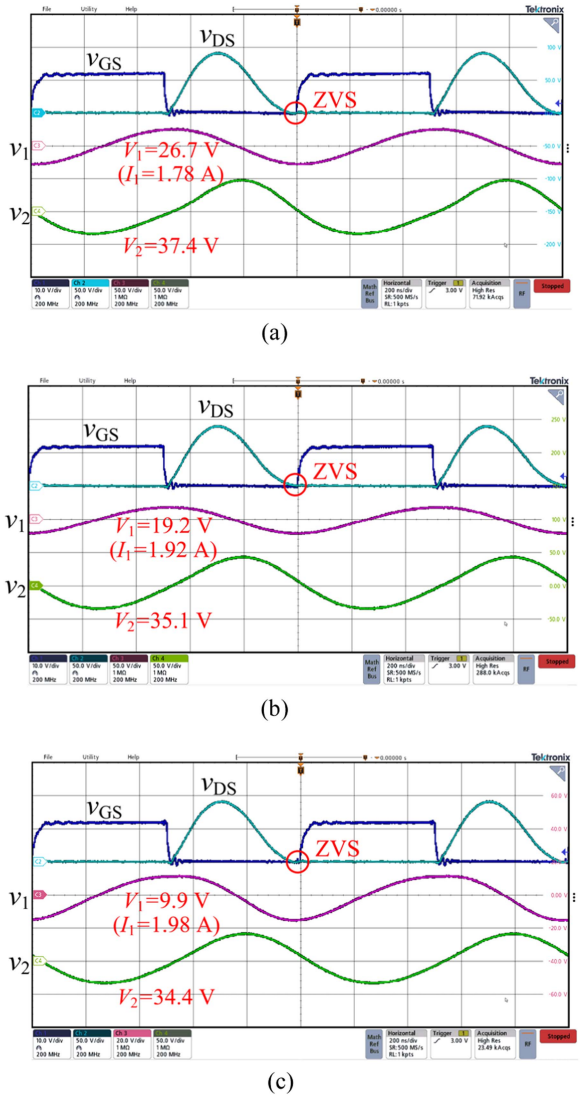

Fig. 12. Experimental waveforms. (a) $R_1 = 15\ \Omega$, $R_2 = 8\ \Omega$. (b) $R_1 = 10\ \Omega$, $R_2 = 40\ \Omega$. (c) $R_1 = 5\ \Omega$, $R_2 = 30\ \Omega$.

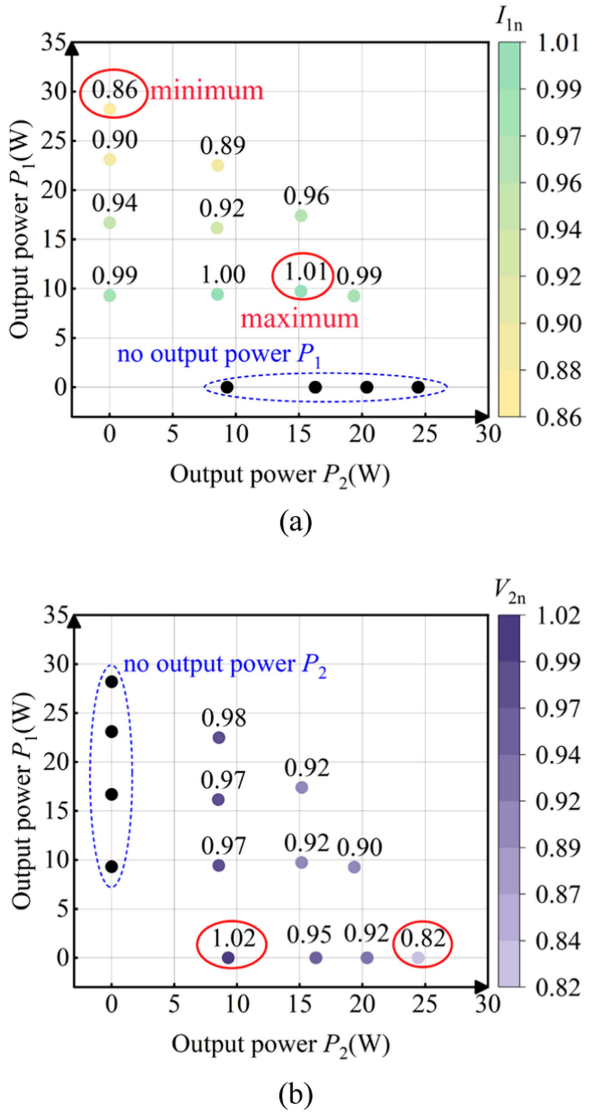

Fig. 13. Load variation of i_1 and v_2. (a) Normalized current I_{1n} changes with output power. (b) Normalized voltage V_{2n} changes with output power.

From Fig. 12, it can be observed that, at different loads, when S_1 turns ON, the switch voltage v_{DS} is always zero, thus, ZVS is achieved. Actually, the voltage across C_s is the forward voltage of the body diode when S_1 turns ON. The voltage will generate a surge current in the S_1-C_s loop. However, due to parasitic parameters in the loop and the limited energy stored in C_s, the surge current is minimal. Furthermore, since this surge current exists solely within the S_1-C_s loop, it does not affect the analysis of the circuit. I_1 and V_2 vary slightly, with I_1 close to 2 A and V_2 close to 38.2 V, which is consistent with the design in Table I. At $R_1 = 10\ \Omega$ and $R_2 = 40\ \Omega$, the circuit has the maximum output power of 32.6 W over the designed load range. Both v_1 and v_2 are approximately sinusoidal. Moreover, v_1 has a phase angle of approximately π and v_2 has a phase angle of approximately 1.5π, which is consistent with (34) and (35).

Fig. 13 shows the variations in the normalized output current I_{1n} and the normalized output voltage V_{2n} concerning the load power. P_1 denotes the measured output power in R_1, and P_2 represents the measured output power in R_2. From Fig. 13(a), it can be seen that I_{1n} has a maximum value of 1.01 and a minimum value of 0.86 where P_1 reaches its maximum of 28.2 W and P_2 is zero. As evident from Fig. 13(b), V_{2n} attains a maximum value of 1.02 and a minimum value of 0.82 where $P_1 = 0$ and $P_2 = 24.4$ W. Thus, the maximum current attenuation of I_{1n} is 14%, and the maximum voltage attenuation of V_{2n} is 18%. As P_1 increases, I_{1n} decreases, while as P_2 increases, V_{2n} decreases, which aligns with the analysis in Fig. 9. Due to power losses in the circuit, the observed current and voltage variations are slightly more pronounced than predicted by the theoretical analysis. It is noteworthy that as the load decreases, the reduction in Q_1 or Q_2 will also influence the experimental results, leading to a higher measured effective value. However, under the experimental conditions of this article, Q_1 and Q_2 are relatively large, and this effect can be negligible.

Fig. 14 shows the measured circuit efficiencies at different load powers. The highest efficiency of the circuit is 92.6% when

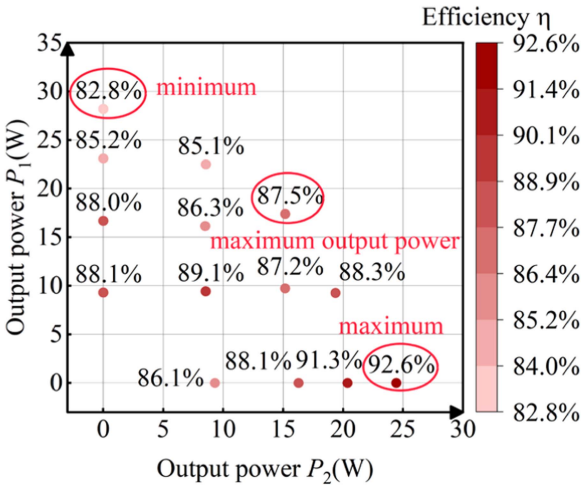

Fig. 14. System efficiency map.

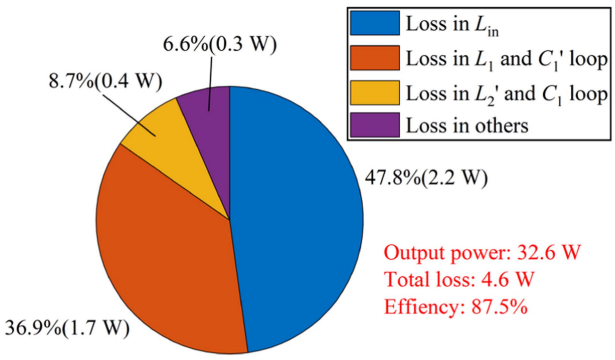

Fig. 15. Loss distribution at maximum output power.

$P_1 = 0$ W and $P_2 = 24.4$ W. The lowest efficiency of the circuit is 82.8% when $P_1 = 28.2$ W and $P_2 = 0$ W. The maximum output power of the circuit is 32.6 W in which $P_1 = 17.4$ W and $P_2 = 15.2$ W, and the circuit's efficiency is 87.5%. It can be seen from Fig. 14 that the parallel resonant cavity has a larger influence on the system efficiency. That is because a large current flows inside L_1, which results in high power loss as P_1 increases.

Fig. 15 illustrates the circuit loss distribution at the maximum output power. The input power is 37.2 W, the output power is 32.6 W, and the power loss is 4.6 W. Ignoring the iron loss of the air-core inductor, the losses of each part are determined by measuring the currents in each branch and calculating the copper loss. The loss in the input inductor L_{in} is 2.2 W, accounting for 47.8% of the total loss, which is the majority of the loss. The loss in the parallel resonant cavity is 1.7 W, accounting for 36.9% of the total loss because of a large circulating current in the L_1-C_1 loop. The loss in the series resonant cavity is much smaller because of the low I_2 value. Since ZVS is achieved in the circuit, the loss of the power switch is very small, which is included in the other loss of the circuit, with a total value of 0.3 W.

C. Dynamic Experiments

To further investigate the effect of load variations, dynamic experiments were conducted under different load conditions.

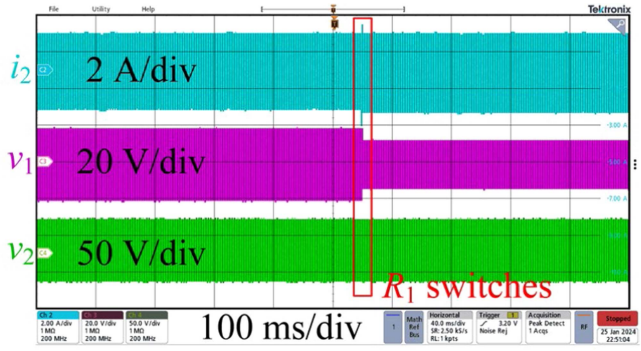

Fig. 16. Experimental waveforms of i_1, v_1, and v_2 when R_1 switches from 8 to 4.4 Ω with $R_2 = 40$ Ω.

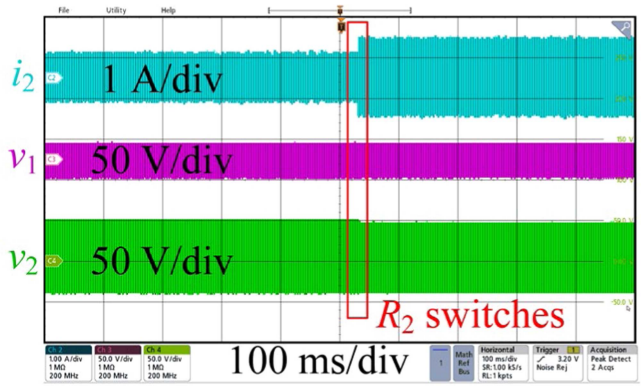

Fig. 17. Experimental waveforms of i_2, v_1, and v_2 when R_2 switches from 75 to 42.8 Ω with $R_1 = 10$ Ω.

First, R_2 was set at 40 Ω, and then R_1 was switched from 8 to 4.4 Ω. i_1, v_1, and v_2 were measured during the switching process. The experimental results are as follows.

As depicted in Fig. 16, when R_1 changed, the voltage v_1 across it does not change instantaneously due to the presence of the capacitor connected across R_1. As a result, a transient current spike occurs in the branch containing R_1. The current i_1 remains relatively unchanged before and after the switch of R_1. However, due to the decreased resistance of R_1, the parallel resonance quality factor Q_1 decreases. This leads to an increase in the harmonic content of i_1, resulting in a slight difference in its amplitude. As R_1 decreases while i_1 remains constant, the voltage v_1 across R_1 decreases after the switch. Meanwhile, the voltage v_2 across R_2 remains constant throughout the entire process.

Then, R_1 was set at 10 Ω, and R_2 changed from 75 to 42.8 Ω. The experimental waveforms of i_2, v_1, and v_2 are as follows.

As shown in Fig. 17, after the switch of R_2, the resistance of R_2 decreases while the voltage remains constant, resulting in an increase in i_2. The voltage v_1 across R_1 remains constant throughout the process. The voltage v_2 approximately remains unchanged before and after the switch, but due to the decreased R_2 and an increased series resonance quality factor Q_2, the harmonic content in v_2 decreases, causing a slight difference in its amplitude. Nevertheless, the fundamental component in v_2 remains relatively stable. Depending on specific application scenarios, this issue can be addressed through the design of a

filtering network. In summary, the experimental results indicate that the two outputs have a small influence on each other during load dynamic switching, which ensures stable constant-output characteristics.

V. Conclusion

A novel load-independent class-E inverter with dual outputs has been proposed in this article. Both series and parallel resonant cavities are integrated inside the circuit with only one power switch. Such a design is suitable for multiple load charging or battery charging where both CC and CV processes are required. The following conclusions can be summarized.

1) With proper resonant parameter design, a CC power source and a CV power source can be generated for the parallel-resonant output and series-resonant output, respectively, while maintaining load-independent ZVS.
2) A wider working range of the proposed load-independent dual-output class-E inverter, which depends on the resonant design, has been analyzed thoroughly considering both the constant output and the ZVS characteristics. A moderate design with $k_{\mathrm{Rn}} = 1$ is suggested to ensure enough working range for both the CC and CV outputs.
3) A 1 MHz class-E inverter hardware with dual outputs has been built and experimental results have been provided to validate the effectiveness of the proposal in this article. The maximum system efficiency reaches 92.6%.

Appendix Solution Process for Q, α, and β

By solving (28) based on (18)–(20), the following three equations can be obtained:

$$\tan\left[\pi\left(D-1\right)q\right] = \pi D q \tag{A1}$$

$$\begin{aligned}&-\sin\left(\alpha\right)-\sin\left(2\pi D+\alpha\right)\\&+\sin\left(\alpha\right)\cos\left[2\pi q\left(D-1\right)\right]\\&+\sin\left(2\pi D+\alpha\right)\cos\left[2\pi q\left(D-1\right)\right]\\&+q\cos\left(\alpha\right)\sin\left[2\pi q\left(D-1\right)\right]\\&+q\cos\left(2\pi D+\alpha\right)\sin\left[2\pi q\left(D-1\right)\right]=0\end{aligned} \tag{A2}$$

$$\begin{aligned}&-\cos\left(\beta\right)-\cos\left(2\pi D+\beta\right)\\&+\cos\left(\beta\right)\cos\left[2\pi q\left(D-1\right)\right]\\&+\cos\left(2\pi D+\beta\right)\cos\left[2\pi q\left(D-1\right)\right]\\&+q\sin\left(\beta\right)\sin\left[2\pi q\left(D-1\right)\right]\\&+q\sin\left(2\pi D+\beta\right)\sin\left[2\pi q\left(D-1\right)\right]=0.\end{aligned} \tag{A3}$$

When a fixed duty cycle D_{const} is given, substituting D_{const} into (A1) yields the solution for q. By utilizing (A1) and (A2), α can be determined. Likewise, using (A1) and (A3), β can be obtained. The procedure for solving α and β is outlined as follows.

For the sake of simplicity in representation, it is assumed that

$$\sigma = 2\pi q\left(D_{\mathrm{const}}-1\right). \tag{A4}$$

Then, from (A1), (A5) can be obtained

$$q = \frac{\tan\left(\frac{\sigma}{2}\right)}{\pi D_{\mathrm{const}}} = \frac{1-\cos\left(\sigma\right)}{\pi D_{\mathrm{const}}\sin\left(\sigma\right)}. \tag{A5}$$

Substituting (A5) into (A2) and after simplification, (A6) can be obtained

$$\begin{aligned}\frac{\cos\left(\alpha\right)-\cos\left(2\pi D_{\mathrm{const}}+\alpha\right)}{\pi D_{\mathrm{const}}} &= \sin\left(\alpha\right)\\&\quad+\sin\left(2\pi D_{\mathrm{const}}+\alpha\right).\end{aligned} \tag{A6}$$

Further simplification yields (A7) as

$$\sin\left(\alpha-\theta\right)+\sin\left(2\pi D_{\mathrm{const}}+\alpha+\theta\right)=0 \tag{A7}$$

where θ is an intermediate variable.

Based on (A7), α can be solved as

$$\alpha = N\pi - \pi D_{\mathrm{const}} \tag{A8}$$

where N is an integer. Since α ranges from 0 to 2π, N can be either 1 or 2. When $N = 1$, the average value of the input current i_{in} is negative, implying that the dc power supply absorbs power while the ac power source v_1 outputs power. In this case, the circuit operates in rectifier mode. When $N = 2$, the circuit operates in inverter mode. Therefore, the final solution is obtained as follows:

$$\alpha = \left(2-D_{\mathrm{const}}\right)\pi. \tag{A9}$$

Similarly, from (A3) and (A5), β can be determined as

$$\beta = N\pi - \frac{\pi}{2} - \pi D_{\mathrm{const}}. \tag{A10}$$

When $N = 2$, the circuit operates in the inverter mode. The final solution of β is obtained as

$$\beta = \left(\frac{3}{2}-D_{\mathrm{const}}\right)\pi. \tag{A11}$$

In conclusion, provided that a specific D_{const} value is given, when q, α, and β satisfy (A1), (A9), and (A11), respectively, the circuit meets the load-independent ZVS condition. The next step involves demonstrating that the circuit meets the constant output conditions specified in (29)–(32). By substituting (A9) and (A11) into (29)–(32) and simplifying the calculations, it can be confirmed that (29)–(32) are valid. Therefore, the solutions of q, α, and β that simultaneously satisfy both the load-independent ZVS condition and constant output conditions are provided by (A1), (A9), and (A11).

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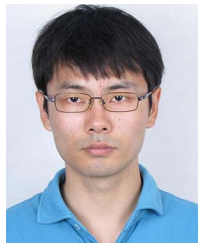

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