Isolated Modular Multilevel Matrix Converter (I-M3C) Based Novel Solid-State Transformer (SST) With Low-Frequency Medium-Voltage AC Port

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***Abstract*—This article proposes a novel solid-state transformer (SST) having a low-frequency medium-voltage ac (LF-MVac) port distinctively, which can be the key equipment for smart distribution networks based on LF-MVac interconnection. The proposed SST has four ports of power-frequency medium-voltage ac (MVac), LF-MVac, low-voltage dc (LVdc), and low-voltage ac (LVac). In addition to the two-level low-voltage dc/ac converter, the proposed SST is mainly composed of an isolated modular multilevel matrix converter (I-M3C), which can achieve single-stage three-port power conversion. First, the topology of the I-M3C is introduced. Then, a simple modulation scheme is provided to achieve single-stage three-port power conversion, and the operating principles of the I-M3C are given in detail. In addition, a control strategy based on dual-*dq* coordinate system is designed, which can achieve stable operation without the complex multistage coordinated control and voltage-balancing control strategies. Finally, the effectiveness of the proposed control strategy is verified through a 10-kV/2-MW full-power simulation platform, and a 100-V/1-kW scaled-down experimental prototype is built to further demonstrate the correctness of the proposed I-M3C.**

***Index Terms*—Isolated modular multilevel matrix converter (I-M3C), low-frequency medium-voltage ac (LF-MVac), single-stage three-port power conversion, solid-state transformer (SST).**

I. Introduction

FOR traditional ac power systems, one of the initial design challenges is selecting standard electrical frequencies. Power transmission between different frequencies has never been a simple task, and the large-scale electrification process will be severely challenged without a standard frequency. Since the 1890s, the power system has been developed with 50 Hz or 60 Hz as the standard operating frequency, and the issue of frequency selection has not been reconsidered [1], [2].

With the development of semiconductor technology, it is more flexible to control the amplitude, frequency, and phase of ac, which improves the feasibility of power transmission at frequencies other than the standard 50 Hz or 60 Hz, such as low-frequency ac (LFac) transmission and dc transmission. LFac transmission not only has transmission capacity and economy, but also has the convenience of a multiterminal flexible connection. And it has its own unique advantages over dc transmission within a certain transmission distance [3], so LFac transmission has been gradually studied by many scholars [4], [5], [6]. At present, LFac transmission is a promising solution to the integration of large offshore wind farms over long distances, and its core equipment is M3C, whose main function is to realize direct frequency conversion [7], [8], [9]. As is well known, high-voltage dc (HVdc) transmission is the power transmission with large capacity and ultra long distance, which can minimize power loss because its frequency can be reduced to 0 Hz [10]. And the key equipment of HVdc transmission is the modular multilevel converter (MMC), whose main function is to realize ac/dc conversion [11], [12]. In addition to HVdc transmission, with the increase of renewable energy generation and the proportion of dc load in distribution networks, the application and development of dc systems in medium and low voltage distribution networks and their medium-voltage interconnection have been gradually studied by many scholars [13], [14], [15]. Therefore, dc transmission and LFac transmission have their own advantages, which are suitable for the economic and efficient upgrading of power grids in different scenarios, and multi-frequency power system is the development trend of future power grids [1].

In order to improve the utilization rate of renewable energy generation systems, medium and low voltage distribution networks are gradually developing towards smart operation and flexible interconnection, ensuring that the distribution networks have the ability to regulate power [14]. The interconnection scheme of medium-voltage distribution networks is

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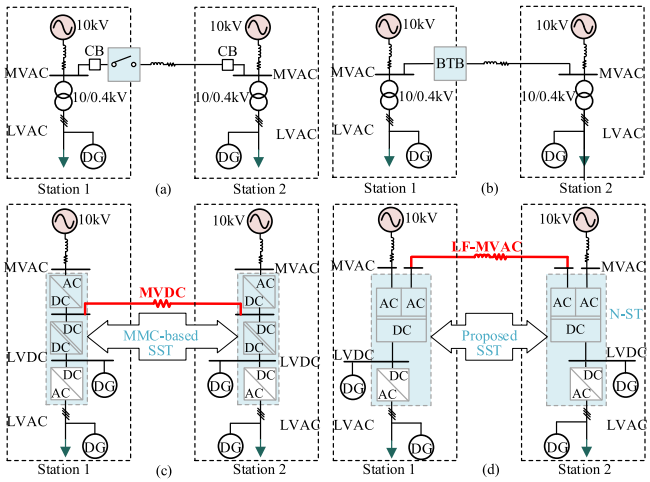

Fig. 1. Interconnection scheme for medium-voltage distribution networks. (a) Based on mechanical contact switches. (b) Based on BTB converter. (c) MVdc-based. (d) LF-MVac-based.

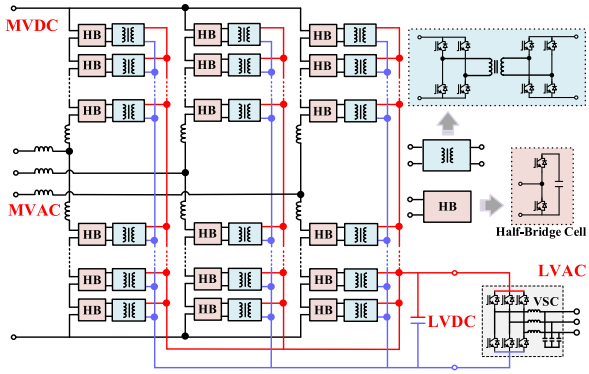

Fig. 2. MMC-based SST.

shown in Fig. 1. And Fig. 1(a) shows a conventional configuration of two medium-voltage ac (MVac) distribution networks interconnected by mechanical contact switches [16], [17], but it has some disadvantages, such as uncontrollable interactive power, slow response speed, high operating costs, and easy expansion of fault influence range. In order to realize the normal flexible connection between the two distribution networks, Fig. 1(b) shows a configuration interconnected by a back-to-back converter (BTB) [18]. It can avoid the low reliability caused by frequent switching of mechanical contact switches, greatly improve the flexibility and rapidity of distribution networks, and make the distribution networks have the advantages of open-loop operation and closed-loop operation.

Fig. 1(c) shows a configuration to realize flexible interconnection between two distribution stations through a medium-voltage dc (MVdc) port, and realizes the configuration of low-voltage ac/dc hybrid distribution derived from [19]. However, the substation equipment and interconnection lines of this configuration need to be rebuilt, so the reconstruction cost is high. The key substation equipment in Fig. 1(c) is the MMC-based solid-state transformer (SST), also known as smart transformer (ST) or power electronics transformer [20], [21]. The MMC-based SST is composed of an MMC rectifier power stage, an isolated dc/dc converter power stage, and a two-level voltage source converter power stage, which is shown in Fig. 2. And the MMC-based SST has four ports (MVac, MVdc, LVdc, and LVac ports), and its LVdc port can be directly connected to the distributed generation (DG), which can meet the distribution network expansion planning in the future. However, the more power conversion stages of the MMC-based SST, the lower its work efficiency and the more complex multistage coordinated control strategies.

Therefore, this article proposes an interconnection scheme based on a low-frequency medium-voltage ac (LF-MVac) port, which can use the existing power-frequency ac interconnection line and greatly save the line construction cost, as shown in Fig. 1(d). In addition, in order to realize the LF-MVac interconnection between two medium-voltage distribution stations, a frequency converter with an LF-MVac port is usually needed. At present, the most commonly used frequency converter in low-frequency transmission is the modular multilevel matrix converter (M3C) [22], [23], [24], [25]. And M3C can realize the conversion from power frequency to low frequency, but it requires a complex voltage-balancing control strategy [26], [27], [28], [29]. Since M3C only has two ports (power-frequency ac port and LFac port), when it needs to realize low-voltage ac/dc hybrid distribution, it requires additional SSTs. Therefore, M3C has no outstanding advantages in medium- and low-voltage distribution networks.

This article introduces the high-frequency link concept [30], [31] into the M3C architecture and proposes a novel SST with four ports (MVac, LF-MVac, LVdc, and LVac ports). The rear stage of the proposed SST is a traditional two-level low-voltage dc/ac converter, and its front stage is an isolated M3C (I-M3C). Compared with M3C, the proposed I-M3C has a LVdc port that can be directly connected to DG, and its control is simpler because it eliminates the complex voltage-balancing control strategy. Therefore, the main advantages of this article are as follows.

1) The proposed SST has LF-MVac and LVdc ports. It can be used as the key equipment of smart distribution networks based on the LF-MVac interconnection.
2) The proposed SST eliminates the independent capacitor between the rectifier power stage and the isolated power stage in the traditional MMC-based SST, thus improving the power density of the SST.
3) The I-M3C in the front stage of the proposed SST can realize single-stage three-port power conversion without a complex voltage-balancing control strategy, and its control strategy is simpler.

The rest of this article is organized as follows. Section II describes the topology structure, modulation scheme, and operating principles of the proposed ST. The mathematical model and control strategy are explained in Section III. In Section IV, the simulation results of the full power simulation platform (10-kV/2-MW) are discussed. A 100-V/1-kW scaled-down experimental prototype and experimental results are given in Section V. Finally, Section VI concludes this article.

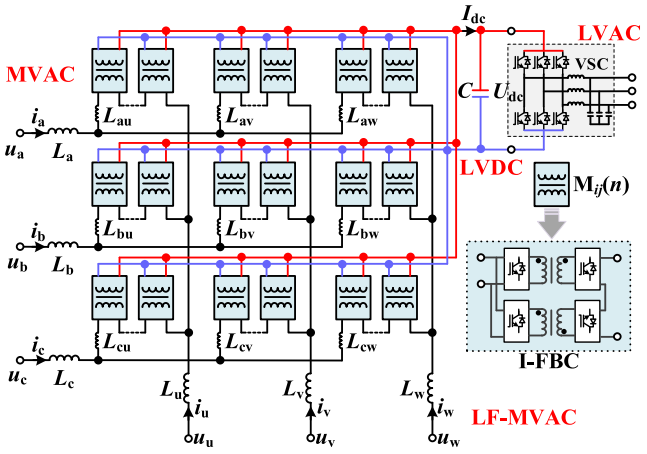

Fig. 3. Proposed SST with LF-MVac port.

II. Topology, Modulation, and Principles of the Proposed SST

A. Topology Description

Fig. 3 shows the topology of the proposed SST with an LF-MVac port. In addition to the two-level low-voltage dc/ac converter, its main component is an I-M3C. The I-M3C has 3×3 basic conversion units, and each conversion unit is composed of n isolated full bridge cells (I-FBCs). I-M3C can achieve high-frequency isolated single-stage power conversion from LVdc to MVac and LF-MVac. Compared to M3C, the LVdc port has been added to meet the access requirements of DG in the distribution networks. Since there are no independent capacitors in the submodules of the proposed SST to suppress the second-order harmonic fluctuations, it has a high power density, which simplifies the complexity of the control system.

In Fig. 3, u_a, u_b, and u_c are the MVac voltages; i_a, i_b, and i_c are the MVac currents; L_a, L_b, and L_c are the MVac filtering inductors; u_u, u_v, and u_w are the LF-MVac voltages; i_u, i_v, and i_w are the LF-MVac currents; L_u, L_v, and L_w are the LF-MVac filtering inductors. And U_{dc} is the LVdc voltage, I_{dc} is the LVdc current, and C is the LVdc voltage stabilizing capacitor. The nine I-M3C conversion units are represented as M_{ij}, where $i = a,b,c$, $j = u,v,w$, and L_{ij} is the filtering inductance of the bridge arm of the nine conversion units.

The I-FBC topology is shown in Fig. 4. The I-FBC is realized by two isolated chopper cells (I-CC_u and I-CC_b) through the ac ports in reverse series and the dc ports in parallel. Here, U_{dc} is the dc port voltage of I-FBC, I_{dc} is the dc port current of I-FBC, u_1 is the output voltage of I-CC_b, u_2 is the output voltage of I-CC_u, u_{ac} is the ac port voltage of I-FBC ($u_{ac} = u_1+u_2$), and i_{ac} is the ac port current of I-FBC. Q_{u1}, Q_{u2}, Q_{u3}, and Q_{u4} are the driving signals of IGBTs at the primary side of I-CC_u; S_{u1}, S_{u2}, S_{u3}, and S_{u4} are the driving signals of IGBTs at the secondary side of I-CC_u; Q_{b1}, Q_{b2}, Q_{b3}, and Q_{b4} are the driving signals of IGBTs at the primary side of I-CC_b; S_{b1}, S_{b2}, S_{b3}, and S_{b4} are the driving signals of IGBTs at the secondary side of I-CC_b. And k is the turns ratio of high-frequency transformer (HFT), and L_r is the leakage inductance of HFT.

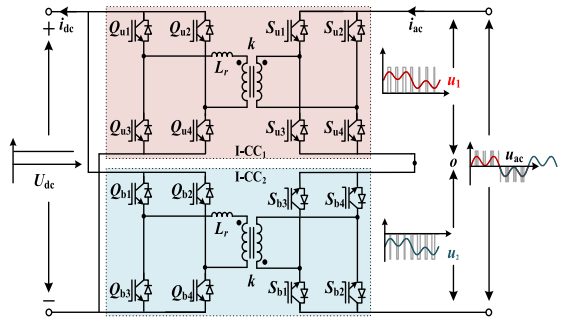

Fig. 4. Topology of I-FBC.

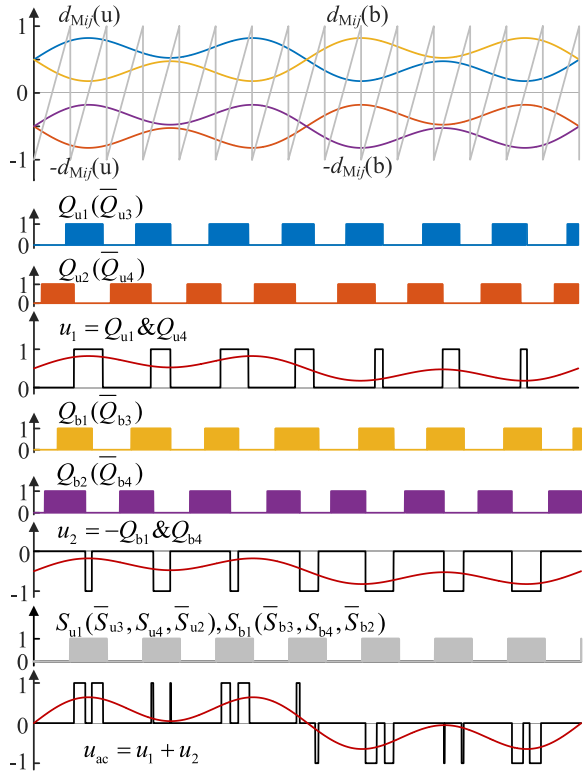

Fig. 5. Modulation scheme of I-FBC.

B. Modulation Scheme

The modulation signal of the I-FBC is composed of two ac modulation signals. The MVac modulation signals are defined as d_a, d_b, d_c, and the LF-MVac modulation signals are defined as d_u, d_v, d_w. The I-FBC's modulation signals in the I-M3C conversion unit M_{ij} are as follows:

$$\begin{cases} d_{Mij(u)} = 0.5 + (d_i + d_j) \\ d_{Mij(b)} = 0.5 - (d_i + d_j) \end{cases}. \tag{1}$$

The I-FBC's modulation signal waveform of the M_{11} conversion unit is given, as shown in Fig. 5. The modulation signals d_{Mij}(u), -d_{Mij}(u), d_{Mij}(b), -d_{Mij}(b) are compared with the sawtooth carrier to generate the driving signals of IGBTs at the dc side $Q_{u1}(\overline{Q}_{u3})$,$Q_{u2}(\overline{Q}_{u4})$,$Q_{b1}(\overline{Q}_{b3})$,$Q_{b2}(\overline{Q}_{b4})$,

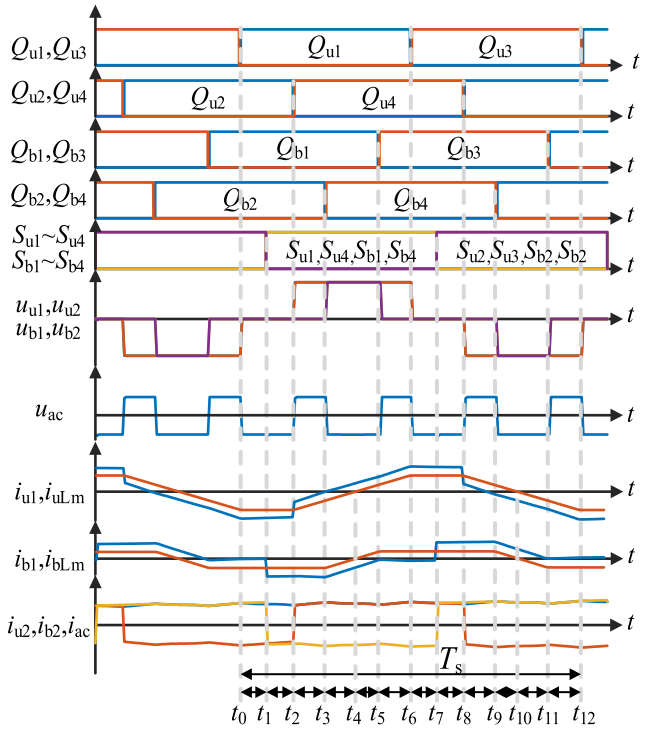

Fig. 6. Detailed theoretical waveforms when the converter operates in positive half cycle of v_{ac}.

and the driving signals of IGBTs at the ac side S_{u1} $(\overline{S}_{u3}, S_{u4}, \overline{S}_{u2})$, $S_{b1}(\overline{S}_{b3}, S_{b4}, \overline{S}_{b2})$. Finally, the u_{ac} is obtained.

C. Operating Principles

The operating principles of I-FBC are presented below in order to have a further understanding of the proposed topology and modulation scheme. Detailed theoretical waveforms are shown in Fig. 6 when the I-FBC operates in the positive half cycle of v_{ac}. Here, the parasitic capacitor in all IGBTs (Q_{u1}–Q_{u4}, Q_{b1}–Q_{b4}, S_{u1}–S_{u4}, and S_{b1}–S_{b4}) is ignored. Considering the operating principles of the I-FBC in the positive half cycle of v_{ac} are similar to those in the negative half cycle of v_{ac}, only the operating principles of the I-FBC in the positive half cycle of v_{ac} will be analyzed. Since the operating principles of the last six stages are symmetric with those of the first six stages, only the operating principles of the first six stages are analyzed below, as shown in Fig. 6. And the graphic representations of the first six stages are presented in Fig. 7.

Stage 1: [t_0–t_1, Fig. 7(a)]. In this stage, Q_{u1}, Q_{u2}, Q_{b1}, Q_{b2}, S_{u2}, S_{u3}, S_{b2}, and S_{b3} are ON. The primary side of the ICC_u's and ICC_b's HFT keeps freewheeling. Then, i_{u1} flows through the antiparallel diode of Q_{u1} and Q_{u2}, i_{b1} flows through the antiparallel diode of Q_{b1} and Q_{b2}, i_{ac} flows through S_{b2}, S_{b3} and the antiparallel diode of S_{u3}, S_{u2}. It is noted that u_{u1}, u_{u2}, u_{b1}, and u_{b2} are zero.

Stage 2: [t_1–t_2, Fig. 7(b)]. This stage starts when S_{u2}, S_{u3}, S_{b2}, and S_{b3} are turned OFF and S_{u1}, S_{u4}, S_{b1}, and S_{b4} are turned ON. The flow directions of i_{u1} and i_{b1} in *Stage 2* are the same with those in Stage 1. Then, i_{ac} flows through S_{b1}, S_{b4} and the antiparallel diode of S_{u3}, S_{u2}. It is noted that u_{u1}, u_{u2}, u_{b1}, and u_{b2} are zero.

Stage 3: [t_2–t_3, Fig. 7(c)]. It is seen that while Q_{u2} is turned OFF and Q_{u4} is turned ON, this stage begins. The primary side of the ICC_b's HFT keeps freewheeling. Then, i_{u1} flows through the Q_{u4} and the antiparallel diode of Q_{u1}, i_{ac} flows through the S_{b1}, S_{b4} and the antiparallel diode of S_{u4}, S_{u1}. It is noted that u_{u1} and u_{u2} are U_{dc}, u_{b1}, and u_{b2} are zero.

Stage 4: [t_3–t_4, Fig. 7(d)]. This stage starts when Q_{b2} is turned OFF and Q_{b4} is turned ON. At this moment in time, i_{u1} changes from negative to positive and flows through Q_{u1} and Q_{u4}. And i_{b1} flows through Q_{b4} and the antiparallel diode of Q_{b1}. The flow direction of i_{ac} in *Stage 4* is identical to that in Stage 3. It is noted that u_{u1}, u_{u2}, u_{b1}, and u_{b2} are U_{dc}.

Stage 5: [t_4–t_5, Fig. 7(e)]. This stage begins when i_{uLm} and i_{bLm} change from negative to positive. The state of other variables remains precisely the same as those in *Stage 4*, with the exception of a change in the direction of the excitation current.

Stage 6: [t_5–t_6, Fig. 7(f)]. When Q_{b1} is turned OFF and Q_{b3} is turned ON, this stage begins. The primary side of the ICC_b's HFT starts freewheeling. Subsequently, i_{b1} flows through Q_{b3} and Q_{b4}'s antiparallel diode. u_{b1} and u_{b2} change from U_{dc} to zero at this point.

III. Control Strategy of I-M3C

A. Mathematical Model

According to Fig. 4 and (1), the equivalent modulation ratio d_{Mij} of I-FBC is

$$d_{Mij} = 2(d_i + d_j). \tag{2}$$

The relationship between MVac and LF-MVac is given according to Kirchhoff's voltage law

$$u_{ij} = u_i - u_j - L_i\frac{\mathrm{d}i_i}{\mathrm{d}t} + L_j\frac{\mathrm{d}i_j}{\mathrm{d}t} - L_{ij}\frac{\mathrm{d}i_{ij}}{\mathrm{d}t} - u_{NO}. \tag{3}$$

The bridge arm voltage u_{ij} of the I-M3C conversion unit can be expressed as

$$u_{ij} = U_{dc} \times 2nk(d_i + d_j). \tag{4}$$

According to Kirchhoff's current law, the relationship between MVac and LF-MVac port current and bridge arm current is as follows:

$$\begin{cases} i_i = i_{iu} + i_{iv} + i_{iw} \\ i_j = -i_{uj} - i_{vj} - i_{wj} \end{cases}. \tag{5}$$

The LVdc port current is equal to the sum of the bridge arm current of nine conversion units after converting to the dc port

$$I_{dc} = \sum(i_{dc-ij}) = \sum(i_{ij} \times 2nk(d_i + d_j)). \tag{6}$$

To sum up, the I-M3C's average model is shown in Fig. 8. Here, u_{ij} is the ac port voltage of nine conversion units, i_{ij} is the ac port current of nine conversion units, and $i_{dc\text{-}ij}$ is the dc port current of nine conversion units. If each conversion unit contains n I-FBCs, the ac port voltage is $n{*}u_{ac}$, the ac port current is i_{ac}, and the dc port current is $n{\times}i_{dc}$.

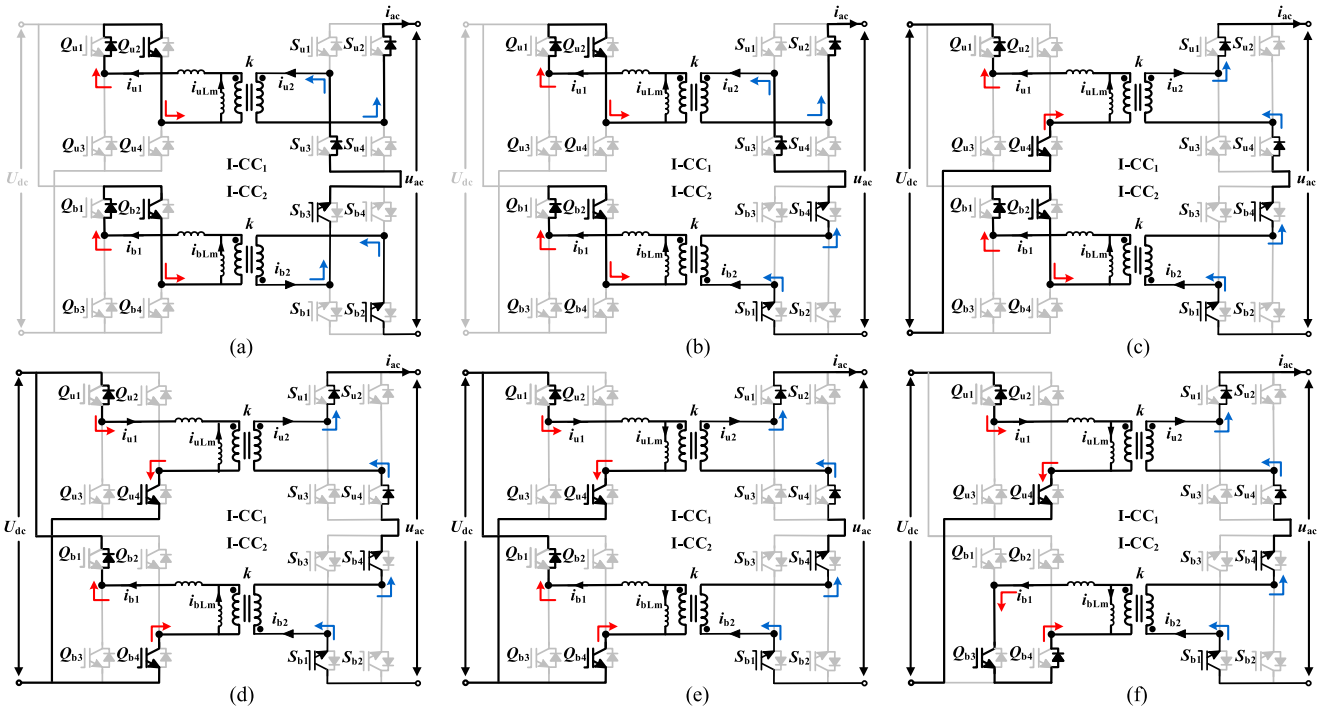

Fig. 7. Graphic representations of the converter's operating principles in positive half cycle of v_{ac}. (a) Stage 1. (b) Stage 2. (c) Stage 3. (d) Stage 4. (e) Stage 5. (f) Stage 6.

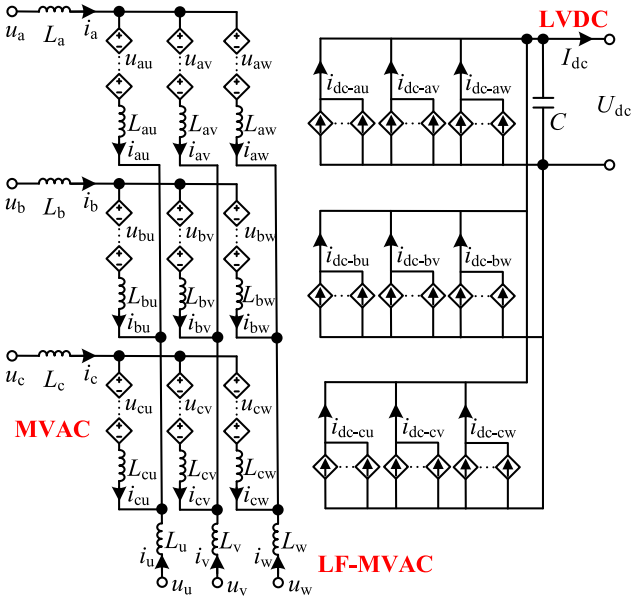

Fig. 8. Average model of I-M3C.

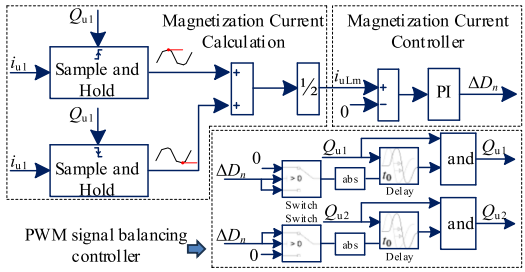

Fig. 9. DC offset control strategy of I-CC's intermediate transformer.

B. Control Strategy

The I-FBC is composed of two I-CCs, as shown in Fig. 4. The operation principle of I-CC is similar to that of the isolated dc/dc converter in CHB-based SST and MMC-based SST, there are dc offset in transformer current. The reasons for the dc offset of the ICC intermediate transformer current are as follows: the voltage–second balance of the magnetizing inductance is not achieved.

According to reference [32], an dc offset control strategy of I-CC's intermediate transformer is designed to avoid causing transformer magnetic saturation. As shown in Fig. 9, the dc offset control strategy includes three parts: magnetization current calculation, magnetization current control, and duty cycle balance control of the first half cycle and the second half cycle of the switch drive signal. The imbalance in duty cycle between the first half and the second half of the switch drive signal is controlled to suppress the dc offset of the magnetizing inductance.

In addition, if the dc component of two ICCs cannot be completely offset, introducing dc bias into the MVac and LF-MVac ports can result in asymmetric three-phase voltages in the I-M3C.

To solve this issue, the controllability of the dc modulation ratio can be used to feedback the dc bias as the control target to the dc modulation ratio. In this case, the dc modulation ratio is

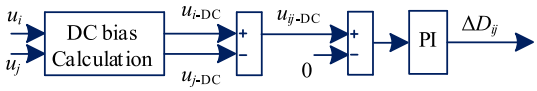

Fig. 10. DC bias control strategy of I-FBC.

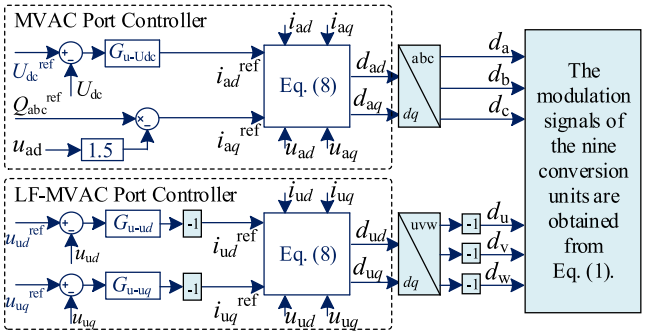

Fig. 11. I-M3C's control strategy based on dual *d-q* coordinate system.

no longer fixed at 0.5, but rather varies as $0.5\pm\Delta D_{ij}$, as shown in (7), and its specific control strategy is illustrated in Fig. 10

$$\begin{cases} d_{\mathrm{M}ij(\mathrm{u})} = (0.5 - \Delta D_{ij}) + (d_i + d_j) \\ d_{\mathrm{M}ij(\mathrm{b})} = (0.5 + \Delta D_{ij}) - (d_i + d_j) \end{cases}. \tag{7}$$

The proposed I-M3C does not need a complex voltage-balancing control strategy. The stable operation of I-M3C can be realized by using dual-*dq* coordinate system. The detailed control strategy is shown in Fig. 11, which includes the controller of the MVac port and the controller of the LF-MVac port. The control objective of the controller of the MVac port is to stabilize the LVdc port voltage and control the reactive power of the MVac port. The control objective of the controller of the LF-MVac port is to stabilize the LF-MVac port voltage. I-M3C has the advantage of simple control.

In Fig. 11, the equation of the current inner loop is shown in the following equation:

$$\begin{cases} d_d = -(i_d{}^{\mathrm{ref}} - i_d)G_{\mathrm{i}d} + \omega L i_q/2nkU_{\mathrm{dc}} + u_d/2nkU_{\mathrm{dc}} \\ d_q = -(i_q{}^{\mathrm{ref}} - i_q)G_{\mathrm{i}q} - \omega L i_d/2nkU_{\mathrm{dc}} + u_q/2nkU_{\mathrm{dc}} \end{cases} \tag{8}$$

where d_d and d_q are *d*-axis and *q*-axis modulation waves, respectively. i_d and $i_d{}^{\mathrm{ref}}$ are the *d*-axis current and its reference value, respectively. i_q and $i_q{}^{\mathrm{ref}}$ are the *q*-axis current and its reference value, respectively. $G_{\mathrm{i}d}$ and $G_{\mathrm{i}q}$ are the transfer functions of the *d*-axis and *q*-axis current PI controllers, respectively. ω is the angular frequency of the power-frequency or low-frequency grid. L is the filter inductance of the power-frequency or low-frequency grid. n is the number of modules. k is the turns ratio of HFT. U_{dc} is the LVdc port voltage. u_d and u_q are obtained by the *dq* transformation of power-frequency or low-frequency grid voltage, respectively.

C. Operating Modes

Fig. 12 shows the schematic diagram of possible operating modes of I-M3C, in which the power conversion between MVac, LF-MVac, and LVdc ports can be clearly comprehended. In

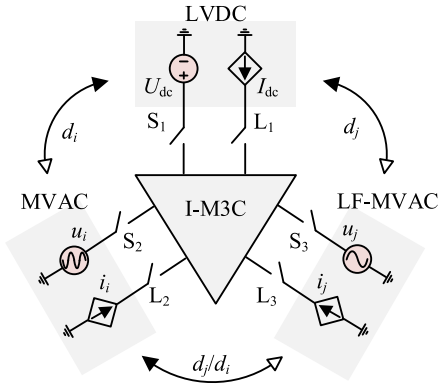

Fig. 12. Operating mode diagram of I-M3C.

TABLE I
OPERATING MODE OF I-M3C

State	Closed S_1	Closed S_2	Closed S_3
Closed L_1	/	Mode 1	Mode 3
Closed L_2	Mode 2	/	Mode 6
Closed L_3	Mode 4	Mode 5	/
Closed L_1, L_2, L_3		Mode 7	

Fig. 12, the power grid connected to each port of I-M3C can be equivalent to a constant voltage source, and the load connected to each port can be equivalent to a controlled current source. There are seven possible operation modes of I-M3C obtained by continuously switching the ON-OFF state of each switch, as shown in Table I. When the switch S_i connected to the constant voltage source is closed, it means that the corresponding port of I-M3C is connected to the power grid, and when the switch L_i connected to the controlled current source is closed, it means that the port is connected to the load, where $i = 1, 2, 3$. And the seven possible operation modes of I-M3C are described as follows.

Mode 1: The power grid at the MVac port transfers power to the load at the LVdc port.

Mode 2: The DG at the LVdc port provides power to the load at the MVac port.

Mode 3: The interconnected distribution network supplies power to the load at the LVdc port through the LF-MVac port.

Mode 4:: The DG at the LVdc port provides power support to the load in the distribution network interconnected by the LF-MVac port.

Mode 5: The power grid at the MVac port transmits power to the interconnected distribution network load at the LF-MVac port.

Mode 6: The power demanded by the load at the MVac port is absorbed from the interconnected distribution network through the LF-MVac port.

Mode 7: The three ports of I-M3C are all connected to the loads. At this time, if any switch from S_1 to S_3 is closed, the connected power supply can simultaneously provide power for the loads at the three ports. Among them, switch S_1 is connected

TABLE II
PARAMETERS OF THE SIMULATION PLATFORM

Parameter	Symbol	Value
LVDC voltage	U_{dc}	750 V
LVDC capacitor	C_{dc}	20 mF
RMS of MVAC voltage	$U_{MVac\text{-}RMS}$	10 kV
MVAC filter	L_i (i=a,b,c)	10 mH
RMS of LF-MVAC voltage	$U_{LF\text{-}MVac\text{-}RMS}$	10 kV
LF-MVAC filter	L_j , C_j (j=u,v,w)	10 mH, 20 μF
Leakage inductor of HFT	L_r	3 μF
Switching frequency	f_s	10 kHz
Turns ratio of HFT	k	380:10000
Inductance of bridge arm	L_{ij}	10 mH
Rated Power	P_N	2 MW

to DG, switch S_2 is connected to the MVac power grid, and switch S_3 is connected to the distribution network interconnected by the LF-MVac port.

In the above-mentioned seven possible operating modes of I-M3C, the functions from *Mode 1* to *Mode 4* are the same as those of cascaded H-bridge (CHB)-based SST, and the functions of *Mode 5* and *Mode 6* are identical to those of M3C. In *Mode 7*, I-M3C can realize the functions of both CHB-based SST and M3C, so as to realize flexible power transfer between its three ports.

IV. SIMULATION VERIFICATION

A 10-kV/2-MW full power simulation platform of the I-M3C is constructed to verify the effectiveness of the I-FBC's dc bias control strategy and the I-M3C's control strategy based on dual-*dq* coordinate system. The parameters of the simulation platform are listed in Table II. In order to reduce simulation calculation time, the turns ratio of HFT is 380:10 000 to reduce the number of cascaded I-FBCs.

To verify the effectiveness of the dc offset control strategy of I-CC's intermediate transformer. A simulation of I-FBC is built. Connect the U_{dc} port to a 750 V dc voltage source. The turns ratio of HFT is 1:1. The simulation waveform is shown in Fig. 13. Before 0.5 s, the magnetization current appears dc offset. With the increase in time, the transformer will be magnetically saturated. At 0.5 s, the dc offset control strategy is started, and the dc offset is successfully suppressed.

Fig. 14 presents the voltage waveforms of the MVac and LF-MVac ports of the I-M3C before and after the application of dc bias control. At 9 s, the dc bias control strategy is activated, with the dc bias control target set to 0. At this moment, the control loop generates a ΔD_{ij} that is superimposed on the dc duty cycle of 0.5. Each modulation ratio of the upper and lower I-CCs in the I-FBC takes on a part of the dc bias cancellation, and the modulation ratio waveforms are shown in Fig. 14. As can be seen in Fig. 14, the voltages at the MVac port and the LF-MVac port can achieve symmetrical operation, and the dc bias can be completely eliminated through the control strategy.

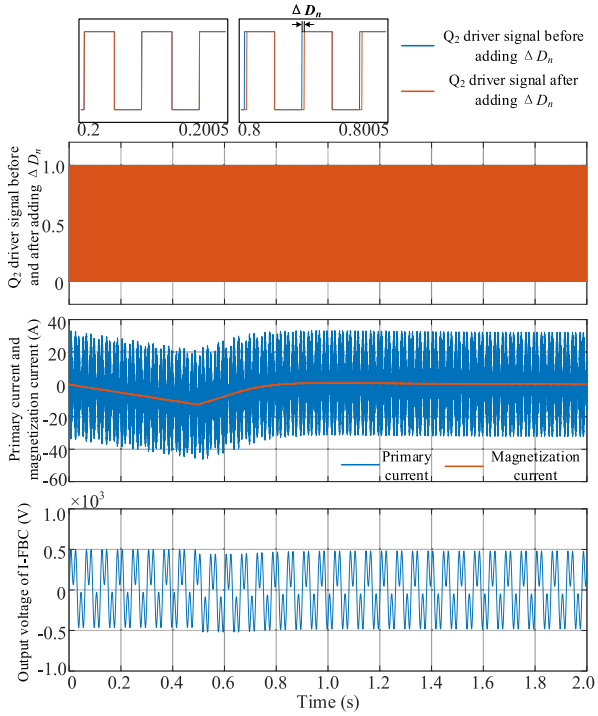

Fig. 13. Simulation waveform before and after DC offset control strategy startup.

Fig. 15 shows the simulation results of the I-M3C's control strategy based on dual-*dq* coordinate system.

Till 0.4 s, the I-M3C operated under steady conditions. The LVdc voltage is stabilized at 750 V, as shown in Fig. 15(a). The LF-MVac voltage is stabilized at 10 kV, which is shown in Fig. 15(d). The power flow direction is from MVac to LVdc, with a size of 2 MW. The LF-MVac port has no load, so there is no active power transmission. There is only a very small reactive power on the filtering device here. The power of the LVdc, MVac, and LF-MVac ports is shown in Fig. 15(g)–(i), respectively.

At 0.4 s, the power of the LVdc port changes from −2 to −1 MW. The power of the MVac port also changes accordingly. The amplitude of MVac current is reduced by half, as shown in Fig. 15(c). The power of the LF-MVac port remains unchanged, as seen in Fig. 15(i). As can be seen in Fig. 15(d), the voltage of the LF-MVac port is controlled to be in a stable state, so the current of the LF-MVac port remains unchanged, which is shown in Fig. 15(e). After a temporary increase of roughly 8 V, the LVdc voltage returned to 750 V after 0.05 s, which is shown in Fig. 15(a).

At 0.7 s, the active power of the LF-MVac port changes from 0 to −0.4 MW, which is shown in Fig. 15(i). The amplitude of the LF-MVac port current increases, as seen in Fig. 15(e). This power is provided by the MVac port, and the active power of the MVac port changes from 1 to 1.4 MW, which is the total active power of the LVdc port and the LF-MVac port, which is shown in Fig. 15(h). After a temporary decrease of approximately 3 V, the LVdc voltage returned to 750 V after 0.05 s, as shown in Fig. 15(a). The voltage of the LF-MVac port experiences a brief fluctuation due to the instantaneous power absorbed by the load.

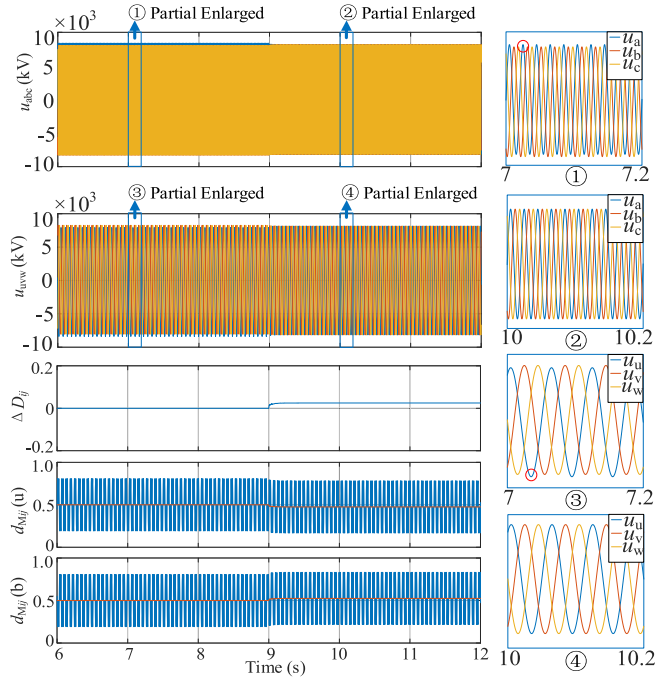

Fig. 14. Voltage waveforms of the MVac and LF-MVac ports of the I-M3C before and after the application of DC bias control.

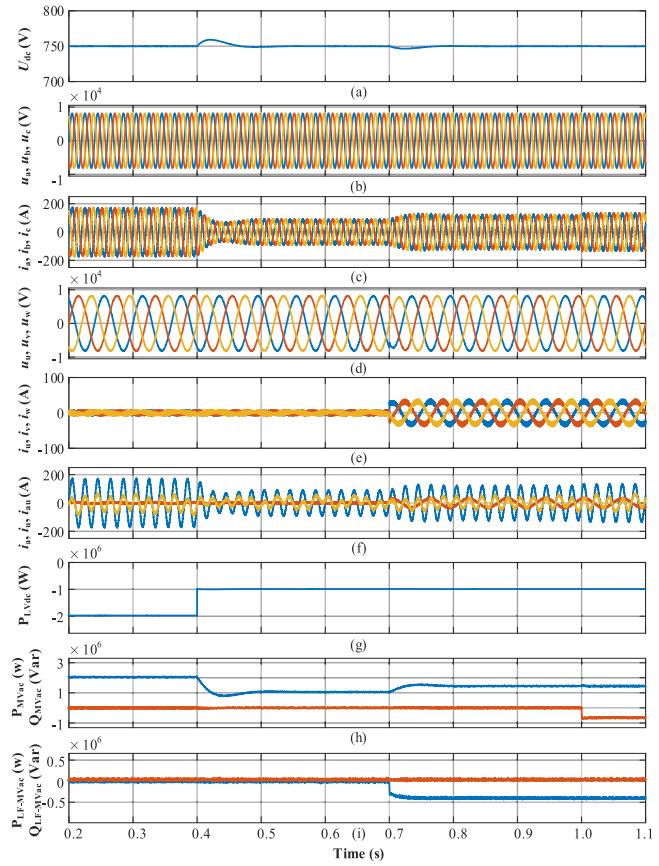

Fig. 15. Closed loop simulation waveforms of I-M3C. (a) LVdc voltage. (b) MVac voltage. (c) MVac current. (d) LF-MVac voltage. (e) LF-MVac current. (f) Bridge arm current of M_{au} conversion unit, a-phase current, and u-phase current. (g) LVdc power. (h) MVac power. (i) LF-MVac power.

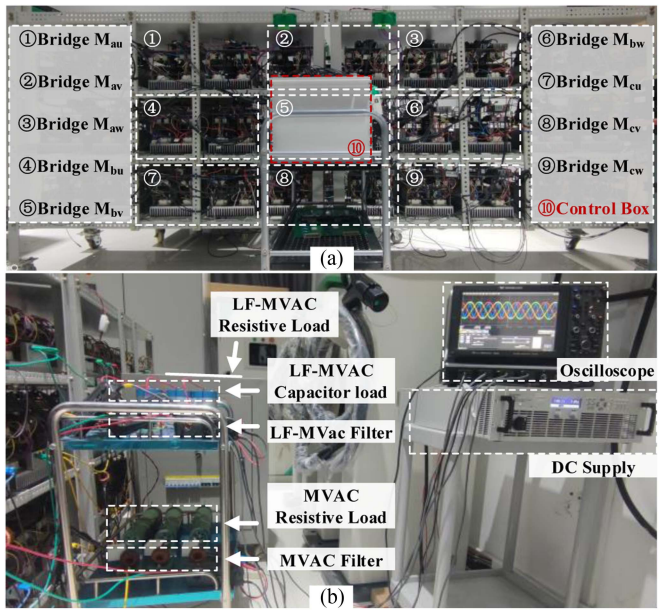

Fig. 16. Experimental prototype of the proposed I-M3C. (a) Front view. (b) Back view.

However, the LF-MVac voltage returns to stability after half a cycle because of the effect of the low-frequency port controller.

At 1.0 s, the control loop on the power-frequency side provides a reactive power command of 0.65 MVar. There is a reactive power of 0.65 MVar, as Fig. 15(h) illustrates. The amplitude of MVac current also increases correspondingly, as shown in Fig. 15(c).

V. Experimental Verification

A 100-V/1-kW experimental prototype of I-M3C is constructed to verify the effectiveness of I-M3C's topology and modulation, which is shown in Fig. 16. The parameters of the experimental prototype are listed in Table III.

A. Experimental Results

Fig. 17 shows the steady-state waveforms of the LVdc, MVac, and LF-MVac ports of the proposed I-M3C. Fig. 17(a) shows the LVdc and MVac voltages. Fig. 17(b) shows the LVdc and LF-MVac voltages. Since the maximum number of channels of the oscilloscope is four. In order to display the voltages of three ports at the same time, the LVdc voltage, the a-phase voltage of the MVac port and the u-phase voltage of the LF-MVac port are given, which is shown in Fig. 17(c). The a-phase voltage and u-phase voltage are analyzed by FFT. It can be seen that the a-phase voltage is 50 Hz and the u-phase voltage is 50/3 Hz. Fig. 17(d) shows the a-phase voltage and b-phase voltage of the MVac port and the u-phase voltage and v-phase voltage of the LF-MVac port. Fig. 17(e) shows the a-phase voltage and a-phase current of the MVac port and the u-phase voltage and u-phase current of the LF-MVac port. The load resistance values of

TABLE III
PARAMETERS OF THE EXPERIMENTAL SYSTEM

Parameter	Symbol	Value
LVDC voltage	U_{dc}	100 V
LVDC capacitor	C_{dc}	2 mF
MVAC Modulation	d_{im} (i=a,b,c)	0.4
AMP of MVAC voltage	$U_{Mvac\text{-}AMP}$	50 V
MVAC filter	L_i	2 mH
LF-MVAC Modulation	d_{jm} (j=u,v,w)	0.4
AMP of LF-MVAC voltage	$U_{LF\text{-}MVac\text{-}AMP}$	50 V
LF-MVAC filter	L_j , C_j	2 mH, 20 μF
Leakage inductor of HFT	L_r	3μF
Switching frequency	f_s	10 kHz
Turns ratio of HFT	k	1:1
Inductance of bridge arm	L_{ij}	5 mH
Rated Power	P_N	1 kW

the MVac and LF-MVac ports are both 10 Ω. The current amplitude is one-tenth of the voltage amplitude.

Fig. 18 shows the steady-state waveforms of the MVac and LF-MVac ports of the proposed I-M3C before filtering. Fig. 18(a) shows the output voltages of M_{au}, M_{av}, and M_{aw} conversion units and the a-phase voltage after filtering. Fig. 18(b) shows the output voltages of M_{au}, M_{av}, and M_{aw} conversion units and the u-phase voltage after filtering. Fig. 18(c) shows the output currents of M_{au}, M_{av}, and M_{aw} conversion units and the a-phase current after filtering. Fig. 18(d) shows the output currents of M_{au}, M_{av}, and M_{aw} conversion units and the u-phase current after filtering. It can be seen that the output voltage of the conversion unit is a high-frequency variable. The output current of the conversion unit does not include high-frequency variables due to the effect of the bridge arm inductance, only power-frequency and low-frequency variables. Fig. 19 shows the steady-state voltage waveforms of the corresponding bridge arm inductances of u-phase.

Fig. 20 shows the transient current waveforms of the MVac and LF-MVac ports with resistance loads under a sudden change in loads at the LF-MVac port. In the initial stage, the loads of the MVac port are 10 Ω, and the loads of the LF-MVac port are infinite. At a certain moment, the loads of the LF-MVac port are changed from infinity to 15 Ω. It can be seen that the currents of the LF-MVac port instantly increase from 0 to around 2.3 A and transits to a new steady state. The currents of the MVac port remain unchanged.

Fig. 21 shows the transient voltage and current waveforms of the MVac and LF-MVac ports with the resistance loads under a sudden change in loads at the LF-MVac port. In the initial stage, the loads of the MVac port are 10 Ω, and the loads of the LF-MVac port are 30 Ω. At a certain moment, the loads of the LF-MVac port are changed from 30 to 10 Ω. It can be seen that the currents of the LF-MVac port instantly increase from 1.3 to around 3.5 A.

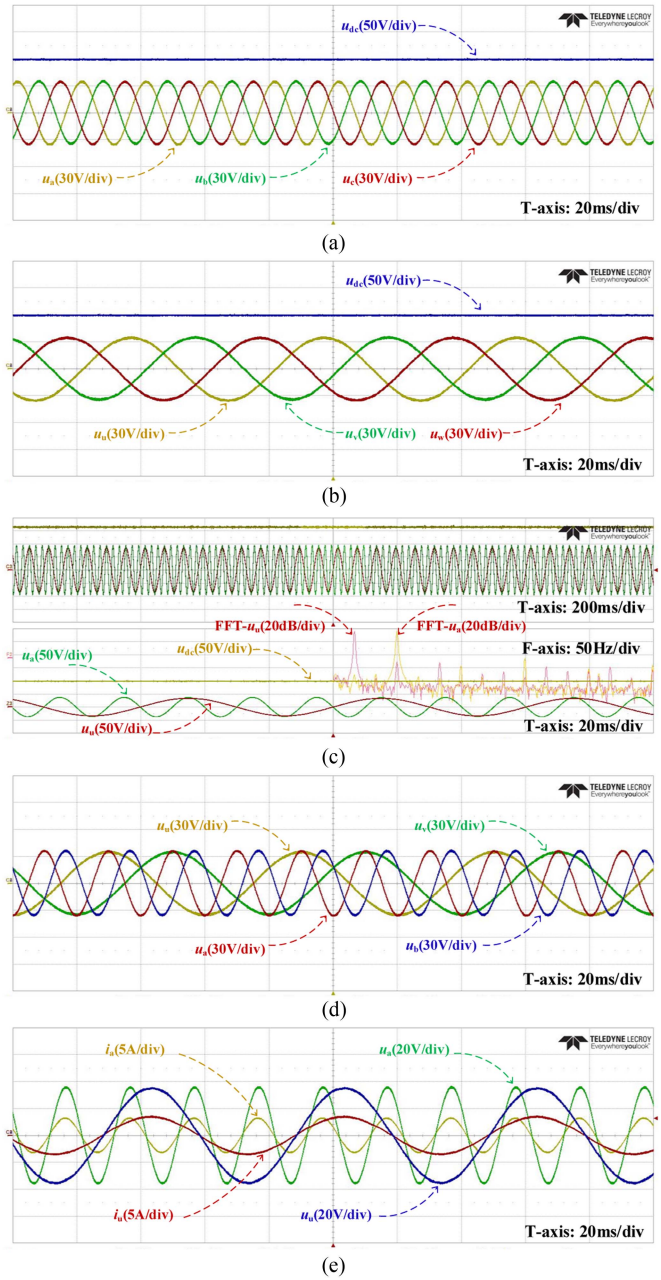

Fig. 17. Steady-state waveforms of LVdc, MVac, and LF-MVac ports of the proposed I-M3C. (a) u_a, u_b, u_c, and u_{dc}. (b) u_u, u_v, u_w, and u_{dc}. (c) u_{dc}, u_a, u_u, and FFT analysis results of u_a, u_u . (d) u_a, u_b, u_u, and u_v. (e) u_a, i_a, u_u, and i_u.

Fig. 22 shows the transient voltage and current waveforms of the MVac and LF-MVac ports with resistance and capacitance loads under a sudden change in loads at the LF-MVac port. In the initial stage, the loads of the MVac port are 10 Ω, and the loads of the LF-MVac port are −j17.65 Ω. At a certain moment, the loads of the LF-MVac port are changed from −j17.65 to 15-j17.65 Ω. It can be seen that the impedance angle changes from −90° to −49°.

Fig. 23 shows the transient voltage and current waveforms of the MVac and LF-MVac ports with resistance-inductance loads

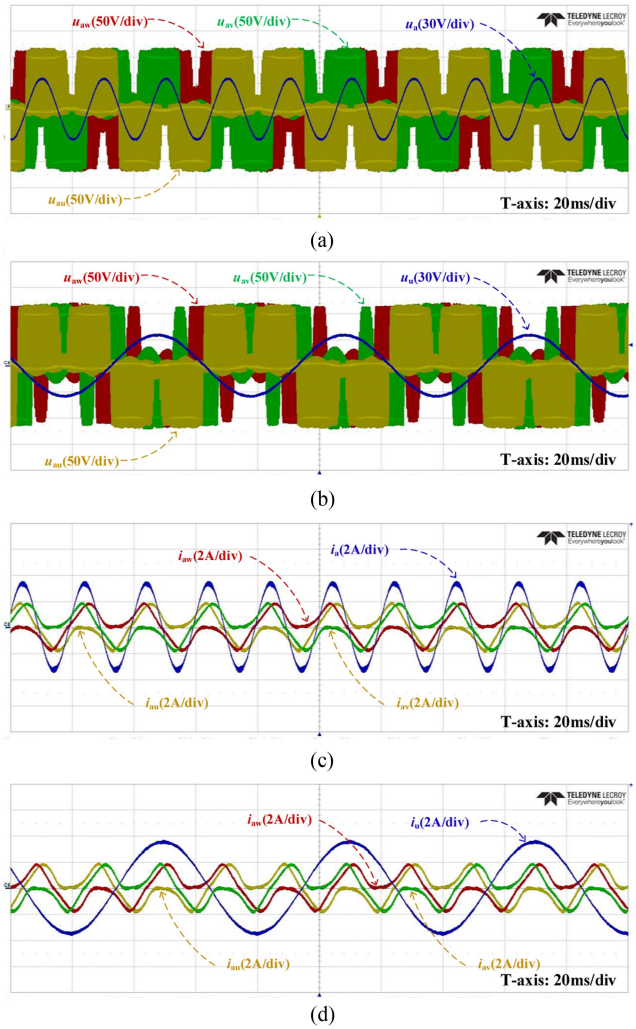

Fig. 18. Steady-state waveforms of MVac and LF-MVac ports of the proposed I-M3C before filtering. (a) u_{au}, u_{av}, u_{aw}, and u_{a}. (b) u_{au}, u_{av}, u_{aw}, and u_{u}. (c) i_{au}, i_{av}, i_{aw}, and i_{a}. (d) i_{au}, i_{av}, i_{aw}, and i_{u}.

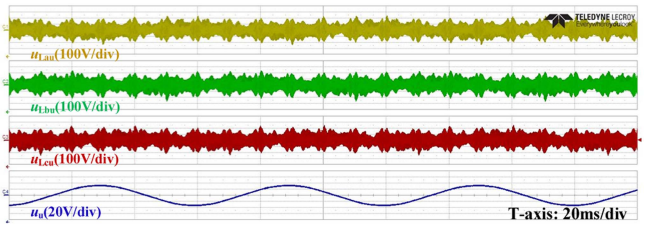

Fig. 19. Steady-state voltage waveforms of the corresponding bridge arm inductances of u-phase.

under a sudden change in loads at the LF-MVac port. In the initial stage, the loads of the MVac port are 10 Ω, and the loads of the LF-MVac port are j15.7 Ω. At a certain moment, the loads of the LF-MVac port are changed from −j15.7 Ω to 10+j15.7 Ω. It can be seen that the impedance angle changes from 90° to 57°.

To sum up, it can be seen that the proposed I-M3C has good steady-state and transient performance.

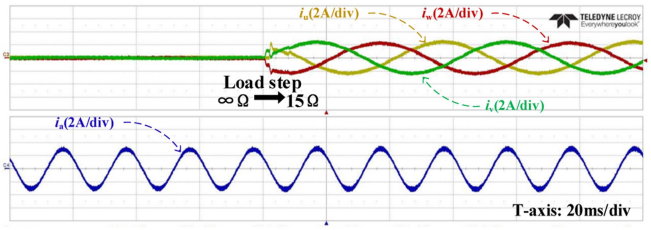

Fig. 20. Three-phase transient current waveform of the LF-MVac port and a-phase transient current waveform of the MVac port when resistance loads suddenly change at the LF-MVac port.

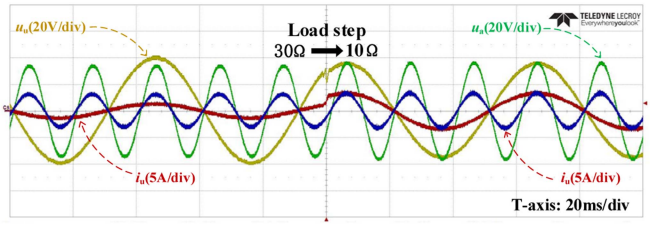

Fig. 21. A-phase transient voltage and current waveforms of the MVac port and u-phase transient voltage and current waveforms of the LF-MVac port when resistance loads suddenly change at the LF-MVac port.

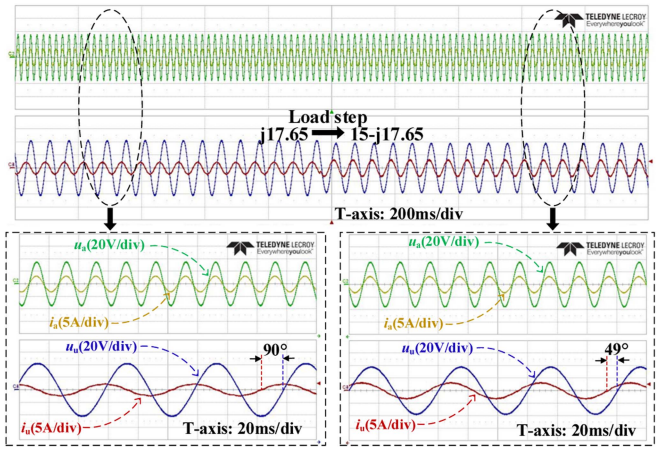

Fig. 22. A-phase transient voltage and current waveforms of the MVac port and u-phase transient voltage and current waveforms of the LF-MVac port when resistance-capacitance loads suddenly change at the LF-MVac port.

B. *Efficiency Analysis*

The principles of the proposed topology were validated on a 300-kW prototype. However, considering the limitations of the laboratory power supply and load capacity, an approximate method is adopted to determine its efficiency curve. Specifically, the efficiency of an I-FBC module was analyzed to obtain the efficiency curve of the proposed topology. (Theoretical calculation data: rated power 15 kW, rated voltage 300 V, rated current 50 A; Experimental test data: 10%–60% of the rated power.)

The losses of I-FBC mainly include the loss of IGBTs, the loss of HFTs, and the loss of the LC filter. The number of IGBTs is sixteen. The number of HFTs is two. The LC filter contains an inductor and a capacitor.

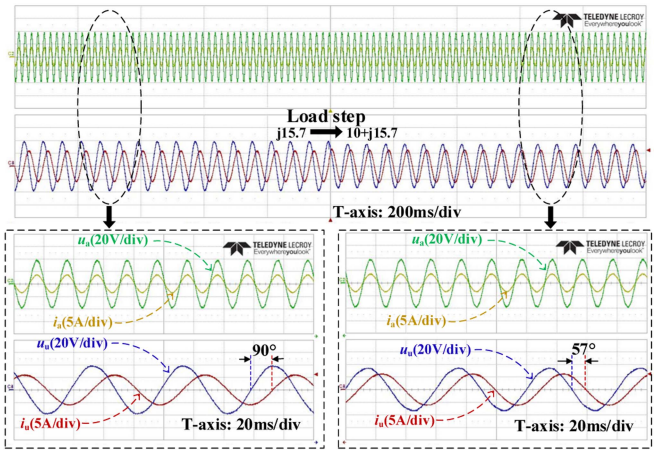

Fig. 23. A-phase transient voltage and current waveforms of the MVac port and u-phase transient voltage and current waveforms of the LF-MVac port when resistance-inductance loads suddenly change at the LF-MVac port.

The losses of IGBT mainly include conduction loss and switching loss [33]. The conduction loss of IGBT is calculated through its saturation voltage drop and the effective value of the current flowing through it. As shown in (9), the switching loss of IGBT is determined by its turn-ON energy, turn-OFF energy, and switching frequency

$$\begin{cases} P_{\text{con}} = V_{\text{CEsat}} \times I_{\text{crms}} \\ P_{\text{sw}} = (E_{\text{on}} + E_{\text{off}}) \times f_{\text{sw}} \end{cases} \tag{9}$$

where P_{con} is the conduction loss; P_{sw} is the switching loss; $V_{\text{CE sat}}$ is the collector-emitter saturation voltage; I_{crms} is the effective value of current flowing through IGBT; E_{on} is the turn-ON energy of IGBT; E_{off} is the turn-OFF energy of IGBT; f_{sw} is the switching frequency; $V_{\text{CE sat}}$, E_{on} and E_{off} can be found in the datasheet of FF200R06KE3.

Transformer losses mainly include core loss and winding loss [34], and the calculation equation is as follows:

$$\begin{cases} P_{\text{Fe}} = F_{\text{w,c}} C_{\text{m}} \times f^{\alpha} \times B_{\text{m}}^{\beta} \times V_{\text{e}} \\ P_{\text{Cu}} = I_{\text{rms}}^2 \cdot R_{\text{winding}} \end{cases} \tag{10}$$

where P_{Fe} is the core loss; P_{Cu} is the winding loss; f is the frequency. $F_{\text{w,c}} C_{\text{m}}$, α, and β are Steinmetz constants under square-wave excitation, the Steinmetz constants of ferrite are $F_{\text{w,c}} C_{\text{m}} = 3.86 \times 10^{-6}$, $\alpha = 1.63$, $\beta = 2.62$. B_{m} is saturation flux density, which is 0.5 T for ferrite material; I_{rms} is the effective value of transformer current; V_{e} is the volume of the magnetic core, it can be found in the datasheet of B67355; R_{winding} is winding resistance, its value is 30 mΩ.

The loss calculation equation of the filter inductor is the same as that of the transformer. It is only due to the difference between the magnetic core and winding that the parameters of V_{e} and R_{winding} are different. The loss of the filter inductor can be obtained by substituting V_{e} and R_{winding} of the filter inductor into (10). The value of V_{e} can be found in the datasheet of B64290L0659, and the value of R_{winding} is 50 mΩ.

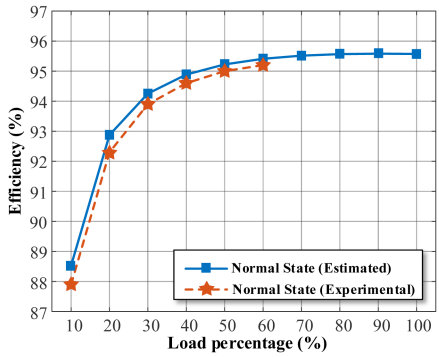

Fig. 24. Efficiency curve of the proposed SST.

The loss calculation equation of the filter capacitor is shown in the following equation [35]:

$$P_{\text{Cap}} = (I_{\text{L.rms}} - I_{\text{R.rms}})^2 \times R_{\text{Cap}} \tag{11}$$

where P_{Cap} is the filter capacitor loss; $I_{\text{L.rms}}$ is the filter inductor current; $I_{\text{R.rms}}$ is the load current; R_{Cap} is the equivalent series resistance (ESR) of the filter capacitor, R_{Cap} can be found in the datasheet of MKP-C4BT, and the value of R_{Cap} is 1.7×10^{-3} Ω.

The total loss calculation equation is shown in the following equation:

$$\begin{aligned} P_{\text{loss}} = {} & P_{\text{con}} + P_{\text{sw}} + P_{\text{Fe-HFT}} + P_{\text{Cu-HFT}} + P_{\text{Fe-inductor}} \\ & + P_{\text{Cu-inductor}} + P_{\text{Cap}} \end{aligned} \tag{12}$$

The efficiency calculation equation is shown in the following equation:

$$\eta = \frac{P_{\text{o}}}{P_{\text{in}}} \times 100\% = \frac{P_{\text{in}} - P_{\text{loss}}}{P_{\text{in}}} \times 100\%. \tag{13}$$

Fig. 24 shows the efficiency curve of the proposed SST. The solid line is the theoretical calculation efficiency, and the dotted line is the actual measurement efficiency. The full load efficiency calculated theoretically is 95.6%, and the 60% load efficiency measured by the I-FBC is 95.2%. Due to the limited load power in the laboratory, only 60% of the rated power can be tested.

The efficiency of CHB-based SST in reference [36] is 95.4%. The isolated dc/dc converter of CHB-based SST in reference [37] is a quad active bridge (QAB), and the QAB efficiency is 97%. If the CHB loss is taken into account, the SST efficiency will not exceed 96%. In [38], the rectifier power stage submodule's efficiency of MMC-based SST is 97%, and the efficiency of QAB is 96%, so the SST efficiency is about 93.12%. In [39], the efficiency of MMC-based SST is 96%.

The efficiency of the proposed SST is similar to that of other SSTs, and its unique LF-MVac port is not available in other SSTs.

C. Comparison With Other SSTs

A detailed comparison among the proposed SST and other similar SSTs is illustrated in Table IV. The comparison issues include basic port configuration, port number, conversion stages,

TABLE IV
COMPARISON OF PROPOSED SST WITH OTHER SSTS

Parameters	Xiao et al. [40]	Briz et al. [41]	Liu et al. [30]	Presented work
SST type	CHB	MMC	I-MMC	I-M3C
MVAC port	Yes	Yes	Yes	Yes
MVDC port	No	Yes	Yes	No
LF-MVAC port	No	No	No	Yes
LVDC port	Yes	Yes	Yes	Yes
LVAC port	Yes	Yes	Yes	Yes
Port number	3	4	4	4
Conversion stages	3	3	2	2
Individual Cap	Needed	Needed	No need	No need
SM's balance	Needed	Needed	No need	No need
Control difficulty	Difficult	Difficult	Simple	Simple

control difficulty, and so on. The characteristics and comparative analysis of each SST are described as follows.

The CHB-based SST in [40] has three ports, including MVac, LVdc, and LVac ports. In addition to the power conversion function of the conventional transformer from MVac side to LVac side, CHB-based SST can also provide an LVdc port for flexible access to DG. However, since it lacks an MVdc port or an LF-MVac port, it cannot be interconnected with other substations to achieve flexible power regulation.

The MMC-based SST in [41] has four ports, including MVac, MVdc, LVdc, and LVac ports. In addition to the basic functions of the CHB-based SST, the MMC-based SST can achieve interconnected with other MV substations to realize flexible power regulation. Since the above-mentioned two SSTs both require adding a large capacitor between the rectifier power stage and the isolated power stage to suppress the second-order harmonic fluctuations, it is necessary to configure a corresponding voltage-balancing and coordinated control strategies, which increases the difficulty of SST control.

The I-MMC-based SST in [30] has the same port configuration as the MMC-based SST. If the low-voltage dc/ac converter at the SST's rear stage is not considered, it can achieve single-stage three-port power conversion among its MVac, MVdc, and LVdc ports. Simultaneously, because it eliminates the individual capacitor between the rectifier power stage and the isolated power stage, there is no need for the complex voltage-balancing control strategy, and the control system is greatly simplified.

The proposed SST has all the advantages of I-MMC-based SST, such as single-stage power conversion, simpler control system, and so on. Compared with the above SSTs, because of its unique LF-MVac port, it can be used as the key equipment to realize the LF-MVac interconnection between smart distribution networks. It is worth noting that the proposed SST cannot provide an MVdc port.

VI. CONCLUSION

This article proposes a novel SST topology with LF-MVac port. The proposed SST has the following advantages.

1) Compared with the other SSTs, the proposed SST has an LF-MVac port, which can provide key equipment for smart distribution networks based on LF-MVac interconnection.
2) Compared with M3C, the I-M3C at the proposed SST's front stage has an LVdc port, which can meet the future demand of medium- and low-voltage smart distribution networks for the access of distributed renewable energy.
3) The I-M3C at the proposed SST's front stage does not require a complex multistage coordinated control strategy or voltage-balancing control strategy. And the stable operation of the I-M3C can be realized by using a control strategy based on dual-*dq* coordinate system.

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