Improved Triple-Switch Triple Mode DC–DC Converter With Suppressed Voltage Oscillations

Motiur Reza Mohammed, *Member, IEEE*, Vinod Khadkikar, *Fellow, IEEE*, Bashar Zahawi, *Senior Member, IEEE*, and Omar Alzaabi, *Member, IEEE*

***Abstract*—Triple switch, triple mode (TSTM) dc–dc converters find extensive utilization in renewable energy applications. Unlike other dc–dc converters, TSTM converters operate with two duty cycles (d, d_1), achieving maximum power point tracking (MPPT) and output voltage regulation simultaneously. However, these converters often exhibit high voltage stress on the switches due to resonance caused by mismatched switch/inductor parameters. This article proposes a new TSTM dc–dc converter for high voltage gain with low voltage stress. The advantages of the proposed converter include the following: 1) elimination of resonance due to parameters mismatch, resulting in the suppression of voltage oscillations, 2) flexibility to regulate the output voltage with two duty cycles, and 3) high voltage gain over a wide range of duty cycles. The article provides a detailed explanation of the converter topology, working principle, steady-state analysis, external characteristics, and closed-loop controller design. The design guidelines and performance comparison are also presented. A 460-W laboratory setup is built, and experimental verification is conducted for the voltage conversion from 24 to 272 V.**

***Index Terms*—DC–DC converter, reduced voltage stress, switched capacitor (SC), triple switch triple mode (TSTM) converters, voltage oscillation.**

I. Introduction

HIGH-GAIN dc–dc converters play a crucial role in renewable energy systems, and fuel cell applications. [1], [2], [3]. The output voltage of renewable energy sources and fuel cells tends to be low and fluctuating [4], [5]. In renewable energy systems and fuel cells, a dc–dc converter regulates the output voltage level of the renewable sources to match the utility demand [2]. High-gain dc–dc converters can be categorized as isolated or nonisolated, depending on whether magnetic isolation is used between the input and output terminals. Magnetic isolation requires a high-frequency transformer (HFT), which causes voltage spikes in power switches due to the leakage inductance [6]. The absence of magnetic isolation in a nonisolated converter significantly reduces both the size and cost of the converter.

Numerous high-gain nonisolated dc–dc converters based on the coupled inductor [7], Z/quasi-Z network [3], [8], [9], switched capacitors (SC) network [3], [10] and switched inductors (SL) network [3], [11], [12] techniques are discussed in literature. Converters utilizing coupled inductors [3], [7] leverage the number of turn ratios as an additional degree of freedom to achieve high voltage gain. However, these converters are associated with high input current ripples, voltage spikes across the switch, and leakage inductance. Clamped circuits are needed to suppress the voltage spike, thereby, increasing the cost and size of the converter [3], [7]. The converters employing SC networks can increase the voltage gain according to the number of SC networks. However, SC networks often experience high current stress due to the alternate charging and discharging of the capacitors.

In [11], an active switched inductor (ASL) is utilized to enhance the voltage gain with low switch voltage stress. However, the diode voltage stress in this converter is higher than the output voltage. Subsequently, several hybrid structures derived by combining ASL networks with SC networks have been explored in the literature [12], [13], [14], [15], [16], [17], [18], [19], [20], [21]. In [12], an ASL network and SC network based hybrid converter is presented and implemented with a photovoltaic source. The SC network used in this structure forms a low-impedance path through the switches, resulting in increased switch current stress. In [13], the authors integrated an asymmetric ladder-SC network with the ASL network for achieving high voltage gain. Like the converter presented in [12], this converter experiences high current stress in the switches due to the low impedance path. To limit the inrush current, a soft start technique is required, thereby, affecting the dynamic performance, especially during frequent starts and stops. In [14], a ladder SC network is merged with a regenerative-boost arrangement and integrated with the ASL network to improve the voltage gain. The regenerative-boost arrangement adds one switch and one inductor to the converter presented in [13], increasing the size and cost of the converter significantly. In [15] and [16], ASL-based converters with quadratic voltage gain are derived by adding a diode-capacitor across the switch of the ASL network. This constitutes a low-impedance path for the switch, resulting in a very high inrush current. Also, the asymmetrical structure of these converters increases the conduction losses due to unequal current stress in the switches and inductors. The

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The authors are with the Advanced Power and Energy Center (APEC), Electrical Engineering Department, Khalifa University, Abu Dhabi 127788, UAE (e-mail: motiur.mohammed@ku.ac.ae; vinod.khadkikar@ku.ac.ae; bashar.zahawi@ku.ac.ae; omar.alzaabi@ku.ac.ae).

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converters presented in [17] and [18] are derived by replacing the simple inductor of the ASL-leg presented in [11] with a passive switched inductor network. These converters use a considerable number of inductors and diodes. The drawbacks of these converters are their very large size, high cost, and low efficiency. In general, the integration of the SC network and ASL network provides high voltage gain. However, issues related to the current spikes in the diodes and switches are inevitable due to bulky SC networks. Moreover, ASL converters are highly sensitive to inductor values and the output capacitance of the switches. During switch-OFF, the inductors form a resonance circuit with the output capacitors of the switches, leading to increased switch voltage stress and decreased efficiency [19], [20], [21]. In [22], a hybrid converter integrating ASL network with quasi-Z-source network is proposed. While this converter achieves a significantly improved voltage gain, it has the drawback of a limited duty cycle ($d \leq 0.5$). Converters with limited duty cycle ranges are very sensitive to any change in the duty cycle value [23].

In [24], a triple switch, triple mode (TSTM) dc–dc converter, derived by integrating a unidirectional switch into the ASL network, is developed. This converter operates with two duty cycles (d and d_1) enhancing the voltage gain. Furthermore, it offers flexibility in output voltage regulation through different combinations of duty cycles, thereby, improving overall efficiency. The voltage lift cell and SC networks are employed to achieve higher voltage gain. In [25], [26], [27], and [28], voltage lift cells are added to the TSTM converter at the input terminals, which increases the current stresses in the switches. In addition, the voltage stress on the output diode and unidirectional switch in converters [24], [25], [26], [27] is higher than the output voltage.

In [29], [28], and [30], voltage gain improvement is achieved by replacing the simple inductors of the ASL network with a passive switched inductor network. However, these converters become bulky due to the increased number of inductors and diodes. In [31], the flexibility of the following three control schemes for hybrid TSTM converter with: 1) controlling d and fixed d_1, 2) fixed d and controlling d_1, and 3) controlling both d and d_1 is discussed. However, TSTM converters [24], [25], [26], [27], [28], [29], [30], [31] exhibit resonance between the inductors and output capacitors of the switches when turned OFF. This resonance results in increased voltage stress on the switches, leading to decreased efficiency.

In this article, a novel TSTM dc–dc converter obtained by integrating ASL and SC networks to achieve high voltage gain is proposed. The characteristics of the proposed converter are summarized as follows.

1) The output capacitor is split into two capacitors. Each capacitor supports one switch of the ASL network when they are turned OFF. Consequently, the voltage oscillation across the switches is eliminated, and the voltage stress across the switch is reduced.
2) The converter has a constant potential difference between the input and output terminals. Therefore, any EMI issues associated with $\frac{dv}{dt}$ are minimized [10].
3) The proposed converter operates with two duty cycles (d, d_1) and offers the flexibility to achieve the desired voltage gain with different combinations of duty cycles. The operational efficiency of the converter can be improved by properly selecting the duty cycles for a given voltage gain.
4) The proposed converter offers several external characteristic curves corresponding to distinct values of d_1. In addition, it has various continuous conduction mode (CMM) and discontinuous conduction mode (DCM) boundaries depending on the value of d_1.
5) The proposed converter possesses three degrees of freedom for controller design, with options such as the following: 1) controlling d and fixing d_1, 2) fixing d and controlling d_1, and 3) controlling both d and d_1.
6) The proposed converter utilizes ASL and SC networks and achieves high voltage gain over a wide range of duty cycles. Unlike converters with limited duty cycle ($d \leq 0.25, d \leq 0.33$, and, $d \leq 0.5$), this converter is less sensitive to any change in the duty cycle value [23].

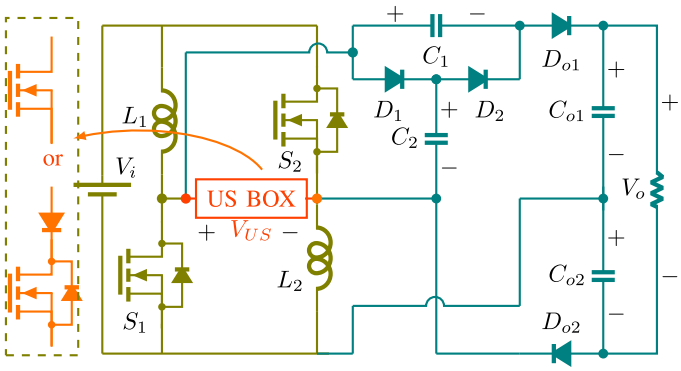


Fig. 1. Proposed high gain TSTM DC–DC converter.

The rest of this article is organized as follows. In Section II, the topology and operating modes of the proposed converter are studied. In Section III, the steady-state analysis, including analytical considerations for CCM, DCM, external characteristics, and an exploration of the influence of nonideal parameters on voltage gain and suppression of voltage oscillation, is added. Sections IV, V, VI, and VII present performance comparisons, design procedures, power loss analysis, and controller design, respectively. The performance of the proposed converter is verified experimentally in Section VIII. Finally, Section IX concludes this article.

II. Proposed Converter and Operating Principle

The proposed TSTM dc–dc converter, shown in Fig. 1, consists of two switches (S_1 and S_2), two inductors (L_1 and L_2), four capacitors (C_1, C_2, C_{o1} and C_{o2}), four diodes (D_1, D_2, D_{o1} and D_{o2}), and a unidirectional switch (US Box). The US box can be realized through either a series combination of a diode with a MOSFET or an IGBT to ensure the unidirectional flow of current. Figs. 2 and 3 depict operational waveforms and circuit conditions of the proposed converter.

Mode-1 [t_o-t_1]: In this mode, both S_1 and S_2 are turned ON, and D_2 is conducting as depicted in Fig. 3(a). The input voltage V_i charges the inductors L_1 and L_2 through S_1 and S_2, respectively, causing the inductor currents to increase linearly.

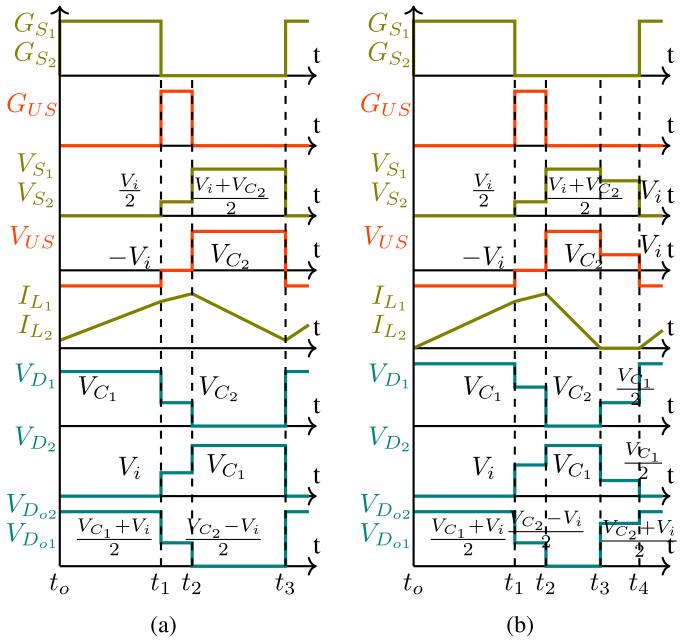


Fig. 2. Key waveforms of the proposed converter for (a) CCM and (b) DCM operations.

In addition, V_i and C_2 charge C_1 through D_2, S_1, and S_2, while C_{o1} and C_{o2} supply power to the load. Here

$$v_{L_1} = v_{L_2} = V_i, \quad V_{C_1} = V_{C_2} + V_i, \quad V_{C_{o1}} + V_{C_{o2}} = V_o \tag{1}$$

$$i_{c_{1,1}} = i_{c_{2,1}} = i_{s_1} - I_{L_1} = i_{s_2} - I_{L_2}\ , i_{c_{o1,1}} = i_{c_{o2,1}} = -I_o \tag{2}$$

where V_x and i_y represent the voltage across the element x; x $\in \{L_1, L_2, C_1, C_2, C_{o1}, C_{o2}\}$, the current in the element y; $y \in \{L_1, L_2, S_1, S_2\}$, and $i_{C,i}$ denotes current in the capacitors C; C $\in \{C_1, C_2, C_{o1}, C_{o2}\}$.

Mode-2 [t_1-t_2]: At instant $t = t_1$, S_1 and S_2 turned OFF, and US BOX is turned ON. Consequently, the inductors L_1, and L_2 are connected in series and are energized by V_i through the US box. As L_1 and L_2 are in series, their charging rate is reduced to half as shown in Fig. 3(b). Also, the output capacitors C_{o1} and C_{o2} supply power to the load. Thus

$$v_{L_1} + v_{L_2} = V_i\ , i_{c_{o1,2}} = i_{c_{o2,2}} = -I_o. \tag{3}$$

Mode-3 [t_2-t_3]: At $t = t_2$, all active switches are turned OFF, and D_1, D_{o1}, and D_{o2} are conducting. The circuit condition is illustrated in Fig. 3(c). In this mode, V_i, v_{L_1}, and v_{L_2} charge capacitor C_2. In addition, V_i, v_{L_1}, and v_{L_2} together with V_{C_1} supply power to the load. In this mode

$$v_{L_1} + v_{L_2} = V_i - V_{C_2}\ , V_{C_1} + V_{C_2} = V_o \tag{4}$$

$$I_{L_1} = I_{L_2} = i_{c_{1,3}} + i_{c_{2,3}}\ , i_{c_{o1,3}} + i_{c_{o2,3}} + I_o = -i_{c_{1,3}}. \tag{5}$$

Mode-4 [t_3-t_4]: Mode-4 arises at $t = t_3$ when the currents in both inductors become zero. Consequently, all semiconductor devices are nonconducting, and the load is supplied through

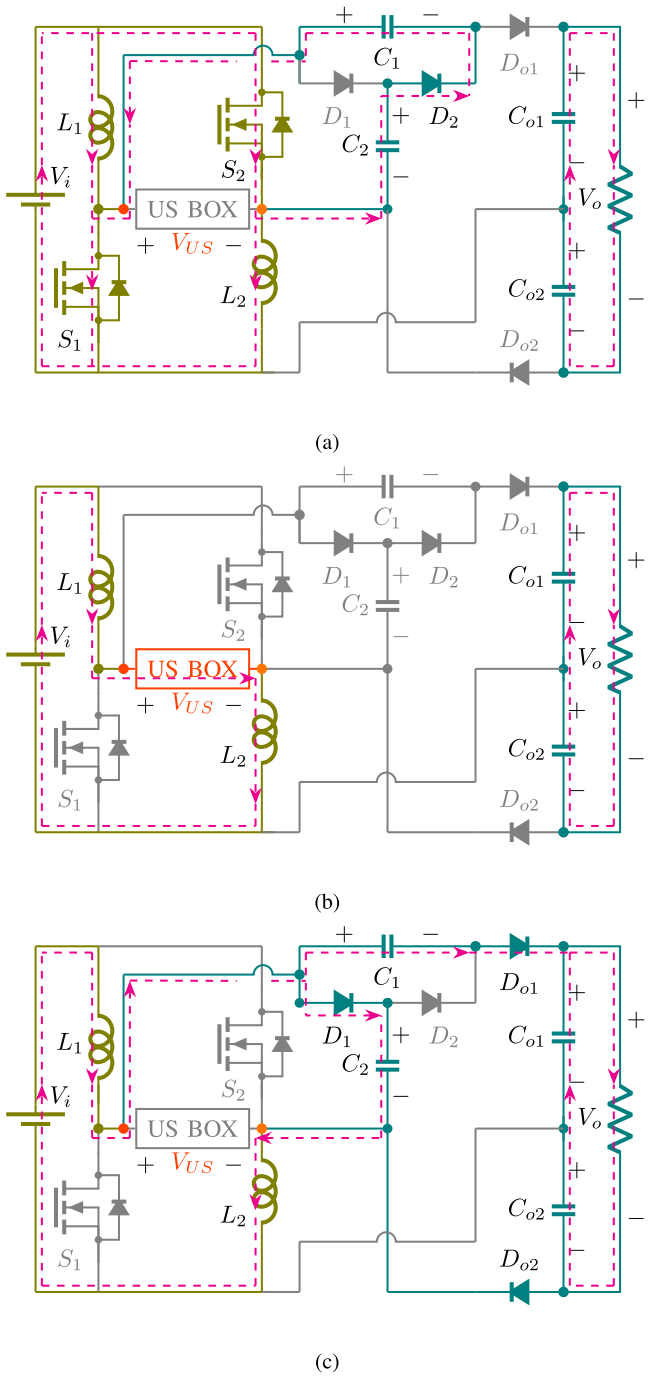


Fig. 3. Circuit conditions of the proposed converter in (a) Mode-1, (b) Mode-2, and (c) Mode-3.

C_{o1} and C_{o2}. In Mode-4, the converter is operating in DCM as shown in Fig. 2(b).

III. Steady State Analysis

A. CCM Analysis

In CCM operation, Fig. 2(a) and Fig. 3 illustrate that the proposed converter operates in Mode-1, Mode-2, and Mode-3. In the following section, the voltage gain, voltage stress, and current stress are analyzed.

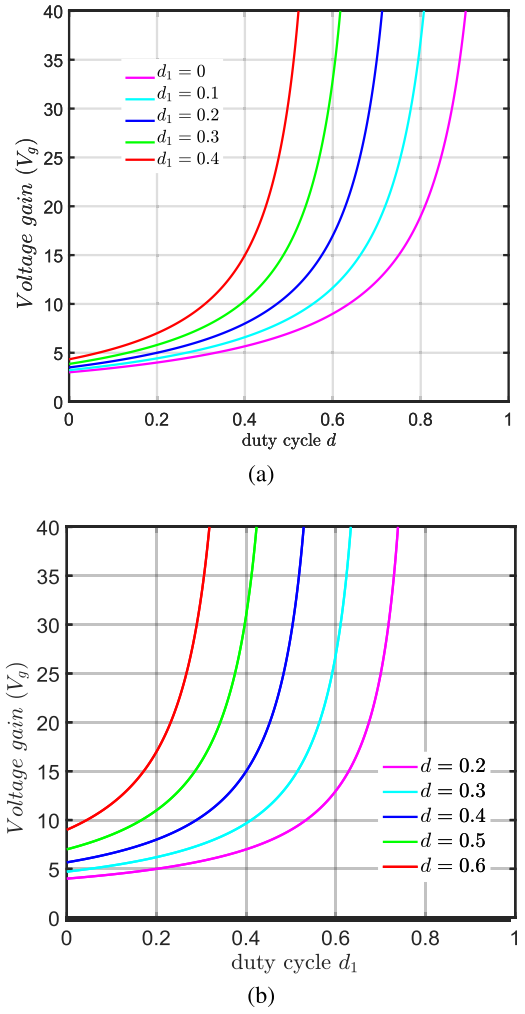


Fig. 4. Voltage gain versus (a) duty cycle d and (b) duty cycle d_1.

1) Voltage Gain: From the volt-second balance equation of L_1 and L_2 over a switching period T_s, the voltage across capacitors C_1, C_2, and the voltage gain (V_g) are obtained as

$$V_{C_1} = \frac{(2-d_1)V_i}{1-d-d_1}, \quad V_{C_2} = \frac{(1+d)V_i}{1-d-d_1},$$
$$V_g = \frac{(3+d-d_1)}{1-d-d_1}. \tag{6}$$

The curves depicting the voltage gain of the proposed converter with different duty cycles are shown in Fig. 4. As seen from Fig. 4(a), the converter can achieve a high gain (say 35) at a low duty cycle (d = 0.6) by adjusting d_1 to 0.3. Also, Fig. 4(a) illustrates that the converter can achieve a high gain (says 35) at low d_1 (=0.4) by changing d to 0.5. Furthermore, from Fig. 4(a) and (b), it can be observed that a desired voltage gain (say 25) can be obtained with different combinations of duty cycles, such as (0.846,0), (0.754,0.1), (0.662,0.2), and (0.569,0.3) corresponding to (d, d_1). Thus, the proposed converter can achieve high gain over a wide range with the flexible combination of duty cycles.

TABLE I
CURRENT STRESS IN POWER DEVICES

Currents	I_{S_1}, I_{S_2}	I_{D_1}	I_{D_2}	$I_{D_{o1}}$, $I_{D_{o2}}$
Peak	$\frac{(1+d-d_1)I_o}{d(1-d-d_1)}$	$\frac{I_o}{1-d-d_1}$	$\frac{I_o}{d}$	$\frac{I_o}{1-d-d_1}$
Average	$\frac{(1+d-d_1)I_o}{(1-d-d_1)}$	I_o	I_o	I_o
RMS	$\frac{(1+d-d_1)I_o}{(1-d-d_1)\sqrt{d}}$	$\frac{I_o}{\sqrt{1-d-d_1}}$	$\frac{I_o}{\sqrt{d}}$	$\frac{I_o}{\sqrt{1-d-d_1}}$

2) Voltage Stress: From Fig. 3(a), the voltage stress across D_1, D_{o1}, D_{o2}, and the US box are given by

$$V_{D_1} = 2V_{D_{o1}} = 2V_{D_{o2}} = \frac{(2-d_1)V_o}{3+d-d_1}, \; V_{US} = -V_i. \tag{7}$$

From Fig. 3(b), the voltage stress across S_1, S_2, D_1, D_2, D_{o1}, and D_{o2} are calculated as

$$V_{S_1} = V_{S_2} = \frac{V_i}{2}, \; V_{D_2} = V_i, \; V_{D_1} = V_{C_2} = \frac{(1+d)V_o}{3+d-d_1} \tag{8}$$

$$V_{D_{o1}} = V_{D_{o2}} = \frac{V_o - V_{C_1}}{2} = \frac{(1+d)V_o}{2(3+d-d_1)}. \tag{9}$$

From Fig. 3(c), the voltage stress across S_1, S_2, D_2, and the US box are calculated as follows:

$$V_{S_1} = V_{S_2} = \frac{V_i + V_{C_2}}{2} = \frac{(2-d_1)V_o}{2(3+d-d_1)} \tag{10}$$

$$V_{D_2} = \frac{(2-d_1)V_o}{3+d-d_1}, \; V_{US} = \frac{(1+d)V_o}{3+d-d_1}. \tag{11}$$

From (7), (8), (9), (10), and (11), the maximum voltage stress on the power devices are

$$V_{S_1} = V_{S_2} = V_{D_{o1}} = V_{D_{o2}} = \frac{(2-d_1)V_o}{2(3+d-d_1)} \tag{12}$$

$$V_{D_1} = V_{D_2} = \frac{(2-d_1)V_o}{3+d-d_1} \tag{13}$$

$$V_{US} = \frac{(1+d)V_o}{3+d-d_1}. \tag{14}$$

3) Current in Inductors: To determine the current in inductors, the knowledge of the current in the capacitors is required. From the conversation of charges in the capacitors, the current in capacitors is obtained as follows:

$$i_{c_{o1,3}} = i_{c_{o2,3}} = \frac{(d+d_1)I_o}{1-d-d_1}, \; i_{c_{1,3}} = \frac{I_o}{1-d-d_1} \tag{15}$$

$$i_{c_{1,1}} = i_{c_{2,1}} = \frac{I_o}{d}, \; i_{c_{2,3}} = \frac{I_o}{1-d-d_1}. \tag{16}$$

From Fig. 3(c), the current in the inductors is given as follows:

$$I_{L_1} = I_{L_2} = \frac{2I_o}{1-d-d_1} \tag{17}$$

4) Current Stress: Fig. 3(a), (b), and (c) show the conduction of power devices. Using (15), (16), and (17), the average current, peak current, and rms current in these devices are derived and presented in Table I.

B. DCM Analysis

Fig. 2(b) shows the key waveforms during DCM operation. In Mode-1 and Mode-2, the inductors store energy. From (1) and (3), the inductor current at $t = t_1$ and $t = t_2$ are determined as follows:

$$i_L(t_1) = \frac{V_i T_s d}{L}\ ,\quad i_L(t_2) = \frac{(2d + d_1)V_i T_s}{2\ L}. \tag{18}$$

At $t = t_2$, the inductors release the energy to the load, and the inductor is fully discharged at $t = t_3$ i.e, $i_L(t_3) = 0$

$$i_L(t_3) = \frac{(V_i - V_o)T_s d_o}{4\ L} + i_L(t_2) \tag{19}$$

where $(t_3 - t_2) = d_o T_s$. Using (18) and (19), d_o is expressed in terms of d and d_1

$$d_o = \frac{2(2d + d_1)V_i}{V_o - V_i}. \tag{20}$$

The average current in D_{o1} is

$$i_{D_{o1}}(\text{avg}) = \frac{i_{D_{o1}(\text{peak})} d_o}{2} = I_o = \frac{V_o}{R_o} \tag{21}$$

where R_o is the load resistance, and $i_{D_{o1}(\text{peak})}$ represents the peak current in D_{o1}. Diode D_{o1} conducts during Mode-3 only, and the peak current in D_{o1} occurs at $t = t_2$. As seen from (16) and (15), the current in C_1 and C_2 are equal. Thus

$$i_{D_{o1}(\text{peak})} = \frac{(2d + d_1)V_i T_s}{4\ L}. \tag{22}$$

From (20), (21), and (22), the voltage gain in the DCM mode is evaluated as follows:

$$V_g(DCM) = \frac{1}{2}\left(1 + \sqrt{1 + \frac{(2d + d_1)^2}{K}}\right) \tag{23}$$

where $K = \frac{Lf_s}{R_o}$ and f_s are the normalized inductor time constant, and switching frequency, respectively.

C. External Characteristics of the Converter

At the boundary condition mode, the voltage gain in CCM and in DCM must be equal. Therefore, from (6) and (23), the normalized inductor time constant at the boundary condition mode, also known as critical normalized inductor time constant K_C, is evaluated as follows:

$$K_C = \frac{(2d + d_1)^2(1 - d - d_1)^2}{8(1 + d)(3 + d - d_1)}. \tag{24}$$

As seen from (24), K_C is a function of d and d_1. The plots of K_C as a function of d and d_1 are shown in Fig. 5(a) and (b), respectively. When K is greater than K_C, the converter operates in CCM. Fig. 5(a) and (b) show that the converter has several CCM and DCM curves. The critical load resistance is also determined as

$$R_C = \frac{8(1 + d)(3 + d - d_1)Lf_s}{(2d + d_1)^2(1 - d - d_1)^2} \tag{25}$$

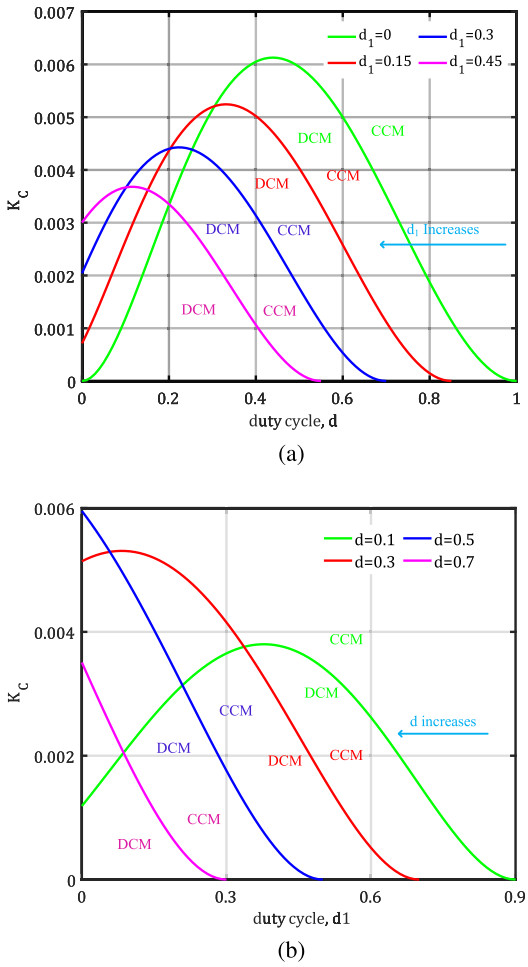


Fig. 5. Boundary condition of the proposed converter as a function of (a) d and (b) d_1.

and the output current is parameterized in terms of $\Gamma = \frac{I_o L f_s}{V_i}$. From (20), (21), and (22), the critical value of Γ is obtained as

$$\Gamma_C = \frac{(2d + d_1)^2}{4(V_g - 1)}. \tag{26}$$

Using (6), Γ_C is rewritten as

$$\Gamma_C = \frac{(V_g - 3)^2(2 - d_1)^2}{4(V_g + 1)^2(V_g - 1)} = \frac{(V_g - 3)^2(1 + d)^2}{4(V_g - 1)^3}. \tag{27}$$

External characteristics illustrate the response of a dc–dc converter to changes in external parameters, such as load variations, or/and input voltage changes. Fig. 6 illustrates the external characteristics of the proposed converter, with dashed lines indicating the boundary conditions. Unlike conventional dc–dc converter, the proposed converter exhibits different external characteristic curves corresponding to distinct values of d_1. In addition, the proposed converter demonstrates various CMM and DCM boundaries depending on the value of d_1.

D. Influence of Nonideal Components on Voltage Gain

The steady-state analysis discussed in Section III-A is based on the ideal model. To investigate the impact of nonideal

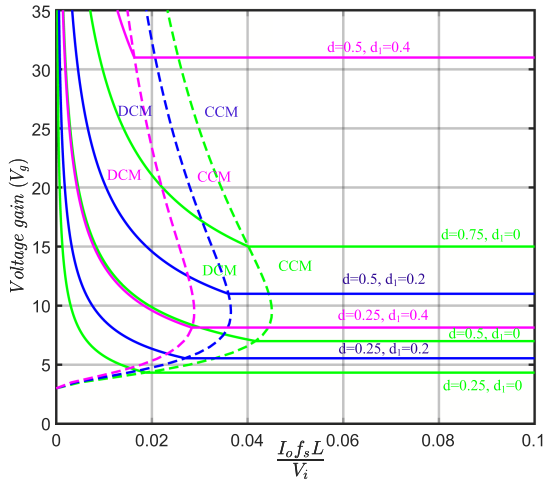


Fig. 6. External characteristics of the proposed converter with constant V_i.

components on the voltage gain, the internal resistance of the power switches (r_{ds_1}= r_{ds_2}= r_{ds_A}= r_{ds}), diodes (r_{d_1}=r_{d_2}= $r_{d_{o1}}$=$r_{d_{o2}}$=r_{d_A} =r_d), inductors (r_{L_1} = r_{L_2}=r_L), and capacitors (r_{c_1}=r_{c_2}=$r_{c_{o1}}$=$r_{c_{o2}}$=r_c), and the forward voltage drop across diodes (v_{f_1}=v_{f_2}=$v_{f_{o1}}$=$v_{f_{o2}}$=v_f) are considered.

The voltage equations for Mode-1, Mode-2, and Mode-3 are, given as follows.

1) Voltage equations in Mode-1

$$v_{L_1} = V_i - I_{L_1} r_L - i_{s_1} r_{ds},\ v_{L_2} = V_i - I_{L_2} r_{L_2} - i_{s_2} r_{ds}$$
$$V_{C_1} = V_i + V_{C_2} - v_f - i_{c_{1,1}}(2r_c + rd) - (i_{s_1} + i_{s_2}) r_s. \tag{28}$$

2) Voltage equations in Mode-2

$$v_{L_1} + v_{L_2} = V_i - v_f - I_{L_1}(2r_L + r_d + r_{ds}). \tag{29}$$

3) Voltage equations in Mode-3

$$v_{L_1} + v_{L_2} = V_i - V_{C_2} - v_f - (I_{L_1} + I_{L_2}) r_L - i_{c_{2,3}}(r_c + r_d)$$
$$V_o = V_{C_1} + V_{C_2} - v_f - i_{c_{1,3}}(r_c + 2r_d) + i_{c_{2,3}}(r_c + r_d). \tag{30}$$

From (28), (29), and (30), the nonideal gain of the proposed converter is

$$V_g' = \frac{\frac{3+d-d_1}{1-d-d_1} - \frac{2(2-2d-d_1)v_f}{(1-d-d_1)V_i}}{1 + \frac{A}{d(1-d-d_1)R_o} + \frac{B}{(1-d-d_1)^2 R_o}} \tag{31}$$

where $A = 2r_{ds} + 2(1-2d-d_1)r_c + (1-4d-d_1)r_d$ and $B = 4r_L + 2(1+d)r_{ds} + r_d(1-d+d_1) + r_c(1-d-d_1)$. The parasitic values of the components given in Table III are included in the calculations, and the experimental setup discussed in Section VIII is used to obtain practical voltage gain at different duty cycles. A comparison between the ideal, nonideal, and practical voltage gains is presented in Fig. 7. Fig. 7 shows that the influence of nonideal components on the voltage gain is very low.

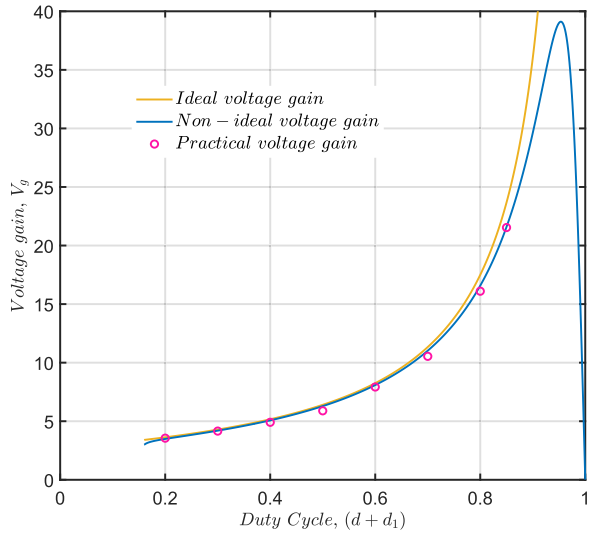


Fig. 7. Influence of parasitic parameters on the voltage gain.

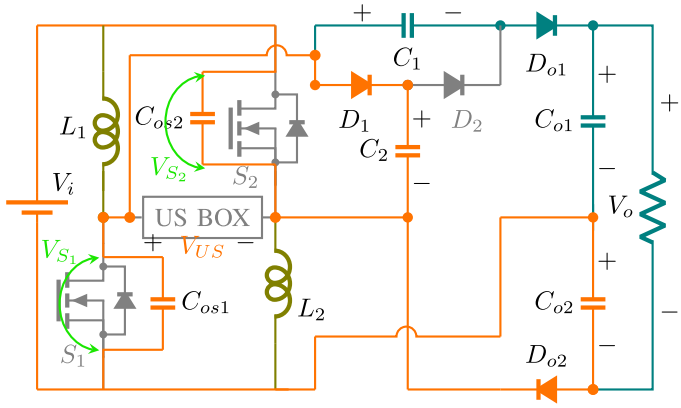


Fig. 8. Suppression of voltage oscillation across S_1 and S_2.

E. Suppression of Voltage Oscillation Across Switches

Any mismatch in the inductance values of inductors (L_1 and L_2) or/and the output capacitance values of the switches (C_{os1} and C_{os2}) forms a resonance circuit in the ASL network, resulting in increased voltage stress. There are always discrepancies in these parameters due to practical limitations. Therefore, the ASL-based converter discussed in [13] and [17], shows a higher switch voltage stress. In the proposed converter, the SC network supports C_{os1} and C_{os2}, thereby, effectively suppressing the voltage oscillation. Fig. 8 illustrates the suppression of the voltage oscillation through the SC network. In Mode-3 (when both switches are OFF), the capacitor C_2 and C_{o2} are in parallel with C_{os_1}, and V_i and C_{o2} are in parallel with C_{os_2}. From Fig. 8, the voltage stress on S_1 and S_2 are obtained as

$$V_{C_{OS1}} = V_{S_1} = V_{C_2} - V_{C_{o2}} \tag{32}$$
$$V_{C_{OS2}} = V_{S_2} = V_i + V_{C_{o2}}. \tag{33}$$

The inductor voltages are obtained as

$$v_{L_1} = V_i - V_{S_1} = V_i - V_{C_2} + V_{C_{o2}} \tag{34}$$
$$v_{L_2} = V_i - V_{S_2} = -V_{C_{o2}}. \tag{35}$$

TABLE II
COMPARISON BETWEEN THE PROPOSED CONVERTER AND EXISTING TSTM CONVERTERS

Topologies	Voltage gain (V_g)	Maximum switch voltage stress ($\frac{V_{SM}}{V_o}$)	Maximum diode voltage stress ($\frac{V_{DM}}{V_o}$)	Maximum inductor current stress	Maximum voltage stress on the US box ($\frac{V_{USM}}{V_o}$)	Sensitivity of L_1, L_2, C_{os1} and C_{os2} on the switchs' voltage	Low impedance path through the switch?	Component Counts				Efficiency $\%\mu$ @ Power Rating
								N_S	N_D	N_L	N_C	
[24]	$\frac{1+d}{1-d-d_1}$	$\frac{V_g+1}{2V_g}$	$\frac{V_g+1}{V_g}$	$\frac{I_o}{1-d-d_1}$	1	Yes	No	3	2	2	1	93.6% 100W
[25]	$\frac{3-d-2d_1}{1-d-d_1}$	$\frac{V_g-1}{2V_g}$	$\frac{V_g-1}{V_g}$	$\frac{I_o}{1-d-d_1}$	$\frac{V_g-2}{V_g}$	Yes	Yes	3	4	2	3	92.06% 500W
[26]	$\frac{2}{1-d-d_1}$	$\frac{1}{2}$	1	$\frac{I_o}{1-d-d_1}$	1	Yes	Yes	3	3	2	2	94.67% 500W
[27]	$\frac{3-d-d_1}{1-d-d_1}$	$\frac{V_g-1}{2V_g}$	$\frac{V_g-1}{V_g}$	$\frac{I_o}{1-d-d_1}$	$\frac{V_g-1}{V_g}$	Yes	Yes	3	4	2	3	96.82% 500W
[28]	$\frac{3+d+3d_1}{1-d-d_1}$	$\frac{V_g-1}{2V_g}$	1	$\frac{I_o}{1-d-d_1}$	1	Yes	Yes	3	10	4	3	94% 400W
[29]	$\frac{1+3d+d_1}{1-d-d_1}$	$\frac{V_g+1}{2V_g}$	$\frac{V_g+1}{V_g}$	$\frac{I_o}{1-d-d_1}$	1	Yes	No	3	8	4	1	94.69% 500W
IAH-SL [30]	$\frac{1+2d}{1-d-d_1}$	$\frac{V_g+1}{2V_g}$	$\frac{V_g+1}{V_g}$	$\frac{I_o}{1-d-d_1}$	1	Yes	No	3	5	3	1	NA
ISH-SL [30]	$\frac{1+3d-d_1}{1-d-d_1}$	$\frac{V_g+1}{2V_g}$	$\frac{V_g+1}{V_g}$	$\frac{I_o}{1-d-d_1}$	1	Yes	No	3	8	4	1	NA
ISH-SL-SC [30]	$\frac{3+5d-d_1}{1-d-d_1}$	$\frac{V_g+1}{4V_g}$	$\frac{V_g+1}{2V_g}$	$\frac{2I_o}{1-d-d_1}$	$\frac{V_g-1}{2V_g}$	Yes	No	3	10	4	3	86.34% 70.8W
Proposed	$\frac{3+d-d_1}{1-d-d_1}$	$\frac{V_g+1}{4V_g}$	$\frac{V_g+1}{2V_g}$	$\frac{I_o}{1-d-d_1}$	$\frac{V_g-1}{2V_g}$	No	No	3	5	2	4	96.35% 460W

TABLE III
PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

Power $P_o = 460$W, $f_s = 50kHz$	$V_i = 24V$,$V_o = 272V$
$L_1 = L_2 = 110\mu$ H, 12A	$r_{L1} = r_{L2} = 18.3m\Omega$
$C_1 = C_2 = 47\mu F, 200V$	$C_{o1} = C_{o2} = 47\mu F, 250$ V, $r_c = 10m\Omega$
MOSFETs:$V_{ds} = 400V$, $r_{ds(on)} = 40m\Omega$, $I_D = 46A$, $C_{oss} = 250pF$	
Diodes: $V_{PRV} = 400V$, $V_f = 1.0V$, $I_f = 26A$, $r_d = 83m\Omega$	

Since, V_i, $V_{C_{o2}}$, and V_{C_2} are constant, the voltage stresses across switches (S_1 and S_2) and inductors (v_{L_1} and v_{L_2}) are also constant even if there is a mismatch in the values of inductors or/and switch's capacitor. Consequently, voltage oscillations due to parameter mismatch are effectively suppressed, marking a significant improvement in the performance of the converter.

IV. COMPARISON WITH EXISTING TSTM CONVERTERS

To illustrate the advantages of the proposed converter, a comprehensive comparison with existing TSTM converters is presented in Table II. This table includes the conventional TSTM converter [24] and derived converters [25], [26], [27], [28], [29], [30]. The converters [25], [26], [27], [28] used switched capacitors block at the input terminals, which resulted in high switch currents. The converters [28], [29], IAH-SL [30], ISH-SL [30], and ISH-SL-SC [30] is derived from the converter [24] by replacing the simple inductor of the switched inductor network with one or two passive inductor network, thereby, the size of these converters is exceptionally high. Further comparisons are presented in terms of voltage gain (V_g), maximum switch voltage stress ($\frac{V_{SM}}{V_o}$), maximum diode voltage stress ($\frac{V_{DM}}{V_o}$), maximum voltage stress on the US box ($\frac{V_{USM}}{V_o}$), the total inductor current stress ($\frac{\sum I_{LM}}{I_o}$), the influence of parameter inconsistency of value of inductors and output capacitor of the switches on the switch's voltage, nature of switch current, component counts (N_S: number of switches, N_D: number of switches, N_L: number of inductors, and N_C: number of capacitors), and efficiency.

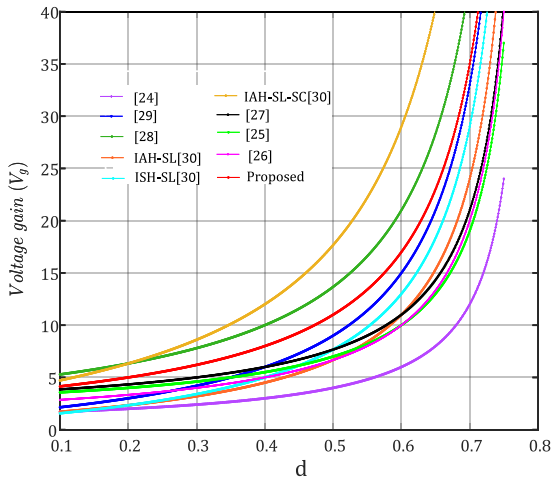


Fig. 9. Voltage gain versus duty cycle.

A. Voltage Gain Comparison

The voltage gain of the proposed converter and converters [24], [25], [26], [27], [28], [29], [30] depends on both duty cycles d and d_1. For gain comparison, the duty cycle d_1 of the unidirectional switch is kept at 20% and gain variation with duty cycle d is plotted in Fig. 9. As observed, the voltage gain of the proposed converter surpasses that of [24], [25], [26], [27], and [29], IAH-SL [30], and ISH-SL [30] for the entire

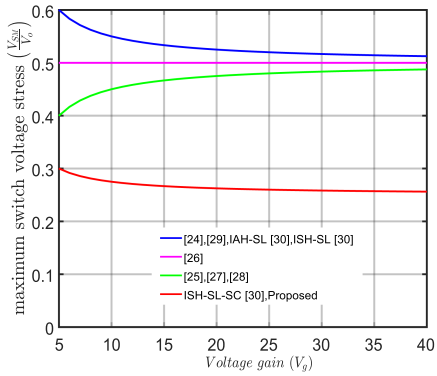
range of d. The converters [28] and ISH-SL-SC [30] exhibit a higher voltage gain compared to that of the proposed converter. However, it is worth noting that these converters are derived from four inductors (two additional) and ten diodes (five additional diodes). Moreover, the size of the converters [28], [29], [30] is larger than the proposed converter as these converters use more inductors. In addition, converters [24], [25], [26], [27], [28], [29], [30] are derived from ASL cell, making them sensitive to parameter mismatches in L_1, L_2, C_{os1}, and C_{os2}. Consequently, these converters show voltage oscillation across the switches, resulting in increased switch voltage stress. Furthermore, the converters [25], [26], [27], [28] feature low impedance path through switches S_1 and S_2, inherently increasing switch current stress [13]. Also, converters [24], [25], [26], [27], [28], [29], [30] have high-frequency potential differences between the input and output terminals, increasing the sensitivity to EMI problems. The proposed converter suppresses the potential voltage oscillation across the switches, and the constant potential difference between input and output terminals reduces EMI issues. The voltage gain of the proposed converter ranges from 5 to 35 when d varies from 0.2 to 0.7. The proposed converter can thus achieve a high voltage gain without operating at an extreme duty cycle.

B. Voltage Stress and Current Stress Comparison

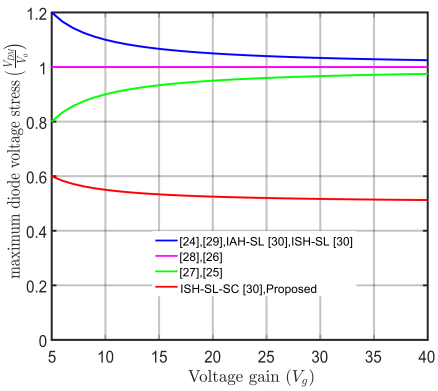
Using Table II, the maximum switch voltage stress, maximum diode voltage stress, maximum voltage stress on the unidirectional switch, and total inductor current stress are plotted against voltage gain. As seen from Fig. 10, the maximum switch voltage stress in the proposed converter is less than 0.3, significantly lower than that of converters [24], [25], [26], [27], [28], [29], IAH-SL [30], and ISH-SL [30]. The maximum switch voltage stress in the proposed converter and ISH-SL-SC [30] are equal. However, it is important to note that the maximum switch voltage stress is calculated under ideal conditions, and the converters [24], [25], [26], [27], [28], [29], [30] exhibit voltage oscillation in practical scenarios due to a mismatch in parameters, as explained in the previous section, resulting in increased voltage stress. Fig. 10(b) and (c) show that the maximum diode voltage stress and maximum voltage stress on the unidirectional switch are much lower than those in [24], [25], [26], [27], [28], and [29], IAH-SL [30], and ISH-SL [30]. Also, Fig. 10(d) shows that the total inductor current stress, which represents the inductor volume of the proposed converter is lower than the remaining other converters. Therefore, the proposed converter has lower voltage stress across the switches, and diodes, and lower current stress in the inductor compared to existing TSTM converters.

C. Voltage Oscillations in TSTM Converters

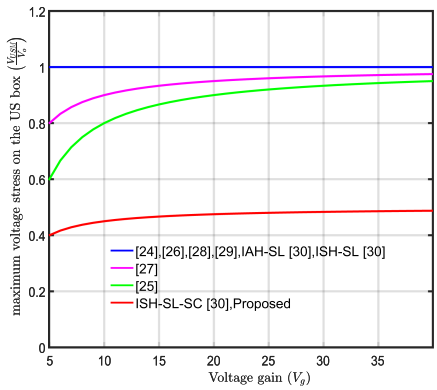
The parameter mismatch between the values of inductors and output capacitors of the switches is inevitable due to practical limitations, resulting in voltage oscillations in ASL-based converters [19]. The equivalent circuit condition of the converters presented in [24], [25], [26], [27], [29], [28], and [30] shown in Fig. 11, when the switches are OFF, and is used to explain the



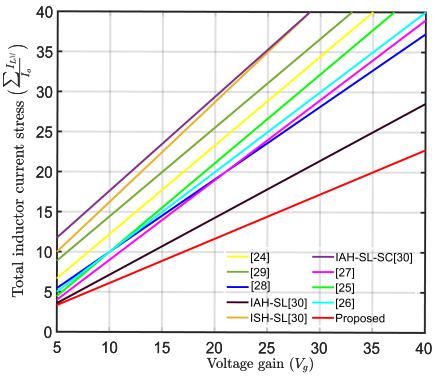
(a)



(b)



(c)



(d)

Fig. 10. Comparison of (a) maximum switch voltage stress, (b) maximum diode voltage stress, (c) maximum voltage stress on the unidirectional switch, and (d) total inductor current stress.

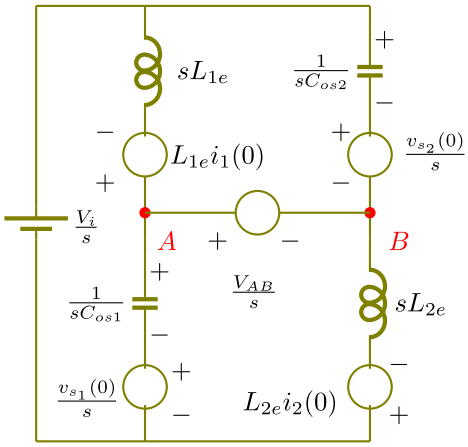


Fig. 11. Effective circuit condition of the existing TSTM converters.

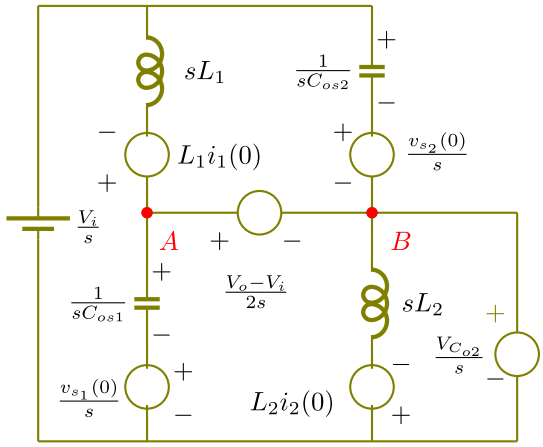


Fig. 12. Effective circuit condition of the proposed converter.

voltage oscillations. From this figure

$$v_{s_1}(s)+v_{s_2}(s)=\frac{V_i+V_{AB}}{s} \tag{36}$$

$$\frac{v_{s_2}(s)+L_{1e}i_1(0)-\frac{V_{AB}}{s}}{sL_{1e}}+\left(v_{s_2}(s)-\frac{v_{s_2}(0)}{s}\right)sC_{os2} =\frac{v_{s_1}(s)+L_{2e}i_2(0)-\frac{V_{AB}}{s}}{sL_{2e}}+\left(v_{s_1}(s)-\frac{v_{s_1}(0)}{s}\right)sC_{os1} \tag{37}$$

where $v_{s_1}(s)$ and $v_{s_2}(s)$ are the voltages across S_1, and S_2, respectively. L_{1e} and L_{2e} are the effective inductances of the ASL network, and V_{AB} is the potential difference between nodes A and B. The inductors L_{1e} and L_{1e} are given by the following: 1) $L_{1e}=L_1$, and $L_{2e}=L_2$ for [24], [25], [26], and [27], 2) $L_{1e}=L_{1a}+L_{1b}$, and $L_{2e}=L_2$ for IAH-SL [30], and 3) $L_{1e}=L_{1a}+L_{1b}$, and $L_{2e}=L_{2a}+L_{2b}$ for [28], [29], ISH-SL [30], and ISH-SL-SC [30]. V_{AB} is given by the following: 1) V_o for [24], [29] and, IAH-SL/ISH-SL [30], 2) (V_o-V_i) for [26], ISH-SL-SC [30], and 3) (V_o-2V_i) for [25], [27], and [28].

From (36) and (37), $v_{s_1}(s)$ and $v_{s_2}(s)$ can be evaluated.

$$v_{s_1}(s)=\alpha V_{AB}+(1-\alpha)V_i-\frac{(i_2(0)-i_1(0))\sin\omega t}{\sqrt{(C_{os_1}+C_{os_2})/\alpha\beta}} -[\beta(V_i+V_{AB}-v_{s_1}(0)) +(1-\beta)v_{s_2}(0)-\alpha V_i-(1-\alpha)V_{AB}]\cos\omega t \tag{38}$$

$$v_{s_2}(s)=\alpha V_i+(1-\alpha)V_{AB}+\frac{(i_2(0)-i_1(0))\sin\omega t}{\sqrt{(C_{os_1}+C_{os_2})/\alpha\beta}} +[\beta(V_i+V_{AB}-v_{s_1}(0)) +(1-\beta)v_{s_2}(0)-\alpha V_i-(1-\alpha)V_{AB}]\cos\omega t \tag{39}$$

where $\alpha=\frac{L_{1e}}{L_{1e}+L_{2e}}$, $\beta=\frac{C_{os1}}{C_{os1}+C_{os2}}$, and $\omega=\sqrt{\frac{L_{1e}+L_{2e}}{L_{1e}L_{2e}(C_{os1}+C_{os2})}}$. In ideal conditions, i.e., when both inductors have the same inductance value and both MOSFETs have the same parasitic capacitance and switching speed, the above equations are simplified to

$$v_{s_1}(s)=v_{s_2}(s)=\frac{V_{AB}+V_i}{2}. \tag{40}$$

This shows that resonance is absent when there is an exact match of parameters. However, due to manufacturing limitations, there will always be a mismatch between the values of the two inductors, the values of two parasitic capacitors, and the switching speed of the two MOSFETs. Thus, in accordance with (38) and (39), voltage oscillations will exist across the switches due to resonance. These oscillations increase the voltage stress. According to the study carried out in [19], the voltage stress in the MOSFETs could be doubled in the condition $i_1(0)=i_1(0)$, $v_{s_1}(0)=0$ and $v_{s_2}(0)=V_{AB}+V_i$. For this condition, the voltage stress of (38) and (39) are further simplified as

$$v_{s_1}(s)=\alpha V_i+(1-\alpha)V_{AB}-[\alpha V_i-(1-\alpha)V_{AB}]\cos\omega t \tag{41}$$

and

$$v_{s_2}(s)=\alpha V_i+(1-\alpha)V_{AB}+[\alpha V_i-(1-\alpha)V_{AB}]\cos\omega t. \tag{42}$$

In contrast, resonance is not present in the proposed converter even with a mismatch between the inductors values, and the values of the drain to source parasitic capacitor. This can be proved through the equivalent circuit condition shown in Fig. 12. A similar analysis is carried out for the proposed converter. From Fig. 12, the following equations are obtained:

$$v_{s_1}(s)+v_{s_2}(s)=\frac{V_o+V_i}{2\,s} \tag{43}$$

$$v_{s_1}(s)=\frac{V_o-V_i+2V_{C_{o2}}}{2\,s} \tag{44}$$

$$v_{s_2}(s)=\frac{V_i-2V_{C_{o2}}}{s}. \tag{45}$$

According to (44) and (45), the voltages across S_1 and S_2 are constant even if there is a mismatch in the values of the inductors and the switch parasitic capacitance. This is one of the major benefits and contributions of the proposed converter.

Hence, the comparative study demonstrates that the proposed converter achieves a higher voltage gain with lower switch voltage stress, lower switch current stress, lower component counts, and smaller size compared to the existing TSTM converters. In addition, the proposed converter mitigates the potential voltage oscillation in the existing TSTM converters.

V. Converter Design and Component Selection

A. Inductor Selection

The current stress on both inductors is equal. Hence, both inductors are designed with equal ratings i.e., $L_1 = L_2 = L$. Based on the analysis given in Section III-A, the current ripple in the inductors is given by

$$\Delta i_L = \Delta i_{L_1} = \Delta i_{L_2} = \frac{(2d + d_1)V_i}{2Lf_s}. \tag{46}$$

For a given percentage limit of inductor current ripple ($\delta i_L\%$), the inductor current ripple Δi_L must be less than $\frac{\delta i_L I_L}{100}$. Hence, the design constraint for the inductor is determined as

$$L \geq \frac{25(2d + d_1)(1 - d - d_1)R_o}{(3 + d - d_1)f_s \delta i_L\%}. \tag{47}$$

B. Capacitor Selection

The rating of the capacitors is determined based on the voltage stress and permissible voltage ripple. The voltage stress on the capacitors is given in (6). From (15) and (16), the voltage ripple in the capacitors is expressed as

$$\Delta v_{C_{oj}} = \frac{(d + d_1)I_o}{C_{oj}f_s} \quad , \quad \Delta v_{C_j} = \frac{I_o}{C_j f_s} \tag{48}$$

where j $\in \{1, 2\}$. For a permissible voltage fluctuation ($\delta v_c\%$), the voltage ripple (Δv_c) in the capacitor must be lower than $\frac{\delta v_c\% V_c}{100}$. Therefore, the capacitance of the C_1, C_2, C_{o1}, and C_{o2} is determined according to the following relation:

$$C_1 \geq \frac{(3 + d - d_1)100}{(2 - d_1)R_o f_s \delta v_{c_1}\%} \quad , \quad C_2 \geq \frac{(3 + d - d_1)100}{(1 + d)R_o f_s \delta v_{c_2}\%} \tag{49}$$

$$C_{o1} \geq \frac{(3 + d - d_1)(d + d_1)200}{(2d + d_1)R_o f_s \delta v_{c_{o1}}\%} \tag{50}$$

$$C_{o2} \geq \frac{(3 + d - d_1)(d + d_1)200}{3(3 - d)R_o f_s \delta v_{c_{o2}}\%}. \tag{51}$$

C. Power Switches and Diodes Selection

Based on the voltage and current stresses, the rating of the power switches and diodes is determined. In (12), (13), and Table I, the voltage stress and current stress on each switch are provided. For operational safety, the device with a rating higher than the analytically obtained values is selected.

VI. Power Loss and Efficiency Analysis

The power loss in the converter is composed of the power MOSFET loss, diode loss, inductor loss, and capacitor loss. The distribution of these losses is analytically evaluated below.

1) *Power MOSFET loss (P_S):* The power losses in the MOSFETs are attributed to switching losses (P_{SW1}), conduction losses (P_{SW2}), and the output capacitor loss (P_{SW3}). These are given by

$$P_{SW1} = \sum_{i=1} kI_{S_i}V_{S_i} = kI_oV_o\frac{(2 - d_1)(1 + d - d_1) + 2d(1 + d)}{d(3 + d - d_1)(1 - d - d_1)} \tag{52}$$

$$P_{SW2} = \sum_{i=1} I^2_{s_i,rms}r_{DS} = \frac{2(2 - d_1)^2 I_o^2 r_{ds}}{d(3 + d - d_1)^2} \tag{53}$$

$$P_{SW3} = \sum_{i=1} \frac{1}{2}f_s C_{osi}V^2_{S_i} = f_s C_{os}V_o^2\frac{(2 - d_1)^2}{8(3 + d - d_1)^2} \tag{54}$$

where $k = f_s\frac{t_r + t_f}{2}$ and t_r and t_f are the rise time and fall time of the switch, and C_{osi} is the output capacitor of the ith switch.

2) *Diode Loss (P_D):* The diode loss is comprised of the diode conduction loss (P_{D1}), and diode reverse recovery loss (P_{D_2}), which is expressed as

$$P_{D1} = \sum_{i=1} I_{D_i,a}.V_{f_i} = 4I_oV_f \tag{55}$$

$$P_{D2} = \sum_{i=1} Q_{rr_i}V_{D_i}f_s = \frac{3(2 - d_1)V_o}{3 + d - d_1}Q_{rr}f_s \tag{56}$$

where $I_{D_i,a}$, V_{f_i}, Q_{rr_i}, and V_{D_i} represent the average current, forward voltage drop, reverse recovery charge, and voltage stress associated with the ith diode.

3) *Inductor Loss (P_L):* The total loss in the inductors is made up of conduction losses (P_{L1}) and core losses (P_{L2}). The analytical expressions of these losses are given by (57), and (59), respectively

$$P_{L1} = \sum_{i=1} I^2_{L_i,rms}r_L = \frac{AV_i^2 + BV_iV_o + CV_o^2}{48Lf_s^2} \tag{57}$$

where $A = 3d - 320\ d^3 + 72d_1 + 48d_1^2 - 143d_1^3 - 12\ d^2(53d_1 - 16)$, $B = 24(-1 + 3\ d^3 - d_1 + 8\ d^2d_1 + 2d_1^3 + d(-2 + 7d_1^2))$, and $C = 4(-1 + d^3 + 3\ d^2d_1 + 3dd_1^2 + d_1^3)$. The core loss of the inductor is determined from the ferrite data sheet curve. The data sheets of MPP core (CM358090E) gives the core power loss per unit volume (ρ_{core}) for a given peak-to-peak flux density (ΔB_{PK}) is expressed as

$$\Delta B_{PK} = \frac{(2d + d_1V_o}{(3 + d - d_1)NA_cf_s} \tag{58}$$

where N and A_c are the numbers of turns and cross-sectional area of the magnetic core. Hence, the total core loss is given by

$$P_{L2} = \rho_{\text{core}}A_cl_e \tag{59}$$

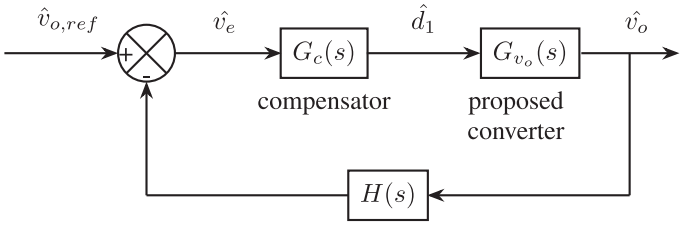


Fig. 13. Closed loop control of the proposed converter.

where l_e is the magnetic path length of the core. The core loss analysis given in the datasheet does not consider the core loss associated with the dc current in the inductor. Thus, the actual core loss would be slightly higher than the calculated value due to the presence of a dc- current component in the inductor [32].

4) *Capacitor loss (P_C):* The power loss in the capacitor is primarily due to the conduction loss

$$P_C = \sum_i I^2_{c_i,rms}.r_c = \frac{2I_o^2(1-d_1+dd_1+d^2)r_c}{d(1-d-d_1)} \tag{60}$$

where r_c is the equivalent series resistance of the capacitor.

VII. Dynamic Modeling and Controller Design

The proposed converter has two inductive and four capacitive energy storage elements. The voltages across the capacitive energy storage elements (C_1, C_2, C_{o1}, and C_{o2}) can be expressed uniquely in terms of the input voltage and duty cycle. Thus, the voltages across these capacitors are constant and mutually dependent. Also, the currents in the inductors (I_{L_1} and I_{L_2}) are equal. Hence, the inductor current (I_{L_1}) and the output voltage ($V_o = V_{C_{o1}} + V_{C_{o2}}$) can be considered as state variables [21], [30]. Using the state-space average method, the dynamic model of the proposed converter can be expressed as follows:

$$\begin{aligned} sL_1\hat{i}_{L_1} &= -\tfrac{1-d-d_1}{4}\hat{v}_o + \tfrac{V_o+V_i}{4}\hat{d} + \tfrac{V_o-V_i}{4}\hat{d}_1 \\ sC_o\hat{v}_o &= \tfrac{d+d_1}{2}\hat{i}_{L_1} - \tfrac{d+d_1}{R_o}\hat{v}_o + \tfrac{(d+d_1)V_o}{(1-d-d_1)R_o}(\hat{d}+\hat{d}_1) \end{aligned} \tag{61}$$

where $C_o = \frac{C_{o1}C_{o2}}{C_{o1}+C_{o2}}$, $\hat{i}_{L_1}$, $\hat{V}_o$, $\hat{d}$, and $\hat{d}_1$ represent the small-signal perturbations in I_{L_1}, V_o, d, and d_1 around the equilibrium point, respectively. The design of the controller provides three degrees of freedom, including 1) controlling d_1 and fixing d, 2) controlling d and fixing d_1, and 3) controlling both d and d_1 to achieve output voltage regulation. In this article, a controller is designed to regulate the output voltage by controlling d_1 only. Therefore, considering zero perturbation in d, the open loop transfer function of the proposed converter is obtained as

$$G_{v_o}(s) = \frac{\hat{v_o}}{\hat{d}_1} = \frac{s+4.97e^4}{5.92e^{-6}s^2 - 1.15e^{-3}s + 60.16}. \tag{62}$$

The closed-loop control structure shown in Fig. 13 is implemented. To achieve stable operation, the voltage loop is regulated with a PI controller. The transfer function of the PI controller is given by

$$G_c(s) = 0.648 + \frac{196.34}{s}.$$

The closed-loop transfer function of the proposed converter is obtained thus, given by

$$G_{v_{CL}}(s) = \frac{1.096e^5\ s^2 + 5.48e^9 s + 1.65e^{12}}{s^3 + 1.094e^5 s^2 + 5.49e^9 s + 1.65e^{12}} \tag{63}$$

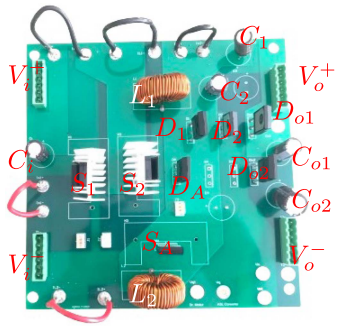
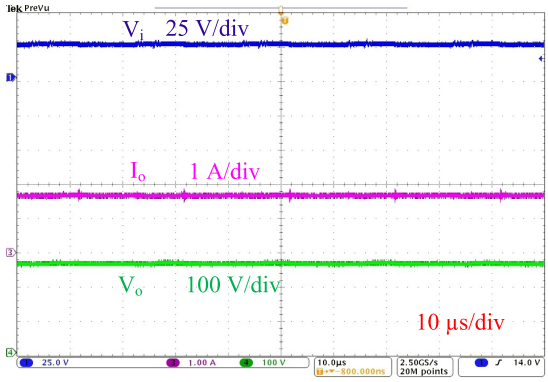


Fig. 14. Experimental prototype.

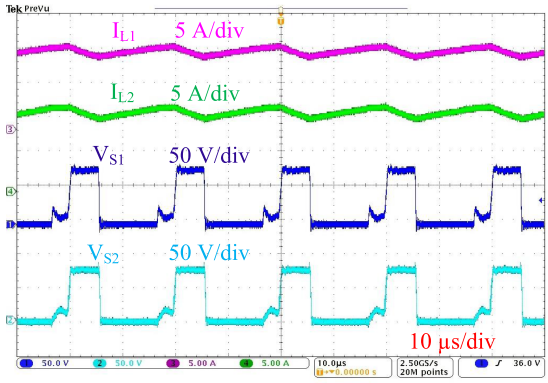
VIII. Experimental Validation

Theoretical analysis of the proposed converter is validated on the experimental board of Fig. 14 with parameters given in Table III. Using DSP TMS320F28335, the gate pulses 1) $d = 55\%$ for S_1 and S_2, and 2) $d_1 = 15\%$ for the unidirectional switch, with a desired phase difference at switching frequency $f_s = 50$ kHz, are generated and given to the grate driver circuit. First, the converter is tested for voltage conversion from 24 to 272 V at 460 W power rating i.e., the output current is 1.69 A for 160.84 Ω of the resistor load. At this operating point, the steady-state results of the proposed converter are shown in Fig. 15. Fig. 15(a) shows the experimental waveforms of input voltage, output voltage, and output current. The measured values of input voltage, output voltage and output current are 24, 267 V, and 1.66 A. The practical voltage gain (11.125) is slightly lower than the theoretical gain (11.33) at $d = 55\%$ and $d_1 = 15\%$. This discrepancy arises due to the forward voltage drop in the diodes, and resistive voltage drop in the switches, diodes, and capacitors.

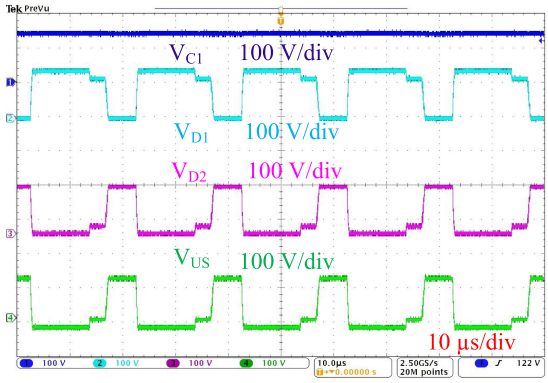
As seen from Fig. 15(b), the inductor currents are increasing during Mode-1 and Mode-2, and decreasing during Mode-3. The average current in inductors (L_1 and L_2) is approximately 11.12 A. Fig. 15(b) also shows that the voltage stress on S_1 and S_2 is free of voltage oscillation. The experimentally obtained switch voltage stress is 73.8 V, much lower than the output voltage. Fig. 15(b), (c), and (d) illustrate the switching pattern of the power devices, ensuring correct operation of the converter. Experimentally observed voltage stress V_{US}, $V_{D_1} \approx V_{D_2}$, and $V_{D_{o1}} \approx V_{D_{o2}}$ are approximately 124, 148, and 74 V, respectively. The measured voltage across C_1 and C_2 are approximately 148, and 124 V, respectively. The experimentally obtained voltage gain, inductor currents, and voltage on the switch, diode and capacitors agree with the steady state results given in Section III-A.



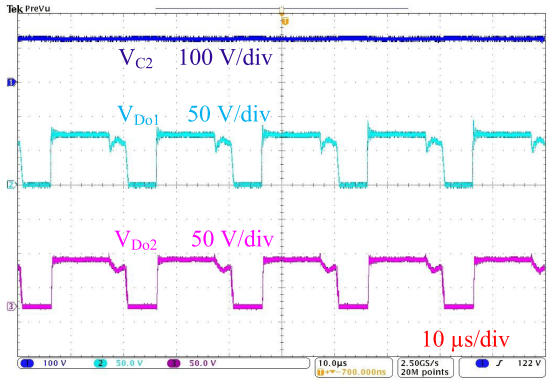
(a)



(b)



(c)



(d)

Fig. 15. Experimental waveforms of (a) input voltage, output voltage, and output current (b) inductor current (I_{L_1}, I_{L_2}), switch voltage stress (V_{S_1}, V_{S_2}) (c) voltage stress on C_1, D_1, D_2, unidirectional switch, and (d) voltage stress on C_2, D_{o1}, D_{o2}.

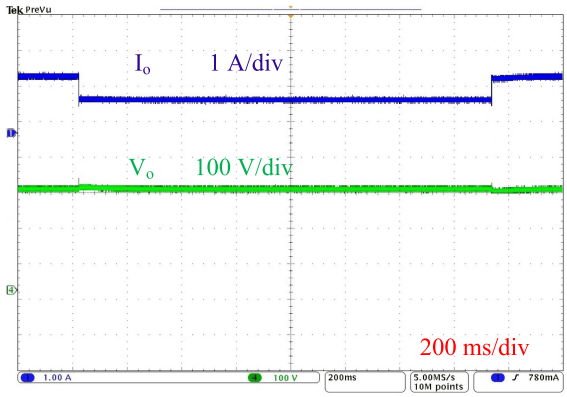


Fig. 16. Closed loop response under load change.

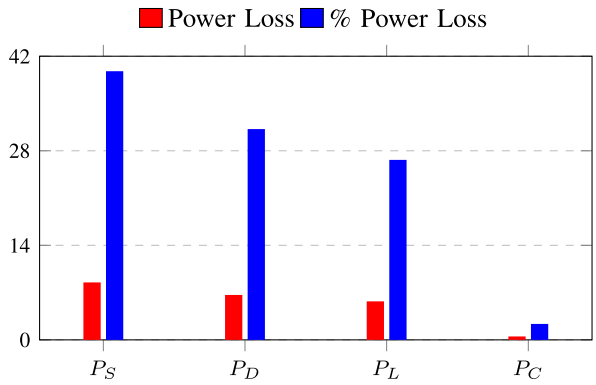


Fig. 17. Loss distribution in circuit components.

Finally, a simple PI controller is employed to regulate the output voltage at 272 V. Fig. 16 demonstrates the output voltage regulation when the load current is 1) suddenly reduced from 1.69 A (100%) to 0.57 A (33.7%) and 2) suddenly increased to 1.69 A (100%). For these load changes, the output voltage shows a voltage dip/rise, which settles in 12 and 8 ms. The closed-loop response shows the output voltage is successfully regulated against the step change in load.

The component parameters given in Table III are used for the theoretical estimation of losses in the proposed converter. Based on the analysis presented in Section VI, the power losses in the switches, diodes, inductors, and capacitors are approximately 8.506, 6.65, 5.7, and 0.5044 W, respectively. The theoretical efficiency of the proposed converter is thus, 95.38%. The numerical values of circuit component losses and their percentage contribution are given in Fig. 17. The experimental efficiency of the converter was measured at different output powers under two different input voltages. Fig. 18 shows the variation of converter efficiency as the load is increased from 100 to 460 W, plotted for two input voltages (24 and 36 V) and the same output voltage of 272 V. As the load increases, the efficiency drops from 96.1% (at 100 W) to 95.0% (at 460 W). This is because the conduction loss in the inductors and the MOSFETs increases as the load is increased for given input and output voltages. Also, the converter operates at a relatively low duty cycle for a high input voltage. Hence, the efficiency of the converter for 36 V input voltage is higher than 24 V input voltage at a particular output power.

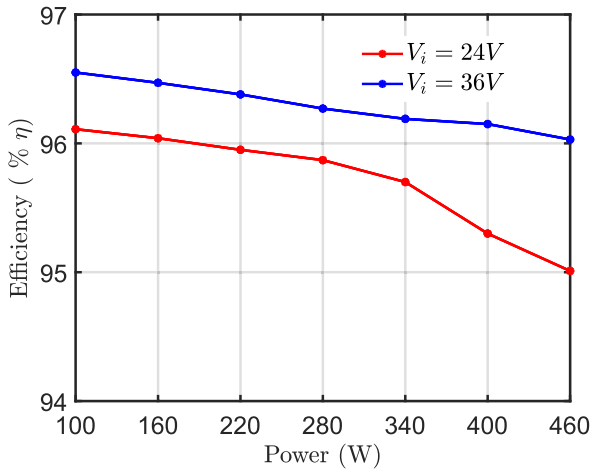


Fig. 18. Measured efficiency curves for the proposed converter topology.

IX. Conclusion

In this article, a novel TSTM dc–dc converter is presented to achieve high voltage gains. The converter works with two dissimilar duty cycles, allowing for the attainment of the desired voltage gain with different combinations of duty cycles (d, d_1). Analytical analyses of existing TSTM dc–dc converters and the proposed converter are presented to demonstrate the existence of resonance in the existing converters and the elimination of resonance in the proposed converter. Unlike other TSTM dc–dc converters, the proposed converter effectively suppresses the resonance that occurs in practice because of the inevitable mismatch in the values of the inductors and the switches' output capacitance. This results in suppressed voltage oscillations, and low switch voltage stress. It offers additional advantages, including low voltage stress on the unidirectional switch and diode, as well as low current stresses in the inductors and switches. The steady-state analysis, parameter design method, loss distribution, voltage, and current stress analysis are discussed in detail. A thorough comparison with recent TSTM converters reveals that the proposed converter can achieve a high voltage gain with comparatively low switch voltage stress, low diode voltage stress, and low inductor current stress. The performance of this converter is experimentally verified in both open-loop and closed-loop operations. For the future, the design of high-power prototypes and integration with renewable systems or electric vehicles, are some of the suggested works.

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Motiur Reza Mohammed (Member, IEEE) received the B.Tech. degree in electrical engineering from SASTRA University, Thanjavur, India, in 2009, the M.Tech. degree in electrical engineering from the College of Engineering Pune, Pune, India, in 2012, and the Ph.D. degree in electrical engineering from the Department of Electrical Engineering, Indian Institute of Technology (Banaras Hindu University), Varanasi, India, in 2018.

He is currently working as a Postdoctoral Fellow with Advanced Power and Energy Center, Khalifa University, Abu Dhabi, UAE. His research interests includes low frequency electromagnetic analysis, electrical motor design, renewable energy systems, power converters for Fuel Cell /Battery interface and V2V technology.

Vinod Khadkikar (Fellow, IEEE) received the M.Tech. degree in power electronics, electrical machines, and drives from the Indian Institute of Technology, New Delhi, India, in 2002, and the Ph.D. degree in electrical engineering from the Ecole de Technologie Superieure, Montreal, QC, Canada, in 2008.

He is currently a Professor with the Department of Electrical Engineering and Computer Science, Khalifa University, Abu Dhabi, United Arab Emirates. From 2008 to 2010, he was a Postdoctoral Fellow with the University of Western Ontario, London, ON, Canada. In 2010, he was a Visiting Professor with the Massachusetts Institute of Technology, Cambridge, MA, USA. His research interests include applications of power electronics in distribution systems and renewable energy resources, grid interconnection issues, power quality enhancement, active power filters, and electric vehicles.

Dr. Khadkikar is a distinguished Lecturer of IEEE Industry Applications Society. He is currently Co-EiC of IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS. He serves as an Associate Editor for IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS and *IET Power Electronics.*

Bashar Zahawi (Senior Member, IEEE) received the B.Sc. and Ph.D. degrees in electrical and electronic engineering from Newcastle University, Newcastle upon Tyne, U.K., in 1983 and 1988, respectively.

Since 2014, he has been with the Department of Electrical and Computer Engineering, Khalifa University, Abu Dhabi, United Arab Emirates, where he is currently a Professor of electrical power engineering. From 1988 to 1993, he was a Design Engineer with a U.K. manufacturer of large variable speed drives and other power conversion equipment. In 1994, he was appointed as a Lecturer in electrical engineering with the University of Manchester, Manchester, U.K. From 2003 to 2004, he was a Senior Lecturer with the School of Electrical and Electronic Engineering, Newcastle University, Newcastle upon Tyne, U.K. His research interests include power conversion and renewable energy integration.

Dr. Zahawi was the recipient of the Crompton Premium awarded by the Institution of Electrical Engineers, U.K., and the Denny Medal awarded by the Institute of Marine Engineering, Science and Technology (IMarEST). He is past Chairman of the IEEE Power and Energy Society United Arab Emirates Chapter.

Omar Alzaabi (Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from Pennsylvania State University, University Park, PA, USA, in 2012, 2014, and 2019, respectively.

He is currently an Assistant Professor of electrical engineering with Khalifa University, Abu Dhabi, United Arab Emirates. He is also a Faculty Member of the Advanced Power and Energy Center (APEC) with Khalifa University. His research interest includes power electronics, renewable energy integration, and electromagnetics and its application to electrified transportation.