Letters

GaN-HEMT Power Module of Aluminum-Clad Printed Circuit Boards for Small Power Loop Inductance and High Cooling Performance

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***Abstract*—Gallium nitride high-electron-mobility transistors (GaN-HEMTs) are promising for high-speed switching capability and small ON-resistance. However, large turn-OFF surge and limited cooling capability due to their small chip size are hindering their application to high power conversion. To solve these problems, this letter proposes a novel power module structure with small power loop inductance and small thermal resistance based on recently proposed power module structures. The proposed structure comprises two aluminum-clad printed circuit boards (PCBs) that sandwich the GaN-HEMT devices. These PCBs generate eddy current inside the aluminum base to reduce power loop inductance and provide an additional thermal path to improve the cooling performance. These features were tested by an experiment that compared 3-kW half-bridge prototype power modules of the proposed and conventional structures. As a result, the proposed structure revealed power loop inductance of 1.4 nH and thermal resistance of 0.72 K/W, which corresponded to a reduction by 53% and 20%, respectively, compared to the conventional structure.**

***Index Terms*—Cooling, gallium nitride high-electron-mobility transistors (GaN-HEMT), power loop inductance, power module, switching surge.**

I. Introduction

GALLIUM nitride high-electron-mobility transistors (GaN-HEMTs) [1], [2] are emerging as promising switching power devices with low ON-resistance and high-speed switching capability. At the first commercial release, GaN-HEMTs were adopted for small power applications. However, GaN-HEMTs increasingly find higher power applications of even more than 1 kW [3], [4], [5].

High-power application of GaN-HEMTs commonly involves high-current high-speed switching, resulting in a large changing rate of the drain current, i.e., di_d/dt, where i_d is the drain current and t is the time. The majority of the power converters are made of one or more half-bridge circuits, which is a series connection of the two power devices connected to a decoupling capacitor, as depicted in Fig. 1. High di_d/dt at the turn OFF of a switching device generates a large turn-OFF surge voltage due to the power loop inductance, which is the parasitic inductance of the power loop wiring path. Therefore, the high-power application of GaN-HEMTs needs a drastic reduction of power loop inductance to suppress the turn-OFF surge so that the drain voltage is below the voltage tolerance.

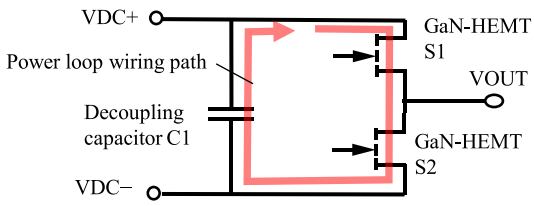

Fig. 1. Half-bridge circuit of GaN-HEMTs.

Besides, the high-power application of GaN-HEMTs tends to require high cooling performance. Due to its small ON-resistance, the GaN-HEMT can conduct large current even with a small chip size. However, this causes large thermal resistance to the heat sink due to the small thermal contact area on the chip. Consequently, the high-power application of the GaN-HEMT requires power module structures that can simultaneously reduce the power loop inductance and the thermal resistance.

A number of power module structures have been proposed for the high-power application of the GaN-HEMT [6], [7], [8], [9], [10]. However, simultaneous reduction of the power loop inductance and the thermal resistance is difficult because many GaN-HEMTs have the thermal contact pad on the same side as the drain and source terminals, hindering flexible power loop wiring design. This problem was solved by recent GaN-HEMTs [11] that have the thermal contact pad on the opposite side of the drain and source terminals. By utilizing these GaN-HEMTs, improved module structures have been proposed [12], [13], [14].

These module structures separately implement power loop wiring on the side of the drain and source terminals and the cooling structure on the side of the thermal pad. Thereby, they achieve design independence of the electric circuit and thermal dissipation. Fig. 2 depicts a typical structure with a half-bridge circuit, adopted by Jørgensen et al. [12]. This structure forms a laminated power bus to minimize the power loop inductance

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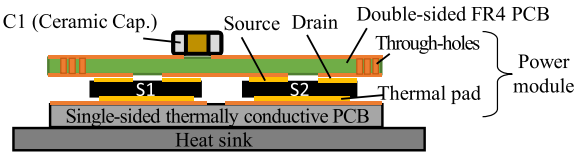

Fig. 2. Conventional GaN-HEMT power module structure. (Gate driver circuit is omitted.)

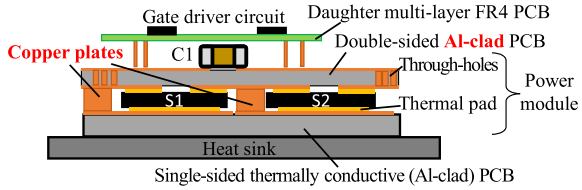

Fig. 3. Proposed GaN-HEMT power module structure.

by soldering a double-sided printed circuit board (PCB) on the drain and source terminals. This PCB is made of an electrically nonconductive base material, such as FR4 and Al_2O_3, similar to many commercially available PCBs. In addition, a single-sided thermally conductive PCB is soldered on the thermal contact pad as the heat spreader to reduce the thermal resistance. This heat spreader is connected to the heat sink.

As briefly reviewed earlier, this conventional structure is beneficial in a simultaneous reduction in the power loop inductance and thermal resistance. Nonetheless, this structure still has room to accept further improvement in reducing both the power loop inductance and the thermal resistance. The purpose of this letter is to propose an improved structure based on this conventional structure for further reduction in both the power loop inductance and the thermal resistance. The reduction effect of the power loop inductance and the thermal resistance was experimentally evaluated by comparing the proposed and conventional structures.

In addition, this letter also experimentally evaluated the temperature rise balance of parallel-connected GaN-HEMTs. The GaN-HEMT power modules for high-power applications commonly comprise parallel-connected GaN-HEMTs to handle large current. Although the same GaN-HEMT devices are commonly utilized for the parallel connection, the current unbalance between these GaN-HEMTs can occur at the switching, causing switching loss unbalance and, therefore, the temperature rise unbalance. As both of these GaN-HEMTs should be kept under the maximum allowable temperature requested by the semiconductor manufacturer, large temperature rise unbalance will result in insufficient thermal dissipation. Therefore, ensuring excellent thermal dissipation needs to evaluate not only the low thermal resistance but also the good temperature rise balance between the parallel-connected GaN-HEMTs, which is the reason for the temperature rise balance measurement.

This letter is an updated version of the conference paper [15]. Based on [15], this letter further evaluated the temperature rise balance of two parallel-connected GaN-HEMTs, which represents the current sharing at the switching.

II. Proposed Structure

Fig. 3 depicts the proposed power module structure. The basic construction of the proposed structure is similar to that of the conventional structure. However, the proposed structure differs from the conventional structure in the following two points.

1) The proposed structure implements the power loop wiring on a double-sided aluminum-clad PCB instead of the double-sided PCB made on an electrically nonconductive base.
2) The proposed structure has copper plates soldered on the top (double-sided) and bottom (single-sided) PCBs to thermally connect each to the other.

The former point can contribute to the power loop inductance reduction. The power loop wiring of the proposed structure forms a laminated bus similar to that of the conventional structure. The laminated bus can reduce the power loop inductance because the wires of the top and bottom PCB layers carry the ac current in the opposite direction during the switching transition, and therefore, the magnetic field outside the power loop wiring can be effectively canceled. However, the magnetic field inside the power loop wiring path can remain in the conventional structure, thus causing the remaining power loop inductance. Meanwhile, the proposed structure can further cancel this remaining ac magnetic field due to the aluminum-clad PCB because the eddy current is generated in the aluminum base. Thereby, the power loop inductance can be further reduced.

The latter point can contribute to reducing the thermal resistance along with the former point. The conventional structure can dissipate the heat generated in the switching devices only from the thermal pad via the bottom (single-sided) PCB. A switching device with a thermal pad is generally designed to dissipate heat from the thermal pad. However, comparatively small but nonnegligible heat can be dissipated also from the drain and source terminals, as these terminals are made of metals attached to the semiconductor chip. Therefore, further improvement in the cooling performance can be expected by implementing an additional thermal path from the drain and source terminals to the heat sink.

The proposed structure implements the single-sided aluminum-clad PCB as the heat spreader. In addition, the proposed structure incorporates copper plates soldered on the two aluminum-clad PCBs. These copper plates thermally connect these PCBs to provide a thermal path from the drain and source terminals of the GaN-HEMTs to the heat sink, in addition to the conventional thermal path from the thermal pad. Certainly, the heat dissipation through this additional path is generally less effective than that of the conventional path. Nonetheless, this additional path can also contribute to a small but nonnegligible reduction of the thermal resistance.

Certainly, the conventional structure may be able to attach the heat sink directly on the top (double-sided) PCB in addition to the heat sink on the bottom (single-sided) PCB. However, attaching the heat sink on the top PCB can be structurally inconvenient or hinder optimal layout design considering that

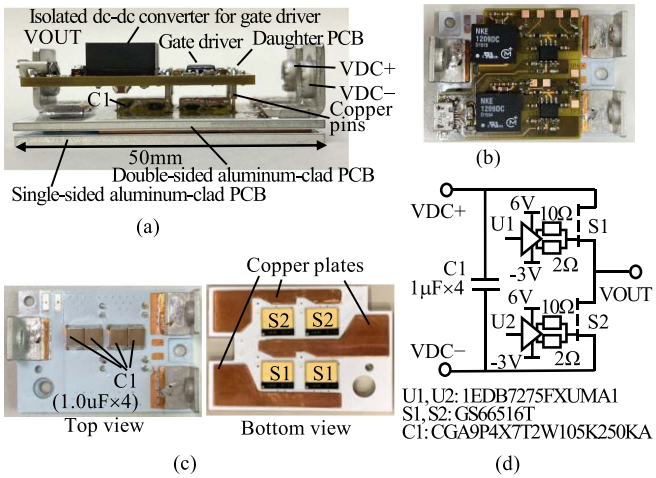

Fig. 4. Photograph and schematics of the proposed power module prototype. (a) Side view. (b) Top view. (c) Double-sided aluminum-clad PCB. (d) Circuit schematics.

the power modules for GaN-HEMTs should incorporate gate drivers and decoupling capacitors inside the modules because these devices should be placed close to the switching devices for high-speed switching. Meanwhile, the proposed structure enables the cooling from the drain and source terminals without attaching the heat sink on the top PCB, thus avoiding the structural inconvenience and restriction of layout design.

The proposed structure may have difficulty in integrating the gate driver circuits on the double-sided PCB because the top and bottom layers of this PCB tend to have extremely thick wire for large current flow in the laminated power bus, which can prevent mounting the small-sized electric components for the gate driver circuit. In this case, the gate driver circuit should be implemented on a daughter FR4 PCB, which is connected to the double-sided aluminum-clad PCB using thin copper pins with minimum wire length. The daughter PCB is placed close to the laminated power bus. However, the aluminum base, which generates the eddy current to cancel the magnetic field generated by the ac current through the power loop wiring, works also as a magnetic shield for the daughter board, protecting the gate driving circuit from the switching noise.

III. Experiment

The experiment evaluated the four performances of the prototypes of the proposed and conventional power module structures: 1) junction-to-case thermal resistance; 2) power loop inductance; 3) turn-OFF switching surge; and 4) temperature rise balance in parallel-connected GaN-HEMTs of the module. The turn-OFF surge was evaluated using the proper prototypes, although the other performances were evaluated using slightly modified prototypes arranged for each experiment.

A. Prototypes

Fig. 4 shows the photograph and the schematics of the prototype of the proposed structure. This prototype has a single half-bridge circuit with decoupling capacitor $C1$. The horizontal module size is 35 mm × 58 mm. (Net size is 35 mm × 50 mm excluding the margin for screw holes.)

The gate driving circuit was made on a four-layer FR4 daughter PCB. The laminated power bus was made on the double-sided aluminum-clad PCB. Each of S1 and S2 was made of a parallel connection of two GaN-HEMTs, GS66516T [11]. This GaN-HEMT is commercially supplied in the flat surface mount mold package with a thermal pad on the one side and with the drain and source terminals on the other side. This GaN-HEMT is not designed for cooling from these terminals, but the significant heat can still be dissipated from the terminals, as shown in the evaluation results of thermal resistance. The thermal pads of the GaN-HEMTs were soldered to the single-sided aluminum-clad PCB, which worked as the heat spreader. These aluminum-clad PCBs have a board thickness of 1.6 mm (including the aluminum base and the isolation layer) and a copper pattern thickness of 210 μm. The isolation layer, separating the copper and the aluminum base, had a thickness of 100 μm. This isolation layer can withstand the electric field greater than 35 kV/mm, which is sufficient to withstand the maximum possible drain–source voltage of GS66516, i.e., 650 V.

The prototype of the conventional structure was made by removing the copper plates and replacing the double-sided aluminum-clad PCB with the double-sided FR4 PCB. (The FR4 thickness is 1.2 mm.) All the PCBs of the conventional structure had the same layout as those of the proposed structure. Hence, the prototypes of the proposed and conventional structures differ in: 1) materials and thickness of the double-sided PCB and 2) existence of the copper plates that thermally connect the two PCBs.

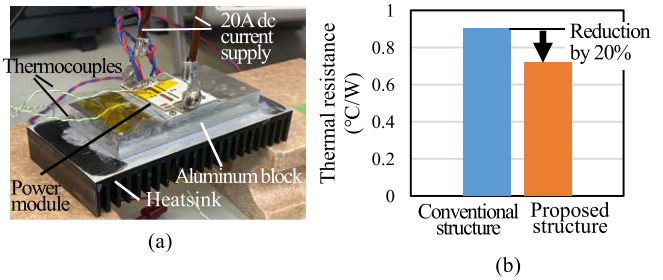

Fig. 5. Experimental setup and result of thermal resistance evaluation. (a) Experimental setup for thermal resistance evaluation. (b) Measured thermal resistance.

B. Thermal Resistance

The measurement of the thermal resistance employed special prototype modules, in which only a single GaN-HEMT device was mounted. These special modules were attached to an aluminum block with a heat sink, as shown in Fig. 5(a). The constant dc current of 20 A was conducted through the drain terminal of the GaN-HEMT, while it was kept at the ON-state continuously by applying 6.0 Vdc between the gate and source terminals. Due to the conduction loss, the GaN-HEMT generated the heat, which was finally dissipated at the heat sink. After the temperature reached the steady state, the aluminum

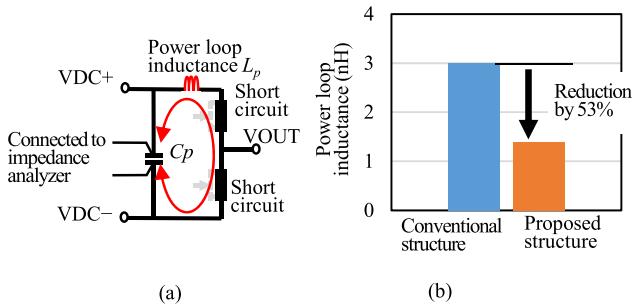

Fig. 6. Experimental setup and result of power loop inductance evaluation. (a) Equivalent circuit. (b) Measured power loop inductance.

block temperature and the dc voltage between the drain and source terminals were measured by the thermocouple and the multimeter, respectively.

The heat generated at the GaN-HEMT was calculated by multiplying the dc voltage and the dc current through the drain terminal, i.e., 20 A. In addition, the ON-resistance was calculated by dividing the dc current by the dc voltage. Then, the junction temperature of the GaN-HEMT was estimated from the relation between the ON-resistance and the junction temperature. This relation was evaluated prior to this experiment by measuring the ON-state resistance with the gate–source voltage of 6.0 Vdc at various temperatures. The thermal resistance was finally calculated from the heat generated at the GaN-HEMT and the difference between the estimated junction temperature and the aluminum block temperature.

Fig. 5(b) shows the result. The proposed structure exhibited a small thermal resistance of 0.72 °C/W, indicating 20% reduction compared to the conventional structure. This reduction can be attributed to the additional thermal path via the double-sided aluminum-clad PCB and the copper plates.

C. Power Loop Inductance

The measurement of the power loop inductance employed the double-sided PCB of each power module because the copper pattern of this PCB causes the power loop inductance. The measurement used a bare double-sided PCB without mounted circuit elements except that the pads for mounting the drain and source terminals of all the GaN-HEMT devices were short circuited by soldering thin copper plates with the thickness of 500 μm and that a 0.1-μF ceramic capacitor C_p was mounted in replace of the decoupling capacitor $C1$. Hence, C_p was shorted by the power loop wiring, forming an LC resonator of C_p and the power loop inductance, as shown in Fig. 6(a).

The power loop inductance was determined by measuring the resonant frequency of this LC resonator. For this purpose, the two terminals of the capacitor were connected to the impedance analyzer IM7581 (Hioki Corp.) to search for the frequency $f_{\rm res}$ that maximizes the impedance. Because $f_{\rm res}$ is identical to the resonant frequency, the power loop inductance L_p was determined according to

$$L_p = 1/4\pi^2 f_{\rm res}^2 C_p. \tag{1}$$

As this power loop inductance measurement method replaces the switching devices with copper plates, the measured inductance does not include the parasitic inductance of the terminal pins and the internal bonding wires of these switching devices. Therefore, this measurement method can cause errors if the switching devices incorporate the terminal pins and the bonding wires. However, GS66516 does not have terminal pins and bonding wires. Therefore, the measurement result represents the actual power loop inductance of the power module incorporating the switching devices.

Fig. 6(b) shows the results. Although the conventional structure exhibited a small power loop inductance of approximately 3 nH, the proposed structure further reduced it by 53%, achieving the power loop inductance of 1.4 nH.

If the double-sided PCB is made on an electrically nonconductive base, the parasitic inductance of the laminated power bus can be approximately predicted [16] as

$$L_p = \mu hl/w \tag{2}$$

where μ is the permeability of the PCB material, h is the PCB thickness, w is the wire width, and l is half of the length of the power loop wiring path. As for the prototype of the conventional structure, $h = 1.2$ mm and $l = 23$ mm; the base material is nonmagnetic. The representative value of the width w can be chosen as twice the width of the drain terminals of the GaN-HEMT device because this module connects two devices in parallel to form the high- and low-side switches. Consequently, (2) estimates $L_p = 2.5$ nH approximately. Because this value is close to the experimentally measured power loop inductance of the prototype of the conventional structure, the power loop inductance of the conventional structure can be consistently regarded to be mainly originating from the parasitic inductance of the laminated power bus. Therefore, the experimentally observed apparent reduction in the power loop inductance by the proposed structure can be interpreted that the proposed structure reduced the parasitic inductance of the laminated power bus, as is expected from the principles of the proposed structure.

D. Turn-off Voltage Surge

The turn-OFF voltage surge of the proposed and conventional structures was evaluated by observing the drain–source voltage of the switching device at the turn OFF at various drain current values. For this purpose, a double-pulse test circuit was constructed using the prototype module and 630-μF capacitor, as shown in Fig. 7(a). Switching device S1 was turned ON with the voltage of 6.0 Vdc and turned OFF with the voltage of -3.0 Vdc, whereas S2 was kept at the OFF-state with the voltage of -3.0 Vdc. The gate resistors for turn-ON and turn-OFF operations were 10 and 2 Ω, respectively. The dc bus voltage was set at 100 and 200 V.

In this experiment, S2 was first kept in the ON-state until the inductor current reached the predetermined level. Then, S2 was turned OFF, and the drain–source voltage of S2 was observed. The turn-OFF voltage surge was determined as the maximum deviation from the dc bus voltage after the turn OFF.

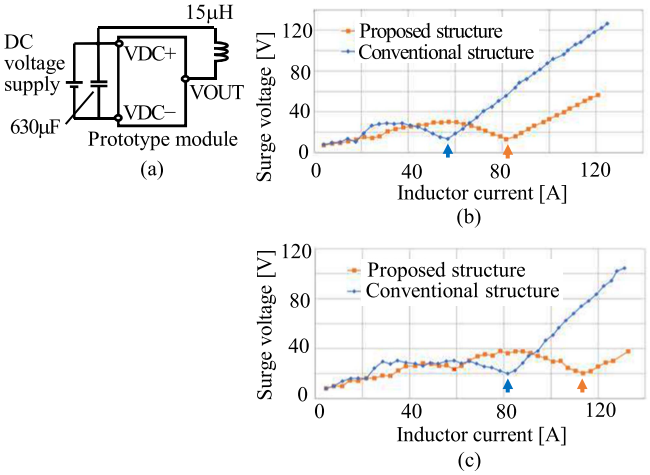

Fig. 7. Experimental setup and result of turn-OFF voltage surge evaluation. (a) Double-pulse test circuit. (b) DC bus voltage = 100 V. (c) DC bus voltage = 200 V.

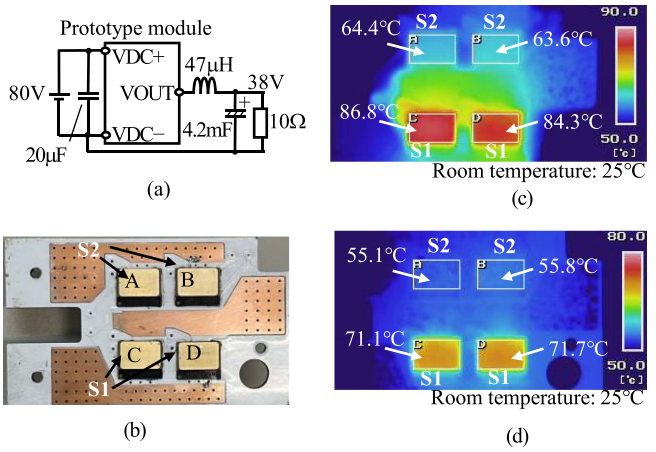

Fig. 8. Experimental setup and result of temperature balance evaluation. (a) Buck chopper circuit. (b) Bottom view of experimental module. (c) Temperature of the conventional structure. (d) Temperature of the proposed structure.

Fig. 7(b) and (c) shows the result. The voltage surge was reduced in the proposed structure when the inductor current I_L was greater than 70 A at the dc bus voltage $V_{\mathrm{IN}} = 100$ V and 95 A at $V_{\mathrm{IN}} = 200$ V. This result is consistent with the power loop inductance reduction of the proposed structure.

The voltage surge of the proposed structure took a local minimum around $I_L = 80$ A when $V_{\mathrm{IN}} = 100$ V and around $I_L = 110$ A when $V_{\mathrm{IN}} = 200$ V. This can be attributed to the nonlinear dependence of the voltage surge on the inductor current, observed in high-speed switching devices, such as GaN-HEMT, as reported in a recent study [17]. According to the simple linear analysis of [17], the voltage surge vanishes at the following I_L, where C_{ds} is the total drain–source parasitic capacitance of the switching device and n is the arbitrary natural number

$$I_L = 2\sqrt{\frac{2C_{\mathrm{ds}}}{L_p}}\frac{V_{\mathrm{IN}}}{(2n+1)\,\pi}. \tag{3}$$

Equation (3) predicted the greatest value of I_L that makes the local minimum as approximately $I_L = 80$ A and 130 A at $V_{\mathrm{IN}} = 100$ and 200 V, respectively, as is consistent with the experiment. (C_{ds} was estimated from the C_{oss} energy storage data.) According to this theory, the power loop inductance reduction shifts this local minimum to a greater inductor current, which may also have contributed to voltage surge reduction at high current turn OFF in the proposed structure.

E. Temperature Rise Balance of Parallel-Connected GaN-HEMTs

The laminated power bus enables a symmetrical power loop layout among parallel-connected GaN-HEMTs. Therefore, the conventional structure can achieve balanced current sharing during the switching and, therefore, balanced temperature rise.

As the proposed structure also has a symmetrical power loop layout, the proposed structure can also expect a balanced temperature rise, if the eddy current distribution in the aluminum base is also symmetrical. Certainly, the eddy current distribution can be expected to be symmetrical because of the symmetrical cross-sectional structure among the parallel-connected GaN-HEMTs. However, the balanced temperature rise of parallel-connected GaN-HEMTs on the laminated power bus of the aluminum-clad PCB has scarcely been reported in the literature. Therefore, this experiment evaluated the temperature rise of parallel-connected GaN-HEMTs of the proposed structure, as this is an essential point for validating the benefit of the proposed structure in thermal dissipation.

The temperature rise evaluation employed special prototype power modules without the single-sided aluminum-clad PCB to observe the temperature difference among GaN-HEMT devices. The thermal pads of all the devices are colored in black to observe the temperature by a thermal camera. A buck chopper was constructed using these modules, as shown in Fig. 8(a). Switches S1 and S2 were operated at 400 kHz with a duty cycle of 49%, outputting 38 V to 10-Ω load resistor. The experimental modules are shown in Fig. 8(b).

Fig. 8(c) and (d) shows the temperature distribution observed in the steady-state operation of the buck chopper. As S1 turns ON at the hard-switching condition, the temperature rise of S1 from the room temperature was higher than that of S2. However, both the proposed and conventional structures exhibited almost the same temperature rise from the room temperature between the parallel-connected GaN-HEMT devices, as is expected from the symmetrical power loop layout. Keeping the balanced temperature rise, the proposed structure further reduced the temperature rise of GaN-HEMT devices due to heat spreading by the aluminum-clad PCB, which is promising for high-power applications.

IV. Conclusion

Excessive turn-OFF switching surge and limited cooling capability are major obstacles for high-power applications of the GaN-HEMT. This letter addressed these issues by proposing an improved power module structure based on the recently proposed structures. The proposed structure further reduces the

power loop inductance and thermal resistance by implementing the laminated power bus on the double-sided aluminum-clad PCB and adding the copper plates for an additional thermal path to the heat sink. The effectiveness of the proposed structure was verified by the experiment, which exhibited a reduction in the power loop inductance, thermal resistance, and turn-OFF switching surge, as well as a balanced temperature rise between parallel-connected GaN-HEMT devices.

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