Finite Control Set Model Predictive Control for Grid-Connected Parallel Power Converters With Guaranteed Optimality

Yu Li, *Member, IEEE*, Jianbo Gao, *Member, IEEE*, Qiwu Wang, Zhenzhen Zhang, Fangfang Zhang, Zhenbin Zhang, *Senior Member, IEEE*, and Fengxiang Wang, *Senior Member, IEEE*

***Abstract*—Model predictive control (MPC) has been applied to parallel power converters to achieve current tracking and zero-sequence circulating current (ZSCC) suppression. To facilitate real-time implementation, simplifications of the optimization problem are commonly made by reformulating the cost function or restricting the feasible control set. However, inappropriate simplifications can lead to suboptimal solutions, degrading control performance. To address this issue, this work formulates a formal finite control set MPC (FCS-MPC) problem for grid-connected parallel power converters. It obtains the optimal solution using the computationally efficient modified sphere decoding algorithm. The guaranteed optimality allows the proposed FCS-MPC to maximize the system control performance in suppressing ZSCC, reducing current distortion, and improving transient response. Furthermore, we propose an alternative cost function that includes the grid-side total current as one of the control variables. Owing to the interleaving-wise mechanism, there is a significant enhancement in the power quality of the grid integration current, particularly at lower switching frequencies. Finally, experimental results from a lab-constructed test bench validate the theoretical analysis.**

***Index Terms*—Circulating current, finite control set (FCS), grid-connected converter, model predictive control (MPC), parallel power converters.**

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Yu Li, Jianbo Gao, Qiwu Wang, and Zhenzhen Zhang are with the Laser Institute, Qilu University of Technology (Shandong Academy of Sciences), Jinan 250104, China (e-mail: liyu@sdlaer.cn; gaojianbo@sdlaser.cn; qiwu@sdlaser.cn; zzz@sdlaser.cn).

Fangfang Zhang is with the School of Information and Automation Engineering, Qilu University of Technology (Shandong Academy of Sciences), Jinan 250353, China (e-mail: zhff4u@qlu.edu.cn).

Zhenbin Zhang is with the School of Electrical Engineering, Shandong University, Jinan 250061, China (e-mail: zbz@sdu.edu.cn).

Fengxiang Wang is with the Quanzhou Institute of Equipment Manufacturing, Haixi Institutes, Chinese Academy of Sciences, Quanzhou 362200, China (e-mail: fengxiang.wang@fjirsm.ac.cn).

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I. Introduction

High-power voltage-source converters are utilized in various industrial areas, including renewable energy generation, electrical drives, and uninterrupted power supplies [1], [2], [3], [4], [5]. These systems frequently employ parallel connections with a modular design concept to increase their rated current. However, the emergence of zero-sequence circulating current (ZSCC), due to the formation of a zero-sequence loop, can lead to harmonic distortion, unbalanced output power, and increased power losses [6]. ZSCC can be categorized into high-frequency ZSCC (HF-ZSCC) and low-frequency ZSCC (LF-ZSCC) [7]. HF-ZSCC, caused by inconsistent switching actions of semiconductors, can be mitigated using advanced pulsewidth modulation (PWM) techniques [8], [9]. On the other hand, LF-ZSCC arises from differences in the low-frequency common-mode voltage (CMV) produced by the parallel units. Specific control strategies are required for the elimination of ZSCC, which is the focus of this article.

To date, many control strategies, such as the proportional-integral (PI) controller based on the average model [10], feedforward control [11], deadbeat control [12], and model predictive control (MPC) and its variants [13], have been proposed to suppress ZSCC. Among these, MPC is an advanced control technique that is well-suited for multivariable optimization. Its other advantages include rapid dynamic responses and the capability to handle nonlinear constraints [14], [15].

In [16], a modified finite control set MPC (FCS-MPC) is proposed to eliminate ZSCC, reduce CMV, and balance the neutral point voltage simultaneously in parallel three-level inverters. To enable computationally efficient implementation, the current tracking problem is first transformed into an equivalent voltage tracking problem. Subsequently, the number of voltage vector candidates is reduced to five or six, depending on the direction of the ZSCC and the sector of the reference voltage. Experimental results show the effectiveness of this fast-processing predictive control solution. In [17], a virtual voltage vector with zero-average CMV and the capability to balance the neutral point voltage is adopted to eliminate ZSCC. Furthermore, a preselection algorithm is utilized to decrease computational complexity, and the synthesized multivector reduces the grid current harmonic distortion.

In [18], a synthesized voltage vector, which consists of an optimal shrunken voltage vector and a zero voltage vector, is implemented. The former is selected to minimize the tracking error of the $\alpha\beta$-axis current, while the latter is strategically chosen to mitigate ZSCC according to its polarity. This control strategy operates autonomously, well-suited for spatially distributed applications. A centralized carrier-based MPC method is presented in [13] that combines the benefits of MPC and interleaving PWM. In particular, the dynamic model of ZSCC is employed to predict its trajectory. Utilizing this prediction model, an unconstrained optimal solution is determined by setting the partial derivative of the cost function with respect to the control variable to zero. Ultimately, interleaved carrier signals are used to cancel the ripple in the total current.

As elaborated above, the recent MPC and its variant approaches demonstrate their benefits in facilitating its implementation, which includes improved computational efficiency and the avoidance of weighting factors [16], reduction of current ripple [17], and reduction of CMV [19]. However, some simplification on the optimization problem—such as reformulating the cost function or restricting the feasible control set—can impact optimality [20], thereby reducing system performance. A common simplification is to treat the paralleled power converters separately and solve the optimization problems of current tracking and ZSCC suppression sequentially [18], [19]. By doing so, suboptimal solutions arise, leading to degraded performance both at steady state and during transients. To overcome these limitations, it is essential to formulate the FCS-MPC problem properly and formally, and to develop a computationally efficient algorithm that ensures the optimality of solutions.

Motivated by this observation, this article proposes a centralized FCS-MPC that integrates the control objectives of current tracking and ZSCC suppression into a unified cost function for parallel power converters to ensure optimality. The main contributions of this work are summarized as follows.

1) A formal FCS-MPC problem is formulated, providing a unified control architecture for parallel power converters. Specifically, the state-space model for parallel power converters is constructed as a single control entity, incorporating the coupling in the zero-sequence loop. On this basis, a modified sphere decoding (MSD) algorithm is employed to efficiently solve the transformed integer optimization problem. Theoretically, the guaranteed optimal control sequence delivers improved ZSCC suppression performance and the minimum current harmonic distortion. Furthermore, it ensures that the power converters make full use of the dc-link voltage, thereby reducing the settling time during transient conditions.
2) An alternative cost function, which integrates the grid-side total current, is developed through flexible modification of the output matrix of the state-space model. This allows the parallel system to operate in a manner akin to an interleaving mechanism. This contribution further mitigates harmonic distortion in the grid-side total current, particularly at low switching frequencies.

The rest of this article is organized as follows. Section II presents the modeling of parallel power converters. Section III formally formulates the FCS-MPC problem. Section IV introduces the MSD algorithm to efficiently solve the FCS-MPC problem. Experimental results that verify the effectiveness of the proposed control method are discussed in Section V. Finally, Section VI concludes this article.

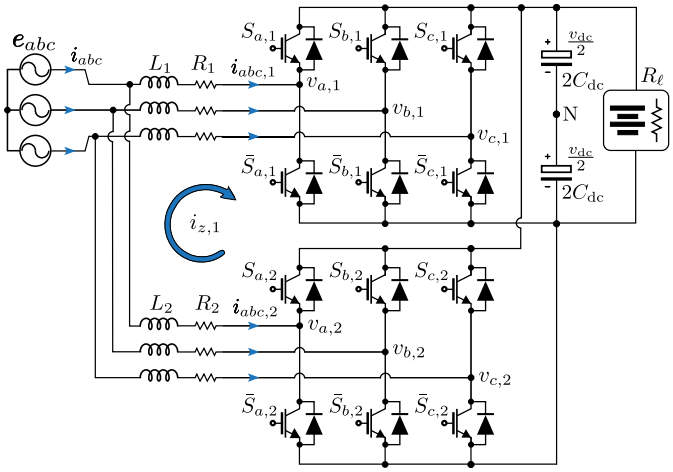


Fig. 1. Grid-connected power converters with parallel connection.

II. System Modeling

The power circuit of parallel grid-connected power converters is shown in Fig. 1. The symbols L_1 and L_2 denote the inductor filters, while R_1 and R_2 represent the equivalent resistance. The dc-link voltage is defined by $v_{\rm dc}$, and the total dc capacitance is represented by $C_{\rm dc}$.

A. Single-Power Converter

Each phase leg consists of two semiconductor switches with freewheeling diodes, and they are operated in a complementary manner. Letting the dc-link virtual midpoint N as the reference potential, the integer variable $u_x \in \{-1, 1\}$ can be used to denote the switch position in one phase leg, where $x \in \{a, b, c\}$. The relationship between the switch position u_x and the switching states $S_{x1},\ S_{x2}$ are given by

$$u_x = \begin{cases} 1, & \text{if } S_{x1} = 1 \text{ and } \bar{S}_{x1} = 0 \\ -1, & \text{if } S_{x1} = 0 \text{ and } \bar{S}_{x1} = 1. \end{cases} \tag{1}$$

Accordingly, the phase leg voltage with respect to the dc-link virtual midpoint N can be expressed as

$$v_x = \frac{v_{\rm dc}}{2} u_x. \tag{2}$$

The lumped switch position vector $\boldsymbol{u}_{abc} = [u_a, u_b, u_c]^T$ can be transformed into the stationary orthogonal reference frame

$$\boldsymbol{u}_{\alpha\beta z} = \boldsymbol{T}\boldsymbol{u}_{abc} \tag{3}$$

where the transformation matrix is defined as

$$\boldsymbol{T} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ 0 & \sqrt{3} & -\sqrt{3} \\ 1 & 1 & 1 \end{bmatrix}. \tag{4}$$

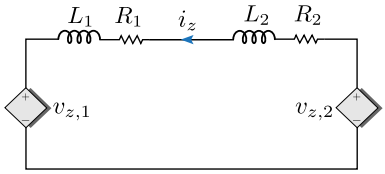


Fig. 2. Equivalent circuit of the ZSCC loop.

Hence, the phase leg voltage on the $\alpha\beta z$ reference frame can be written by

$$\boldsymbol{v}_{\alpha\beta z} = \frac{v_{\rm dc}}{2}\boldsymbol{T}\boldsymbol{u}_{abc}. \tag{5}$$

B. Zero-Sequence Loop

According to (3), the zero-sequence voltage v_z can be expressed as $v_z = (v_a + v_b + v_c)/3$. Similarly, the zero-sequence current is defined as $i_z = (i_a + i_b + i_c)/3$. Applying Kirchhoff's voltage law with the current direction defined in Fig. 1, we obtain the following equation:

$$\begin{cases} v_{a,1} + L_1\dfrac{\mathrm{d}i_{a,1}}{\mathrm{d}t} + R_1 i_{a,1} &= v_{a,2} + L_2\dfrac{\mathrm{d}i_{a,2}}{\mathrm{d}t} + R_2 i_{a,2} \\ v_{b,1} + L_1\dfrac{\mathrm{d}i_{b,1}}{\mathrm{d}t} + R_1 i_{b,1} &= v_{b,2} + L_2\dfrac{\mathrm{d}i_{b,2}}{\mathrm{d}t} + R_2 i_{b,2} \\ v_{c,1} + L_1\dfrac{\mathrm{d}i_{c,1}}{\mathrm{d}t} + R_1 i_{c,1} &= v_{c,2} + L_2\dfrac{\mathrm{d}i_{c,2}}{\mathrm{d}t} + R_2 i_{c,2}. \end{cases} \tag{6}$$

Upon summing up the left and right sides of (6) and considering the definition of v_z and i_z, we obtain the following:

$$L_1\frac{\mathrm{d}i_{z,1}}{\mathrm{d}t} + R_1 i_{z,1} + v_{z,1} = L_2\frac{\mathrm{d}i_{z,2}}{\mathrm{d}t} + R_2 i_{z,2} + v_{z,2}. \tag{7}$$

Note that $i_{z,1} = -i_{z,2}$, and we define $i_z = i_{z,1}$. To this end, the dynamics of the zero-sequence loop can be written by

$$(L_1 + L_2)\frac{\mathrm{d}i_z}{\mathrm{d}t} + (R_1 + R_2)i_z = v_{z,2} - v_{z,1}. \tag{8}$$

The equivalent circuit of the ZSCC loop for paralleled converters can be depicted in Fig. 2.

C. Parallel Power Converters

We consider the parallel power converters as an entire system, as they are coupled in the zero-sequence loop. Consequently, the parallel system can be modeled in the stationary $\alpha\beta z$ reference frame as

$$\begin{cases} L_1\dfrac{\mathrm{d}i_{\alpha,1}}{\mathrm{d}t} + R_1 i_{\alpha,1} = e_\alpha - v_{\alpha,1} \\ L_1\dfrac{\mathrm{d}i_{\beta,1}}{\mathrm{d}t} + R_1 i_{\beta,1} = e_\beta - v_{\beta,1} \\ L_2\dfrac{\mathrm{d}i_{\alpha,2}}{\mathrm{d}t} + R_2 i_{\alpha,2} = e_\alpha - v_{\alpha,2} \\ L_2\dfrac{\mathrm{d}i_{\beta,2}}{\mathrm{d}t} + R_2 i_{\beta,2} = e_\beta - v_{\beta,2} \\ (L_1 + L_2)\dfrac{\mathrm{d}i_z}{\mathrm{d}t} + (R_1 + R_2)i_z = v_{z,2} - v_{z,1} \end{cases} \tag{9}$$

where e_α, e_β denote the grid voltage, and v_α, v_β represent the phase leg voltages on the $\alpha\beta$ reference frame, respectively. The predictive current controller relies on the system model to predict the future trajectory as a function of the three-phase switch position. By inserting (5) into (9), the continuous-time state-space model can be derived as

$$\dot{\boldsymbol{x}} = \boldsymbol{F}\boldsymbol{x} + \boldsymbol{G}_1\boldsymbol{u} + \boldsymbol{G}_2\boldsymbol{d} \tag{10}$$

where

$$\boldsymbol{x} = \begin{bmatrix} i_{\alpha,1},\ i_{\beta,1},\ i_{\alpha,2},\ i_{\beta,2},\ i_z \end{bmatrix}^T$$

$$\boldsymbol{u} = \begin{bmatrix} u_{a,1},\ u_{b,1},\ u_{c,1},\ u_{a,2},\ u_{b,2},\ u_{c,2} \end{bmatrix}^T, \boldsymbol{d} = \begin{bmatrix} e_\alpha,\ e_\beta \end{bmatrix}^T$$

and the system matrices are found at the bottom of this page. Accordingly, the discrete-time representation is obtained using the forward Euler discretization method as

$$\boldsymbol{x}(k+1) = \boldsymbol{A}\boldsymbol{x}(k) + \boldsymbol{B}_1\boldsymbol{u}(k) + \boldsymbol{B}_2\boldsymbol{d}(k) \tag{11}$$

where

$$\boldsymbol{A} = \boldsymbol{I}_5 + \boldsymbol{F}T_s,\ \boldsymbol{B}_1 = \boldsymbol{G}_1 T_s,\ \boldsymbol{B}_2 = \boldsymbol{G}_2 T_s \tag{12}$$

with the sampling interval of T_s, and where $\boldsymbol{I}_5$ denotes the five-dimensional identity matrix.

III. FCS-MPC Problem Formulation

A. Control Target

The control objective of the current loop is to regulate the grid current to track its reference in the steady state. More specifically, the grid current's total harmonic distortion (THD) should be kept at a minimum to meet the grid codes. On the other hand, the ZSCC should be maintained near zero to reduce copper losses. When the current reference changes, fast dynamic performance is essential, meaning that the settling time should be as short as possible. Ultimately, it is desirable to maintain a low switching frequency for the paralleled power converters to minimize switching losses in the power switches.

$$\boldsymbol{F} = -\begin{bmatrix} \frac{R_1}{L_1} & 0 & 0 & 0 & 0 \\ 0 & \frac{R_1}{L_1} & 0 & 0 & 0 \\ 0 & 0 & \frac{R_2}{L_2} & 0 & 0 \\ 0 & 0 & 0 & \frac{R_2}{L_2} & 0 \\ 0 & 0 & 0 & 0 & \frac{R_1+R_2}{L_1+L_2} \end{bmatrix}, \boldsymbol{G}_1 = \frac{-v_{\rm dc}}{2}\begin{bmatrix} \frac{1}{L_1} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{L_1} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_2} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{L_2} & 0 \\ 0 & 0 & \frac{-1}{L_1+L_2} & 0 & 0 & \frac{1}{L_1+L_2} \end{bmatrix}\begin{bmatrix} \boldsymbol{T} & \boldsymbol{0}_{3\times3} \\ \boldsymbol{0}_{3\times3} & \boldsymbol{T} \end{bmatrix}, \boldsymbol{G}_2 = -\begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & \frac{1}{L_1} \\ \frac{1}{L_2} & 0 \\ 0 & \frac{1}{L_2} \\ 0 & 0 \end{bmatrix}.$$

B. Modified Integer Quadratic Problem

The optimization problem is formulated as a reference tracking problem. Conventionally, each converter tracks its own current reference. Meanwhile, the ZSCC is intended to be regulated to maintain a value close to zero. Hence, the output variables $\boldsymbol{y}(k)$ can be defined as

$$\boldsymbol{y}(k) = \boldsymbol{C}\boldsymbol{x}(k) \tag{13}$$

with $\boldsymbol{C} = \boldsymbol{I}_5$. The cost function with a prediction horizon of one can be formulated by

$$J = ||\boldsymbol{y}_{\text{ref}}(k+1) - \boldsymbol{y}(k+1)||^2_{\boldsymbol{Q}} + \lambda_u ||\Delta \boldsymbol{u}(k)||^2_2 \tag{14}$$

where $\boldsymbol{y}_{\text{ref}} = [i^*_{\alpha,1}, i^*_{\beta,1}, i^*_{\alpha,2}, i^*_{\beta,2}, i^*_z]^T$ denotes the reference of the state variables, $||\star||^2_2$ signifies the squared ℓ_2-norm of a vector, the penalty weighting matrix $\boldsymbol{Q}$ is symmetric and positive definite, and $\lambda_u > 0$ is the weighting factor to balance the tracking accuracy and the switching effort. The switching increment $\Delta\boldsymbol{u}(k)$ at time step k is defined as $\Delta\boldsymbol{u}(k) = \boldsymbol{u}(k) - \boldsymbol{u}(k-1)$. In (14), the first term penalizes the current tracking error, while the second term penalizes the switching efforts. In this way, each converter tracks its reference with minimum tracking error, and the grid-side total current i_{abc} exhibits a sinusoidal envelope accordingly.

Note that the grid-side total current i_{abc} is the primary concern regarding power quality. On the other hand, power-sharing among parallel power converters is also important. Therefore, the current from any one converter should be considered as a control objective. Thereby, the output reference can be modified as

$$\boldsymbol{y}_{\text{ref}} = [(i^*_{\alpha,1} + i^*_{\alpha,2}), (i^*_{\beta,1} + i^*_{\beta,2}), i^*_{\alpha,1}, i^*_{\beta,1}, i^*_z]^T. \tag{15}$$

Inspired by this finding, an alternative output matrix, namely

$$\boldsymbol{C} = \begin{bmatrix} 1 & 0 & 1 & 0 & 0 \\ 0 & 1 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{16}$$

is proposed in this article. With this output matrix, the total current on the grid side is regulated directly. Rather than focusing on each respective converter's grid-side current, the alternative output matrix $\boldsymbol{C}$ facilitates the minimization of the grid-side total current's tracking error. This approach allows for the cancellation of the current ripple in the parallel units, akin to an interleaving mechanism, thereby further enhancing the power quality of the grid-side total current.

To demonstrate the discussed mechanism, simulations are carried out for $\boldsymbol{C} = \boldsymbol{I}_5$ and the definition in (16) using the ideal state space model. The weighting factor λ_u is adjusted to make the average switching frequency f_{sw} approximately equal. Both the initial and operating conditions are set identically to ensure a fair comparison. The test results shown in Fig. 3 indicate that lower current distortions of the phase current for each converter ($i_{a,1}$, $i_{a,2}$) are achieved when $\boldsymbol{C} = \boldsymbol{I}_5$. However, significantly improved power quality regarding the total grid-side current (i_a) is observed when using (16) as the $\boldsymbol{C}$ matrix, thanks to its current ripple cancellation ability across parallel converters. This effect is distinctly visible in the zoomed-in portion of Fig. 3.

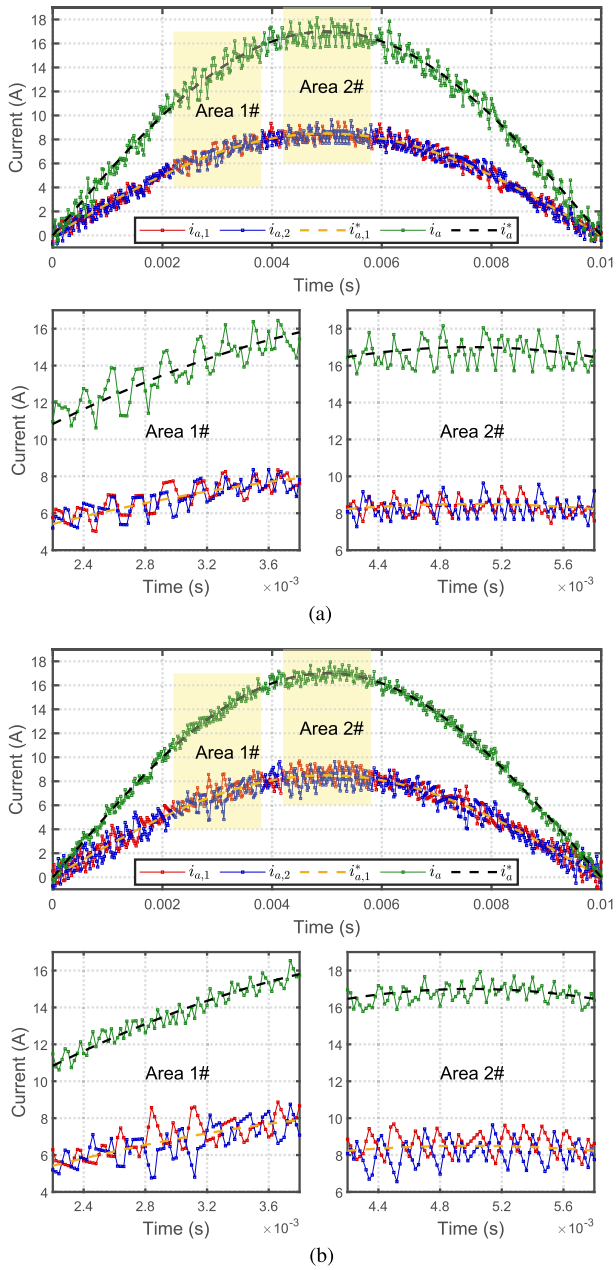


Fig. 3. Simulation results considering different $\boldsymbol{C}$ matrices. (a) $\boldsymbol{C} = \boldsymbol{I}_5$ with $f_{\text{sw}} \approx 5.1$ kHz. (b) as $\boldsymbol{C}$ defined in (16) with $f_{\text{sw}} \approx 4.9$ kHz.

Remark 1: Minimizing current distortion by directly regulating the total current is an intuitive approach. However, this goal can also be accomplished by appropriately designing the weight matrix $\boldsymbol{Q}$. By substituting (13) into (14), we obtain

$$\begin{aligned} J &= ||\boldsymbol{C}\boldsymbol{x}_{\text{ref}}(k+1) - \boldsymbol{C}\boldsymbol{x}(k+1)||^2_{\boldsymbol{Q}} + \lambda_u ||\Delta\boldsymbol{u}||^2_2 \\ &= \Delta\boldsymbol{x}^T(k+1)\boldsymbol{C}^T\boldsymbol{Q}\boldsymbol{C}\Delta\boldsymbol{x}(k+1) + \lambda_u ||\Delta\boldsymbol{u}||^2_2 \\ &= \Delta\boldsymbol{x}^T(k+1)\boldsymbol{Q}^*\Delta\boldsymbol{x}(k+1) + \lambda_u ||\Delta\boldsymbol{u}||^2_2 \end{aligned} \tag{17}$$

where $\Delta\boldsymbol{x}(k+1) = \boldsymbol{x}_{\text{ref}}(k+1) - \boldsymbol{x}(k+1)$. Thus, when the $\boldsymbol{C}$ matrix is defined as in (16), and the weighting matrix is $\boldsymbol{Q}$,

we can determine that $\boldsymbol{Q}^* = \boldsymbol{C}^T\boldsymbol{Q}\boldsymbol{C}$, resulting in the same cost function with $\boldsymbol{C} = \boldsymbol{I}_5$.

In addition, in a digitally controlled system, the time delay effect should be considered due to the sampling and calculation time. An effective method to compensate for this time delay is to predict the state variables one step ahead using the measurement at time step k [21]. Then, the cost function is rewritten as

$$J = ||\boldsymbol{y}_{\text{ref}}(k+2) - \boldsymbol{y}(k+2)||^2_{\boldsymbol{Q}} + \lambda_u||\Delta\boldsymbol{u}(k+1)||^2_2. \quad (18)$$

Note that the integer input constraint can be stated as $\boldsymbol{u} \in \mathbb{U} = \mathcal{U}^6 = \{-1, 1\}^6$, where $\mathcal{U}$ denotes the set of discrete three-phase two-level power converter's switch positions, and $\mathbb{U}$ is the 6-times Cartesian product of the set $\mathcal{U}$. Now, we formulate the integer quadratic program (IQP) underlying FCS-MPC as

$$\begin{aligned}
\boldsymbol{u}_{\text{opt}}(k+1) &= \arg \underset{\boldsymbol{u}(k+1)}{\text{minimize}}\ J \\
\text{s.t. } \boldsymbol{x}(k+2) &= \boldsymbol{A}\boldsymbol{x}(k+1) + \boldsymbol{B}_1\boldsymbol{u}(k+1) + \boldsymbol{B}_2\boldsymbol{d}(k+1) \\
\boldsymbol{y}(k+1) &= \boldsymbol{C}\boldsymbol{x}(k+1) \\
\Delta\boldsymbol{u}(k+1) &= \boldsymbol{u}(k+1) - \boldsymbol{u}(k) \\
\boldsymbol{u}(k+1) &\in \mathbb{U}. \qquad (19)
\end{aligned}$$

Regarding the IQP (19), it can usually be solved by an exhaustive search method for very short horizons. However, for paralleled power converters, the number of admissible switch positions is $2^6 = 64$ for the case of a horizon equal to one. In this case, the computational challenge arises when employing the exhaustive search method.

As mentioned earlier, some modifications to the IQP (19) are intentionally made to simplify computational complexity. However, reformulating the cost function or restricting the feasible control set can impact optimality [20]. To guarantee the optimality, an efficient MSD algorithm [2] and its alternatives [22], [23] have been proposed for solving the optimization problem efficiently.

IV. Efficient Method for Solving the IQP

A. Transformed Unconstrained Optimum

In [2], the detailed process of transforming the cost function into compact vector form is provided. The basic idea is to incorporate the dynamic model (11) and (13) into the cost function. With similar algebraic manipulation (see [2, Appendix 5.B]), we obtain the following compact form:

$$J = (\boldsymbol{u}(k+1))^T\boldsymbol{H}\boldsymbol{u}(k+1) + 2(\boldsymbol{\Theta}(k+1))^T\boldsymbol{u}(k+1) + \theta(k+1) \quad (20)$$

where

$$\begin{aligned}
\boldsymbol{H} &= (\boldsymbol{C}\boldsymbol{B}_1)^T\boldsymbol{Q}(\boldsymbol{C}\boldsymbol{B}_1) + \lambda_u\boldsymbol{I}_6 \\
\boldsymbol{\Theta}(k+1) &= \boldsymbol{B}_1^T\boldsymbol{C}^T\boldsymbol{Q}(\boldsymbol{y}_{\text{ref}}(k+2) - \boldsymbol{C}\boldsymbol{A}\boldsymbol{x}(k+1) \\
&\quad - \boldsymbol{C}\boldsymbol{B}_2\boldsymbol{d}(k+1)) + \lambda_u\boldsymbol{u}(k) \\
\theta(k+1) &= ||\boldsymbol{y}_{\text{ref}}(k+2) - \boldsymbol{C}\boldsymbol{A}\boldsymbol{x}(k+1) - \boldsymbol{C}\boldsymbol{B}_2\boldsymbol{d}(k+1)||^2_{\boldsymbol{Q}} \\
&\quad + \lambda_u||\boldsymbol{u}(k)||^2_2. \qquad (21)
\end{aligned}$$

Algorithm 1: Non-Recursive Sphere Decoding.

function $\boldsymbol{u}_{\text{opt}}(k+1) = \text{SphDec}(\rho^2, \bar{\boldsymbol{u}}_{\text{unc}}(k+1))$
$j = 6$
$\boldsymbol{b} = [-1, -1, -1, -1, -1, -1]^T$
$\boldsymbol{d}^2 = [0, 0, 0, 0, 0, 0]^T$
OptimalFound = False
while OptimalFound = False **do**
  $u_j = b_j$
  $d'^2 = (\bar{u}_{\text{unc},j} - \boldsymbol{V}_{(j,j:6)}\boldsymbol{u}_{j:6})^2 + d_j^2$ ▷ Eq. (26)
  if $d'^2 \le \rho^2$ **then**
    if $j = 1$ **then**
      $\boldsymbol{u}_{\text{opt}}(k+1) = \boldsymbol{u}$
      $\rho^2 = d'^2$
      $b_j = b_j + 2$
    else
      $j--$
      $d_j^2 = d'^2$
    end if
  else
    $b_j = b_j + 2$
  end if
  for $q = 1$ to 5 **do**
    if $b_q > 1$ **then**
      $b_q = -1$
      $j = q + 1$
      $b_j = b_j + 2$
    end if
  end for
  if $b_6 > 1$ **then**
    OptimalFound = True
  end if
end while

Note that $\boldsymbol{H}$ is symmetric and positive definite; therefore, it can be decomposed by an upper triangular matrix $\boldsymbol{V}$ [2], namely Cholesky decomposition[1]

$$\boldsymbol{V}^T\boldsymbol{V} = \boldsymbol{H}. \quad (22)$$

The upper triangular matrix $\boldsymbol{V}$ can be obtained in MATLAB using the command `chol`. Based on the vector form of the cost function and Cholesky decomposition, the FCS-MPC problem (19) can be transformed into an integer least-squares problem

$$\begin{aligned}
\boldsymbol{u}_{\text{opt}}(k+1) &= \arg \underset{\boldsymbol{u}(k+1)}{\text{minimize}}\ ||\boldsymbol{V}\boldsymbol{u}(k+1) - \bar{\boldsymbol{u}}_{\text{unc}}(k+1)||^2_2 \\
\boldsymbol{u}(k+1) &\in \mathbb{U} \qquad (23)
\end{aligned}$$

where

$$\bar{\boldsymbol{u}}_{\text{unc}}(k+1) = \boldsymbol{V}\boldsymbol{H}^{-1}\boldsymbol{\Theta}(k+1) \quad (24)$$

is the transformed unconstrained optimal solution.

[1] In linear algebra, Cholesky decomposition is the decomposition of a positive-definite matrix into the product of an upper triangular matrix and its (conjugate) transpose, which is useful for efficient numerical solutions.

B. MSD Algorithm

The MSD algorithm has been proposed and utilized for predictive control in power converters and electrical drives with long horizons [2], [22], [23]. This technique is adopted in this work to reduce the computational burden. MSD works by evaluating potential solutions $\boldsymbol{u}(k+1) \in \mathbb{U}$ within a defined radius ρ, centered around the transformed unconstrained optimum $\bar{\boldsymbol{u}}_{\text{unc}}(k+1)$, i.e.,

$$||\bar{\boldsymbol{u}}_{\text{unc}}(k+1) - \boldsymbol{V}\boldsymbol{u}(k+1)||_2 \leq \rho(k). \tag{25}$$

The process involves progressively narrowing the search radius and eliminating solutions that do not meet the criteria (25). The optimal solution $\boldsymbol{u}_{\text{opt}}(k+1)$, is identified when only one admissible solution is within the sphere. To start, an initial solution is selected, which could be either the so-called Babai estimation [24] or an educated estimation. The former is determined by rounding the unconstrained optimum to the closest integer solution, while the latter is resembled by the previous step optimal solution $\boldsymbol{u}_{\text{opt}}(k)$. The minimum of the two options can be configured as the initial radius to improve the efficacy of the MSD algorithm.

Since $\boldsymbol{V}$ is upper triangular, the radius can be written as

$$\begin{aligned} d'^2 = &\left(\bar{u}_{\text{unc},6} - v_{(6,6)}u_6\right)^2 \\ &+ \left(\bar{u}_{\text{unc},5} - v_{(5,5)}u_5 - v_{(5,6)}u_6\right)^2 + \cdots \end{aligned} \tag{26}$$

where $\bar{u}_{\text{unc},i}$ and u_i denote the ith $(i = 1, 2, \ldots 6)$ element of $\bar{\boldsymbol{u}}_{\text{unc}}$ and $\boldsymbol{u}$, and $v_{(i,j)}$ refers to the (i,j)th entry of $\boldsymbol{V}$. The nonrecursive MSD algorithm, which is proposed in [23], is summarized in Algorithm 1 with proper modification to fit the problem on hand. The optimal control $\boldsymbol{u}$ is built component by component from the bottom to the top since $\boldsymbol{V}$ is upper triangular, i.e., $u_6 \rightarrow u_5 \rightarrow \cdots \rightarrow u_1$. This assembly process of $\boldsymbol{u}$ differs from that shown in [23].

C. Control Structure and Reference Generation

In this work, we consider two parallel power converters operating in rectification mode as an illustrative example. The control block diagram is depicted in Fig. 4. A PI controller is utilized to regulate the dc bus voltage v_{dc} to be constant. The output of the outer loop generates the d-axis current reference i_d^*. When combined with the q-axis current reference i_q^*, the grid-side total current reference in the $\alpha\beta$ frame can be obtained by applying the following transformation:

$$\begin{bmatrix} i_\alpha^* \\ i_\beta^* \end{bmatrix} = \begin{bmatrix} \cos\varphi & -\sin\varphi \\ \sin\varphi & \cos\varphi \end{bmatrix} \cdot \begin{bmatrix} i_d^* \\ i_q^* \end{bmatrix}.$$

We define $[i_{\alpha,1}^*, {}^* i_{\beta,1}]^T = [i_{\alpha,2}^*, i_{\beta,2}^*]^T = 0.5 \cdot [i_\alpha^*, i_\beta^*]^T$ to achieve equal power sharing in the parallel power converters. In addition, we set $i_z^* = 0$ to suppress the ZSCC. As a result, the output reference $\boldsymbol{y}_{\text{ref}}$ can be generated as

$$\boldsymbol{y}_{\text{ref}} = [i_{\alpha,1}^*, i_{\beta,1}^*, i_{\alpha,2}^*, i_{\beta,2}^*, i_z^*]^T \tag{27}$$

for $\boldsymbol{C} = \boldsymbol{I}_5$, and

$$\boldsymbol{y}_{\text{ref}} = [i_\alpha^*, i_\beta^*, i_{\alpha,1}^*, i_{\beta,1}^*, i_z^*]^T \tag{28}$$

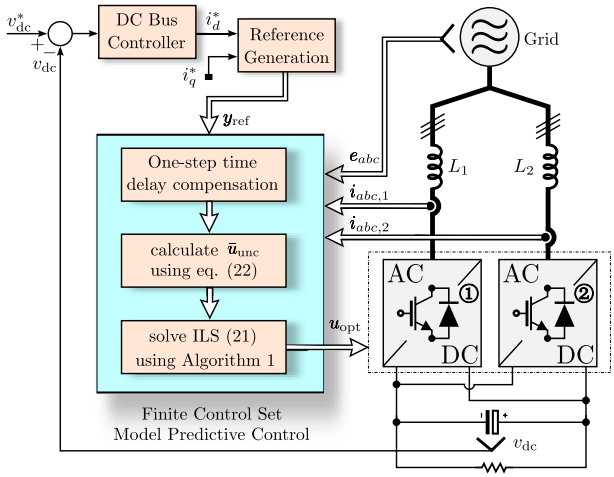


Fig. 4. Control block diagram of FCS-MPC with reference tracking and ZSCC suppression for grid-connected parallel power converters.

Fig. 5. Experimental test bench.

for $\boldsymbol{C}$ defined in (16). Subsequently, the proposed FCS-MPC is implemented, and the optimal control $\boldsymbol{u}_{\text{opt}}$ is applied to the power stage to track the current reference.

V. Experimental Results

The hardware setup, depicted in Fig. 5, incorporates Imperix Ltd's rapid control prototyping and two three-phase two-level grid-connected power converters to facilitate the implementation of the proposed control algorithm. We use different values of inductors for the parallel power converters. The outer voltage loop regulates the dc bus voltage at 350 V, the load connected to the dc bus is 33.3 Ω. In addition, we set $i_q^* = -10$ A for each single converter to make the amplitude of the phase current close to its rated value. The detailed parameters of the power conversion system are summarized in Table I.

In the article, three methods are implemented to conduct a comprehensive comparative study. In particular, the first method

TABLE I
DETAILED PARAMETERS OF PARALLEL POWER CONVERTERS

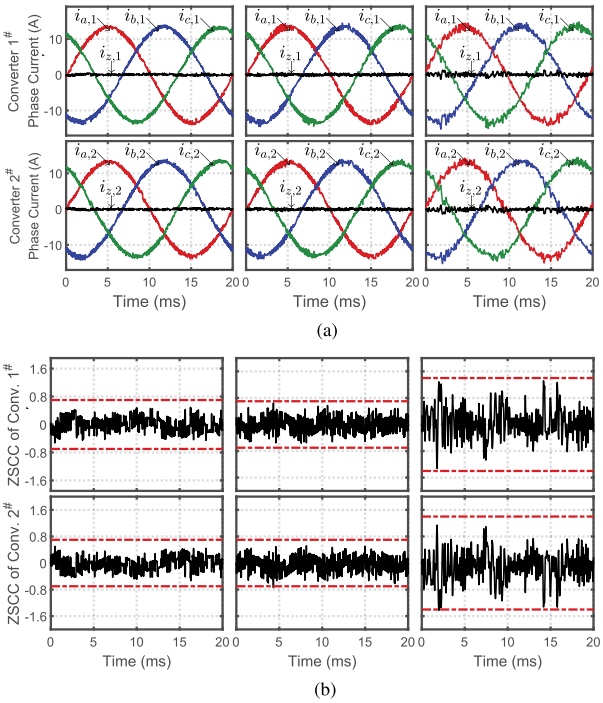
Parameter	Value	Parameter	Value
Inductor L_1	4.5 mH	Parasitic Res. R_1	20 mΩ
Inductor L_2	3.2 mH	Parasitic Res. R_2	20 mΩ
Grid freq. f_g	50 Hz	Grid vol. (RMS) e	110 V
DC vol. $v_{\rm dc}$	350 V	Sampling freq. f_s	Meth-1: 50 kHz Meth-2: 50 kHz Meth-3: 20 or 25 kHz

TABLE II
DESCRIPTION OF CONTROL METHODS

Method	Description	Control Targets
Meth-1	applies FCS-MPC to solve problem (19) with $\boldsymbol{C} = \boldsymbol{I}_5$	$i_{a,1}$, $i_{a,2}$, i_z
Meth-2	applies FCS-MPC to solve problem (19) with $\boldsymbol{C}$ defined in (16)	i_a, $i_{a,1}$, i_z
Meth-3	applies a synthesized voltage vector, consisting of an optimal shrunken voltage vector and a zero voltage vector	$i_{a,1}$, $i_{a,2}$, i_z

TABLE III
AVERAGE AND MAXIMAL NUMBER OF SWITCHING SEQUENCES FOR DIFFERENT METHODS

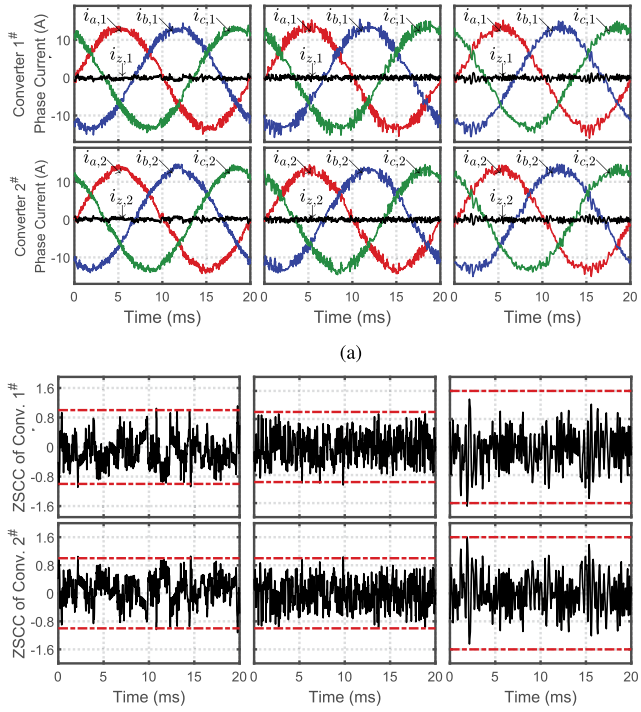
Meth.	avg. SS	max. SS	execution time
Meth-1	3.24	6	13.34 μs
Meth-2	3.24	6	13.34 μs
Exhausitve search	64	64	22.40 μs
Meth-3	16	16	7.32 μs



(a)

(b)

Fig. 6. Time-domain phase current and ZSCC waveform at higher average switching frequencies: Meth-1 (left), Meth-2 (middle), Meth-3 (right). (a) Waveform of the phase current and the ZSCC. (b) Zoomed-in view of the ZSCC.



(a)

(b)

Fig. 7. Time-domain phase current and ZSCC waveform at lower average switching frequencies: Meth-1 (left), Meth-2 (middle), Meth-3 (right). (a) Waveform of the phase current and the ZSCC. (b) Zoomed-in view of the ZSCC.

(Meth-1) applies FCS-MPC to solve problem (19) with $\boldsymbol{C} = \boldsymbol{I}_5$, i.e., it directly regulates the phase current of each converter and ZSCC. Alternatively, the second method (Meth-2) adopts FCS-MPC to solve problem (19) with $\boldsymbol{C}$ defined in (16). Specifically, it regulates the grid-side total current, one converter's phase current, and ZSCC. For both Meth-1 and Meth-2, Algorithm 1 is used to reduce the computational load. In our test, the sampling frequency f_s of Meth-1 and Meth-2 is 50 kHz. The weighting matrix $\boldsymbol{Q}$ is selected as $\boldsymbol{Q}_{\rm M1} = \boldsymbol{I}_5$ for Meth-1, and

$$\boldsymbol{Q}_{\rm M2} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0.5 & 0 & 0 \\ 0 & 0 & 0 & 0.5 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{29}$$

is designed for Meth-2. The average switching frequency $f_{\rm sw}$ can be adjusted by tuning the weighting factor λ_u (see Table IV). Lastly, the third method, which is proposed in [18], is denoted by Meth-3. This method sets switching frequency $f_{\rm sw}$ slightly lower than its sampling frequency f_s due to the employment of the synthesized voltage vectors. We set f_s equal to 25 kHz or 20 kHz for Meth-3 to facilitate the comparative study. Table II summarizes these three methods.

A. Computational Burden

The computational burden of the three methods is analyzed here. The metrics used to evaluate the computational burden

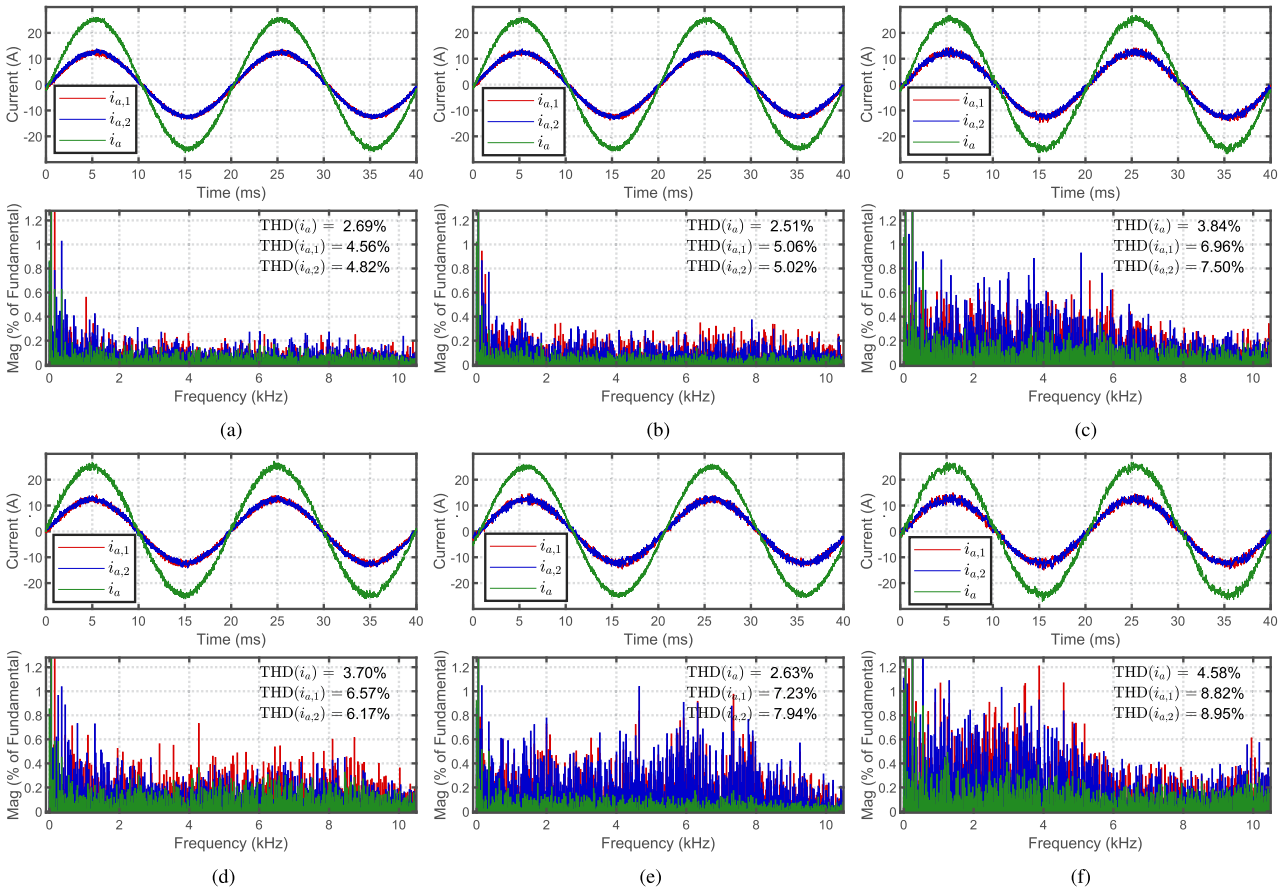


Fig. 8. Time-domain phase current waveform and harmonic amplitude spectrum for different control methods. (a) Meth-1 with $f_{\rm sw} \approx 9.2$ kHz. (b) Meth-2 with $f_{\rm sw} \approx 9.1$ kHz. (c) Meth-3 with $f_{\rm sw} \approx 22$ kHz. (d) Meth-1 with $f_{\rm sw} \approx 5.2$ kHz. (e) Meth-2 with $f_{\rm sw} \approx 4.9$ kHz. (f) Meth-3 with $f_{\rm sw} \approx 17$ kHz.

include the number of switching sequences (a six-dimensional column vector) and execution time. For Meth-1 and Meth-2, we recorded the number of switching sequences traversed over ten thousand consecutive time steps. The average and maximum number of switching sequences are presented in Table III. When MSD is employed in both Meth-1 and Meth-2, the computational efficiency is nearly identical. This similarity arises because all matrices used in MSD are precomputed offline, and the algorithm for both Meth-1 and Meth-2 is implemented in the same manner. Specifically, Table III indicates that an average of 3.24 switching sequences are required per time step for both methods, and the upper bound on the number of switching sequences is 6. The execution time, which includes the outer dc-link voltage loop, coordinate transformation, PLL, and MSD, is $13.34\,\mu s$. In comparison, the exhaustive search method must traverse all 64 switching sequences, resulting in an execution time of $22.40\,\mu s$. This duration is impractical for a sampling frequency set to 50 kHz. This comparison demonstrates that MSD is sufficiently computationally efficient when the minimum initial radius is chosen.

Meth-3 examines 16 switching sequences at each time step. However, it utilizes a simpler prediction model (a two-dimensional state-space model) because it treats the parallel power converters individually and addresses the optimization problem sequentially. The execution time for Meth-3 is $7.32\,\mu s$. Although Meth-3 is computationally efficient, its control performance is degraded due to the simplifications made in the optimization problem. A detailed comparison of control performance will be discussed subsequently.

B. ZSCC Suppression Performance

In this part, the ZSCC suppression performance of parallel power converters at steady state is investigated. Two critical aspects of control performance are considered, i.e., the suppression of ZSCC and the THD of grid integration current. To examine the tradeoff between the current THD and switching frequency, the weighting factor λ_u is finely tuned to obtain the appropriate average switching frequency $f_{\rm sw}$. Two typical scenarios are considered, i.e., high switching frequency scenario (approximately 9 kHz for Meth-1 and Meth-2, and 22 kHz for Meth-3), and low switching frequency scenario (approximately 5 kHz for Meth-1 and Meth-2, and 17 kHz for Meth-3).

Fig. 6(a) displays the time-domain waveforms of the phase current and ZSCC under various control methods. The average switching frequencies at steady state for Meth-1, Meth-2, and Meth-3 are 9.2 kHz, 9.1 kHz, and 22 kHz, respectively. The three-phase current shows a sinusoidal envelope, and the ZSCC is effectively regulated around zero, highlighting the efficacy of all examined control methods in ZSCC suppression. However,

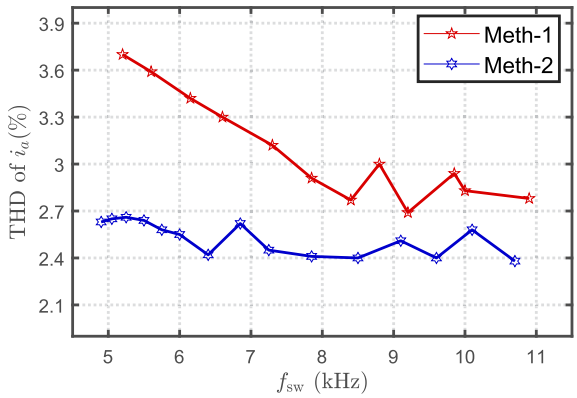


Fig. 9. Comparative study of Meth-1 and Meth-2 considering the tradeoff between grid-side current THD and average switching frequency.

the zoomed-in ZSCC shown in Fig. 6(b) reveals the superiority of Meth-1 and Meth-2, where the ZSCCs are contained within $\pm$ 0.7 A. The proposed FCS-MPC technique enables parallel power converters to simultaneously minimize the tracking error for both phase current and zero-sequence current. By contrast, the magnitudes of ZSCC reach $\pm$ 1.4 A with Meth-3, primarily due to its hysteresis-based control strategy for ZSCC, resulting in a higher current ripple.

Identical operating conditions are replicated with lower average switching frequencies, and the experimental results are depicted in Fig. 7. Specifically, the average switching frequencies at steady state for Meth-1, Meth-2, and Meth-3 are 5.2 kHz, 4.9 kHz, and 17 kHz, respectively. Despite an increase in current ripples compared to the previous tests due to the reduction in average switching frequencies, the phase current and zero-sequence current are still well regulated. The ZSCCs remain within $\pm$ 1A for Meth-1 and Meth-2, while the magnitudes of Meth-3 reach 1.6 A. In summary, compared to Meth-3, the proposed methods significantly reduce the ZSCC at much lower average switching frequencies.

C. Phase Current Distortions

When conducting the comparative study of power quality, current distortion should be evaluated at approximately the same average switching frequency, i.e., examining current distortions per switching frequency. The data for Fourier analysis are sampled with a time resolution of $4\,\mu s$. The time-domain current waveform of phase A (including $i_{a,1}$, $i_{a,2}$, and i_a) and the magnitude of the harmonics spectrum are shown in Fig. 8. Upon comparing the performance across these three scenarios, Meth-1 and Meth-2 (as proposed in this article) outperform Meth-3 (as proposed in [18]) with a significant reduction in THD, despite their switching frequency being much lower than that of Meth-3. This difference in performance is attributed to the proposed FCS-MPC ensuring an optimal solution, whereas suboptimality arises when solving the optimal problem sequentially in Meth-3.

Furthermore, by comparing the performance of Meth-1 and Meth-2 in detail, more insights are revealed. Meth-1 achieves lower THDs of the phase current for each individual converter ($i_{a,1}, i_{a,2}$) compared to Meth-2. However, Meth-2 accomplishes

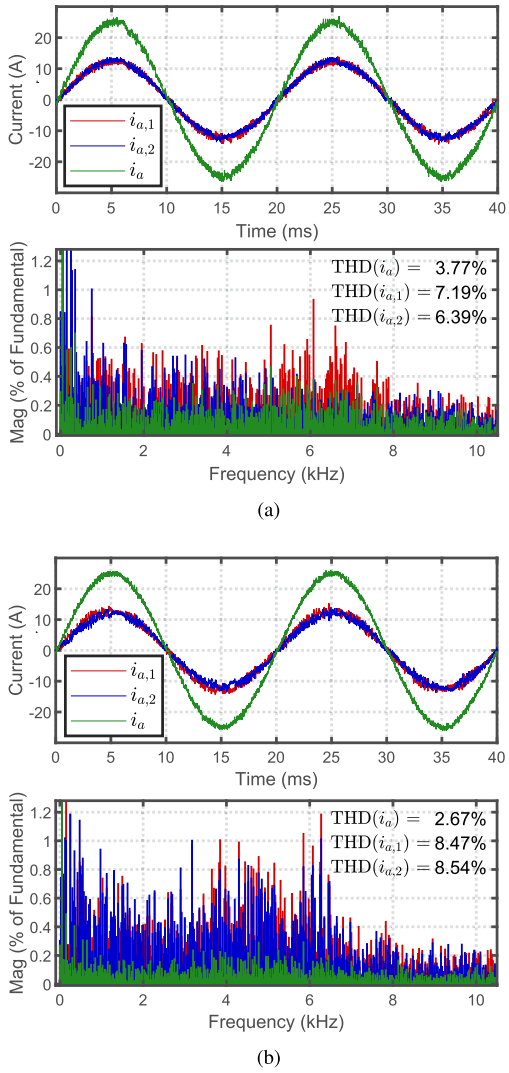


Fig. 10. Time-domain phase current waveform and harmonic amplitude spectrum considering parameter variations. (a) Meth-1 with +20% and -20% parameter variations in the nominal value of L_1 and L_2, respectively. (b) Meth-2 with +20% and -20% parameter variations in the nominal value of L_1 and L_2, respectively.

a much better power quality when considering the total grid-side current (i_a). As previously explained, Meth-2 facilitates current ripple cancellation in each parallel converter. The quantitative comparison is summarized in Table IV. In summary, Meth-2 outperforms Meth-1 in terms of grid-side total current distortions per switching frequency. This improvement becomes more significant at lower switching frequencies, which is depicted in Fig. 9.

D. Robustness Against Parameter Variations

In power converters, the inductance can vary over time, potentially leading to discrepancies between the physical system and the predictive model. It has been validated that FCS-MPC is generally robust to such parameter variations. In this work, the impact of the model parameter variations is experimentally verified. We introduce a mismatch between the parameters of

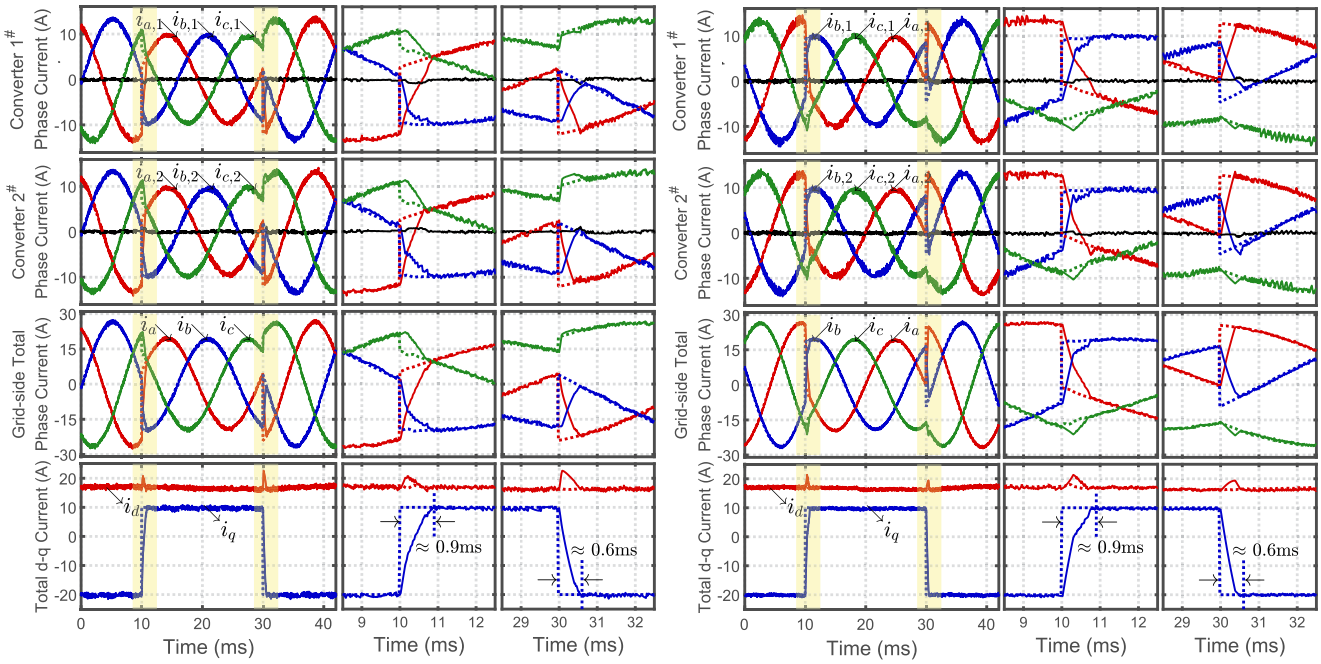


Fig. 11. Time-domain phase current waveform during transients for Meth-1 and Meth-2. (a) Meth-1 with $\lambda_u = 0.05$. (b) Meth-2 with $\lambda_u = 0.05$.

TABLE IV
CURRENT THD COMPARISON FOR DIFFERENT CONTROL METHODS

Method	Q	f_{sw}	λ_u	Current THDs		
				i_a	$i_{a,1}$	$i_{a,2}$
Meth-1	Q_{M1}	9.2 kHz	0.05	2.69%	4.56%	4.82%
Meth-2	Q_{M2}	9.1 kHz	0.04	2.51%	5.06%	5.02%
Meth-3	/	22 kHz	/	3.84%	6.96%	7.50%
Meth-1	Q_{M1}	5.2 kHz	0.22	3.70%	6.57%	6.17%
Meth-2	Q_{M2}	4.9 kHz	0.15	2.63%	7.23%	7.94%
Meth-3	/	17 kHz	/	4.58%	8.82%	8.95%

TABLE V
CURRENT THD INVESTIGATION CONSIDERING PARAMETER VARIATIONS

Meth.	Model Parameter Variations		f_{sw}	THD (i_a)
Meth-1	$L_{1,\mathrm{n}}$	$L_{2,\mathrm{n}}$	5.2 kHz	3.70%
Meth-1	$120\% \times L_{1,\mathrm{n}}$	$80\% \times L_{2,\mathrm{n}}$	6.1 kHz	3.77%
Meth-2	$L_{1,\mathrm{n}}$	$L_{2,\mathrm{n}}$	4.9 kHz	2.63%
Meth-2	$120\% \times L_{1,\mathrm{n}}$	$80\% \times L_{2,\mathrm{n}}$	5.5 kHz	2.67%

the predictive model in the controller and the actual values of the filter inductors. Specifically, L_1 is adjusted to a +20% variation and L_2 to a -20% variation from their nominal values $L_{1,\mathrm{n}}$ and $L_{2,\mathrm{n}}$. The experimental time-domain phase current waveform and harmonic amplitude spectrum are depicted in Fig. 10. The performance of the system, considering these parameter mismatches, is summarized in Table V. The test results indicate that the average switching frequency f_{sw} is slightly higher with these parameter mismatches. Nevertheless, the current distortion is marginally higher than the scenarios without parameter mismatch. In summary, the proposed solution demonstrates robustness to model parameter variations.

E. Performance During Transients

As well identified, FCS-MPC enables the power converters to achieve extremely fast dynamic behavior during transients. To validate these benefits, steps are imposed on the q-axis current reference. In particular, the i_q^* for each converter steps from -10 A to 5 A at 10 ms, and then steps back at 30 ms. The experimental results of the three-phase current and the transformed total current on the dq-axis are depicted in Figs. 11 and 12, where the dotted lines denote the corresponding reference values. The transient process details, highlighted in yellow, are enlarged on the right-hand side. A tracking error arises on the d-axis current during the q-axis current steps. However, this error dissipates after the transient. Crucially, the ZSCC stays low throughout, avoiding significant fluctuations.

In Fig. 11(a) and (b), the control schemes of Meth-1 and Meth-2 are implemented. As observed, the current trajectories converge to their reference values rapidly for both methods. The settling times are extremely short, i.e., approximately 0.9 ms for stepping up and 0.6 ms for stepping down. As depicted in Fig. 12, the settling time becomes significantly longer when Meth-3 is implemented, approximately 1.9 ms for stepping up and 1.1 ms for stepping down. This is attributed to the synthesized voltage vector resulting in a reduction in the amplitude of the effective voltage vector applied to the $\alpha\beta$ plane. In contrast, by ensuring optimality, Meth-1 and Meth-2 allow the power converter to achieve the fastest transient response (in theory) considering the physical constraints.

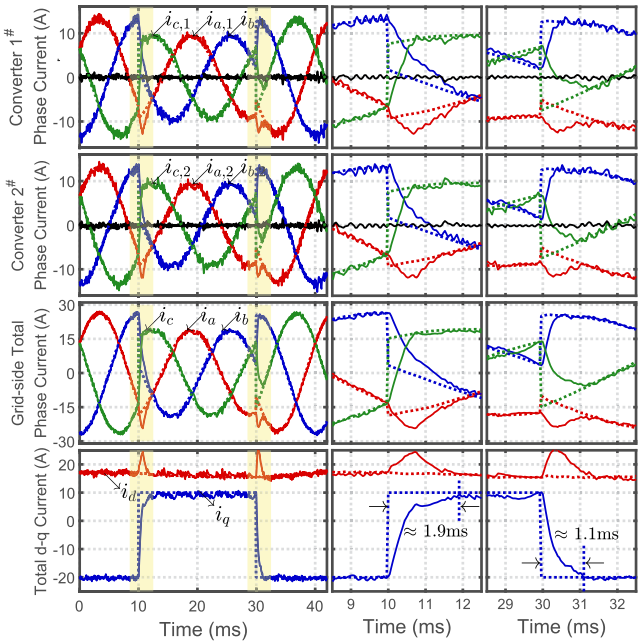


Fig. 12. Time-domain phase current waveform during transients for Meth-3.

VI. Conclusion

FCS-MPC is a promising alternative for the control of parallel-connected power converters due to its ability to handle multivariable and nonlinearity constraints. However, inappropriate simplifications of the optimization problem can degrade control performance in terms of power quality per switching frequency and transient response. This work formulates the current tracking and ZSCC suppression problem of parallel converters as a formal FCS-MPC problem. A computationally efficient MSD algorithm is used to facilitate its real-time implementation. The guaranteed optimal solution maximizes the control performance at steady state and during transients. Furthermore, an alternative cost function that regulates the grid-side total current is designed to further reduce the distortion of grid integration current. We evaluate the proposed control scheme using two parallel grid-tied AFE rectifiers. Comprehensive experimental results demonstrate its effectiveness in reducing current distortion and improving transient response.

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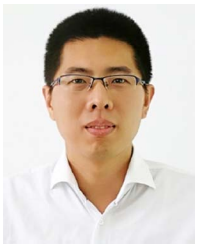
Yu Li (Member, IEEE) was born in Shandong, China, in 1986. He received the M.S. degree in power electronics and electric drives from the School of Automation, Northwestern Polytechnical University, Xi'an, China, in 2012, and the Ph.D. degree in electrical engineering from the School of Electrical Engineering, Shandong University, Jinan, China, in 2022.

From 2013 to 2015, he was a Research Engineer with the Department of Electrical and Computer Engineering, Kettering University, Flint, MI, USA. Since 2022, he has been an Assistant Professor with the Laser Institute, Qilu University of Technology (Shandong Academy of Sciences), Jinan, China. His research interests include control in power electronics converters, energy storage systems, and microgrids.

Jianbo Gao (Member, IEEE) was born in Shandong, China. He received the B.S., M.S., and Ph.D. degrees in automation from Tsinghua University, Beijing, China, in 1994, 1997, and 2001, respectively.

In 2001, he was a Researcher with the Fraunhofer Institute for Biomedical Engineering, St. Ingbert, Germany, where he became the Technical Director of the Chinese Branch of the Institute, Beijing, China, in 2002 and left in 2008. After a short stay in the automotive industry, he has been a Researcher with the Institute for Electric Drive Systems and Power Electronics, Technical University of Munich, Munich, Germany, since 2010. Since 2017, he has been a Full Professor and Team Director with the Laser Institute, Qilu University of Technology (Shandong Academy of Sciences), Jinan, China. His research interests include power electronics, electric drives, and signal processing technologies.



Qiwu Wang was born in Shandong, China, in 1986. He received the M.S. degree in mechanical engineering from the Royal Institute of Technology, Stockholm, Sweden, in 2012. He is currently working toward the Ph.D. degree in electric engineering from the Technical University of Munich, Munich, Germany.

He is currently an Assistance Professor with the Qilu University of Technology (Shandong Academy of Science), Jinan, China. His research interests include power electronics, motor drive and motion control, predictive control of nonlinear systems, as well as real-time heterogeneous computations.

Zhenzhen Zhang was born in Shandong, China. He received the master's degree in condensed matter physics from the School of Information Science and Engineering, Ocean University of China, Qingdao, China, in 2014. He is currently working toward the Ph.D. degree in instrument science and technology from Beihang University, Beijing, China.

Since 2020, he has been an Associate Professor with the Laser Institute, Qilu University of Technology (Shandong Academy of Sciences), Jinan, China. His research interests include power electronics, nondestructive testing, and automatic control.

Fangfang Zhang received the M.S. degree in control theory and control engineering from the Beijing University of Technology, Beijing, China, in 2003, and the Ph.D. degree in control theory and control engineering from Shandong University, Jinan, China, in 2014.

She is currently an Associate Professor with the School of Information and Automation Engineering, Qilu University of Technology (Shandong Academy of Sciences), Jinan, China. Her research interests include modeling and control of power electronics.

Zhenbin Zhang (Senior Member, IEEE) was born in Shandong, China, in 1984. He received the Ph.D. degree (*summa cum laude*) in electrical engineering from the Institute for Electrical Drive Systems and Power Electronics (EAL), Technical University of Munich (TUM), Munich, Germany, in 2016.

He was a Postdoctoral in Electrical and Energy Engineering with the TUM. Since 2017, he has been a Full Professor with Shandong University, Jinan, China, where he is currently the Director for both the Laboratory of More Power Electronics Energy Systems and the Institute of Sustainable Energy and Smart Grids. His research interests include power electronics and electrical drives, sustainable energy system, smart- and microgrids.

Dr. Zhang was the recipient for VDE Award-2017 in Suedbayern, Germany, and an Associate Editor for IEEE TRANSACTIONS POWER ELECTRON. He is currently an IET Fellow Member and IET Chartered Engineer.

Fengxiang Wang (Senior Member, IEEE) was born in Jiujiang, China, in 1982. He received the B.S. degree in electronic engineering and the M.S. degree in automation from Nanchang Hangkong University, Nanchang, China, in 2005 and 2008, respectively, and the Ph.D. degree in electrical engineering from the Institute for Electrical Drive Systems and Power Electronics, Technische Universitaet Muenchen, Munich, Germany, in 2014.

He is currently a Full Professor and the Director of the Quanzhou Institute of Equipment Manufacturing, Haixi Institutes, Chinese Academy of Sciences, Beijing, China. His research interests include predictive control and sensorless control for electrical drives and power electronics.

Dr. Wang is an IET Fellow and an Associate Editor for IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS and IEEE TRANSACTIONS ON ENERGY CONVERSION. As the General Chair, he organized IEEE 5th International Symposium on Predictive Control of Electrical Drives and Power Electronics (PRECEDE).