Experimental and Simulated Verification of Power Cycling Reliability for Thin and Low Warpage Power Modules

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***Abstract*—Meeting both high-frequency and high-speed requirements is essential, and the small form factor designs for the architecture of high-powered modules are acknowledged to impact their reliability in subsequent applications. However, conventional power modules utilizing a direct bonded copper substrate still encounter warpage issues stemming from the manufacturing process. This results in suboptimal heat dissipation after heat sink assembly, leading to a failure to meet automotive specifications for high voltage and high current resistance. To address this concern, our research proposes a thin and low warpage power module with an insulating metal substrate and a thermal interface material structural design. This aims to enhance heat dissipation capacity while maintaining low warpage and ensuring high mechanical reliability. The study employs coupling simulation technology integrating a process-oriented approach with a follow-up automotive specification power cycle reliability test. This allows for estimation of the warpage behavior caused by the power module process and the mechanical response of the solder layer within the module. To validate the accuracy and credibility of the simulation results, actual vehicle fabrication and related power cycling experiments are conducted. Furthermore, an improvement solution for the power module is proposed to offer a high industrial competitiveness of the long-term packaging reliability.**

***Index Terms*—Finite element analysis, insulated metal substrate, power cycling, power module.**

I. Introduction

The urgent issues of energy conservation, carbon reduction, and environmental equity led to the signing of the Paris Agreement at the United Nations Climate Summit in 2015, replacing the Kyoto Protocol. This landmark agreement advocates for the global development of technological products aimed at reducing carbon emissions, resulting in a heightened demand for pure electric vehicles (EVs) and micro hybrid EVs after 2015. It signifies that the development and technology of power modules for personal mobile vehicles have become indispensable key technologies for the future. The auxiliary power module is a critical component in EVs that enables an efficient power transmission and require higher power ratings, voltage ranges, higher reliability over time [1]. In order to meet the requirements of high power density systems, the selection, and characteristic analysis of materials within their structures are important [2]. In the meanwhile, a more complete cooling system must be developed [3]. Thus, the development and challenges of power module packaging technology are issues worthy of investigation [4], [5]. It should be noticed that the heat dissipation capability of the module has a great impact on its performance [6], [7].

Based on power component types [8], power modules are categorized into metal oxide semiconductor field effect transistor (MOSFET) modules [7], insulated gate bipolar transistor (IGBT) modules [7], silicon carbide (SiC) modules [9], and gallium nitride modules [10]. The power module structure primarily comprises a power chip, ceramic substrate (direct bond copper or DBC), heat dissipation base plate (Baseplate), and housing. Power chips are affixed to the composite substrate, composed of insulating material and metal, through a reflow [11]. Traditional power modules with a DBC substrate, consisting of a ceramic substrate and a layer of copper metallization, often encounter warpage issues postassembly due to the stack of multiple layers of heterogeneous materials with varying properties. This warping adversely affects the overall heat dissipation performance of the power module and the heat sink when assembled. In response, insulated metal substrate (IMS) technology has been developed as a replacement for DBC substrates [12]. The design utilizes IMS based IGBT modules with a specification of 1700 V to optimize thickness and achieve thermal and insulation capabilities [13]. For high voltage applications, the insulation reliability of IMS portion is necessary to be greatly enhanced [14]. IMS boasts a simpler process and a reduced number of stacked layers, resulting in thinner thickness than DBC. Comprising thermal interface material and two layers of copper, IMS utilizes thermal interface materials (TIMs) to fill gaps between materials, reducing the contact thermal resistance in heat conduction [15]. Given the poor thermal conductivity of air (0.026 W/m·K), treated as adiabatic, TIMs effectively decrease

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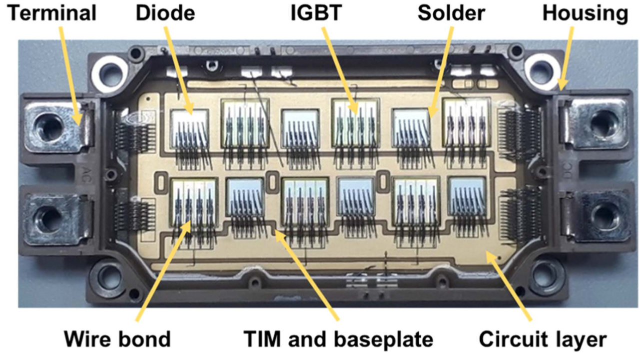

Fig. 1. IMS power module with 1200 V/600 A.

TABLE I
POWER MODULE SPECIFICATION WITH SI IGBT AND SIC MOSFET

Maker	Type	Voltage (V)	Current (A)	Packaging type
Industrial Technology Research Institute (ITRI)	Si IGBT	1200	600	IMS
Mitsubishi	Si IGBT	1200	225–800	IMS or DBC
Infineon	Si IGBT	1200	225–900	IMS or DBC
Wolfspeed	SiC MOSFET	1200	(30–760)	DBC
Rohm	SiC MOSFET	1200	80–576	-
Mitsubishi	Si IGBT	1700	225–600	IMS or DBC
Infineon	Si IGBT	1700	225–900	DBC
Wolfspeed	SiC MOSFET	1700	310–650	DBC
Rohm	SiC MOSFET	1700	250	-

the contact thermal resistance, enhancing the heat dissipation capacity of the power module. Power modules can be categorized into IMS and DBC types based on the composite substrate. In recent years, there has been a trend toward developing thinner modules with excellent heat dissipation capabilities, making IMS-type power modules the forefront of this development [16], [17]. Fig. 1 illustrates the IMS power module discussed in this study, consisting of six groups of IGBT chips and diodes with a withstand voltage and rated current of 1200 V and 600 A, respectively. Table I summarizes the specifications of Si IGBT, SiC MOSFETs, and this research in recent years.

The power module structure involves heterogeneous integration, leading to a coefficient of thermal expansion (CTE) mismatch within the module [18]. Consequently, the power module must undergo a series of reliability tests, including thermal cycling test (TCT) [19] and power cycling test (PCT) [20], to encompass its complete life cycle. Following TCT and PCT, the systematic assessment methods and the establishment of lifetime model are important issues to be discussed for power modules [21]. IGBT power modules are complex structures composed of different materials, and their failure modes can be mainly divided into two categories: 1) chip-related and 2) packaging-related [22]. Reliability of power components needs to be monitored during operation to avoid the occurrence of failure or breakdown [23]. The power cycling test involves applying current to the power module, with the test results closely resembling the actual operating conditions of the module. The fatigue effects of

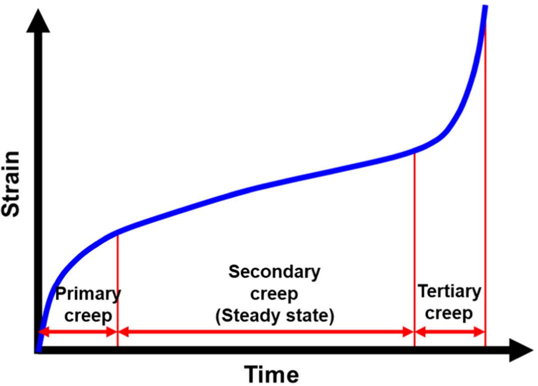

Fig. 2. Schematic of time-dependent creep strain.

aluminum wires inside the structure are also of concern in the failure zone during power cycling [24]. As such, power cycling stands as a crucial reliability test for power modules and it is regarded as the most critical aging test to evaluate the reliability of power components [25]. The temperature profile corresponding to the actual operating time of the module has a great impact on the life of the power module [26]. The effects of junction temperature swing (T_j) and mean junction temperature (T_{jm}) are critical factors in PCT for the reliability of power modules [27], [28], [29]. The power cycling test can be categorized into second-level and minute-level tests based on the turn-ON time of the chip. Common failure locations in second-level power cycling tests often occur at wire bonding spots. Conversely, minute-level power cycling tests commonly reveal failures at the chip solder [30]. However, the residual stress present in the power module after the manufacturing process can cause the solder material to accumulate plastic strain before undergoing the power cycling test. It is noticed that the prewarped design of substrates during processes is beneficial to diminish the warpage of a whole module [31]. Therefore, in addition to discussing the power cycling test of the power module, this research will delve into the effect of process residual stress on different failure locations. Simultaneously, the finite element model in this study will incorporate a plastic case and molding material to precisely analyze the mechanical behavior of the solder layer.

II. ANAND VISCOPLASTIC MODEL

As a material is subjected to a constant load below its yield strength, the phenomenon of permanent deformation increasing with time is known as creep. In the case of ductile materials such as metals, especially when maintained at a temperature exceeding one-third of their melting point for extended periods, the influence of creep behavior becomes more pronounced. As illustrated in Fig. 2, material creep behavior can be categorized into three stages: 1) primary creep, 2) secondary creep, and 3) tertiary creep. During primary creep, when the material is under a constant stress load, the strain rate diminishes over time due to strain hardening. The subsequent stage is secondary creep, characterized by a stable strain rate that represents a significant portion of the inelastic strain in the creep process. Consequently, many creep constitutive equations are explored and discussed

in this stage to model steady-state creep. The final stage is tertiary creep, where, owing to substantial damage from extensive deformation, necking of the material occurs. This results in a drastic reduction in the cross-sectional area, leading to significant stress concentration. Consequently, the stress can no longer be considered a constant value. Moreover, the strain rate sharply increases over time until the material ultimately fails.

The operational temperature of automotive power modules typically exceeds one-third of the melting point temperature of the solder material. Under these conditions, the impact of the creep phenomenon on mechanical performance becomes notably significant. In reliability tests for high-power modules, such as thermal cycling and power cycling, the solder material is particularly susceptible to damage from the creep effect. Therefore, the creep behavior of solder materials should be accounted for. Common creep theories include the Garofalo-Arrhenius creep theory and the Anand viscoplastic model. Given that the Anand model comprehensively describes both plastic behavior and creep phenomena, this study employs the Anand model to investigate the failure behavior of the solder material [32], [33].

Garofalo [32] first proposed the Anand viscoplastic model. For viscoplastic materials with isotropic and small elastic deformation, a constitutive equation that considers time and temperature is established. The constitutive equations of the Anand model are detailed in

$$\dot{\varepsilon} = A\exp\left(\frac{-Q}{RT}\right)\left[\sinh\left(\xi\frac{\sigma}{s}\right)\right]^{\frac{1}{m}} \tag{1}$$

where $\dot{\varepsilon}$ is the strain rate, A is the preexponential factor, Q is the activation energy, R is the gas constant, T is the absolute temperature, ξ is the stress multiplier, σ is the stress, s is the deformation resistance, and m is the strain rate sensitivity

$$\dot{s} = \left\{h_0\left|\left(1-\frac{s}{s^*}\right)\right|^a \text{sign}\left(1-\frac{s}{s^*}\right)\right\}\dot{\varepsilon}_I \tag{2}$$

where $\dot{s}$ is the deformation resistance to time differential, h_0 represents the strain hardening and dynamic recovery of the material, s^* is the saturation value of deformation resistance, a is the strain hardening and softening sensitivity, $\dot{\varepsilon}_I$is the inelastic strain rate

$$s^* = \tilde{s}\left[\frac{\dot{\varepsilon}_I}{A}\exp\left(\frac{Q}{R\theta}\right)\right]^n \tag{3}$$

where $\tilde{s}$ is the saturation coefficient of deformation resistance. In contrast to the Garofalo-Arrhenius model, the Anand viscoplastic equation provides a more detailed description of the internal structure of the material. In the Anand viscoplastic model, the deformation resistance (s) has its physical meaning as the resistance against plastic flow. The model assumes that its resistance is isotropic. Describes the plastic deformation state of the structure when the internal structure of the material is subjected to load. If the s value increases, the strain rate would decrease, indicating internal hardening of the material. This caused the material to undergo strain hardening after plastic deformation. Then, the material has more ability to resist deformation, and the effect of creep would decrease accordingly. If the material

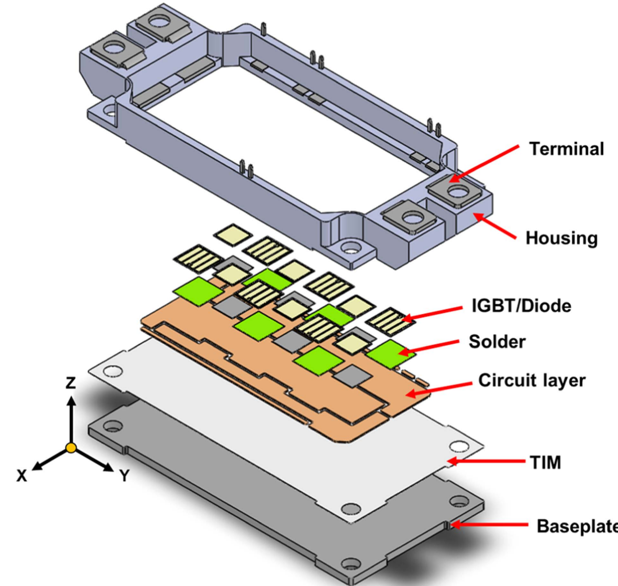

Fig. 3. Exploded assembly diagram of power module with IMS substrate.

is under fixed temperature and strain rate conditions, there will be a fixed relationship between s and σ [34]. Moreover, Q is activation energy. If the Q value becomes larger, it means that the energy barrier for creep deformation of the material is larger and it is more difficult to deform. If the ambient temperature is one-half greater than the melting point of the material, it can be simplified to a fixed value. Because the working environment temperature of the power module is higher than half the melting point temperature of the solder layer for a long time. Thus, Q can be simplified to a fixed value [34]. A, Q, $\tilde{s}$, h_0, m,ξ, a, n, s_0 are all parameter results of curve fitting. Therefore, the Anand viscoplastic model not only describe time-related behavior, but also describe the plastic deformation properties of nonlinear materials to more accurately analyze the mechanical response of materials.

III. Simulation Model of IMS Power Module

This study examines the IMS power module rated at 1200 V/600 A, with the stack structure illustrated in Fig. 3. The sequential arrangement from top to bottom includes the terminals, plastic housing, IGBT power chip, diode, solder material, circuit layer, TIM material, and baseplate. Following assembly, epoxy resin is injected into the plastic case to safeguard the power chip, wire bonding, and copper circuit layer of the power module.

The finite element model of the power module with an IMS substrate is depicted in Fig. 4. To precisely analyze the warping behavior arising from the manufacturing process, the finite element model is constructed based on the actual size of the vehicle. The geometric dimensions of each material are outlined in Table II. The dimensions of the IGBT power chip are 11.9 mm in length and width, with a thickness of 140 μm. The diode chip measures 9.3 mm in both length and width, also with a thickness of 140 μm. The solder layer for the IGBT power chip

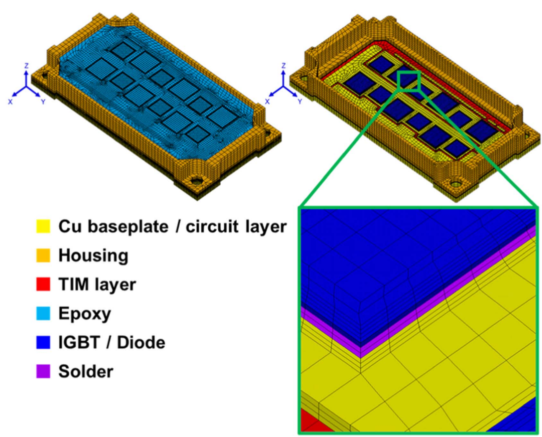

Fig. 4. Finite element model of power module with IMS substrate.

TABLE II
GEOMETRICAL SIZE OF POWER MODULE WITH IMS SUBSTRATE

	Length (mm)	Width (mm)	Thickness
Baseplate	122.3	62	3 mm
TIM layer	122.3	62	150 μm
Circuit layer	97	44.5	500 μm
Chip solder	12.2	12.2	100 μm
Diode solder	9.6	9.6	100 μm
Chip	11.9	11.9	140 μm
Diode	9.3	9.3	140 μm
Housing	122.3	62	13 mm
Epoxy	100	50	9.67 mm

is 12.2 mm long and wide, with a thickness of 100 μm. The solder layer for the diode chip is 9.6 mm long and wide, with a thickness of 100 μm. The copper baseplate has dimensions of 122.3 mm in length, 62 mm in width, and 3 mm in thickness. It features holes with a diameter of 6.6 mm at the four corners to aid in positioning during assembly with the plastic case. The TIM material, responsible for bonding the copper circuit layer to the copper baseplate, shares the same length and width as the copper baseplate, with a thickness of 15 μm. The copper circuit layer measures 97 mm in length, 44.5 mm in width, and 500 μm in thickness. Additionally, it incorporates an etched circuit design to control the conductivity of the chip. The plastic case has dimensions of 122.3 mm in length, 62 mm in width, and 13 mm in thickness. Similar to the copper baseplate, it features holes at the four corners for positioning and has internal space, measuring 100 mm in length and 50 mm in width, filled with epoxy resin. The epoxy resin, with a thickness of approximately 9.7 mm, serves to cover copper circuits, chips, and wires within the plastic case.

On the technical side, the finite element model comprises a total of 425 694 elements, utilizing Solid185 and Solid70 element types for simulation analysis. Solid185, a three-dimensional (3-D) element with eight nodes and three degrees of freedom per node, is employed for the establishment of the 3-D finite element model and solid mechanics analysis. Solid70 is utilized for thermal analysis in the 3-D finite element model.

Table III presents the material coefficients employed in the simulation analysis of the power module featuring an IMS substrate. The table outlines crucial mechanical properties for

TABLE III
MATERIAL PROPERTIES OF POWER MODULE SIMULATION WITH IMS SUBSTRATE

<table>
<tr><th></th><th colspan="2">Young's modulus (GPa)</th><th>Yielding strength (MPa)</th><th colspan="2">CTE (ppm/K)</th><th>Poisson's ratio</th></tr>
<tr><td>Baseplate (Copper)</td><td colspan="2">118</td><td>173</td><td colspan="2">17.7</td><td>0.35</td></tr>
<tr><td rowspan="2">TIM layer (Model: Nipponrika H10)</td><td colspan="2" rowspan="2">14.4</td><td rowspan="2">N/A</td><td><200 °C</td><td>>200 °C</td><td rowspan="2">0.24</td></tr>
<tr><td>12</td><td>49</td></tr>
<tr><td>Circuit layer (Copper)</td><td colspan="2">118</td><td>173</td><td colspan="2">17.7</td><td>0.35</td></tr>
<tr><td rowspan="6">Solder (SAC305)</td><td>-55 °C</td><td>17.71</td><td rowspan="6">N/A</td><td colspan="2" rowspan="6">22.5</td><td rowspan="6">0.4</td></tr>
<tr><td>-25 °C</td><td>13.26</td></tr>
<tr><td>25 °C</td><td>11.65</td></tr>
<tr><td>75 °C</td><td>8.09</td></tr>
<tr><td>125 °C</td><td>5.16</td></tr>
<tr><td>180 °C</td><td>2.62</td></tr>
<tr><td>Chip (Silicon)</td><td colspan="2">169.5</td><td>N/A</td><td colspan="2">3</td><td>0.28</td></tr>
<tr><td rowspan="3">Plastic case</td><td colspan="2" rowspan="3">20</td><td rowspan="3">N/A</td><td><120 °C</td><td>>120 °C</td><td rowspan="3">0.4</td></tr>
<tr><td>XY:18</td><td>XY:18</td></tr>
<tr><td>Z:27</td><td>Z:57</td></tr>
<tr><td>Epoxy</td><td colspan="2">20</td><td>111</td><td colspan="2">15</td><td>0.4</td></tr>
</table>

each material, encompassing Young's modulus, yield strength, coefficient of thermal expansion, and Poisson's ratio. The baseplate and circuit layer consist of copper. In addition to specifying Young's modulus for linear elasticity, the material accounts for copper's nonlinear properties through yield strength. These nonlinear characteristics capture the prebending behavior of the IMS substrate induced by residual stress from the hot-pressing process. Through the use of the prebending approach with applied displacement boundary conditions, the initial deformed state of copper baseplate is beneficial to improve the accuracy of warpage estimation. On the other hand, the TIM material utilized is a blend of polymer materials and ceramic particles. When subjected to temperatures exceeding 200 °C, the TIM material experiences a shift in its coefficient of thermal expansion, transitioning from 12 ppm/K to 49 ppm/K. With regard to the CTE characteristics of TIM and plastic case at different temperatures, it is almost a constant in the solid state. By contrast, when the polymer exceeds its glass transition temperature (T_g), the CTE would vary significantly because the internal state of the material changes from a harder glassy state to a softer rubbery state. As for epoxy, both the process and the power cycling conditions do not exceed 161 °C of T_g. Accordingly, the above-mentioned effect can be ignored in this study.

The study mainly investigates the coupling impact of manufacturing processes and power cycling test on the reliability of solder layer. The description of mechanical behavior by nonlinear material characteristics of the solder layer needs to be carefully taken into account. Given that the solder layer is a critical failure site in power modules, meticulous consideration of its mechanical properties is imperative. This study employs the SAC 305 tin-silver-copper solder layer. In addition to addressing the temperature-dependent linear elastic Young's modulus, the research applies the Anand creep theory to elucidate the creep phenomenon and plastic behavior of solder materials under varying temperatures. The Anand creep coefficient of SAC305 is detailed in Table IV [34]. The Anand model parameters of

TABLE IV
ANAND CREEP COEFFICIENT OF SAC305 [34]

A (s^{-1})	Q/R (K^{-1})	$\tilde{s}$ (MPa)	h_0 (MPa)	m
3501	9320	30.2	180,000	0.25
ξ	a	n	s_0 (MPa)	
4	1.78	0.01	21	

TABLE V
MATERIAL PROPERTY OF POWER MODULE THERMAL ANALYSIS

	Conductivity (W/mK)	Density (kg/m^3)	Specific heat (J/kg*K)
Baseplate (Copper)	380	8940	385
TIM layer	12	2165	840
Circuit layer (Copper)	380	8940	385
Solder (SAC305)	50	7294	250
Chip (Silicon)	100	2328	804
Plastic case	1	1960	740
Epoxy	1	1950	740

SAC305 used in this study are referred to the literature [34]. Through the 15 sets of tensile-loading experimental conditions composed of three different strain rates and five different temperatures, the above-mentioned parameters are acquired by these extractive stress-strain curves when the curve fitting approach is introduced. The IGBT chip and the diode chip are crafted from silicon-based materials, providing the requisite electrical properties for converting electrical energy into mechanical work. As silicon-based materials are inherently brittle, their plastic behavior is considered negligible. The plastic case is constructed from composite plastic with glass fiber material. Consequently, the CTE of the plastic case exhibits directional variation. In the horizontal direction (*xy* plane), the CTE is 18 ppm/K, whereas in the vertical direction (*z*-direction), it is 27 ppm/K. The presence of glass fiber reinforcement further influences the coefficient of thermal expansion along the vertical direction. Beyond the glass transition temperature of 120 °C, the coefficient of thermal expansion in the vertical direction increases from 27 ppm/K to 57 ppm/K, whereas the thermal expansion coefficient in the horizontal direction remains steady at 18 ppm/K. Epoxy serves as the molding material for the power module. During the curing process, epoxy undergoes chemical shrinkage. Notably, chemical shrinkage can induce structural deformation and warpage in power modules. To quantify this property, the study employs differential scanning calorimetry and pressure–volume–temperature–cure methods. The results indicate that the epoxy undergoes a chemical shrinkage of 0.192%.

Table V compiles the thermal material properties of each component in the power module under investigation. It is noticed that all the thermal material properties considered in this model are assumed to be temperature-independent because the temperature effect is slight in the testing range from 25 °C to 125 °C. The conductivity of the plastic case and molding material is denoted as 1, significantly lower than the other materials. This minimal conductivity poses challenges in effective heat dissipation for these two components. In contrast, the copper material boasts a high conductivity of 380 W/mK, surpassing that of other materials in the structure. This implies that the majority of heat

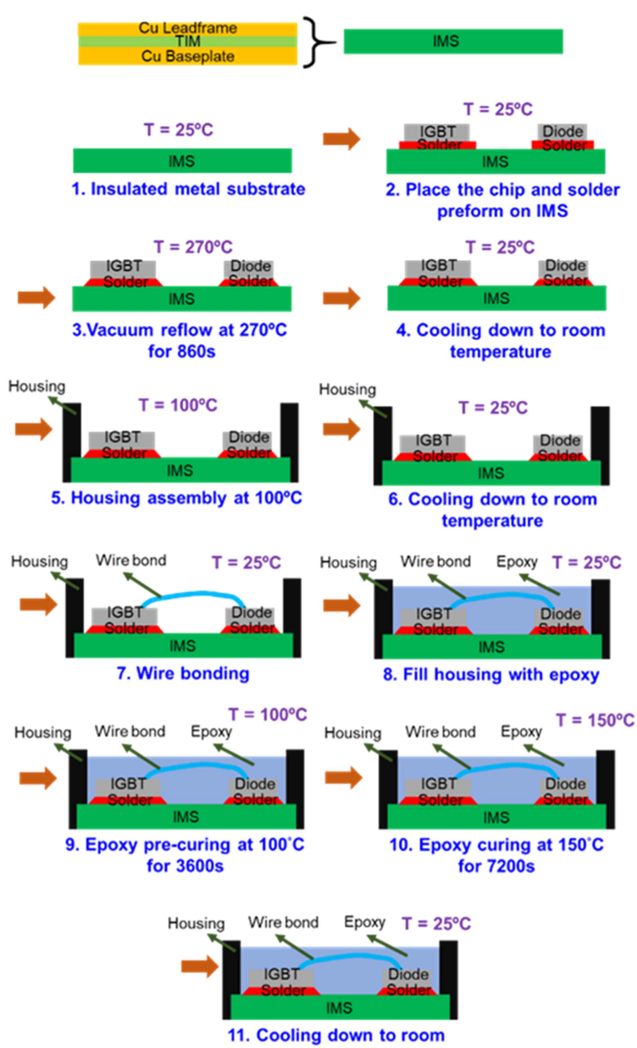

Fig. 5. Main manufacturing process of IMS power module.

generated by the IGBT chip module during power cycling can only be efficiently transferred to the cooling system through the copper metal. Consequently, the primary heat dissipation method for the power module heavily relies on the inherent heat dissipation capabilities of the IMS substrate. Despite the TIM layer exhibiting a low conductivity of 12 W/mK, its thin layer thickness minimizes its impact on the overall conductivity of the substrate. Overall, the IMS substrate demonstrates outstanding heat dissipation capability.

IV. MANUFACTURING PROCESS AND SIMULATION VERIFICATION

The objectives of this study are to investigate the impact of the manufacturing process and the coupling effects of power cycles on the solder layer in power modules, and to analyze the significance of finite element analysis (FEA) of the manufacturing process in relation to the power cycle reliability of power modules. Fig. 5 illustrates a flowchart outlining the manufacturing process steps for a power module with an IMS substrate.

TABLE VI
PROCESS WARPAGE EXPERIMENT RESULTS OF POWER MODULE WITH IMS SUBSTRATE

Warpage (unit: μm)	Pre-bending	Reflow	Epoxy curing
Sample 1	38	−59	
Sample 2	43	−40	60
Sample 3	47	−59	76
Sample 4	44	−49	
Average	43	−49.3	68
Standard deviation	3.24	6.72	8

The process involves chip reflow, plastic case assembly, wire bonding, and epoxy curing. Initially, the chip and solder are placed on an IMS substrate, and a high-temperature vacuum reflow at 270 °C is employed to melt the solder. Once the chip is bonded to the IMS substrate and cooled to room temperature, the chip reflow process is considered complete. Subsequently, the plastic case is assembled onto the IMS substrate, and the two are joined at a high temperature of 100 °C. After cooling to room temperature, wire bonding is conducted, connecting the signal and electrical properties between the power chip, diodes, and terminals. Finally, colloidal epoxy is poured into the plastic housing, covering the chip, wire bonding, and the copper circuit layer on the IMS substrate. The mixture is heated to 100 °C for prebaking for one hour to enhance the mechanical properties of the epoxy as it transitions from liquid to a solid state. The temperature is then raised to 150 °C for two hours to achieve complete curing of the epoxy. The cured epoxy, with increased hardness, acts as a protective layer to prevent damage to the circuit layer, chip, and wire from mechanical or environmental impacts. Upon cooling to room temperature, the manufacturing process for the power module with an IMS substrate is considered complete.

A. Manufacturing Process of Experiment

Table VI presents the results of the process warpage experiment measured by the color confocal measurement module for the power module with an IMS substrate. The experiment involved four groups of samples to measure warpage during the prebending, chip reflow, and epoxy curing processes. The average and standard deviation of the warpage at each process step were calculated. The molding material used in Sample 1 and Sample 4 differed from the epoxy discussed in the present study; therefore, the warpage during epoxy curing for these two samples is not considered in this analysis. The results indicate an average warpage of 43 μm and a standard deviation of 3.24 μm during the prebending process. Additionally, an average warpage of -49.3 μm and a standard deviation of 6.72 μm were observed during the reflow process. Furthermore, the cured epoxy resin exhibited an average warpage of 70.2 μm with a standard deviation of 8 μm. Fig. 6 illustrates the contour of warpage measured at each manufacturing process step.

B. Simulation Verification of Warpage

The boundary conditions employed in the simulation analysis to examine the warpage effect of the power module process in this study are depicted in Fig. 7. To prevent rigid body displacement, point A on the baseplate is selected, and the displacements in the three orthogonal directions are set to zero. Simultaneously, to prevent rigid body rotation along the X-axis and Z-axis, the X- and Z-direction displacements of another point B on the baseplate are constrained to zero. The Z-direction displacement of the third point C is set to zero to prevent rigid body rotation along the Y-axis. These boundary conditions not only prevent the rigid body displacement and rotation of the finite element model but also allow the model to freely expand and contract

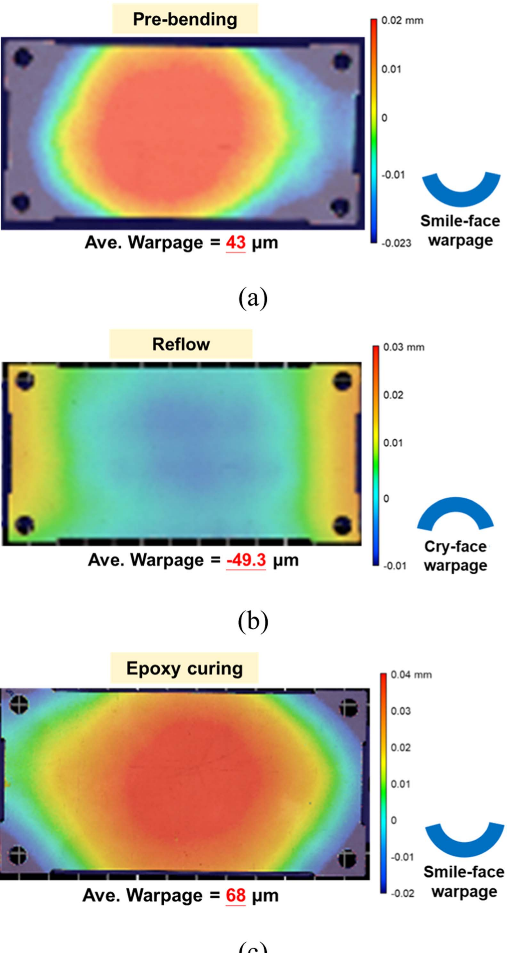

Fig. 6. Warpage contour of each manufacturing process. (a) Prebending. (b) Reflow. (c) Epoxy curing.

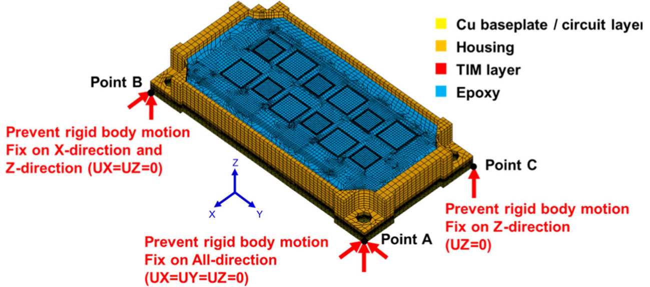

Fig. 7. Boundary conditions of IMS substrate power module.

with temperature changes. Consequently, this setup enables the estimation of the warping behavior of the power module resulting from the coefficient of thermal expansion mismatch during the manufacturing.

The experimental measurements indicate that the copper circuit layer, TIM material, and copper baseplate integrated into an IMS substrate exhibit a warpage of 43 μm. To enhance the accuracy of warpage estimation in the manufacturing process simulation of the power module, the IMS substrate underwent prebending by 43 μm. This prebending involved inducing residual stress in the IMS substrate through displacement boundary conditions with a spherical radius, resulting in a 43 μm warpage. Before performing the power module process simulation, the IMS substrate underwent prebending by 43 μm to improve the accuracy of warpage estimation in the manufacturing process simulation. First, residual stress of the IMS substrate was induced by the displacement boundary of the spherical radius, affecting the IMS substrate to have a 43 μm warpage. Second, the IMS substrate was heated to 270 °C to accurately analyze the mechanical response during the reflow process. Then, it was cooled down to 217 °C, and the elements of chips and solders were set to "Birth" to simulate the influence of the mechanical behavior when the solder material changes from liquid to solid below 217 °C and then lowers to room temperature. Third, the element of the plastic shell was set to "Birth" at room temperature. Next, the temperature was raised to 100 °C and then cooled to room temperature to simulate the plastic case assembly process. Finally, the finite element model was heated to 150 °C, and the element of the epoxy was set to "Birth" and then cooled to room temperature. The epoxy cannot respond mechanically to the power module until the epoxy was heated to the curing temperature because the curing temperature of the epoxy in the present study was 150 °C. Therefore, the process of preoven at 100 °C was not considered in the simulation step of epoxy curing. As epoxy has a chemical shrinkage of 0.192%, this study used the volume shrinkage caused by temperature changes to simulate the effect of chemical shrinkage on warpage behavior. The manufacturing simulation results of the power module with IMS substrate are shown in Fig. 8. A positive value of warpage was smile-face warpage type, and a negative value of warpage was cry-face warpage type. Fig. 8(a) shows the simulation result of the prebending process of the IMS substrate. Utilizing the prebending simulation method of the spherical boundary, the IMS substrate exhibited a prewarpage of 43 μm before the process, accounting for the influence of the initial stress inside the IMS substrate at this time. Fig. 8(b) shows the simulation result of the reflow process. When the IMS substrate heated up to 250 °C, the CTE of TIM material changed to 49 ppm/K. At this time, the thermal expansion caused by the TIM material was more than the copper baseplate, causing the warpage to change from smile-face to cry-face. The mechanical behavior transition from cry-face to smile-face was limited because the thermal stress and thermal strain during cooling were concentrated on the chip and the solder. Therefore, the reflow process was cry-face warpage, with a warpage value of -43 μm. Fig. 8(c) shows the warpage simulation result of the epoxy curing process. The main reason for the warpage direction from cry-face to smile-face was caused by the chemical shrinkage of epoxy. When epoxy was cured at high temperature, the power module owned a smile-face of approximately 120 μm due to chemical shrinkage. Subsequently, as the epoxy transitioned from a liquid to a solid state, it withstood the thermal shrinkage of the power module when it cooled to room temperature. The epoxy curing resulted in smile-face warpage with a value of 70.2 μm.

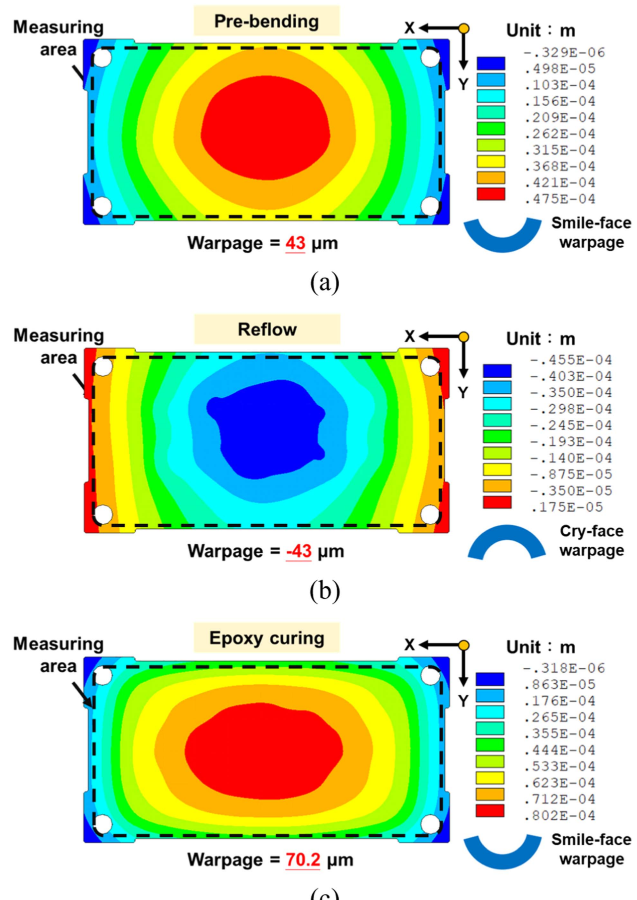

Fig. 8. Simulation results of process warpage of IMS substrate power module. (a) Prebending. (b) Reflow. (c) Epoxy curing.

Fig. 9 depicts a comparison and validation between the FEA simulation results and experimental data for the manufacturing process. The warpage prior to the assembly process (prebending), as simulated by the FEA, aligns with the average value of the experimental results (43 μm). This indicates a consistency between the simulation estimation and the experimental measurements at this stage. Furthermore, the warpage errors during reflow and epoxy curing are 12.78% and 3.23%, respectively. Despite the warpage error during reflow surpassing 10%, the simulation result remains within the standard deviation range of 6.72 μm. It should be noticed that the foregoing reference listed in Table VI is calculated from the experimental results of four samples after the reflow process. Therefore, the FEA simulation results for the manufacturing process fall below the standard deviation range observed in the experimental data. The deviation occurred in the stage of reflow process could be attributed to that time-dependent mechanical behavior during the

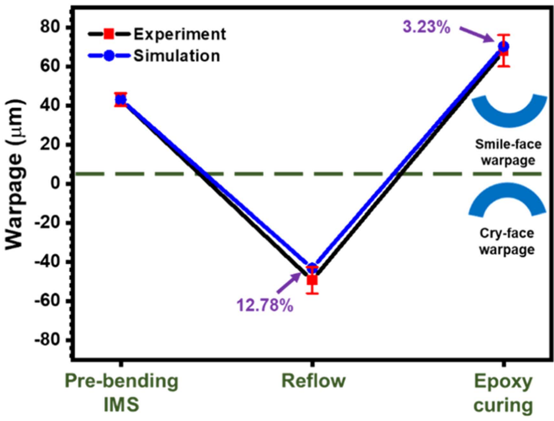

Fig. 9. Line graph of process warpage experiment and finite element simulation results.

TABLE VII
EXPERIMENTAL CONDITIONS OF POWER CYCLING TEST

Current (A)	384
Voltage (V)	1.645
ΔT_j	100
t_{on} (min)	2
t_{off} (min)	2

complete heating and cooling curve of the actual reflow process is difficult to represented by the proposed simulation approach. In this study, that the elements belong to chip and solder is activated to "Birth" during reflow at 217 °C, which indicates that their mechanical response at this moment are directly revealed. The foregoing supposition is slightly dissimilar as compared with the actual reflow condition. Accordingly, a difference in the results of warpage magnitudes between simulation and the experiment is effectuated. In addition, the potential cause for the difference generated at the curing period of epoxy resin might result from the viscoelastic characteristics of epoxy and its mechanical impact prior to the degree of cure at gel point are not taken into the simulated analysis account.

V. Power Cycling Test and Simulation Verification

The main reliability tests for power modules encompass the power cycling test, thermal cycling test, and aging test. Among these, the power cycling test holds particular significance due to its proximity to the actual operation of the power module. Therefore, it stands as one of the most crucial tests for power modules. This study discusses the power cycling reliability test of power modules with IMS substrate, concurrently exploring the impact of process residual stress on the power cycle simulation results.

A. Experiment Result of Power Cycling Test

In this study, the MicRed Industrial Power Tester 1500 A conducted the power cycling test, adhering to the specifications of the Automotive Electronics Council. As per the specifications, the experimental conditions entail a fixed junction temperature amplitude ΔTj. Table VII outlines the specifics of the power cycling test conditions. In general, the power cycling tests can be divided into the second-level cycling period and the minute-level cycling period. For the second-level cycling period, the heat is mostly concentrated in the chip area due to the short switching time. In the meanwhile, the reliability performance of the aluminum wiring contact area is mainly observed. By contrast, the heat in the minute-level cycling period will be transferred to the IMS substrate due to the long switching time. The assembly reliability of solder layer has, therefore, become the critical concern needed to examine. In this research, the reliability performance of chip solder layer and IMS within the proposed module architecture is the main analysis target. Accordingly, a swing period of 2 min is set for experimental testing. To scrutinize failure behaviors, such as delamination or cracking of the solder layer, a minute-level power cycling test condition is applied, with each cycle for turn-ON and turn-OFF lasting approximately 2 min. The test condition for ΔTj is set at 100 °C. To elevate the junction temperature from 25 °C to 125 °C, a current of 384 amperes is applied to the IGBT chip, accompanied by a working voltage of 1.645 v for the IGBT chip.

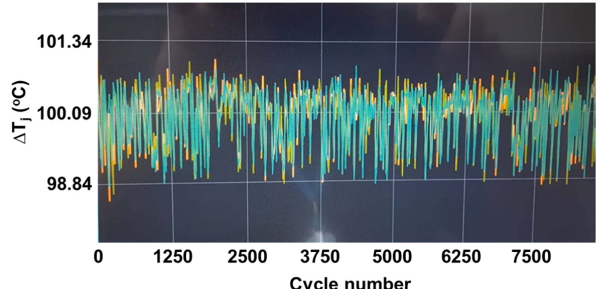

Fig. 10. ΔT_j for each cycle of the power module under the power cycle.

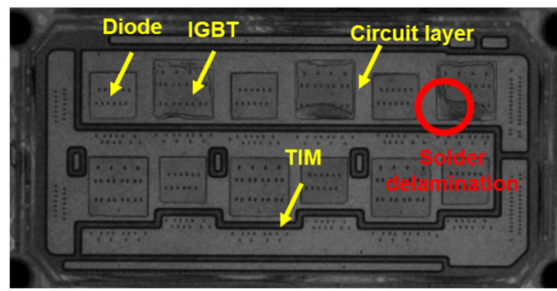

Fig. 11. SAM of IMS power module after 20 000 power cycles.

Fig. 10 shows the ΔT_j of the power module throughout the power cycle. The ΔT_j of each cycle is approximately 100 °C, which meets the experimental conditions. Fig. 11 shows the experimental outcomes following 20 000 power cycles for a power module with IMS substrate. The results of the experiment were scanned for soldering by a scanning acoustic microscope (SAM). The findings reveal delamination in all solder connections of the IGBT chip, with a particularly pronounced instance of severe delamination observed on the right chip.

B. Simulation Result of Power Cycling Test

Power cycle simulation serves as a method for analyzing the interplay of multiple physical fields, including electricity,

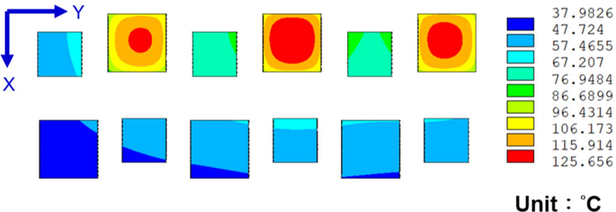

Fig. 12. Temperature distribution of the chip of the power module when it is turned ON.

thermal, and structural aspects. In this study, a FEA of power cycling is undertaken utilizing an indirect coupling approach. The process commences with thermal analysis, and the outcomes of this analysis are employed as the boundary conditions for subsequent structural mechanics analysis, elucidating the mechanical response of the power module under the power cycling load.

The power loss (P) of the power chip during the power cycling load is determined by multiplying the conduction current (I) and the operating voltage (V), yielding a total power loss of 631.7 W. Given the parallel connection of the three high-side chips in the power module, it is assumed that the conduction current is evenly distributed among them during operation. Consequently, the power loss for each chip is approximately 210.6 W, as indicated in the FEA simulation. To manage the heat generated by power loss and ensure cooling to room temperature within the turn-OFF time, a cooling system is implemented. The study employs an equivalent heat convection coefficient to represent the cooling system's heat dissipation capacity. The equivalent convection coefficient (2930 W/m^{2}K) is calculated based on the structural thermal resistance of the power module, measured using the thermal transient tester. The structural thermal resistance is determined to be 0.055 K/W for the power module with IMS substrate, and 0.045 K/W for the cooling system. During the power cycling test, the power chip experiences a 2-min application of power loss when turned on and a 2-min removal of power loss when turned OFF. This cycle repeats every 4 min. Ten simulation cycles are conducted to analyze the mechanical behavior of the power module under the power cycling test conditions.

The junction temperature distribution during the power cycle of the power module when the chip is turned ON is presented in Fig. 12, whereas the deviation of chip junction temperature over time is depicted in Fig. 13. Within the 2-min turn-ON mode, the junction temperature ascends to 125.7 °C, and upon turning OFF, it rapidly declines to 25.4 °C. The temperature differential between the junction temperature during turn-ON and turn-OFF phases approximates 100 °C. Evidently, the thermal boundary conditions and simulation align with the power cycling test conditions outlined in this study. Given the substantial heat generated from power loss, the IMS substrate effectively dissipates heat around the chip. However, due to the overlapping heat dissipation path from the middle chip to the IMS substrate with the chips on both sides, more heat accumulates at the center than at the sides of the chips. Consequently, a high-temperature area is observed at the middle chip. The mechanical behavior analysis of the power module is conducted under power cycling test conditions based on thermal analysis and boundary conditions, and the findings will be subsequently applied to the structural analysis.

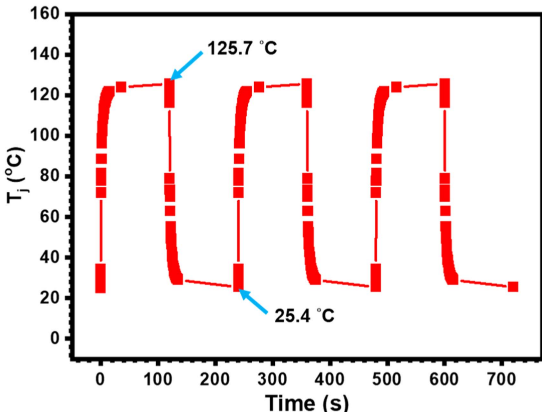

Fig. 13. Relationship of junction temperature and time under power cycling.

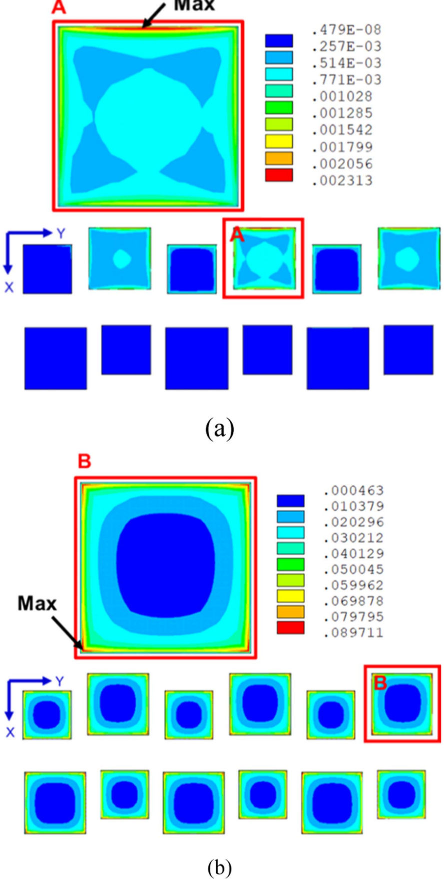

Fig. 14. Equivalent plastic strain distribution of solder layer under 10 power cycles. (a) Without process residual stress. (b) With process residual stress.

Fig. 14(a) shows the finite element simulation results of the power cycling test without considering the process load. In order to ensure that the accumulated plastic strain increment in each subsequent cycle is a stable value that is capable of estimating the power module reliability, the plastic strain increment of multiple cycles is, therefore, calculated through simulation. In this study,

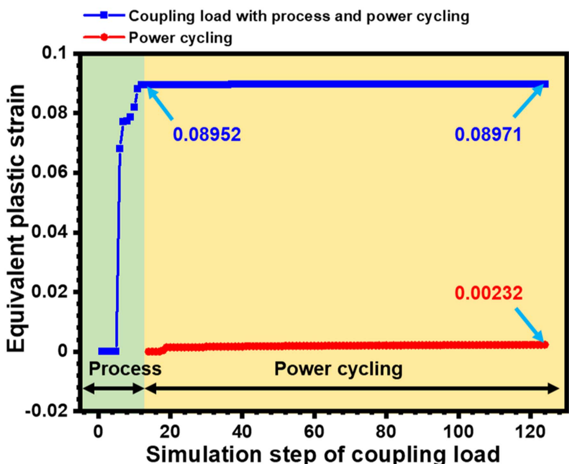

Fig. 15. Comparison diagram of the power module under power cycle load with or without the influence of process residual stress on the solder layer.

the plastic strain increment is stable within 5–8 cycles, so 10 cycles are selected as the analytic results. After undergoing 10 power cycles, the solder layer accumulates an equivalent plastic strain of 0.2313%. The deformation of the solder layer, induced by power loss, is constrained by the plastic case and molding material, leading to the concentration of plastic accumulation at the upper edge of the chip. Conversely, Fig. 14(b) illustrates the finite element simulation results of the power cycling test with the inclusion of the process load. During the power cycles, fluctuations in the temperature of the solder layer and each component during the assembly process cause the accumulation of plastic strain at the corners of the solder layer. The maximum value is observed at the lower-left corner of the right heating chip. Consequently, the equivalent plastic strain of the solder layer concentrates on the edge of the lower-left corner of the heating chip on the right side. This outcome aligns with the SAM diagram presented in Fig. 11, reflecting the results of the 20 000 power cycles. Furthermore, the residual stress from the manufacturing process induces the solder layer to accumulate an equivalent plastic strain of 8.971% after 10 power cycles.

Fig. 15 provides a comparative illustration of the power module under power cycle load, considering or disregarding the influence of process residual stress on the solder layer. The solder layer undergoes a plastic strain of 8.952% after the process, attributed to the thermal expansion mismatch between different materials. This initial strain contributes to the accumulation of the solder layer's plastic strain, reaching 8.971% after 10 power cycles. The incremental change in equivalent plastic strain of the solder layer approximates a fixed value of 1.2×10^{-5}. It is imperative to underscore the significance of considering process residual stress in power cycle FEA or reliability life evaluation of the power module. The mismatch in thermal expansions between materials during the process results in a notable plastic strain in the solder layer. If this residual stress is overlooked, there is a risk of misestimating failure locations in the power module. Therefore, when delving into the power cycle FEA of the power module, the coupling load effect of the assembly process and the power cycle should be considered.

TABLE VIII
FULL FACTORIAL DESIGN PARAMETER COMBINATION OF YOUNG'S MODULUS AND CTE OF EPOXY RESIN

	Level 1	Level 2	Level 3
Factor A Young's modulus (GPa)	10	20	30
Factor B CTE (ppm/K)	10	15	20

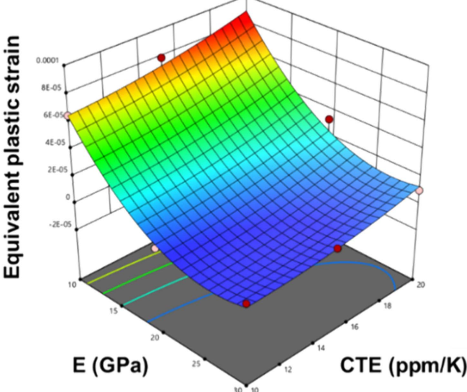

Fig. 16. Response surface distribution of the Young's modulus and CTE of epoxy resin to the equivalent plastic strain of the solder layer.

C. Design of Experiments With Epoxy

Epoxy is used to protect the wire bond, copper circuit layer and solder of the power module. However, an excess of filled epoxy resin can result in warpage issues, impacting the solder layer during the curing process. To assess the influence of the Young's modulus and CTE of epoxy resin on warpage and solder layer behavior, this study employs ANOVA by the Central Composite Design of Response Surface Methodology. The Young's modulus (Factor A) and CTE of epoxy resin are the focal points of analysis, each with three levels. This necessitates a full factorial design with 9 experimental points. The design range for Young's modulus and CTE of epoxy is outlined in Table VIII, spanning from 10 GPa to 30 GPa and 10 ppm/K to 20 ppm/K, respectively. Fig. 16 shows the 3-D response surface distribution depicting the impact of Young's modulus and CTE on the equivalent plastic strain of the solder layer. The ANOVA reveals that the interaction between these factors is not significant. Consequently, when assessing the influence of Young's modulus and CTE on the equivalent plastic strain of the solder layer, analyzing each factor individually is sufficient to determine an optimized parameter combination. Fig. 17 shows the individual effects of the two factors on the equivalent plastic strain of the solder layer. A larger CTE of epoxy exacerbates the CTE mismatch with the chip, intensifying thermal stress on the chip due to power loss. This thermal stress is transferred to the solder layer, amplifying the equivalent plastic strain. Notably, at an epoxy Young's modulus of 30 GPa and CTE of 10 ppm/K, the solder layer inside the structure exhibits the lowest equivalent plastic strain.

On the other hand, this study also explores the impact of the aforementioned factors on the warpage behavior of the power module. Fig. 18 presents the 3-D response surface distribution

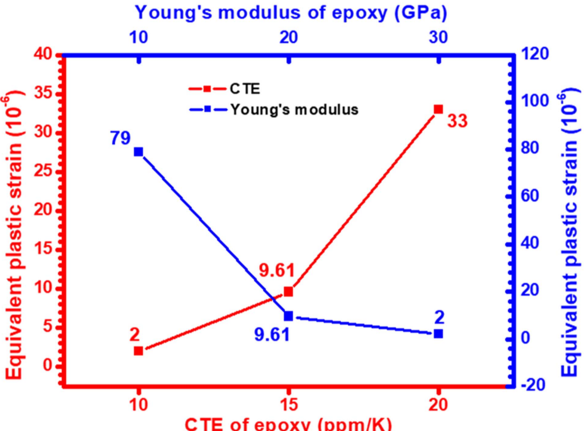

Fig. 17. Individually discuss the effect of Young's modulus and CTE on the solder layer.

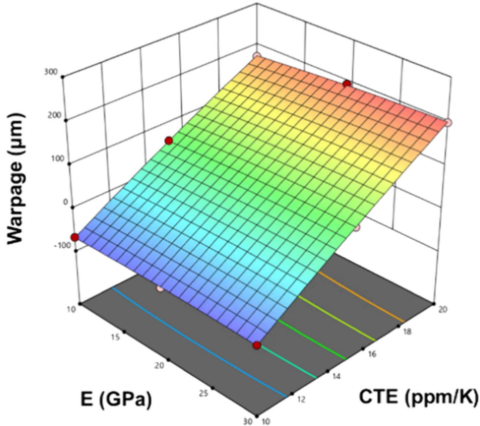

Fig. 18. Response surface distribution of the Young's modulus and CTE of epoxy resin to the warpage of power module.

illustrating the influence of Young's modulus and CTE on the warpage of the power module. Given that Young's modulus and CTE exhibit no interaction effect on the power module's warpage, the subsequent discussion separately addresses the effects of the Young's modulus and the CTE of the epoxy resin, as depicted in Fig. 19. When the epoxy undergoes curing at high temperatures, the power module experiences approximately 150 μm of warpage due to the CTE mismatch of materials and chemical shrinkage. Subsequent cooling to room temperature results in a rebound of the power module's warpage to 70.2 μm, attributed to the release of thermal expansion. Consequently, a larger Young's coefficient of the epoxy resin implies greater resistance to rebound, whereas a smaller Young's coefficient renders the power module more susceptible to spring back and warpage upon cooling. At a CTE of 10 ppm/K, the epoxy's shrinkage after high-temperature curing is less than that of the baseplate (17.7 ppm/K), leading to cry-face warpage in the power module. Conversely, with a CTE of 20 ppm/K, the higher thermal shrinkage of the epoxy compared with the baseplate results in an increased power module warpage of 194.9 μm. The warpage range influenced by CTE is approximately 260 μm, significantly more pronounced than the 12 μm range affected

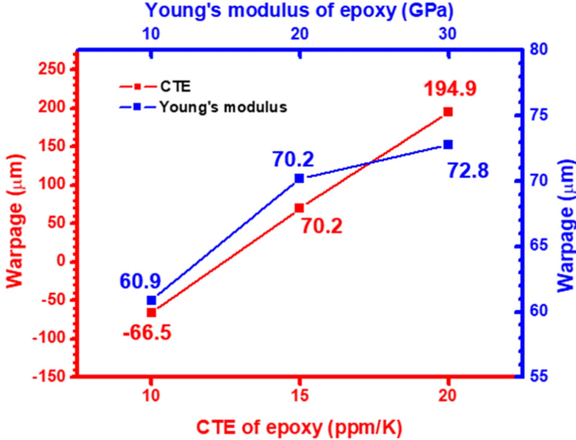

Fig. 19. Individually discuss the effect of Young's modulus and CTE on the warpage of power module.

by Young's modulus. Consequently, the CTE of epoxy exerts a more substantial impact on warpage. For optimal warpage estimation of the power module, the recommended parameter combination is a Young's modulus of 10 GPa and a CTE of 15 ppm/K.

VI. Conclusion

This study successfully establishes a comprehensive process-oriented and power cycle coupling FEA process for power modules with IMS substrates, delving into the impact of residual stress from the manufacturing process on power cycle tests. The finite element model employed accounts for the geometric dimensions of each component in the power module, incorporating the actual shape of the copper circuit layer, the number of chips, and the solder layers. To ensure accurate analysis of power module warpage and the plastic behavior of the solder layer, the study also considers the influence of the plastic case and molding material. In the simulation analysis, the temperature dependence of the solder layer on Young's modulus is considered, and the Anand model is utilized to describe the plastic behavior and creep phenomenon of the solder layer. Recognizing the significance of epoxy resin's chemical shrinkage in influencing power module warpage, the study employs a volume shrinkage simulation method resulting from thermal shrinkage to calculate the effect of equivalent chemical shrinkage on warpage.

To analyze the coupling effect of the process-oriented and power cycling test for power modules with IMS substrates, the study conducts FEA for the process-oriented power module. Comparison with experimental results of the actual assembly process warpage indicates that, despite errors in reflow and epoxy curing steps, the simulation results fall within the standard deviation range of the experimental values. Thus, the proposed simulation method is deemed applicable for power cycle test analysis, considering the residual stress introduced during the manufacturing process. Moreover, the FEA of the power cycling test reveals that the power module's solder layer, without process residual stress, accumulates an equivalent plastic strain of 0.231% after 10 cycles, with a stable increment per cycle

of 0.004%. Conversely, when accounting for the assembly process's residual stress, the solder layer accumulates an equivalent plastic strain of 8.971% after 10 power cycles, showing a stable increment per cycle of 0.0012% lower than that without process stress. Thus, considering process residual stress during the power cycle test simulation is crucial to avoid misjudging the power module's failure behavior and reliability.

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