Enhancing Efficiency in Multireceiver Wireless Charging With Voltage Constraints Using Two-Stage Optimization Algorithm

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***Abstract*—This article proposes an optimization method to maximize the transmission efficiency of multireceiver wireless power transfer (WPT) system while satisfying the load voltage output at the receivers. This method takes the duty cycle of the full bridge inverter at the transmitter and the boost ratio of the dc–dc converters as optimization variables. First, based on the consideration of rectifier circuits and dc–dc converters, a circuit analysis is conducted on the multireceiver WPT system, and the calculation formula for load voltage and system transmission efficiency is obtained. Second, the problem is transformed into an optimization problem with conditional constraints, and a two-stage optimization algorithm combining genetic algorithm and interior point method is designed to ensure the achievement of a stable global optimal solution. Finally, the study determines the duty cycle of the inverter and the receiver voltage boost ratio that satisfy specified constraints when maximizing efficiency. Validation of the output voltage and transmission efficiency across a wide voltage range and under various load conditions is performed on a physical platform.**

***Index Terms*—Efficiency maximization, optimization, voltage constraint, wireless power transfer (WPT).**

I. Introduction

IN RECENT years, with the advancement of research in wireless power transfer (WPT), its portability, safety, and extensive applications have gradually been explored. Currently, WPT system has been applied in medical diagnostic equipment [1], portable equipment [2], electric vehicles [3], and other application scenarios.

In the aforementioned charging scenarios, the primary approach is single-to-single (S-S) WPT, involving a transmitting coil and a receiving coil for power transmission. This charging method is straightforward but has many drawbacks, including limited power, reduced efficiency in the presence of coil misalignment, and restricted compatibility with charging devices. Currently, the focus of related research largely revolves around the investigation of multi-to-single [4], single-to-multi (S-M) [5], and multi-to-multi [6] wireless charging to address the challenges present in S-S WPT system. Among them, multicoil WPT system is a feasible scheme with broader application prospect. The added multicoil design can provide higher charging power and charging efficiency, and can also realize multiload power supply and dynamic wireless charging [7]. However, the increase of the number of coils will lead to more complicated coupling relationship and more power loss on the coils, so a simple and fast scheme is urgently needed to provide stable power distribution for multiple loads and reduce the loss in the system power transmission as much as possible [8]. Therefore, as the core problem of improving system efficiency, the problem of power distribution and efficiency maximization has become the hot research direction of WPT system [9].

Currently, there are several main approaches for power allocation and efficiency maximization in wireless charging systems: solving using mathematical formulas, online efficiency maximization tracking and mutual inductance estimation. The approach of mathematical formulas solving is to calculate the position where the gradient of the system efficiency function with respect to the controllable variables is zero, thus obtain the peak point of efficiency maximization. It is a method fully based on theoretical equivalent mathematical model [10], [11]. On the other hand, the online efficiency maximization tracking approach involves closed-loop control of the output power at receivers and adjusting the current of transmitting coils at transmitters to dynamically track efficiency maximization [12]. The mutual inductance estimation method involves switching the corresponding transmitting coil based on the estimated mutual inductance between the receiving coil and the transmitting coil, which is a simplified engineering method [13], [14].

However, there are still some challenges in related research. First, the approach of solving using mathematical formulas can only handle relatively simple problems, and too complex problems will make it extremely difficult to solve [15]. When existing constraints, the penalty features imported by the constraints may disrupt the original distribution characteristics of the objective function and make the function equation complex and

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the calculation of extreme points difficult. Therefore, most current research focuses on achieving maximum system efficiency under unconstrained conditions, without considering the power output of the load [16], [17]. Second, the mainstream method for calculating load voltage is to convert the receiver rectifier circuit and dc–dc topology circuit into an equivalent resistance and obtain the calculated value through voltage division. This method outputs an ac voltage and requires additional circuits, such as rectifiers and filters, for practical application [18]. In the S-S and S-M wireless charging scenarios, the losses in the rectifier circuit cannot be ignored when the mutual inductance voltage at the receiver is not high [19]. Furthermore, control-based maximum efficiency tracking algorithms need longer search time due to the requirement for constant sampling and adjustment process. It is typically only suitable for dynamically maximizing efficiency in single-variable control problems [20]. When multiple controllable variables are present, the exponential increase in the search space often makes it challenging to track the global optimum solution for multicoil optimization problems. On the other hand, the mutual inductance estimation method only controls the switching state of the coils without adjusting the corresponding duty cycle, thus unable to achieve real maximum efficiency. In addition, most of the research on WPT systems focuses on fixed output scenarios. Limited research has been conducted on power allocation in low-voltage output environments or multiple voltage outputs [21].

To overcome the issues, an optimization method for maximizing system efficiency under constrained output voltage is proposed. This method can ensure the global optimal solution in a relatively short solution time. In addition, the article also considers the voltage drop loss of the rectifier bridge to improve the accuracy of the output voltage and system efficiency calculation. The main contributions of this article are listed as follows.

1) This article incorporates the voltage drop losses in the rectification circuit during circuit analysis for the accuracy of output voltage and efficiency calculations at low voltage.
2) In order to achieve global efficiency optimization within a shorter optimization time while ensuring the constraints of output voltage, this article devises a two-stage optimization method to attain maximum global efficiency.
3) This article incorporates the boost ratio of dc–dc topology as an optimization variables in constructing the optimization formulation for expanding the application scope, which facilitate simpler system control implementation. In addition, constraints on coil current are considered.

The rest of this article is organized as follows. In Section II, the output voltage and system efficiency of the multireceiver WPT system are analyzed based on circuit theory. In Section III, the power allocation and efficiency maximization problem is transformed into an optimization problem, and a two-stage optimization algorithm is introduced. Section IV validates the effectiveness of the optimization algorithm for wide-range output voltage and efficiency optimization through building a physical platform. In addition, comparative analyses of outputs under different load conditions are also conducted in this section. Finally, Section V concludes this article, followed by a prospective discussion on the application potential of the optimization methodology.

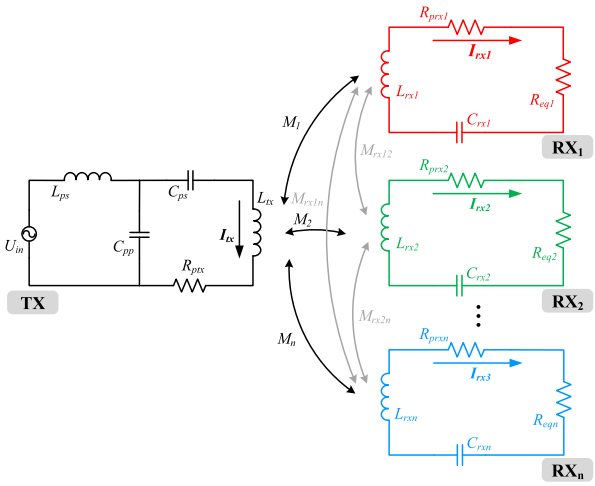

Fig. 1. Basic principle of S-M WPT system.

II. Analysis of Multireceiver WPT System

The fundamental structure of the multireceiver WPT system studied in this article is illustrated in Fig. 1. This system consists of a transmitting coil connected to an LCC topology and multiple receiving coils connected to LC topologies. In the diagram, L_{ps}, C_{ps}, and C_{pp} are compensation parameters for the LCC topology, L_{tx} is the self-inductance of the transmitting coil, and U_{in} is the effective value of the input voltage. M_i represents the mutual inductance between the transmitting coil and the ith receiving coil, L_{rxi} is the self-inductance of the receiving coil, C_{rxi} is the compensation capacitor at the receiver, and R_{eqi} represents the equivalent load at the output. If the circuit operates at the angular frequency of ω, the resonance relationship between inductance and capacitance in the LCC topology should satisfy (1) [22]. The detailed derivation process is described in Appendix

$$\omega^2 = \frac{1}{L_{ps}C_{pp}} = \frac{1}{(L_{tx} - L_{ps})\,C_{ps}}. \tag{1}$$

A. Circuit Analysis

The structure shown in Fig. 1 represents a simplified conceptual circuit. In practical applications, considering various loads and working environments, the power requirements at the load typically involve a specific range of dc input. The high-frequency ac output at receiving coils cannot be directly used for power supply applications.

To address these practical considerations, we add a full-bridge rectifier and buck–boost circuit to guarantee a stable dc output voltage. The equivalent load is altered by adjusting the boost ratio of the buck–boost circuit. Prior to the LCC topology, a dc–ac full-bridge inverter circuit is employed to generate

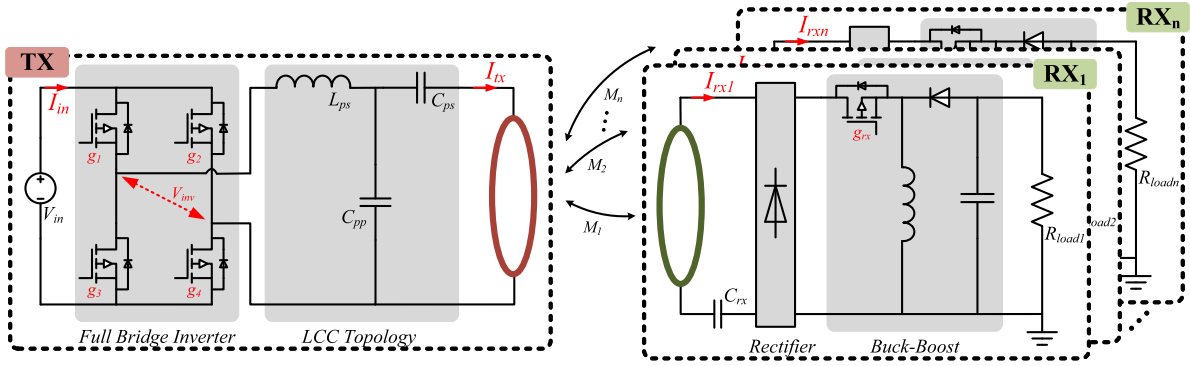

Fig. 2. Circuit structure of the S-M WPT system.

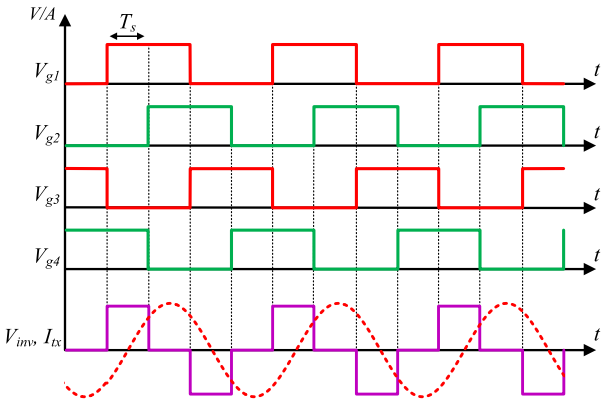

Fig. 3. Phase-shift control principle for full-bridge inverter.

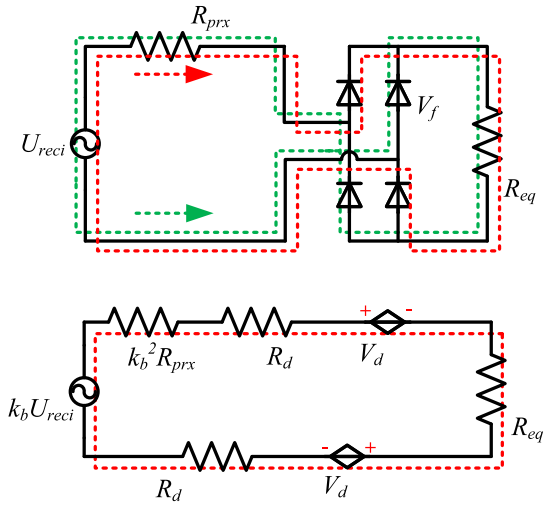

Fig. 4. Half-cycle equivalent of the receiver-side rectifier circuit.

high-frequency ac input. The MOSFETs switch states of the inverter circuit and the buck–boost circuit are controlled by a microcontroller unit (MCU). We adjust the phase difference and duty cycle of the upper and lower bridge MOSFETs of the inverter circuit, respectively, to change the root mean square (rms) value of the input voltage and the boost ratio of the load voltage. The circuit structure is illustrated in Fig. 2.

The rms value of the input voltage before the LCC topology is related to the duty cycle of the inverter output voltage and can be adjusted by varying the phase difference of the MOSFETs in the inverter circuit, as depicted in Fig. 3. Assuming a phase difference T_s between the pulsewidth modulation (PWM) signals g_1 and g_2, where $T_s = D_s \times T$, and T represents the period of the PWM signal, the rms value of the output voltage of the full-bridge inverter can be calculated using the following equation:

$$U_{\text{inv}} = \frac{2\sqrt{2}}{\pi} V_{\text{in}} \sin\left(D_s \pi\right). \tag{2}$$

At this point, combining (1) and (2), the current at the transmitter can be computed, as shown in (3). In instances with restricted output current, neglecting the mutual inductance between the receiving coils is feasible. Consequently, the receiver voltage U_{reci} for the ith receiver can be easily calculated

$$I_{tx} = \frac{U_{\text{inv}}}{\omega L_{px}} = \frac{2\sqrt{2} V_{\text{in}} \sin\left(D_s \pi\right)}{\pi \omega L_{px}} \tag{3}$$

$$U_{\text{reci}} = j\omega M_i I_{tx} = j\frac{2\sqrt{2} M_i V_{\text{in}} \sin\left(D_s \pi\right)}{\pi L_{px}}. \tag{4}$$

Assuming the actual load resistance is R_{load}, for the ith receiver, the ratio of the output voltage to input voltage of the buck–boost circuit is k_{vi}, the equivalent load at the receiver satisfies the following equation:

$$R_{\text{eqi}} = \frac{R_{\text{load}}}{{k_{vi}}^2}. \tag{5}$$

Assuming the rms value of the voltage induced from the transmitter to the ith receiver is U_{reci}, and the voltage drop of the full-bridge rectifier diodes is V_f, considering half of the rectification cycle, as shown in Fig. 4, the output current can be calculated as follows:

$$I_{\text{out}i} = \frac{k_b U_{\text{reci}} - 2V_d}{{k_b}^2 R_{prxi} + 2R_d + 2R_{\text{eqi}}} \tag{6}$$

where $k_b = \pi/2\sqrt{2}$ is the voltage ratio of the dc side to the ac side of the full-bridge rectifier circuit [23]. V_d and R_d represent the equivalent fixed voltage drop and parasitic resistance of the rectifier diodes.

Therefore, the output voltage can be calculated as

$$V_{\text{out}i} = I_{\text{out}i} R_{\text{eqi}} k_{vi} = \frac{k_b U_{\text{reci}} R_{\text{load}} - 2V_d R_{\text{load}}}{k_{vi} k_b{}^2 R_{prxi} + 2k_{vi} R_d + k_{vi} R_{\text{eqi}}}. \tag{7}$$

B. Efficiency Analysis and Loss Estimation

The loss of the full-bridge rectifier circuit can not be neglected under the condition of relatively low voltage at the receiver. Hence, a detailed analysis of diode losses is conducted.

In practical applications, the voltage drop across diodes is not constant and depends on factors, such as the current passing through them and the operating time. When not considering the effects of temperature changes, it is generally approximated as a series connection of a fixed voltage drop diode and a resistor. The rectifier diode used in this paper is $C3D10065$. According to its datasheet, at a temperature of 25 °C, V_d is 0.9075, and R_d is 0.055. Assuming the rms value of the current passing through the rectifier diode is I_f, the diode voltage drop V_f can be calculated as follows:

$$V_f = V_d + I_f \times R_d. \tag{8}$$

Therefore, the power dissipated across the rectifier diode can be calculated as

$$P_{vf\text{loss}} = 2V_f I_f = 2V_d I_f + 2{I_f}^2 R_d. \tag{9}$$

In addition, there are also losses that occur in the resistance of the coils at the transmitter and receivers. The corresponding losses are given by

$$P_{\text{coilloss}} = {I_{tx}}^2 R_{ptx} + \sum_{i=1}^{n} {I_{rxi}}^2 R_{prxi}. \tag{10}$$

Combining the calculation formulas for transmitter current, receiver current, and load current provided in Section II-A, the efficiency estimation formula for the entire circuit structure is established as follows:

$$\eta = \frac{\sum_{i=1}^{n} P_i}{P_{\text{in}}} \approx \frac{\sum_{i=1}^{n} P_i}{P_i + P_{vf\text{loss}} + P_{\text{coilloss}}} = \frac{\sum_{i=1}^{n} |I_{rxi}|^2 R_{\text{eqi}}}{\sum_{i=1}^{n} |I_{rxi}|^2 (R_{\text{eqi}} + R_{prxi}) + |I_{tx}|^2 R_{ptx} + 2V_f |I_f|}. \tag{11}$$

The efficiency estimation formula for the system takes into account the primary losses in the circuit structure, including losses caused by the resistance of the transmitting and receiving coils, as well as diode losses in the rectification bridge.

III. Problem Formulation and Optimization Methodology

A. Problem Formulation

In the theoretical calculations described above, methods for calculating the load voltage output and system efficiency have been provided. Therefore, it is possible to construct a optimization problem based on the aforementioned theory.

This article constrains the output voltage and optimizes efficiency by adjusting the MOSFETs phase shift value D_s at the transmitter inverter and the boost ratio k_{vi} at the receiver buck–boost circuit. Assuming there are n receivers, with constraints on the output voltage $V_{\text{out}i}$ for the ith receiver, a maximum coil current of $I_{\max}$, and considering that the duty cycle does not exceed the maximum PWM period value, with a maximum relative error of ξ for the output voltage, an optimization problem can be established as follows:

$$\max_{D_s, k_{v1}, k_{v2} \ldots, k_{vn}} \eta \quad \text{s.t.} \begin{cases} \frac{|V_{\text{out}i} - V_{\text{out}i}{}^*|}{V_{\text{out}i}{}^*} < \xi, & i = 1, 2 \ldots, n \\ 0 < I_{rxi} < I_{\max}, & i = 1, 2 \ldots, n \\ 0 < I_{tx} < I_{\max}, \\ 0 < D_s < 1 \end{cases} \tag{12}$$

where I_{tx} can be calculated using (3), while I_{rxi} can be replaced with $k_b I_{\text{out}i}$.

In the optimization problem (12), this article treats the phase-shift ratio of the inverter and the boost ratio of the buck–boost circuit as optimization variables, rather than directly optimizing the duty cycle of the buck–boost circuit's MOSFETs. This approach is chosen because the buck–boost module used in this article already has a closed-loop control logic. It employs a proportional-integrated-proprietary (PID) algorithm to control the output voltage at the load, ensuring that the output voltage is a multiple of the input k_v. Furthermore, compared to controlling the duty cycle of the buck–boost, adjusting the boost ratio is more intuitive. In addition, this approach exhibits greater universality. Given the myriad of dc–dc topology structures, when adopting alternative dc–dc configurations, the method employed in this study only requires consideration of how to adjust their voltage boost ratios.

Remark 1: The algorithm proposed in this article can also be applied to more complex scenarios with multiple transmitting coils. When there are m transmitting coils and n receiving coils, the corresponding optimization objective can be redefined as

$$\max_{D_{s1}, D_{s2} \ldots, D_{sm}, k_{v1}, k_{v2}} \eta \quad \text{s.t.} \begin{cases} \frac{|V_{\text{out}i} - V_{\text{out}i}{}^*|}{V_{\text{out}i}{}^*} < \xi, & i = 1, 2 \ldots, n \\ 0 < I_{rxi} < I_{\max}, & i = 1, 2 \ldots, n \\ 0 < I_{txi} < I_{\max}, & i = 1, 2 \ldots, m \\ 0 < D_{si} < 1, & i = 1, 2 \ldots, m. \end{cases} \tag{13}$$

B. Optimization Methodology

Equation (12) represents a constrained single-objective multivariate optimization problem, which generally can be solved using nonheuristic optimization methods. In this article, an interior point penalty function method is employed for solving, where the primary concept involves transforming the constraints into penalty functions while setting barriers at boundary conditions [24]. Assuming x represents the optimization variables, with the system's transmission efficiency as f, and with constraints $g(x) < 0$, a new objective function f_{new} can be defined

as follows:

$$f_{\text{new}} = f + rH(x) = f + r\frac{1}{g(x)} \tag{14}$$

where r is a positive number. As $g(x) \to 0$, the corresponding f_{new} will tend to infinity, ensuring the algorithm iterates within the constraint boundaries.

However, as a nonheuristic optimization technique, the interior point method (IPM) possesses certain limitations. Initially, the first few iterations may move away from the constraint boundary due to the large initial condition of r. Therefore, it is preferable to set the initial point of the IPM to be within the feasible region. Second, given a specific initial point, the optimization proceeds in a certain direction to obtain the nearest local optimum that satisfies the constraints. As a result, the final solution remains fixed and may not necessarily be the global optimum.

To address the drawbacks of the IPM, this article introduces the genetic algorithm (GA) from heuristic methods to optimize the starting point of IPM, forming a two-stage optimization approach. To ensure rapid iteration into the feasible region, the GA adopts the fitness function from (15)

$$f_{\text{new}} = f - P\left[\max\{0, g(x)\}\right]^2 \tag{15}$$

where P represents a large positive penalty term. When $g(x)$ is greater than 0, the penalty term yields a very large value, resulting in a negative value for the final fitness value.

The core concept of the two-stage algorithm involves initially using the GA in the first stage to optimize the fitness function to a value greater than 0, indicating the starting point for the second stage satisfies the constraints. Subsequently, the IPM is employed to further seek the optimal solution. The algorithmic flow is demonstrated in Fig. 5.

The overall framework for optimizing and controlling the WPT system using optimization algorithms for validation is shown in Fig. 6.

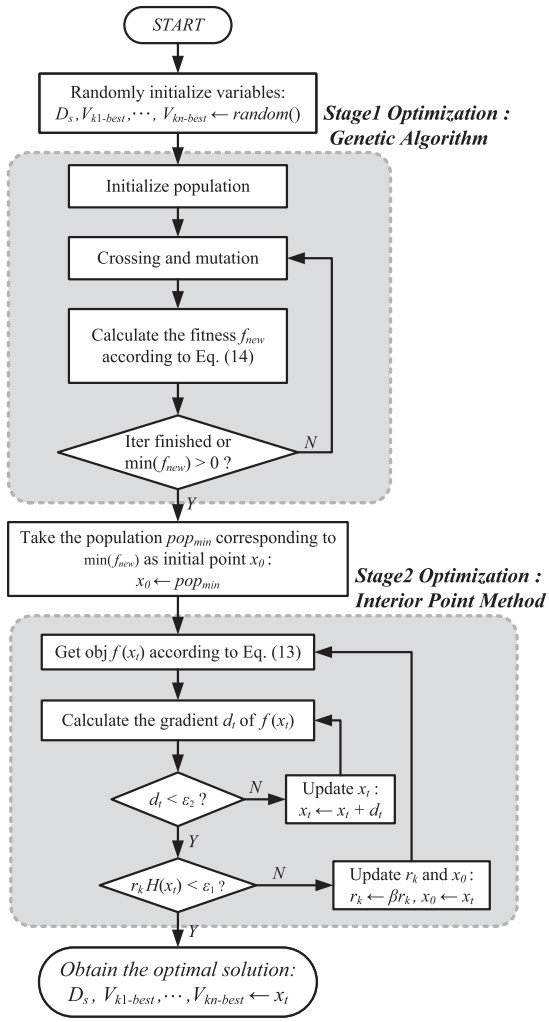

Fig. 5. Flow chart of the GA-IPM algorithm and two stages in the algorithm.

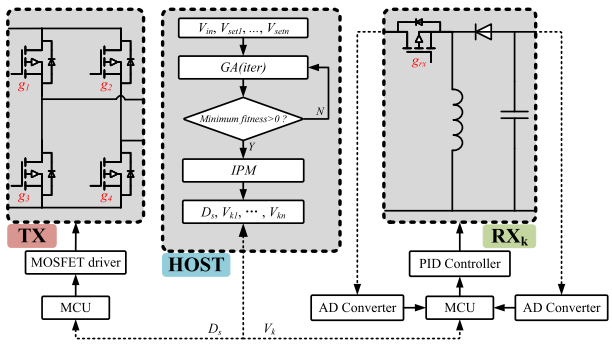

Fig. 6. Overall framework of optimization and control.

IV. Experimental Verification

A. Experiment Platform

In order to validate the theoretical analysis presented in Section II, an experimental platform is set up consisting of one transmitting coil and three receiving coils, as shown in Fig. 7.

The experimental platform consists of four main components: the power supply module, transmitter, transmitter–receiver platform, and receiver. The transmitter module includes a inverter and an LCC topology module, where the inductance and capacitance values in the LCC topology are formed an approximate full compensation with the self-inductance of the transmitting coil. The transmitter–receiver platform is constructed using a double-layer acrylic board to simulate scenarios with multiple receiving coils. The coils are wound around with 400-strand cross-section wires with a diameter of 0.05 mm. The receiving coils are uniformly placed within the circular region corresponding to the transmitting coil. Each coil has different numbers of turns and dimensions, as given in Table I, which determine the mutual inductance between each receiving coil and the transmitting coil. The receiver module includes a capacitor compensation structure, a full-bridge rectifier module, and a buck–boost module. At the end of the buck–boost module, a dc load testing instrument is connected to simulate various load conditions.

The self-inductance of the coils is related to their own radius and the number of turns. The compensation parameters for the

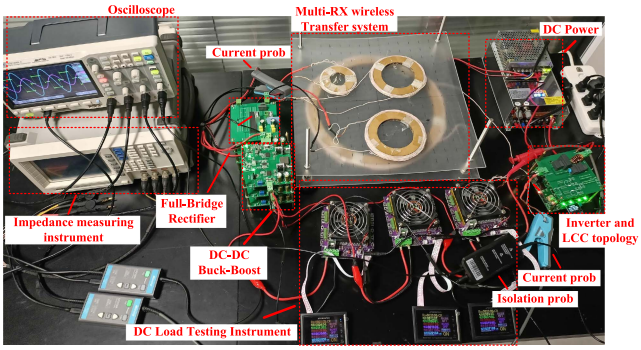

Fig. 7. Experiment platform.

TABLE I
SYSTEM PARAMETERS

	Parameter	Value	Parameter	Value
System	f	$100khz$	V_{in}	$50V$
Coil	R_{ptx} R_{prx2}	$511m\Omega$ $205m\Omega$	R_{prx1} R_{prx3}	$298m\Omega$ $121m\Omega$
	L_{tx} L_{rx2}	$162.75uH$ $61.74uH$	L_{rx1} L_{rx3}	$114.02uH$ $25.07uH$
	r_{tx} r_{rx2}	$34cm$ $12cm$	r_{rx1} r_{rx3}	$12cm$ $8cm$
	N_{tx} N_{rx2}	14 14	N_{rx1} N_{rx3}	20 14
Circuit	L_{ps} C_{pp} C_{rx2}	$22.93uH$ $17.81nF$ $45.09nF$	C_{ps} C_{rx1} C_{rx3}	$101.48nF$ $23.22nF$ $101.1nF$
Mutual	M_1 M_3	$18.26uH$ $4.79uH$	M_2	$13.47uH$
Position	P_{rx1} P_{rx2} P_{rx3}	$(2.5cm, -10cm)$ $(5.1cm, 7.2cm)$ $(-9.4cm, 7.1cm)$		

transmitter LCC topology can be designed using (1), and the compensation circuit for the receiver can be designed using $\omega = 1/\sqrt{L_{rx}C_{rx}}$. The self-inductance and compensation circuit parameters are measured using an *LCR* bridge, and the mutual inductance is calculated by measuring the induced voltage at the receiver while measuring the current at the transmitter according to (4). The system parameters are listed in Table I.

In Table I, f denotes the operating frequency of the system, and the corresponding resonant frequency is $\omega = 2\pi f$. V_{in} is the dc voltage input of the inverter, R represents the coil resistance measured by the *LCR* bridge, L represents the coil self-inductance, r and N represent the winding radius and turns of the coil, respectively, M_i is the mutual inductance between the ith receiving coil and the transmitting coil, and P is the horizontal coordinate of the receiving coil. In the experiment, the rms value of the current on the transmitting coil can be adjusted by controlling the phase difference of the MOSFETs.

B. Performance Validation of Optimization Algorithms

To validate the effectiveness and reliability of the proposed two-stage optimization algorithm, simulation experiments are conducted, where the output voltage is constrained by $V_{\text{out1}} =$ 24 V, $V_{\text{out2}} = 12$ V, and $V_{\text{out3}} = 3.3$ V, the maximum relative error of the output voltage is 2%, and the maximum current of the transmitting and receiving coils is considered 4 A. After 1000 random initializations, the algorithm proposed in this article is compared with the IPM and GA in terms of computational speed and optimization results, as illustrated in Fig. 8.

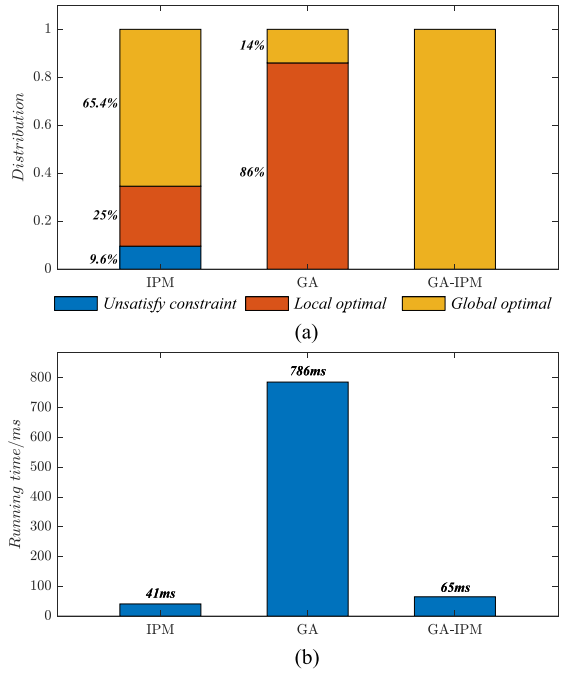

Fig. 8. Comparison of optimization results of three algorithms. (a) Proportion of optimized distribution after multiple random initialization of algorithms. (b) Average running time.

According to Fig. 8, some conclusions can be summarized. Specifically;

1) the IPM may result in optimization that does not satisfy constraints, achieves a local optimum, or reaches a global optimum,
2) all optimization results of GA satisfy the constraint conditions, but the obtained solution may not be the global optimal solution,
3) the two-stage optimization algorithm designed in this paper consistently achieves the global optimum in all running results, and
4) the running time of GA is obviously the longest. Compared with IPM, the two-stage optimization algorithm presented in this article has a little longer running time, but both of them are far less than GA.

To further elucidate the principle behind the algorithm's attainment of global optimum, Fig. 9 illustrates the iterative processes of the three algorithms in a two-variable constrained optimization problem. In Fig. 9, the *X*- and *Y*-axes represent the two optimization variables, and the *Z*-axis represents the fitness of the objective function, with color indicating the corresponding numerical value. The goal of the optimization is to achieve the maximum value of the objective function within the specified constraints. The solid red lines depict the iteration process of

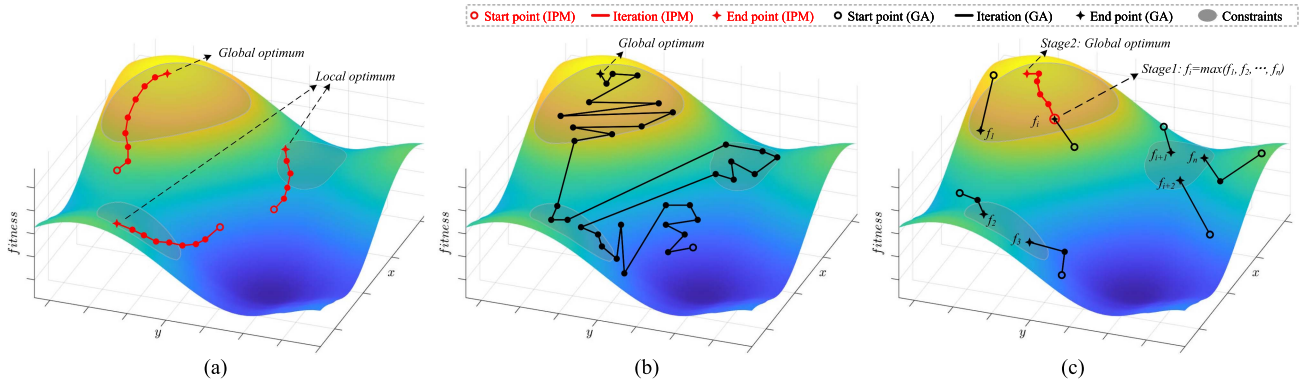

Fig. 9. Iteration process of three algorithms. (a) Iterative process of IPM algorithm, easily captured in local optimum. (b) Iterative process of GA algorithm, approaching the global optimal solution after long iterations. (c) Iterative process for the proposed two-stage optimization algorithm, fast and well-balanced—GA-IPM.

different algorithms, while the transparent gray region represents the feasible domain formed by the constraint conditions. Fig. 9(a)–(c) correspond to the optimization results of the IPM algorithm, GA algorithm, and GA-IPM algorithm, respectively.

As shown in Fig. 9(c), initially, in the first stage, the algorithm randomly initializes a population consist of multiple individuals and iterates using GA to obtain multiple feasible solutions within the constraints, corresponding to objective function values of f_1–f_n. Subsequently, the solution corresponding to the maximum objective function value f_i within the constraint boundary of the first stage is taken as the start point of the second stage optimization, and IPM is employed for further refinement. In the first stage, several strategies are adopted to optimize the running time of the GA algorithm. First, a large penalty term P is adopted to enable the algorithm to quickly reach the feasible domain; Second, when the individual reaches the feasible domain, the corresponding solution will be terminated to accelerate the iteration speed of the remaining solutions. By ensuring that the endpoint of the first stage is within the feasible domain, the algorithm avoids the inadequacy in inappropriate initial point selection that might lead to convergence towards local optimum. In addition, Fig. 9(a) and (b) shows the iterative process using only IPM or GA algorithm, respectively. The optimization result of IPM is greatly affected by the optimization starting point and easily falls into the constrained local optimal solution, while the GA algorithm requires more iterations to get close to the global optimal solution.

C. Verification of Output Voltage

In this section, we validate the optimization results derived from the two-stage optimization algorithm as discussed in the preceding section. First, the parameters of the experimental platform are adjusted in accordance with the results of the optimization algorithm. Then, the measured results of the corresponding output voltage and transmission efficiency are recorded and compared, as presented in Table II.

In the experiment, the load instrument adopts constant resistance (CR) mode with a resistance value set at 20 Ω. The efficiency measured in the experiment is dc to dc value, where the input power is the product of the voltage at the input and the mean value of the input current, and the output power is the sum of the power measured by the electronic load instruments. The duty cycle of the full bridge inverter is set to 26.33%, and the boost ratios of the three receiver buck–boost circuits are 1.02, 0.70, and 0.64, respectively, according to the solution result of the two-stage optimization algorithm. It can be observed that the actual output voltage is very close to the optimized voltage value, which proves the effectiveness of the theoretical calculation in this article.

TABLE II
RESULT COMPARE

Parameter	Optimization	Measure	Error
V_{out1}	$24.48V$	$23.98V$	2.04%
V_{out2}	$12.24V$	$12.01V$	1.88%
V_{out3}	$3.23V$	$3.22V$	0.31%
Efficiency	84.19%	84.10%	0.11%

To validate the accuracy of the output voltage within multiple output ranges further, we adjust one or more sets of voltage values within the three receivers while keeping the values of other sets unchanged for repeated optimization verification. In the specific experiments, we initially set the full-bridge inverter to its maximum output and manually adjusted the boost ratios of the three receiver dc–dc converters separately. Under the constraint of ensuring that the coil current satisfies the current carrying capacity, the maximum output values of the three load voltages are obtained as 38, 34, and 14 V, respectively. Subsequently, to validate the proposed method, a total of 14 experiments are conducted by setting the output voltages using an equidistant stepping approach. The voltage adjustment step sizes for these experiments are set as 2, 2, and 1 V, respectively. Finally, the proposed optimization algorithm is employed to determine the duty cycle of the inverter, boost ratio of the dc–dc converters, and theoretical output voltages for each set of experiments. Based on each optimization result, experimental platform parameters are adjusted to obtain the actual output voltages. The parameters for different voltage outputs are updated every 5 s, and the optimization results for voltage are recorded and compared with the actual voltage output, as shown in Fig. 10.

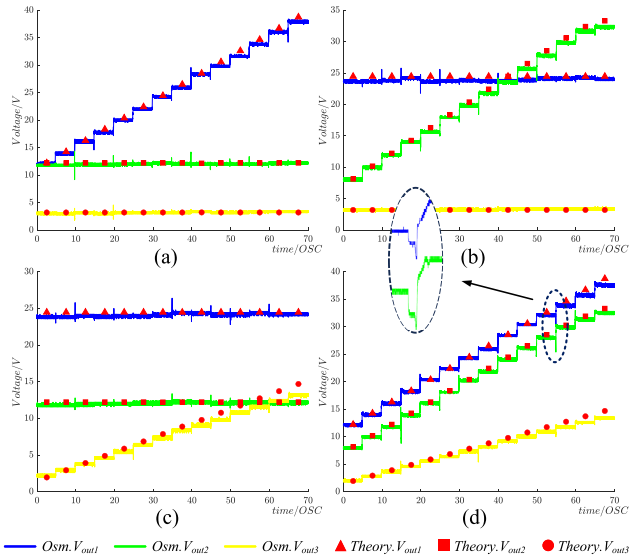

Fig. 10. Comparison between oscilloscope waveform and theoretical/measured load voltage. (a)–(c) Voltage measurement results when adjusting the voltages from V_{out1} to V_{out3} individually. (d) Voltage measurement result of adjusting V_{out1} to V_{out3} at the same time. The enlarged part represents the oscillation when adjusting the voltage.

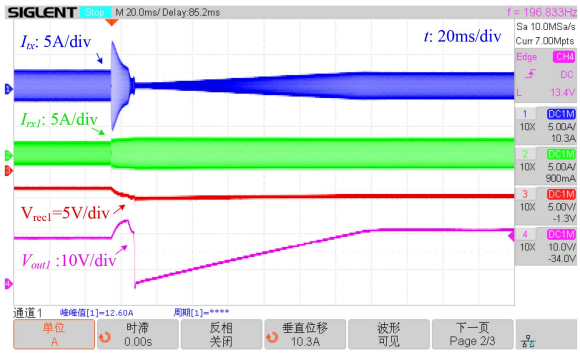

Fig. 11. Voltage and current sampling waveforms at voltage-switching moment.

Overall, the actual output voltage closely follows the optimized constraint voltage, demonstrating the reliability of this article's derivation of load voltage values for the WPT system. According to the magnified portion in Fig. 10(d), significant voltage oscillations (approximately 100 ms) may occur when the output voltage switches. This phenomenon is likely caused by the synchronous switching between the transmitter inverter and the receiver buck–boost circuit. To validate this statement, the coil current, the receiver voltage and the output voltage are sampled at the voltage switching moment, as shown in the Fig. 11. It can be observed that at the moment of voltage adjustment, the coil current at the transmitter instantaneously increases and then rapidly decreases to zero, while the output voltage experiences a significant oscillation drop. Subsequently, both the transmitter current and the output voltage gradually increase to the steady-state value after the adjustment. This explanation confirms that the occurrence of oscillations is indeed due to the temporary imbalance in the LCC topology caused by adjusting the inverter duty cycle, which eventually stabilizes after a certain period of time.

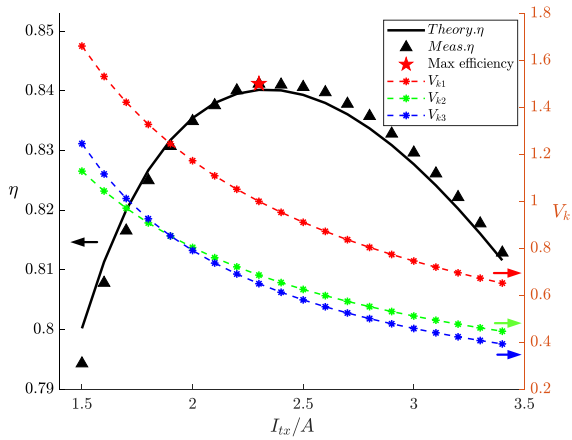

Fig. 12. Variation of transmission efficiency and boost ratio of buck–boost circuit with transmitter current.

D. Max Transmission Efficiency Verification

In Section IV-C, this article achieved the constrained load voltage $V_{\text{out1}} = 24$ V, $V_{\text{out2}} = 12$ V, $V_{\text{out3}} = 3.3$ V and maximized the transmission efficiency through two-stage optimization algorithm, resulting in an overall efficiency value of 84.1%. To verify that the efficiency is the highest achievable efficiency while satisfying this optimization constraint, it is crucial to measure the efficiency values corresponding to different duty cycles and boost ratios when the load voltage is constrained to specific levels. Therefore, we adjust the output voltage control strategy of the buck–boost circuit to a fixed value rather than a specific boost ratio controlled by a PID closed-loop adjustment. The output value is set to the corresponding constrained voltage, and the efficiency measurements are taken by adjusting the duty cycle of the transmitter inverter module to achieve different transmitting coil currents. Finally, we obtain the variations in overall transmission efficiency and the variations in the boost ratio of each receiver buck–boost circuit, as shown in Fig. 12.

It is clear that that the efficiency optimum obtained by the optimization algorithm aligns with the experimentally measured efficiency peak, indicating that the results derived from the algorithm are reliable.

E. Load Adjustment Verification

In the previous descriptions, our validations are all based on a controlled load resistance of 20 Ω for the three receiving coils. This represents a relatively light load for the structure constructed in this article. Therefore, it is necessary to further verify the reliability of the algorithm under higher loads. We conducted voltage adjustment verification and efficiency optimization verification with load resistances of 15 and 10 Ω, following the same experimental methodology as previously explained.

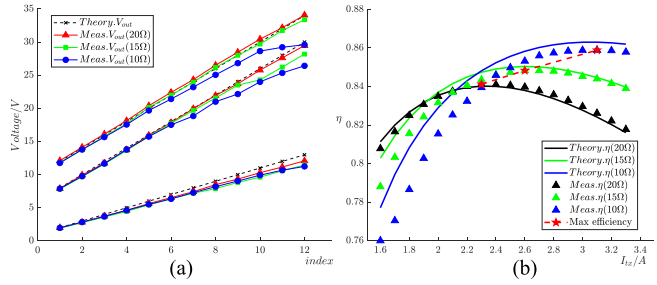

Fig. 13. Comparison of output voltage and transmission efficiency for different load resistances. (a) Synchronous voltage adjustment under three different load conditions. (b) Efficiency comparison of constant voltage output at different loads.

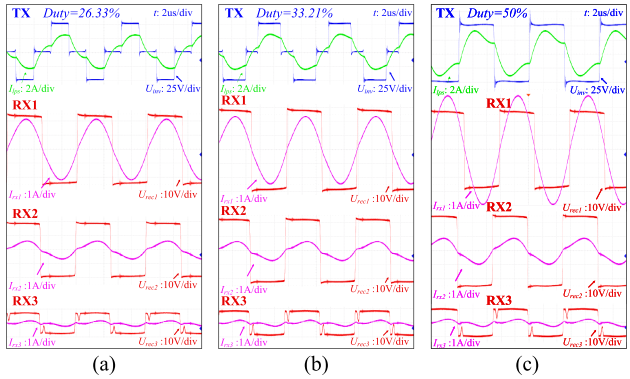

Fig. 14. Voltage and current waveforms as the load resistance changes with constrained output voltages of 24, 12, and 3.3 V, respectively. (a) $R_{\text{load}} = 20\,\Omega$. (b) $R_{\text{load}} = 15\,\Omega$. (c) $R_{\text{load}} = 10\,\Omega$.

For the voltage adjustment verification, we conducted three sets of voltage synchronous adjustments for load resistances of 15 and $10\,\Omega$ under CR mode, as described in the fourth verification in Fig. 10(d). We observed the optimized voltage values and the actual output voltage results for different load values, as shown in the Fig. 13(a). In addition, we also test the variations in optimized efficiency values and the actual measured efficiency for different load resistance values, and the results are recorded in the Fig. 13(b).

Fig. 13(a) shows that under different loads, the voltage outputs of the three receivers are still very close to the theoretical output values. However, when the output voltage is the same, the smaller the resistance, the greater the corresponding voltage output error due to the increase in power. This is consistent with common sense.

The efficiency curve in Fig. 13(b) reflects some potential characteristics of WPT systems. First, when the current in the transmitting coil is low, the overall transmission efficiency decreases significantly, and the measurement error is also greater. As the current increases, the measurement accuracy gradually improves. This is because at lower transmitting coil currents, the buck–boost circuit must provide a higher boost ratio to obtain the same output voltage, which reduces the equivalent resistance of the load and increases the current on the receiving coil [25]. Second, as the load resistance decreases, the measurement error increases, which is also a result of the higher receiver current under the same output voltage. Finally, as the load resistance decreases, the peak point of system transmission efficiency becomes higher. Therefore, for the same output voltage, the higher the output power, the greater the maximum system efficiency value that can be achieved.

Fig. 14 shows the waveforms of the inverter output voltage, inverter output current, receiver voltage and current under different load resistances, when the three load outputs are stable at 24, 12, and 3.3 V. The inverter duty cycle and the boost ratio of the dc–dc converters are the optimal solutions obtained through optimization. It can be seen that as the load increases, the duty cycle of the inverter output, the inverter output current, the receiver voltage and the current of each receiving coil all increase. In Fig. 14, all the timing starting points of waveform are consistent because we use the inverter output voltage as a unified trigger signal for each measurement.

Overall, the validation of the algorithm presented in this paper for higher load transmission efficiency is also reliable. According to Fig. 13, for load resistance values of 20 and $15\,\Omega$, the algorithm obtains the optimal efficiency point consistent with the theoretical values. However, the algorithm's optimal current value is 0.1 A higher than the theoretical value at $10\,\Omega$. This level of efficiency deviation is entirely acceptable, demonstrating the practical value of the algorithm proposed in this article.

V. Conclusion

In summary, to maximize the transmission efficiency of wireless charging setups, this article establishes a universal efficiency theoretical calculation formulation for multireceiver wireless charging devices and proposes a two-stage optimization algorithm with output voltage constraints. The optimization method has the capability to adjust the output voltage according to different application scenarios and topologies. Experimental results demonstrate that, under conditions of output voltages at 24, 12, and 3.3 V with a load resistance of $20\,\Omega$, the proposed method achieves a maximum transmission efficiency of 84.1%. Furthermore, experimental adjustments of output voltage and load resistance validate the algorithm's efficiency across a wide voltage output range. This research provides robust theoretical support for the design and optimization of multireceiver WPT system.

Appendix
Derivation of LCC Topology Compensation and Parameter Calculations

A. LCC Topology Parameter Design Method

The core idea of LCC topology parameter design is achieved by satisfying the T-symmetric network, which can realize the conversion of voltage and current, as shown in Fig. 15 [26]. In the consideration of the T-symmetric network, L_{ps} acts as the equivalent inductance jX on the left-hand side, C_{pp} as the capacitance $-jX$ at the bottom, and the combination of C_{ps} and L_{tx} forms the inductance jX on the right-hand side, with Z_0 being approximately equivalent to the reflection impedance of

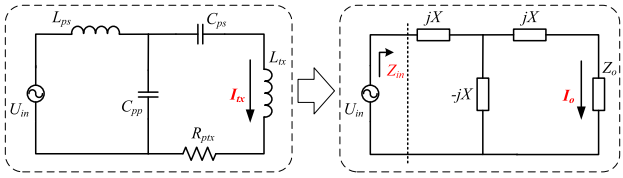

Fig. 15. *LCC* topology equation.

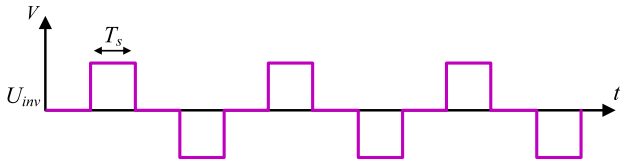

Fig. 16. Output waveform of the inverter.

the secondary coil. Under these compensation conditions, (16) needs to be satisfied, and it is equivalent to (1)

$$j\omega L_{ps} = j\frac{1}{\omega C_{pp}} = \frac{1}{j\omega C_p s} + j\omega L_{tx}. \tag{16}$$

For the right-hand side equivalent circuit, the input impedance Z_{in} and the output current I_o can be calculated as follows:

$$Z_{\text{in}} = jX + (-jX)//(jX + Z_o) = \frac{1}{X^2 Z_o} \tag{17}$$

$$I_o = \frac{-U_{\text{in}} jX}{Z_{\text{in}}\left[-(jX)//(jX + Z_o)\right]} = \frac{U_{\text{in}}}{jX}. \tag{18}$$

Considering the operating frequency ω of the system, the output current of the system can be equivalent to $I_o = U_{\text{in}}/j\omega L_{ps}$. This means that the output current of the transmitting coil is independent of the load and can be adjusted by L_{ps} and U_{in}.

B. LCC Topology Parameter Selection Method

The parameters of the LCC topology at the transmitter need to be determined by combining the self-inductance of the transmitting coil, the maximum current carrying capacity of the coil and the input voltage.

In the experimental conditions presented in this article, the 400-strand cross-section wires with a diameter of 0.05 mm are used, which can withstand a maximum current of approximately 4 A. The input voltage V_{in} of dc power supply is 50 V, so when the full-bridge inverter works at 50% duty cycle output, the effective value of the inverter output voltage U_{inv} can be calculated as $U_{\text{inv}} = 2\sqrt{2}/\pi V_{\text{in}} \sin(D_s\pi) \approx 45.0158$ V according to the (2), the L_{ps} inductance value should be greater than the value that $U_{\text{inv}}/\omega I_{\max} \approx 17.9$ μH. Therefore, considering the common inductance parameter value in the practical application, the L_{ps} selected in this experiment is 22 μH magnetic ring inductance, and the actual value measured by the *LCR* bridge is 22.93 μH. As shown in Table I.

After L_{ps} is selected, the values of C_{pp} and C_{ps} are further determined according to (1). In the experiment, the C_{pp} and C_{ps} are corrected by connecting multiple MMKP82 capacitors in parallel, and the final actual compensation values are 101.48 and 17.81 nF.

C. Inverter Output Voltage RMS Value Calculation

Assume that the modulation index of the full-bridge inverter is denoted as D_s, and the corresponding duration of the high-level state of the inverter is T_s in half period. The waveform of the output voltage can be represented as Fig. 16.

The output voltage of the inverter is a symmetrical rectangular waveform. Due to the filtering characteristics of the LCC topology, the primary effect during the resonance process is the fundamental harmonic component of the inverter. Equation (19) can be obtained by performing a Fourier decomposition of this waveform

$$U_{\text{inv}}(t) = \sum_{n=1}^{\infty} \frac{4V_{in}}{n\pi} \sin(n\pi D_s) \sin(n\omega t). \tag{19}$$

Considering the fundamental component when n is 1, the effective value can be calculated as $U_{\text{inv}} = \frac{2\sqrt{2}}{\pi} V_{\text{in}} \sin(D_s\pi)$. This formula corresponds to (2) in this article.

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