Letters

Dead-Time Compensation Method in Cascaded H-Bridge Inverter to Mitigate Zero-Crossing Distortion by Reflecting the Ratio of Current Polarity

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***Abstract*—This letter proposes an enhanced dead-time compensation method in cascaded H-bridge (CHB) inverters to mitigate current zero-crossing distortion (ZCD) by reflecting the ratio of current polarity. Typically, dead-time compensation involves adding an offset voltage, whose sign is determined by the current polarity, to the switching reference voltage. However, in digital signal processor (DSP)–based CHB systems, when the current polarity changes, offset voltages with an incorrect sign might be applied for the following reasons. First, due to the shadow register function in DSP, the offset voltage from previous samples is applied. Second, because the DSP only measures current at sampling points, if the current polarity changes within a control period (i.e., between sampling points), it cannot recognize the polarity change until the next sampling point. These two deteriorate current ZCD. Therefore, when the current polarity changes, the proposed method predicts the reference current of the next sample to prevent incorrect offset voltage caused by the shadow register. Furthermore, by using the reference currents of the present and predicted values, the current polarity ratio within a control period is reflected in the offset voltage; thus, mitigating current ZCD. The validity of the proposed dead-time compensation method is verified through experimental results conducted with a seven-level CHB inverter.**

***Index Terms*—Cascaded H-bridge (CHB) inverter, dead-time compensation, digital signal processor (DSP), shadow register, zero-crossing distortion (ZCD).**

I. Introduction

CASCADED H-bridge (CHB) inverters consist of several H-bridges in series, and this configuration enables their widespread use in high-voltage grid-connected systems [1], [2]. However, since CHB inverters with phase-shift pulsewidth modulation (PS PWM) form output voltages by accumulating H-bridge voltages, which have phase differences among them, voltage errors in H-bridges caused by dead times are also cumulative [3]. This leads to a relatively large amount of current zero-crossing distortion (ZCD), defined as the distortion in the vicinity of zero [4], in grid currents compared to two-level inverters. Thus, to achieve low harmonics, adequate dead-time compensation is necessitated [5].

The voltage errors caused by the dead-time effect are related to the grid current polarity. If the grid current is positive, the voltage error is negative; if negative, it is positive. Thus, dead-time compensation is conducted by adding an offset voltage to the original switching reference voltages, with the same magnitude but an opposite sign of the voltage error [6]. This implies that applying the wrong sign to the offset voltage rather exacerbates current ZCD. This can occur at the zero-crossing point of the grid current due to switching current ripples, as well as delays from the shadow register and communication.

There are only a few studies on dead-time compensation for multilevel converters. Li et al. [3] and Minshull et al. [7] presented methods for compensating for both the dead-time effect and the voltage drop caused by power semiconductors. Minshull et al. [7] analyzed the voltage drop caused by power semiconductors and the dead-time effect in diode-clamped multilevel converters using vector diagrams. This article compensated for the voltage drop by applying a lookup table that was prederived offline. In [3], the accuracy was increased by compensating for the voltage drop of the CHB through mathematical modeling. The studies of [3] and [7] focused more on compensating for the voltage drop of multilevel converters, whereas the dead-time compensation method used was the same as the one presented in [6]. Therefore, compensation errors may occur at the zero-crossing point, leading to ZCD deterioration.

Other previous works [8], [9], [10], [11], [12] also all rely on the dead-time compensation formula of [6]. Szwarc et al. [8] presented a dead-time compensation that additionally considers the parasitic capacitance discharge time in a multilevel neutral point clamped inverter. As this is merely adding a new term to the existing formula of [6], it cannot prevent ZCD deterioration. Schellekens et al. [9] set the offset voltage to zero within a specific range around zero-crossing point to reduce the current

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polarity detection error caused by switching current ripple, but this cannot be considered as a fundamental solution to ZCD. Abronzini et al. [10] introduced dead-time compensation in a CHB for model-based predictive current control (PCC). This method compensates for the offset voltage using the error between the measured current and the reference current. Although the formula is expressed in a different form due to the characteristics of PCC control, it is ultimately equivalent to that in [6]. Recent studies in [11] and [12] attempted to further improve dead-time compensation performance. These studies also use the formula from [6] but apply the predicted current polarity, derived from modeling of the CHB system, to the formula. With the prediction of the current, this method can prevent polarity detection errors caused by communication delays, and it showed some effectiveness in mitigating ZCD. However, it has the drawback of being dependent on system parameters.

The main objective of this letter is to propose a more accurate dead-time compensation for digital signal processor (DSP)–based CHB systems to mitigate ZCD. Therefore, it focuses on two issues not addressed in the previous studies when determining the offset voltage. The first issue is the delay of the switching reference voltage caused by the shadow register. In CHB systems, the shadow register of the DSP is commonly used to prevent the vertical crossing (also known as missed edge) phenomenon of PWM [13], [14]. It stores the switching reference voltage and later updates it at a predetermined point in time, generally at the minimum and maximum of the triangular carrier. Due to this updating delay, near the zero-crossing point of the grid current, the offset voltage determined from the previous samples is actually applied at the present sample, leading to incorrect compensation. For instance, if the current polarities are negative and positive at the previous and present samples, respectively, the offset voltage at the present value must be positive. However, due to the delay caused by the shadow register, the switching reference voltage with the negative offset voltage from the previous sample is applied to the present sample, and it remains until the next minimum or maximum point of the triangular carrier.

The second issue is the current polarity change within a control period. While the actual current is analog, digital processors, including DSPs, only measure this current at sampling points. This means that if the current polarity varies within a control period (i.e., between sampling points), the DSP cannot recognize the polarity change until the next sample. For instance, if the measured current at the present sample by the DSP is negative but the actual analog current changes to positive shortly after being sampled, assigning the negative sign to the offset voltage results in incorrect compensation.

To address the first issue, the proposed method predicts the reference current of the next sample, allowing it to detect the current polarity change in advance. This enables the prevention of incorrect sign imposition caused by the shadow registers on the offset voltage. To deal with the second issue, once a current polarity change is detected, the ratio of current polarity within a control period is reflected in the offset voltage calculation using the present and predicted reference currents. Therefore, the offset voltage formula of the proposed method differs from those

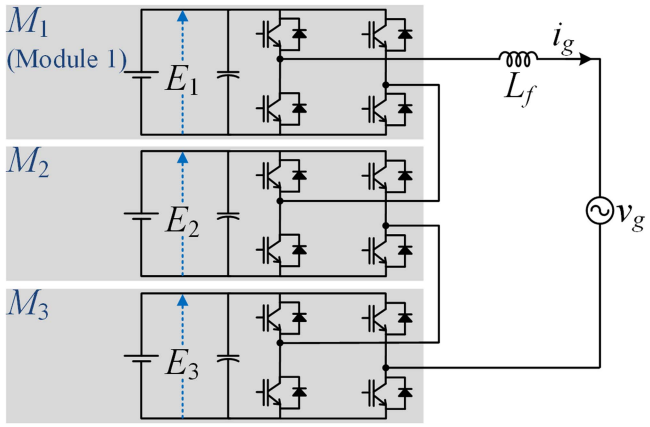

Fig. 1. Topology configuration of a seven-level CHB inverter in a single-phase grid-connected system.

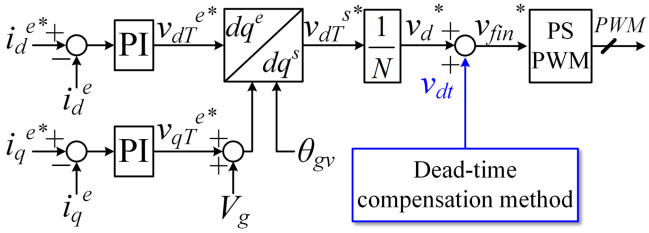

Fig. 2. Control block diagram for grid current with dead-time compensation.

in the previous studies. The proposed method inherently incorporates the compensation for communication delay presented in [11] and [12] as well, because it uses the predicted values of the reference currents. By applying the proposed dead-time compensation, further mitigation of the current ZCD is achieved. The validity of the proposed dead-time compensation method is verified through experimental results conducted with a seven-level CHB inverter.

II. Limitations of the Conventional Compensation Method

For ease of understanding, the descriptions in this letter are based on the seven-level CHB inverter in a single-phase grid-connected system, as shown in Fig. 1. The seven-level CHB consists of three modules (M_j, $j = 1, 2, 3$), and their corresponding dc-link voltages are denoted as E_j, where L_f, v_g, and i_g represent the filter inductor, grid voltage, and grid current, respectively.

Fig. 2 shows the block diagram of grid current control with dead-time compensation. dq-axis currents in the synchronous reference frame ($i_{dq}{}^e$) are controlled by proportional-integral controllers according to their references ($i_{dq}{}^{e*}$), forming $v_{dT}{}^{s*}$. $v_{dT}{}^{s*}$ is divided by the module number (N, which is 3 here), generating the original switching reference voltage ($v_d{}^*$). Subsequently, the offset voltage for dead-time compensation (v_{dt}) is added to $v_d{}^*$, forming $v_{fin}{}^*$ ($v_{fin}{}^* = v_d{}^* + v_{dt}$). In the conventional dead-time compensation method [3], [6], [7], [8],

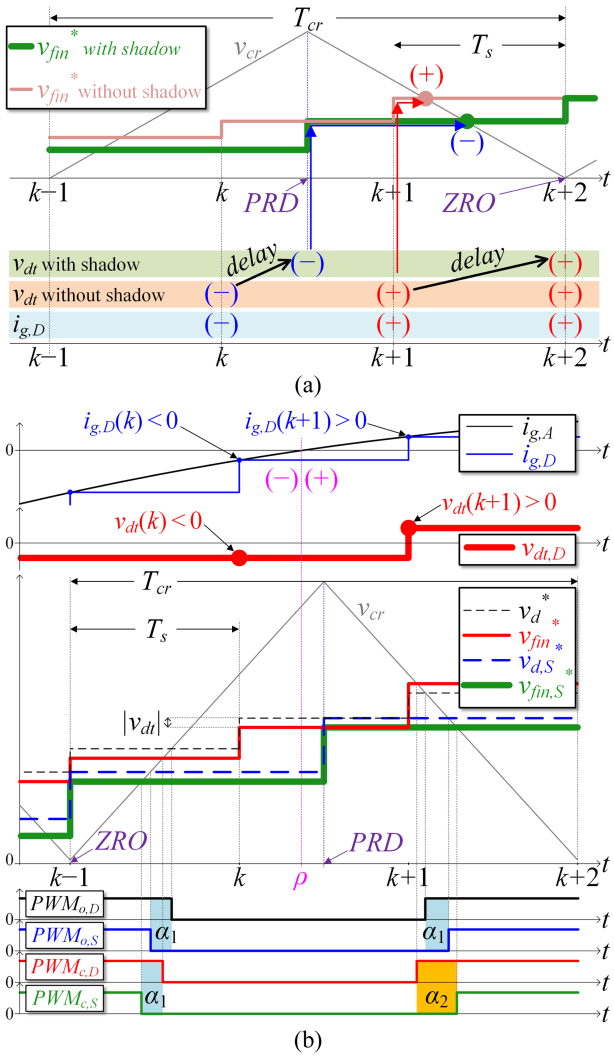

Fig. 3. Incorrect dead-time compensation in the conventional method caused by the shadow register. (a) Process of applying incorrect v_{dt}. (b) PWM error due to incorrect v_{dt}.

[9], [10], [11], [12], v_{dt} is defined as

$$v_{dt} = \begin{cases} 2E\,T_d f_{cr}, & (i_g > 0) \\ -2E\,T_d f_{cr}, & (i_g < 0) \end{cases} \tag{1}$$

where T_d and f_{cr} denote dead-time and carrier frequency. In (1), to simplify the equation, it was assumed that $E_1 = E_2 = E_3 = E$ [11]. This approach is valid because $v_{fin}{}^*$ is normalized by E_j when PS PWM is performed in M_j.

According to (1), the polarity of i_g determines the sign of v_{dt}. This means that the imposition of the wrong sign on v_{dt} results in incorrect compensation. The first scenario of this issue is attributed to the shadow register, as depicted in the time sequence diagram in Fig. 3(a). v_{cr}, T_{cr}, T_s, and $i_{g,D}$ denote the carrier, carrier period, control period, and DSP-sampled grid current, respectively, having k as the kth sampling point where $i_{g,D}$ is measured and control begins. The shadow register stores the previous sample values of $v_{fin}{}^*$ and updates them at the maximum (*PRD*) and minimum (*ZRO*) points of the carrier. As $v_{fin}{}^* = v_d{}^* + v_{dt}$, v_{dt} is also not updated at every T_s but at *PRD* and *ZRO*, causing a delay. As shown in the figure, the original v_{dt} is negative at kth and changes to positive at the $(k+1)$th. However, due to the shadow register, the negative v_{dt} at $(k+1)$th is not immediately updated but is instead updated at *PRD* and maintained until the next *ZRO* [$(k+2)$th]. This delay causes a negative v_{dt} to be applied instead of a positive v_{dt} at the switching point, resulting in incorrect compensation. Fig. 3(b) shows the PWM error caused by this issue. The PWMs corresponding to $v_d{}^*$ and $v_{fin}{}^*$, which are the original values without the shadow register, are $PWM_{o,D}$ and $PWM_{c,D}$, respectively. However, after processing through the shadow register, $v_d{}^*$ and $v_{fin}{}^*$ are converted into $v_{d,S}{}^*$ and $v_{fin,S}{}^*$, respectively, and $PWM_{o,S}$ and $PWM_{c,S}$ are output accordingly, where α_1 is the error between $PWM_{o,D}$ and $PWM_{o,S}$ that exists even without dead-time compensation. The polarity of analog current ($i_{g,A}$) changes at ρ, thus, $v_{dt}(k)$ is negative, and $v_{dt}(k+1)$ is positive. With regard to $v_{fin}{}^*(k+1)$, the positively valued $v_{dt}(k+1)$ is applied, resulting in the correct output, $PWM_{c,D}$. In contrast, $v_{fin,S}{}^*$ at *PRD* takes its value from $v_{fin}{}^*(k)$ and remains until the next *ZRO*, reflecting the negatively valued $v_{dt}(k)$ when forming $PWM_{c,S}$. This leads to the significant PWM error α_2, exacerbating current ZCD.

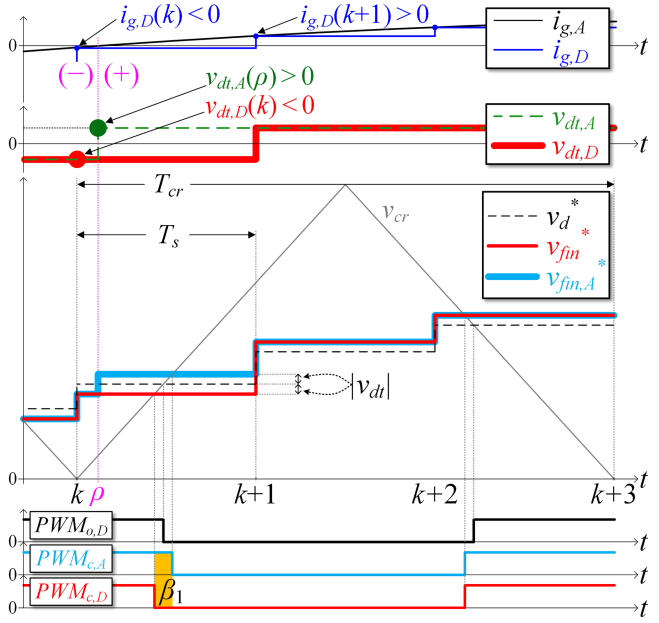

Fig. 4. Incorrect dead-time compensation in the conventional method due to polarity changes within a control period.

The second scenario of incorrect compensation is related to the nature of digital systems. In Fig. 4, the polarity change point ρ is placed within T_s and is closer to the kth sample than to the $(k+1)$th sample. This indicates that the polarity ratio of $i_{g,A}$ within T_s leans more toward positive. If the polarity of $i_{g,A}$ at ρ could be reflected, a positively valued $v_{dt,A}(\rho)$ would be applied to form $v_{fin,A}{}^*(\rho)$, resulting in $PWM_{c,A}$. However, in the DSP, the negatively valued $v_{dt,D}(k)$, which persists until the $(k+1)$th sample, is used to form $v_{fin}{}^*(k)$, generating $PWM_{c,D}$. This leads to the PWM error β_1, deteriorating current ZCD.

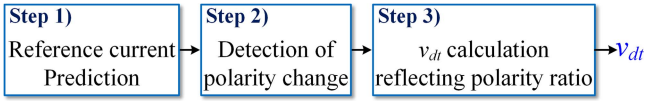

Fig. 5. Entire process of the proposed method.

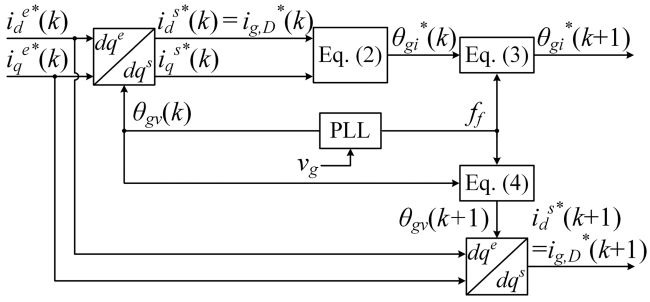

Fig. 6. Specific block diagram of step 1): The reference current prediction in the proposed method.

III. Proposed Compensation Method

The proposed dead-time compensation is also conducted by adding v_{dt} to v_d^*, as depicted in Fig. 2. However, the process of v_{dt} calculation differs from that in Section II. Therefore, the block labeled "dead-time compensation method" in Fig. 2 is replaced by the one in Fig. 5. Fig. 5 shows the entire process of the proposed dead-time compensation method, which consists of three steps: 1) reference current prediction, 2) detection of polarity change, and 3) v_{dt} calculation reflecting polarity ratio.

A. Step 1) Reference Current Prediction

In the proposed method, it is assumed that the grid current tracks its reference value well; thus, reference values of grid current are used instead of the measured ones to avoid the misdetection of current polarity caused by noise and switching current ripple. Fig. 6 shows the specific block diagram of step 1) shown in Fig. 5. The objective of Fig. 6 is to predict the reference grid current for the $(k+1)$th sample ($i_{g,D}{}^*(k+1)$) and its phase angle ($\theta_{gi}{}^*(k+1)$) at the kth sample. The process in Fig. 6 is as follows. First, the values at the kth sample, i.e., $\theta_{gi}{}^*(k)$ and $i_{g,D}{}^*(k)$, need to be calculated. By transforming $i_{dq}{}^{e*}(k)$ in reverse based on the phase angle of the grid voltage (θ_{gv}), which is given by the phase-locked loop (PLL), the values in the stationary reference frame ($i_{dq}{}^{s*}(k)$) are derived, where $i_d{}^{s*}(k)$ is the same as $i_{g,D}{}^*(k)$. Regarding $\theta_{gi}{}^*(k)$, it is calculated using $i_{dq}{}^{s*}(k)$ as shown in the following equation:

$$\theta_{gi}^*(k) = \tan^{-1}\left[i_q^{s*}(k)/i_d^{s*}(k)\right] + \pi/2. \tag{2}$$

Next, using $\theta_{gi}{}^*(k)$, $\theta_{gi}{}^*(k+1)$ is predicted as

$$\theta_{gi}^*(k+1) = \theta_{gi}^*(k) + 2\pi f_f T_s \tag{3}$$

where f_f denotes the fundamental frequency of the grid voltage provided by the PLL. After that, the one-sample predicted value of $\theta_{gv}(k)$, i.e., $\theta_{gv}(k+1)$, is predicted in the same manner as in (3); thus, $\theta_{gv}(k+1)$ is defined as

$$\theta_{gv}(k+1) = \theta_{gv}(k) + 2\pi f_f T_s. \tag{4}$$

Finally, $i_{dq}{}^{s*}(k+1)$ is derived by transforming $i_{dq}{}^{e*}(k)$ in reverse using $\theta_{gv}(k+1)$, where $i_d{}^{s*}(k+1)$ is the same as $i_{g,D}{}^*(k+1)$. As a result, by determining the polarity of the predicted $i_{g,D}{}^*(k+1)$, it is possible to prevent the application of incorrectly signed v_{dt} due to the shadow register. If there is a communication delay, the process in step 1) is iterated to predict values for the number of delayed samples. For instance, if there is a communication delay of one sample, one additional sample is predicted, and $i_{g,D}{}^*(k+2)$ and $\theta_{gi}(k+2)$ are derived for use in the next processes, i.e., step 2) and step 3).

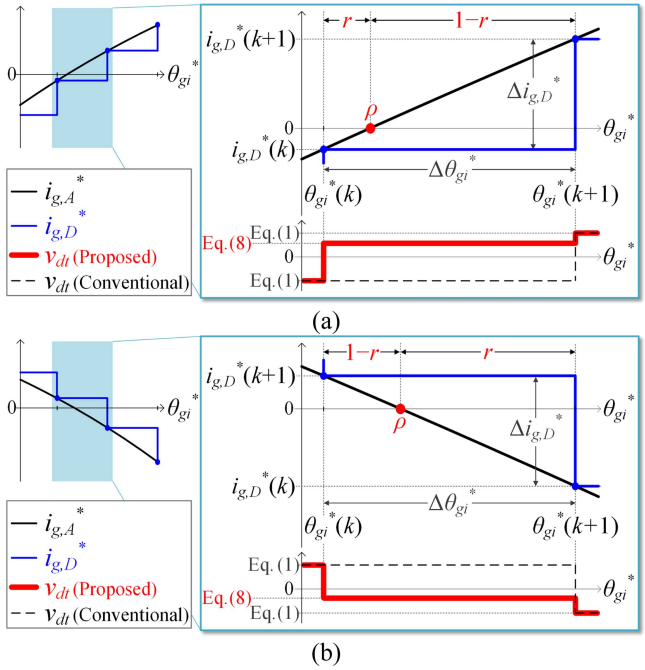

Fig. 7. Detection of $i_{g,A}{}^*$ polarity changes and v_{dt} calculation reflecting the polarity ratio. (a) $m > 0$. (b) $m < 0$.

B. Step 2) Detection of Polarity Change

To implement the polarity ratio reflection in the proposed dead-time compensation method, it is necessary to first detect current polarity changes. As shown in Fig. 7, the ideal analog reference current ($i_{g,A}{}^*$) is assumed to exist. Because $i_{g,D}{}^*(k)$ and $i_{g,D}{}^*(k+1)$ are given from step 1), the polarity changes of $i_{g,A}{}^*$ can be detected based on the following equation:

$$i_{g,D}^*(k) \cdot i_{g,D}^*(k+1) < 0. \tag{5}$$

If (5) is satisfied, it indicates that the polarity of $i_{g,A}{}^*$ changes at ρ within T_s; thus, step 3) is performed to calculate v_{dt} reflecting the polarity ratio. In the opposite case, v_{dt} is determined by (1).

C. Step 3) v_{dt} Calculation Reflecting Polarity Ratio

If the condition (5) is satisfied, it is first necessary to determine whether $i_{g,A}{}^*$ is increasing or decreasing. This determination can be made by calculating the slope (m), which represents the change in $i_{g,D}{}^*$ ($\Delta i_{g,D}{}^*$) relative to the change in $\theta_{gi}{}^*$ ($\Delta\theta_{gi}{}^*$). The value of m is defined as

$$m = \frac{\Delta i^*_{g,D}}{\Delta\theta^*_{gi}} = \frac{i^*_{g,D}(k+1) - i^*_{g,D}(k)}{\theta^*_{gi}(k+1) - \theta^*_{gi}(k)} \tag{6}$$

The scenarios of positive and negative m correspond to Fig. 7(a) and (b), respectively. In both figures, the proportion of time during T_s that $i_{g,A}{}^*$ is negative is defined as the polarity ratio (r), and accordingly, the proportion of time that it is positive is defined as $1-r$.

r can also be calculated as the proportion of phase angles instead of the time proportion. Given that ρ is 2π when $m > 0$ and π when $m < 0$, r is derived using $\theta_{gi}{}^*(k)$ and $\theta_{gi}{}^*(k+1)$ obtained from step 1), as expressed in the following equation:

$$r = \begin{cases} \frac{2\pi - \theta^*_{gi}(k)}{\theta^*_{gi}(k+1) - \theta^*_{gi}(k) + 2\pi}, & (m > 0) \\ \frac{\theta^*_{gi}(k+1) - \pi}{\theta^*_{gi}(k+1) - \theta^*_{gi}(k)}, & (m < 0) \end{cases}. \tag{7}$$

With the calculated r, v_{dt} in the proposed dead-time compensation is defined as follows:

$$\begin{aligned} v_{dt} &= -2ET_d f_{cr} r + 2ET_d f_{cr}(1-r) \\ &= 2ET_d f_{cr}(1-2r). \end{aligned} \tag{8}$$

It can be seen that v_{dt} in (8) is expressed differently from that in (1). In the conventional method, v_{dt} is either $2ET_df_{cr}$ or $-2ET_df_{cr}$ depending on the polarity of i_g. However, as depicted in Fig. 7, v_{dt} from (8) is positioned between $2ET_df_{cr}$ and $-2ET_df_{cr}$ due to the reflection of r. v_{dt} is added to $v_d{}^*$ to generate $v_{fin}{}^*$, as shown in Fig. 2. As this $v_{fin}{}^*$ compensates for the dead time more effectively than the conventional method, it consequently achieves better mitigation of current ZCD. The theory of the proposed dead-time compensation method can be applied to all digital systems without modification.

IV. Experimental Results

The proposed dead-time compensation method was verified through an experimental setup with a seven-level CHB inverter, as shown in Fig. 8. The DSP model TMS320F28377D was used for the master board and subboards, and there is a communication delay of one sample between the master board and the subboards. Due to this communication delay, as explained in Section III-A, for the experimental implementation of the proposed method, the two-sample predictions $i_{g,D}{}^*(k+2)$ and $\theta_{gi}(k+2)$ were used. In all experiments, T_s, f_{cr}, L_f, and T_d were set to 200 μs, 1.67 kHz, 1.9 mH, and 5 μs, respectively.

Fig. 9 depicts the experimental results of v_{dt} when i_g polarity changes. In this experiment, i_g was controlled at $5A_{pk}$. During the shaded control period, when the polarity changes, the conventional method produces a completely negative v_{dt}, as defined by (1), illustrated in Fig. 9(a). In contrast, the v_{dt} of the proposed method slightly increases toward the positive direction

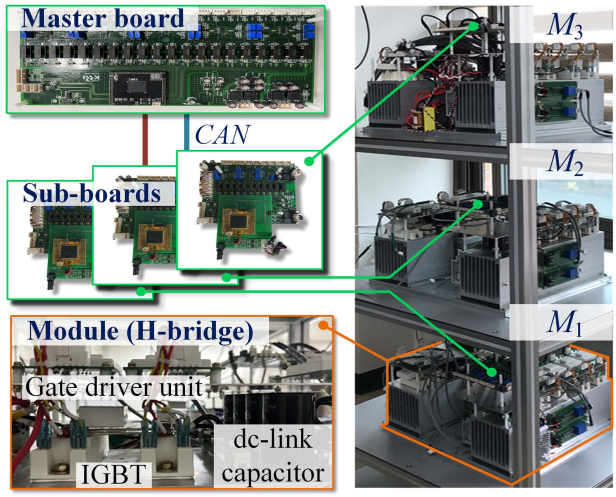

Fig. 8. Experimental setup.

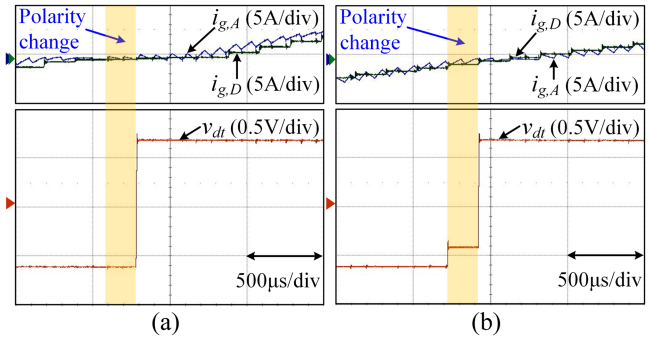

Fig. 9. Experimental results: Comparison of v_{dt}. (a) Conventional method. (b) Proposed method.

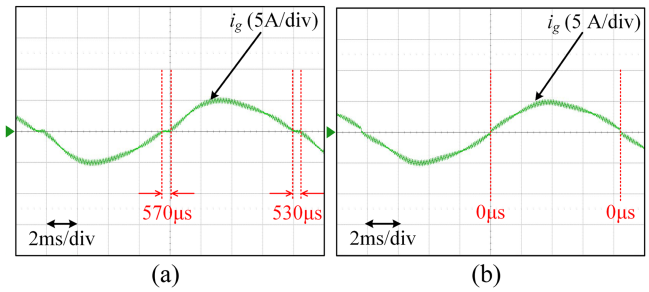

Fig. 10. Experimental results: comparison of distortion in i_g. (a) Conventional method. (b) Proposed method.

because it is derived by (8), reflecting the current polarity ratio. Consequently, i_g waveforms of both methods differ, as shown in Fig. 10. In Fig. 10(a), i_g in the conventional method exhibits a large amount of ZCD, about 570 μs and 530 μs. Conversely, as depicted in Fig. 10(b), i_g in the proposed method shows no ZCD; thus, the distortion in i_g is relatively small. Regarding FFT comparisons, it is clear that the proposed method results in lower odd harmonics compared to the conventional method, as shown in Fig. 11. Specifically, the third, fifth, and seventh harmonics were reduced by about 42%, 42%, and 67%, respectively, in comparison to the conventional method.

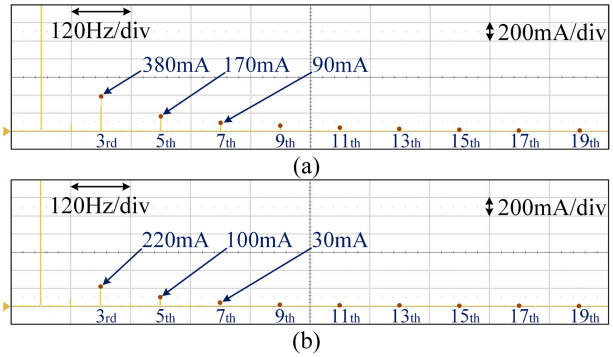

Fig. 11. Experimental results: Comparison of FFT in i_g. (a) Conventional method. (b) Proposed method.

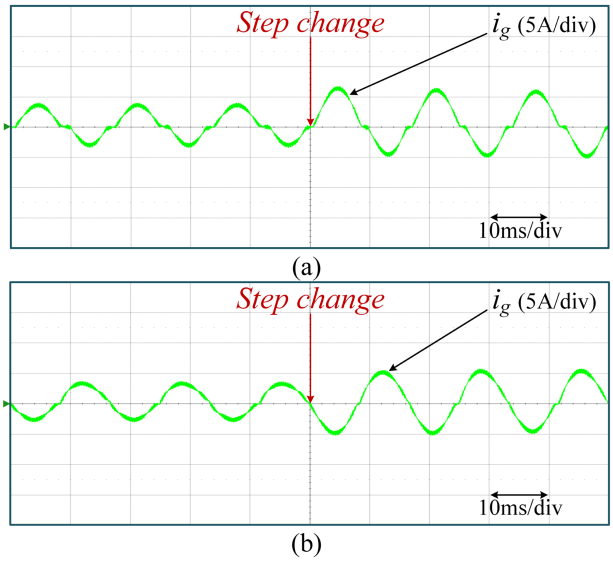

Fig. 12. Experimental results: comparison of transient response to step change in i_g. (a) Conventional method. (b) Proposed method.

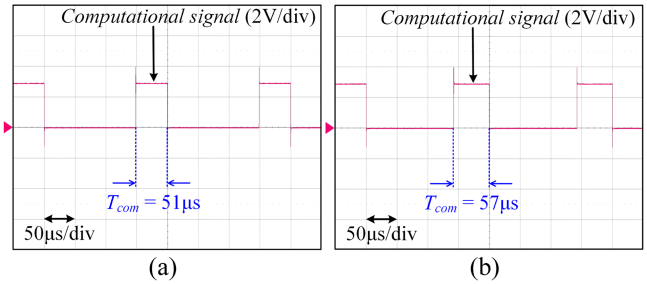

Fig. 13. Experimental results: comparison of $T_{\rm com}$. (a) Conventional method. (b) Proposed method.

Fig. 12 shows the comparison of the transient response to a step change in i_g, where i_g varies from $3A_{\rm pk}$ to $5A_{\rm pk}$. As the proposed method uses the reference value of i_g, there is some remaining distortion in i_g, as shown in this experiment. However, it still demonstrates superior compensation effects compared to the conventional method. If the switching current ripple is very small and a hardware setup resilient to noise is ensured, applying the proposed method based on measured values could further reduce the distortion in i_g.

A comparison of computational time ($T_{\rm com}$) is also provided, as shown in Fig. 13. Despite providing better dead-time compensation, the proposed method only increases $T_{\rm com}$ by approximately 6 μs compared to the conventional method.

V. Conclusion

This letter proposed an enhanced dead-time compensation method in CHB inverters to mitigate current ZCD. In the conventional dead-time compensation method, incorrect compensation occurs due to the shadow register and current polarity changes within a control period. However, the proposed method, which predicts the reference current for the next sample and calculates the ratio of the reference current polarity, results in adequate compensation. With the proposed method, mitigation of ZCD is achievable. The experimental results proved that the proposed method is more effective in terms of mitigating current ZCD and reducing odd harmonics.

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