Comprehensive Analysis of Synchronous Rectifying Signal Delay of High-Frequency *LLC* Resonant DC/DC Converter

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***Abstract*—*LLC* resonant dc/dc converters are widely applied in various scenarios, such as electronic device power supplies, vehicle chargers, etc. To improve the efficiency of the *LLC* converter, synchronous rectifiers (SR) are employed. However, due to various reasons, such as the hardware propagation delay, the SR gate signal can lag behind the secondary-side current particularly when the switching frequency of the *LLC* converter approaches the mega-Hertz level. This delay has a critical impact on the operation mode and the output characteristic of the *LLC* converter. Starting with the SR delay mechanism, this article comprehensively analyzes the operation of the *LLC* converter and derives the time-domain model under SR signal delay. The output gain and accurate power loss model of MOSFETs under different working modes are built to study the impact of SR signal delay on the *LLC* converter. The relationship between the SR signal delay and the *LLC* converter characteristics is quantified and summarized. Two new working stages of the *LLC* converter are revealed. Simulation and experimental studies are conducted to validate the theoretical analysis results. This article can provide the theoretical basis for optimizing the design of a high-frequency *LLC* converter.**

***Index Terms*—High-frequency, *LLC* resonant converter, signal delay, synchronous rectifier (SR), time-domain model.**

I. Introduction

LLC resonant dc/dc converters are extensively applied in the industry due to their attractive features, such as low switching power loss, high power density, and galvanic insulation [1]. The aforementioned superiorities enable them to dominate the market segments, such as electric vehicle chargers, electronic device power supply, renewable energy generation, aviation power systems, etc [2], [3], [4]. As the demand of increasing power density conversion systems rises in the industry, the application of wide bandgap (WBG) devices enables them to operate at higher switching frequency, thus the power density can be further improved. As reported in [5], a 1-kW *LLC* resonant converter using gallium nitride HEMTs can reach 1-MHz switching frequency while the power density is 140 W/in^3.

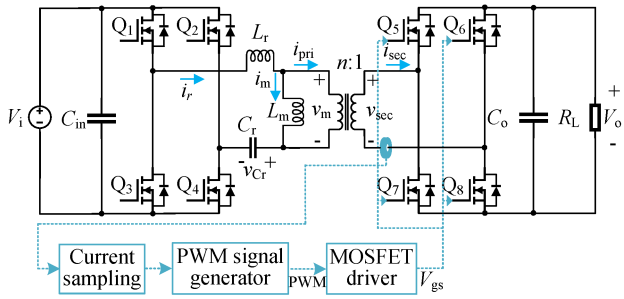

Fig. 1. Topology of an *LLC* converter with SR signal generation circuit.

The increasing switching frequency can effectively shrink the size of passive components while it also poses challenges for the converter design in terms of EMI noise immunity, magnetics, power dissipation, PCB layout, etc. A major challenge that hinders the improvement of high-frequency resonant converters is the implementation of synchronous rectifier (SR) gate signal generation [6]. SR is employed for the dc/dc converter output bridge as shown in Fig. 1. Compared with the conventional diode rectifier, using power MOSFET on the output side can reduce the conduction loss caused by the forward voltage on the rectifier diodes. However, the SR signal generation of a high-frequency dc/dc converter with WBG devices is very challenging, particularly for the Mega-Hertz level. An SR generation system is comprised of two major parts: the signal detection circuit which determines the correct turn-ON moment and the signal generation circuit. The signal detection circuit is usually more difficult than the signal generation module.

There are three state-of-the-art SR generation methodologies for high-frequency converters in the industry as follows.

1) Zero-crossing point detection of the secondary side ac current [7], [8], [9], [10], [11]. Usually, it requires a current sensor to measure the ac current of the rectifier. Via detecting the current direction, it can generate the gate signals for the MOSFETs.

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2) Source-drain voltage (V_{sd}) detection method [12], [13], [14], [15], [16], [17]. This function is generally integrated into the gate driver. When V_{sd} is higher than the threshold voltage, the gate driver output is pulled up to turn ON the MOSFETs. However, before V_{sd} reaches the threshold voltage, the current still flows across the body diode and the power loss caused by the forward voltage cannot be completely eliminated. Thus, some auxiliary circuits are introduced in the gate driver to minimize the conduction time of the body diode [13], [16].
3) Model-based method [18], [19], [20], [21], [22], [23], [24], [25]. It incorporates a mathematical model inside the controller to derive the current zero-crossing moment. The phase delay between primary and secondary MOSFETs and the duty cycle are all adjustable based on the calculation results.

The first two methods can be implemented using closed-loop analog circuits. The model-based method is usually based on model-predictive control using a digital controller.

However, the boosting switching frequency introduces a critical downside to the state-of-the-art SR solutions due to the following challenges.

1) The very short switching period requires ultra-fast signal processing units and sensors.
2) The high switching slew rate of the power devices raises large noises which makes the feedback current signal unclear.
3) The signal propagation delay caused by the hardware which is usually hundreds of nanoseconds should be considered now since a switching period can be finished within a microsecond.

The aforementioned two challenges can be tackled via optimizing the utilized hardware and components. The signal propagation delay, as plotted in Fig. 2, now attracts the attention of the industry. For the *LLC* resonant converters with switching frequency lower than 100 kHz, the impact of the SR signal delay can be roughly neglected. However, when the switching frequency approaches MHz, its impact should be considered in this condition. The delay will result in secondary side MOSFETs turning OFF after zero current crossing and affect the operation of the *LLC* converter [12]. However, the impact of the SR signal delay on the *LLC* converter has not been thoroughly studied previously.

In prior to tackling the problem caused by the signal delay, it is necessary to study its impact on the operation of the *LLC* converter which has not been thoroughly investigated. In the industry, the analysis of the resonant converter is usually conducted with the fundamental harmonic analysis (FHA) method as demonstrated in [26], [27], and [28] for preliminarily estimating the voltage gain characteristic. However, a concern of FHA is its accuracy since the high-order harmonics are neglected. Therefore, it is no longer feasible to analyze the SR signal delay, particularly when the switching frequency is far away from the resonant frequency. The time-domain model, first proposed in [29], can be utilized to precisely analyze the power loss and the gain characteristics of the *LLC* converter in various load conditions. These advantages make it appropriate for the *LLC* converter design optimization [30], [31], [32].

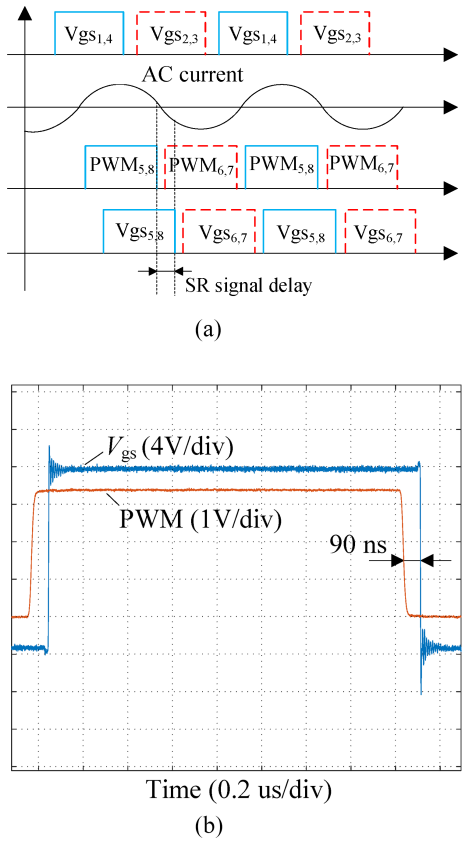

Fig. 2. Time delay phenomenon between PWM and gate drive signal. (a) Formation of SR signal delay. (b) Experimental waveforms.

Due to the aforementioned reasons, to provide the theoretical basis for mitigating the impact of SR signal delay on the high-frequency *LLC* converter, this article comprehensively analyzes the impact of SR signal delay on the resonant converter. The contributions of this article can be summarized as follows.

1) The impact of the SR signal delay on the *LLC* converter is comprehensively studied. This article reveals that the SR signal delay will lead to two new working stages of the *LLC* converter and the distortion of the ac current. The time-domain model of the *LLC* converter under SR signal delay has been derived.
2) The mechanism of how the SR signal delay impacts the output gain and the MOSFET power loss of the high-frequency *LLC* converter is demonstrated.
3) The equations for quantitatively calculating the influence of the SR signal delay on the voltage gain and the MOSFET power loss of the *LLC* converter are given in detail.
4) The proposed model as well as the theoretical analysis results can be utilized to optimize the design and improve the efficiency of high-frequency *LLC* converter.

The rest of this article is organized as follows. Section II introduces the origin of the SR delay, then analyzes the working stages and constructs the time-domain model of the *LLC* converter considering SR signal delay. Section III comprehensively studies the impact of SR signal delay on the *LLC* converter and verifies the analytical results with simulation. Then, the

TABLE I
DELAY TIME RANGE OF THE MAIN COMPONENTS IN AN SR GENERATION CIRCUIT

Hardware component	Delay time range (ns)
Gate driver IC	90–270 [34]
Operational amplifier	8–160
Logical gate circuit	8–11
PWM port of DSP	25

experimental verification is conducted in Section IV. Finally, Section V concludes this article.

II. THE TIME-DOMAIN MODEL OF THE *LLC* CONVERTER UNDER SR SIGNAL DELAY

A. The Analysis of the SR Delay Source

A dominant percentage of the SR signal delay is contributed by the signal processing or propagation of the hardware. Hardware components need time to process signals and generate the corresponding output. Specifically, the current or voltage signals are generally processed by sensors, signal conditioning circuits, sampling circuits, control units, and gate drivers. Most chips have input–output propagation delay time. For instance, DSP signal processing speed is determined by its clock frequency. The bandwidth of Op-Amp determines its delay time. Table I lists the approximated input–output propagation delay time range of the main components. It indicates that a majority of the total SR signal delay time is introduced by the gate driver chip.

B. The Operating Principle of Continuous Current Mode

Continuous current mode (CCM) is a working mode of the *LLC* converter when switching frequency f_{sw} is higher than the resonant frequency f_{r1} which is defined as [33]

$$f_{r1} = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{1}$$

where L_r is the resonant inductance and C_r is the resonant capacitance. In this mode, the magnetizing inductor L_m will not resonate with L_r and C_r.

The waveforms in the normal condition and the SR signal delay condition are compared in Fig. 3(a) and (b). The major difference between the normal condition and SR signal delay condition is the gate-source voltage v_{gs} lag behind the ac current. In the SR signal delay situation, during t_0 and t_1, the magnetizing current i_m keeps descending due to the delayed turn-OFF of the MOSFETs Q6 and Q7. Because i_m is lower than i_r, the direction of v_{sec} and i_{sec} are different now, which will cause reversed power flow from the load side. Meanwhile, the turn-OFF delay of the MOSFETs will lead to the new working stage of the *LLC* converter. The following part will derive the equations of the time-domain model in the positive half cycle. Note that the negative half cycle is zero-symmetric to the positive one, so their equations will not be given here.

Interval 1 [t_0, t_1]: In this interval, Q1 and Q4 turn ON, and Q6 and Q7 remain conductive. The equivalent circuit of the *LLC* converter is depicted in Fig. 4. The working stage of this interval does not exist in the normal condition. From Fig. 3(a), in

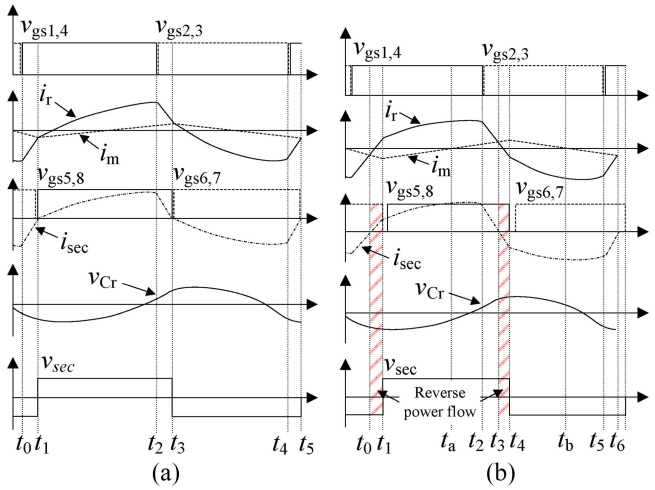

Fig. 3. Operating waveforms of an *LLC* converter in CCM. (a) Normal condition without SR signal delay. (b) With SR signal delay.

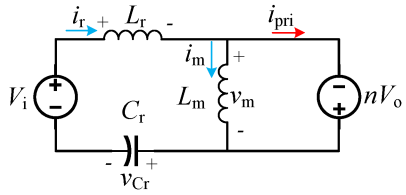

Fig. 4. Equivalent circuit of CCM in Interval 1.

the normal condition, i_r equals to i_m when Q5 and Q8 turn OFF. However, in the SR signal delay condition depicted in Fig. 3(b), due to the delayed turn-OFF of Q6 and Q7, i_m will keep increasing after equaling to i_r since v_m is not changed. According to KCL, i_{sec} can be calculated as

$$i_{sec} = n\left(i_r - i_m\right). \tag{2}$$

The direction of i_{sec} is positive. However, v_{sec} is still negative in this interval because of the turn-OFF delay of MOSFET. The transformer extracts energy from the load side to the resonant tank and i_m keeps increasing. L_m is charged by the input side and load side simultaneously. Since the peak i_m under SR signal delay is higher than the normal condition, L_m plays the role of a boost inductor in this interval.

According to Kirchhoff voltage law and neglecting the drain-source voltage V_{ds} of all MOSFET, the following equation can be derived:

$$v_{Lr} + v_{Cr} = v_i + nv_o. \tag{3}$$

Substituting $v_{Lr} = L_r \frac{di_r}{dt}$ and $i_r = C_r \frac{dv_{Cr}}{dt}$ into (3), the following equation can be obtained:

$$L_r C_r \frac{d^2 v_{cr}}{dt^2} + v_{cr} = v_i + nv_o. \tag{4}$$

The particular solution of (4) can be given as

$$v_{cr} = k_1 \cos\omega_r t + k_2 \sin\omega_r t + v_i + nv_o. \tag{5}$$

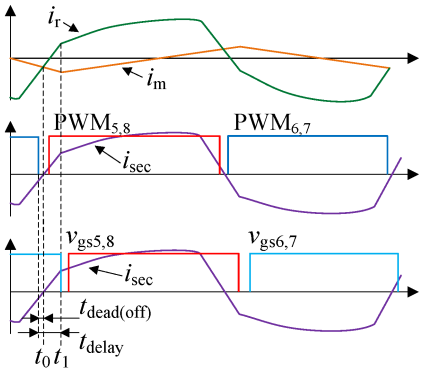

Fig. 5. Waveforms of PWM signal and gate driver signal of CCM.

Thus, i_r can be derived as

$$i_r = C_r \frac{dv_{cr}}{dt} = \omega_r C_r \left(-k_1 \sin \omega_r t + k_2 \cos \omega_r t\right) \tag{6}$$

where ω_r denotes the resonant angular frequency. Coefficients k_1 and k_2 depend on the initial conditions of the circuit.

Apart from the voltage and current equations, the initial values of v_{cr} and i_r, i.e., $v_{cr,t0}$ and $i_{r,t0}$, are necessary for the time-domain model. The initial time t_0 is assumed to be zero. The SR signal delay time t_{delay} is defined as the time between the falling edge of the control signal and $V_{\text{gs5,8}}$ signals. Switching dead time should be considered for t_1. The relationship between the PWM signal and gate signals is plotted in Fig. 5. The driving voltage $v_{\text{gs5,8}}$ and $v_{\text{gs6,7}}$ are delayed PWM signals, thus t_1 can be calculated as

$$t_1 = \max\left\{t_{\text{delay}} - t_{\text{dead(off)}}, 0\right\} \tag{7}$$

where $t_{\text{dead(OFF)}}$ is the time gap between the falling edge of the PWM signal and the zero current point of i_{sec}.

Because v_m is now $-nv_{\text{o}}$, i_m in this interval can be derived as

$$i_m(t) = -\frac{nv_o}{L_m} t + \frac{nv_o}{L_m}\left(t_1 - \frac{1}{4f_{\text{sw}}}\right). \tag{8}$$

Considering the energy conservation law between input and output in a half cycle [35], the initial voltage of the resonant capacitor, $v_{cr,t0}$, can be obtained. During t_0 and t_3, the charge of the resonant capacitor is

$$Q_c = C_r \cdot \Delta v_{cr} = C_r\left(v_{cr,t3} - v_{cr,t0}\right). \tag{9}$$

From Fig. 3(b), $v_{cr,t0}$ and $v_{cr,t3}$ are zero-symmetric. Substituting $v_{Cr,t3} = -v_{Cr,t0}$ into (9), the charge of resonant capacitance can be expressed as

$$Q_c = -2C_r v_{cr,t0}. \tag{10}$$

The input energy of the *LLC* converter is

$$E_i = v_i Q_c = -2v_i C_r v_{cr,t0}. \tag{11}$$

The output energy of the converter is determined by the load as

$$E_o = \frac{v_o^2}{2R_L f_{\text{sw}}}. \tag{12}$$

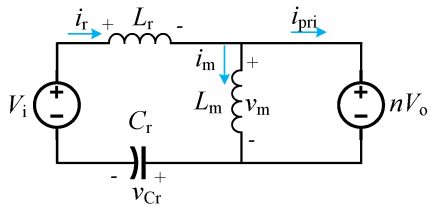

Fig. 6. Equivalent circuit of CCM in Interval 2.

The efficiency of the *LLC* converter is assumed to be η. Because $\eta E_i = E_o$, $v_{cr,t0}$ can be calculated as

$$v_{cr,t0} = -\frac{v_o^2}{4\eta R_L f_{\text{sw}} v_i C_r}. \tag{13}$$

Substituting $t = t_0$ into (5) and combining with (13), k_1 can be calculated as

$$k_1 = -\frac{v_o^2}{4\eta R_L f_{\text{sw}} v_i C_r} - v_i - nv_o. \tag{14}$$

During this interval, v_m is $-nv_o$. Considering the symmetric characteristic of i_m, k_2 can be obtained as

$$\begin{cases} i_{m,t_1} = -i_{m,t_4} = -\frac{nv_o}{4f_{\text{sw}} L_m} \\ t_4 - t_3 = t_1 - t_0. \end{cases} \tag{15}$$

Thereby, $i_{r,t0}$ can be calculated as

$$i_{r,t_0} = i_{m,t_0} = \frac{nv_o\left(4f_{\text{sw}} t_1 - 1\right)}{4f_{\text{sw}} L_m}. \tag{16}$$

Substituting $t = t_0$ into (6) and combining with (16), k_2 can be calculated as

$$k_2 = \frac{nv_o\left(4f_{\text{sw}} t_1 - 1\right)}{4f_{\text{sw}} L_m \omega_r C_r}. \tag{17}$$

Interval 2 $[t_1, t_2]$*:* In this interval, Q1, Q4, Q5, and Q8 turn ON and the equivalent circuit is depicted as shown in Fig. 6. The polarity of v_m swaps due to the conduction of Q5 and Q8, thus L_m begins to discharge and i_m decreases to zero due to the positive v_m. During the time of zero point of i_m, namely t_a, and t_2, L_m is charged and i_m increases.

Similarly, v_{Cr} and i_r can be derived as follows:

$$v_{cr} = k_3 \cos \omega_r\left(t - t_1\right) + k_4 \sin \omega_r\left(t - t_1\right) + v_i - nv_o \tag{18}$$

$$i_r = \omega_r C_r\left[-k_3 \sin \omega_r\left(t - t_1\right) + k_4 \cos \omega_r\left(t - t_1\right)\right]. \tag{19}$$

Substituting $t = t_1$ into (20) and (21) and combining (5) and (6), k_3 and k_4 can be calculated as follows:

$$k_3 = k_1 \cos \omega_r t_1 + k_2 \sin \omega_r t_1 + 2nv_o \tag{20}$$

$$k_4 = -k_1 \sin \omega_r t_1 + k_2 \cos \omega_r t_1. \tag{21}$$

v_m equals to nv_o in this interval. Combining (7), i_m in this interval can be described as

$$i_m(t) = \frac{nv_o}{L_m}\left(t - \frac{1}{4f_{\text{sw}}}\right). \tag{22}$$

Interval 3 $[t_2, t_3]$*:* In this interval, Q2 and Q3 turn ON, Q5 and Q8 are still conductive. The equivalent circuit of the *LLC* converter is shown in Fig. 7. Because the input voltage changes

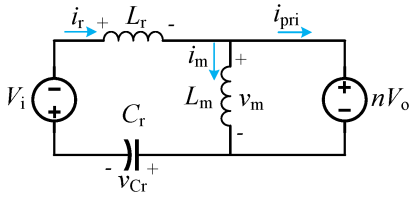

Fig. 7. Equivalent circuit of CCM in Interval 3.

to $-V_i$, L_r begins to discharge. i_m still increases since v_m is nv_o in this interval. i_{sec} is positive since i_r is still higher than i_m. The transformer delivers power from the input side to the load side.

Similarly, v_{Cr} and i_r can be derived as follows:

$$v_{cr} = k_5 \cos\omega_r (t - t_2) + k_6 \sin\omega_r (t - t_2) - v_i - nv_o \tag{23}$$

$$i_r = \omega_r C_r \left[-k_5 \sin\omega_r (t - t_2) + k_6 \cos\omega_r (t - t_2)\right]. \tag{24}$$

From Fig. 4(b), t_2 is the initial time of this interval and also the end time of Interval 2. Substituting $t = t_2$ into (23) and (24) and combining (18) and (19), k_5 and k_6 can be derived as follows:

$$k_5 = k_3 \cos\omega_r (t_2 - t_1) + k_4 \sin\omega_r (t_2 - t_1) + 2v_i \tag{25}$$

$$k_6 = -k_3 \sin\omega_r (t_2 - t_1) + k_4 \cos\omega_r (t_2 - t_1). \tag{26}$$

Since v_m is still nv_o in Interval 3, the expression of i_m is the same with (22). To calculate k_5 and k_6, the time t_2 still should be determined. Since t_3 is $1/(2f_{\text{sw}})$, $i_{r,t3}$ and $i_{m,t3}$ can be calculated as follows:

$$i_{r,t_3} = \omega_r C_r \left[-k_5 \sin(\omega_r t_3 - \omega_r t_2) + k_6 \cos(\omega_r t_3 - \omega_r t_2)\right] \tag{27}$$

$$i_{m,t_3} = \frac{nv_o (1 - 4f_{\text{sw}} t_1)}{4L_m f_{\text{sw}}}. \tag{28}$$

Considering $i_{r,t3} = i_{m,t3}$, an equation can be established as

$$\omega_r C_r \begin{bmatrix} -k_5 \sin(\omega_r t_3 - \omega_r t_2) \\ +k_6 \cos(\omega_r t_3 - \omega_r t_2) \end{bmatrix} = \frac{nv_o (1 - 4f_{\text{sw}} t_1)}{4L_m f_{\text{sw}}}. \tag{29}$$

t_2 can be calculated by solving (29). Now, k_5 and k_6 which are the function of t_2 can be calculated. All the equations necessary for the time-domain model in CCM are given.

C. The Operating Principle of Discontinuous Current Mode

The discontinuous current mode (DCM) is the working mode of the *LLC* converter when f_{sw} is lower than f_{r1}. In this mode, L_m resonates with L_r and C_r. The analysis is organized in the same way as CCM.

The waveforms of the *LLC* converter in the normal condition and SR signal delay are depicted in Fig. 8. Compared with the normal condition, a distortion region is formed between i_r and i_m under SR signal delay. i_{sec} crosses the time-axis and its direction flips. However, due to the turn-OFF delay of Q5 and Q8, v_m and v_{sec} remain positive. Thus, a new interval that causes reverse power flow is generated.

Interval 1 [t_0, t_2]*:* Q2 and Q3 turn OFF while Q1 and Q4 turn ON. The equivalent circuits are shown in Fig. 9. The body diodes of Q5 and Q8 turn ON before the rising edge of the SR

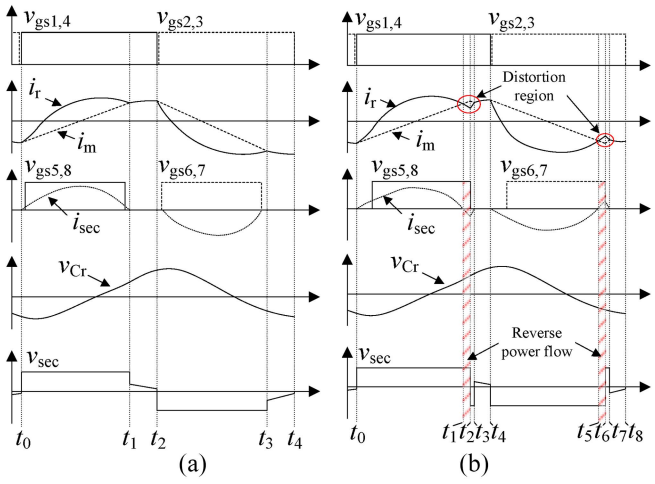

Fig. 8. Operating waveforms comparison of the *LLC* converter in DCM. (a) Under normal condition. (b) Under SR signal delay condition.

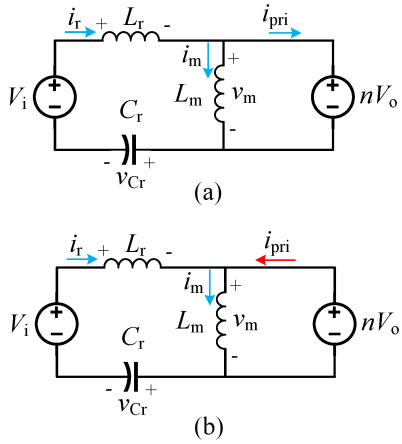

Fig. 9. Equivalent circuit s of DCM in Interval 1. (a) During t_0 and t_1. (b) During t_1 and t_2.

gate drive signals. Thus, the MOSFET turn-ON delay extends the conduction time of the body diode. During t_0 and t_1, as shown in Fig. 8(b), this interval is the same with the normal condition, and the equivalent circuit is shown in Fig. 9(a).

During t_1 and t_2, Q5 and Q8 remain conductive due to the turn-OFF delay. i_m keeps increasing since v_m is still nv_o. For the reason that i_r is lower than i_m, the direction of i_{sec} turns negative. The equivalent circuit during t_1 and t_2 is shown in Fig. 9(b). Therefore, the transformer delivers power from the load side to the resonant tank. This reversed power is undergone by L_m and the peak magnetizing current is higher compared with the normal condition. This interval does not exist in the normal condition.

Referring to the deriving process of CCM, v_{Cr} and i_r can be derived as follows:

$$v_{cr} = k_1 \cos\omega_r t + k_2 \sin\omega_r t + v_i - nv_o \tag{30}$$

$$i_r = \omega_r C_r (-k_1 \sin\omega_r t + k_2 \cos\omega_r t) \tag{31}$$

where k_1 and k_2 are undetermined coefficients depending on the initial condition of the circuit. Referring to the deriving process

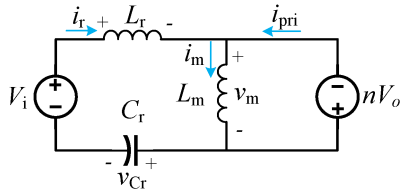

Fig. 10. Equivalent circuit of DCM in Interval 2.

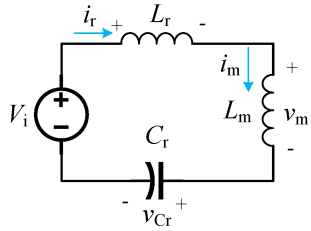

Fig. 11. Equivalent circuit of DCM in Interval 3.

(9)–(17) of CCM, k_1 and k_2 can be derived as

$$k_1 = -\frac{v_o^2}{4\eta R_L f_{sw} v_i C_r} - v_i + nv_o$$
$$k_2 = \frac{k_1 \omega_r C_r L_m \sin \omega_r t_1 + nv_o t_1}{\omega_r C_r L_m (\cos \omega_r t_1 - 1)}. \quad (32)$$

v_m is nv_o in this interval, and $i_{r,t0}$ equals to $i_{m,t0}$, thus i_m can be obtained as

$$i_m = \frac{nv_o}{L_m} t + k_2 \omega_r C_r. \quad (33)$$

Interval 2 [t_2, t_3]*:* Q1 and Q4 remain conductive, while Q5 and Q8 turn OFF. The equivalent circuit of this interval is shown in Fig. 10. Body diodes of Q6 and Q7 turn ON due to the negative i_{sec}, resulting in the transformer voltage flipping. Thus, L_m begins to discharge to the resonant tank and the load side, i_m decreases until the current relationship $i_r = i_m$ is satisfied. However, the voltage of L_r in Interval 2 is higher than in Interval 1, which means higher *di/dt* on L_r in Interval 2. Thus, Interval 2 is usually shorter than Interval 1. The energy extracted from the load side during t_1 and t_2 is more than the energy released to the load side during t_2 and t_3. L_m transfers energy from the load side to the resonant tank in SR signal delay conditions. Combining Interval 2, a distorted region has formed between the waveforms of i_r and i_m. Similarly, v_{Cr} and i_r can be derived as

$$v_{cr} = k_3 \cos \omega_r (t - t_2) + k_4 \sin \omega_r (t - t_2) + v_i + nv_o \quad (34)$$

$$i_r = \omega_r C_r [-k_3 \sin \omega_r (t - t_2) + k_4 \cos \omega_r (t - t_2)]. \quad (35)$$

Since t_2 is the initial time of this interval and the end time of the former interval, combining (30) and (31), and (34) and (35), k_3 and k_4 can be calculated as

$$k_3 = k_1 \cos \omega_r t_2 + k_2 \sin \omega_r t_2 - 2nv_o$$
$$k_4 = -k_1 \sin \omega_r t_2 + k_2 \cos \omega_r t_2. \quad (36)$$

Since v_m is $-nv_o$ in this interval, i_r can be obtained as

$$i_m = -\frac{nv_o}{L_m}(t - t_2) + \frac{nv_o}{L_m} t_2 + k_2 \omega_r C_r. \quad (37)$$

Interval 3 [t_3, t_4]*:* At t_4, i_r equals to i_m and i_{sec} reduces to zero, resulting in the shut-down of the secondary side body diodes. The equivalent circuit of this interval is shown in Fig. 11. However, since the switching period in DCM is longer than a resonant period, Q1 and Q4 keep conductive after i_r equals i_m. Thus, the status $i_r = i_m$ can be maintained until the primary MOSFETs gate signals flip. In this interval, L_m begins to join in resonance since $i_r = i_m$, thus the angular resonant frequency is ω_m which is defined as

$$\omega_m = \frac{1}{\sqrt{(L_r + L_m) C_r}}. \quad (38)$$

In this interval, C_r resonates with L_r and L_m. The voltage equation should be revised as

$$(L_r + L_m) C_r \frac{d^2 v_{cr}}{dt^2} + v_{cr} = v_i. \quad (39)$$

Thus, v_{Cr}, i_r, and i_m can be derived as follows:

$$v_{cr} = k_5 \cos \omega_m (t - t_3) + k_6 \sin \omega_m (t - t_3) + v_i \quad (40)$$

$$i_m = i_r = \omega_m C_r [-k_5 \sin \omega_m (t - t_3) + k_6 \cos \omega_m (t - t_3)]. \quad (41)$$

Combining (34) and (35), the coefficients k_5 and k_6 can be calculated as follows:

$$k_5 = k_3 \cos \omega_r (t_3 - t_2) + k_4 \sin \omega_r (t_3 - t_2) + nv_o$$
$$k_6 = \frac{\omega_r}{\omega_m} [-k_3 \sin \omega_r (t_3 - t_2) + k_4 \cos \omega_r (t_3 - t_2)]. \quad (42)$$

t_4 equals to $1/2f_{sw}$. t_1 can be estimated with the time-domain model in the normal condition since Interval 1 of both conditions is similar. According to Fig. 8(b) and the symmetrical feature of i_m, the following equation can be derived:

$$i_{r,t0} + i_{r,t4} = 0. \quad (43)$$

Referring to the deriving process of (41) and (42) and combining (43), (54) can be established

$$k_2 \omega_r C_r + \omega_m C_r [-a \sin (\omega_m (t_4 - t_1)) + b \cos (\omega_m (t_4 - t_1))] = 0 \quad (44)$$

where

$$a = k_1 \cos \omega_r t_1 + k_2 \sin \omega_r t_1 - nv_o$$
$$b = \left(\omega_r / \omega_m\right) (-k_1 \sin \omega_r t_1 + k_2 \cos \omega_r t_1). \quad (45)$$

Solving (44), t_1 can be obtained. Referring to Fig. 12, t_2 is determined by the SR turn-OFF delay. Thus

$$t_2 = t_1 + \max \{t_{delay} - t_{dead(off)}, 0\}. \quad (46)$$

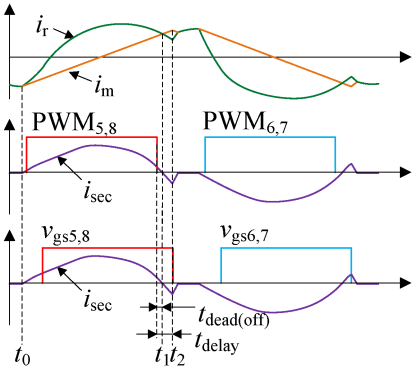

Fig. 12. Relationship between PWM signal and gate driver signal of DCM.

Because $i_{r,t3} = i_{m,t3}$, substituting $t = t_3$ into (35) and (37), t_3 can be obtained as

$$\begin{bmatrix} -k_3 \sin \omega_r (t_3 - t_2) \\ +k_4 \cos \omega_r (t_3 - t_2) \end{bmatrix} = -\frac{nv_o}{L_m \omega_r C_r}(t_3 - t_2) + \frac{nv_o t_2}{L_m \omega_r C_r} + k_2. \tag{47}$$

Now the expressions of all unknown variables associated with the time-domain model are derived. The waveforms in the DCM condition can be plotted via calculation.

D. Operation at the Resonant Frequency

The resonant frequency f_{r1} is the boundary condition between CCM and DCM. The *LLC* converter reaches its peak efficiency when operating at f_{r1} and it can be called the *LLC*–DCX converter in this condition [32]. Fig. 13(a) reveals that the gate signals of the secondary side should be in the same phase as the primary side in the normal condition. The reason is that the time of i_r equals i_m occurs when the primary-side MOSFETs gate signals flip.

Fig. 13(b) shows the waveforms of *LLC*–DCX under SR signal delay. The converter has the characteristics of CCM and DCM simultaneously. Since the (t_0, t_4) waveforms are different from the waveforms (t_6, t_7), 1.5 times switching periods are required for analysis.

Interval 1 [t_0, t_1]*:* Q1 and Q4 turn ON, Q6 and Q7 remain conductive due to the SR signal delay. Thus, i_m keeps increasing after it equals i_r at t_0. This interval is the same as Interval 1 of CCM.

Interval 2 [t_1, t_4]*:* Q1, Q4, Q5, and Q8 turn ON. As shown in Fig. 13(c), in this stage, since the initial resonant current $i_{r,t0}$ is lifted rapidly due to the turn-OFF delay of Q6 and Q7, the magnitude of i_r is not changed, and the frequency of i_r is still f_{r1}. $i_{r,t4}$ is much lower than the normal condition. However, i_m is minorly changed due to the large L_m, so the time of i_r when it equals to i_m occurs earlier than the normal condition. Then, due to the turn-OFF delay of Q5 and Q8, v_m remains nv_o, and i_m keeps increasing. During t_3 and t_4, Q5 and Q8 turn OFF, and i_{sec} decreases to zero, thus L_m begins to resonate with L_r and C_r since secondary-side MOSFETs turn OFF. Therefore, the operating waveforms are similar to DCM. It should be noted that the resonant current of t_4 is lower than the normal condition.

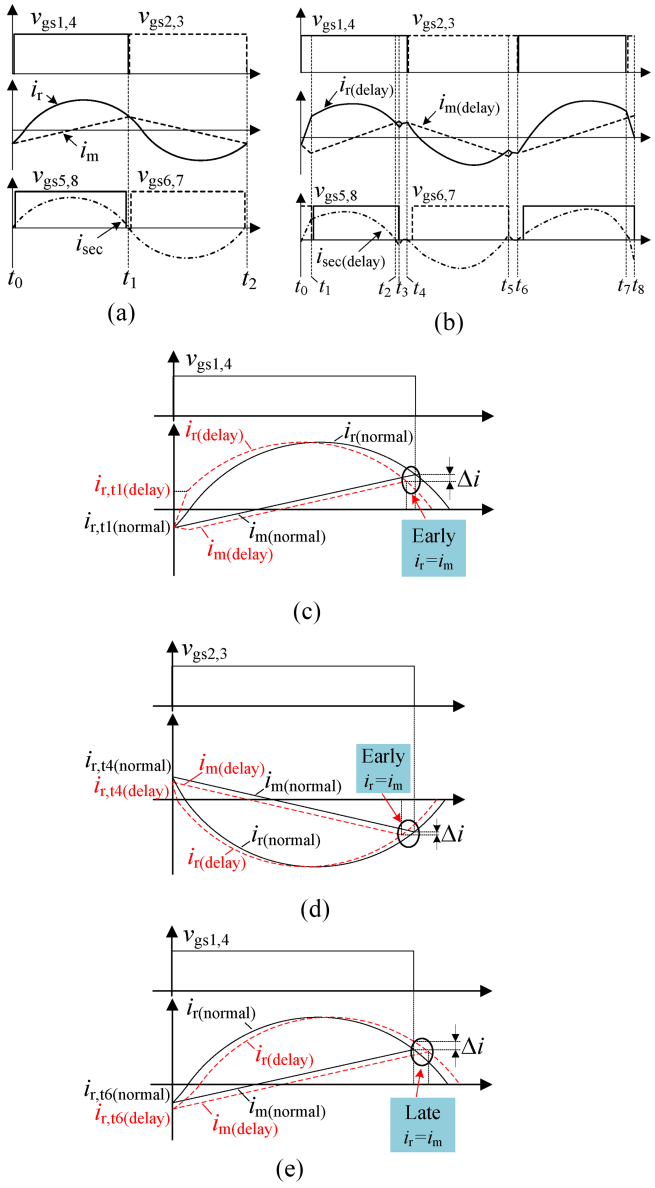

Fig. 13. Operating waveforms of the *LLC*–DCX converter. (a) Waveforms in the normal condition. (b) Waveforms with the SR signal delay. (c) Waveforms formation of Interval 2. (d) Waveforms formation of Interval 3. (e) Waveforms formation of Interval 4.

Interval 3 [t_4, t_6]*:* Q2, Q3, Q6, and Q7 turn ON. Interval 3 is also the negative half-period of resonance. Similarly, since the initial resonant current of this interval is higher than the normal condition, as shown in Fig. 13(d), the intersection point of i_r and i_m occurs earlier than Q2 and Q3 turn-OFF, and the converter remains at DCM. It should be noted that the resonant current of the end time is also lower than the normal condition.

Interval 4 [t_6, t_7]*:* Q1, Q4, Q5, and Q8 turn ON, and the converter begins positive period resonance. Similarly, since the initial resonant current of this interval is lower than the normal condition, the magnitude of i_r is not changed, and the frequency of i_r is still f_{r1}, the end current of i_r is higher than the normal condition. However, i_m is minorly changed due to the large L_m;

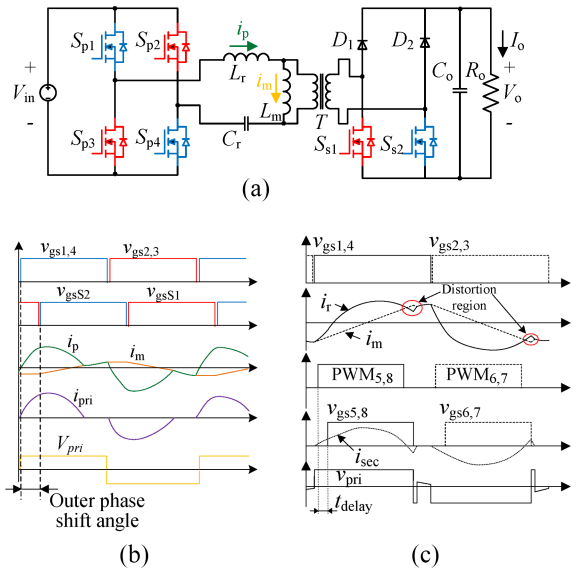

Fig. 14. Comparison between secondary PSM and SR signal delay. (a) Topology of the *LLC* converter under the secondary PSM [36], [37]. (b) Waveforms of *LLC* converter which is shown in (a) under the secondary PSM. (c) Waveforms of *LLC* converter under the SR signal delay.

therefore, the intersection point of i_r and i_m occurs later than Q1 and Q4 turn-OFF, which is shown in Fig. 13(e). Thus, L_m does not resonate with L_r and C_r in this interval, and the working mode of the *LLC* converter returns to CCM.

In conclusion, with the SR signal delay, an *LLC*–DCX bounces between CCM and DCM. Interval 2 and 3 are DCM, while Interval 1 and 4 are CCM. The following 1.5 half-periods will be reversed.

E. The Differences Between the Secondary PSM and the SR Signal Delay

The secondary phase-shift modulation (PSM) of the full-bridge *LLC* converter controls phase delay between the primary MOSFETs and the secondary MOSFETs [25], [36], [37]. The gate drive signal waveforms of the *LLC* converter under secondary PSM and SR signal delay are shown in Fig. 14. Although there is a similarity between the secondary PSM and the delay on the waveforms, the following differences make their impact on the characteristics different.

1) The secondary PS angle is adjustable by the algorithm while the SR signal delay time is caused by the propagation delay of hardware and is uncontrollable.
2) The purpose of applying secondary PSM in the full-bridge *LLC* converter is to synchronize the gate drive signal of secondary-side MOSFETs with the ac current [23], [39] or to realize some specific control target. To avoid the reverse power from the load side to the resonant tank, employing diodes on the secondary side to block the reverse power [36], [37], or turning OFF the secondary MOSFETs before zero current crossing [12], [39], Thus, the state-of-the-art secondary PSM will not cause the turn-OFF delay and reverse power flow, while the SR signal delay will lead to these impacts.

TABLE II
MAIN PARAMETERS OF THE VIRTUAL CONVERTER

Parameter	Values
Input voltage	400 V
Output voltage	200–480 V
Output current	0–12 A
Resonant inductance	10 μH
Resonant capacitance	33 nF
Magnetic inductance	50.26 μH
Transformer ratio	13:10
Resonant frequency	277 kHz
ON-resistance of primary MOSFET ON-resistance of secondary MOSFET	60 mΩ
ON-resistance of body diode	125 mΩ

III. THE IMPACT ANALYSIS OF SR SIGNAL DELAY

In this section, the impact of SR signal delay on the *LLC* converter is quantitatively analyzed using the proposed time-domain model. A simulation study is conducted using PLECS™ with the setup listed in Table II.

A. The Impact on the Voltage Gain

1) CCM: The output energy during a half-switching period is

$$E_o = \int_0^{\frac{1}{2f_{sw}}} v_o i_o dt = \frac{v_o^2}{2R_L f_{sw}}. \tag{48}$$

The input energy can be calculated as

$$E_{in} = \int_0^{\frac{1}{2f_{sw}}} v_i i_r dt. \tag{49}$$

According to energy conservation law, the input energy should be equal to the output energy, i.e., $\eta E_{in} = E_o$. Therefore, the voltage gain M of the *LLC* converter can be expressed in (50). It should be noted that the SR signal delay affects the operation and the efficiency of the converter. However, for estimating the voltage gain of the converter, the impact of the efficiency variation is slight and can be neglected. Thus, the efficiency of normal conditions can be used as

$$M = \frac{2\eta C_r f_{sw} R_L \begin{pmatrix} -k_1 - k_3 - k_5 + k_1 \cos\varphi_1 + \\ k_3 \cos(\varphi_2 - \varphi_1) + k_5 \cos(\varphi_3 - \varphi_2) \\ + k_2 \sin\varphi_1 + k_4 \sin(\varphi_2 - \varphi_1) \\ + k_6 \sin(\varphi_3 - \varphi_2) \end{pmatrix}}{v_o} \tag{50}$$

where $\omega_r t_1 = \varphi_1$, $\omega_r t_2 = \varphi_2$, $\omega_r t_3 = \varphi_3$, and $\omega_r t_4 = \varphi_4$. k_1 to k_6 can be obtained referring to the model driving process of CCM.

With (50), the impact of the SR signal delay on the voltage gain of the *LLC* converter in CCM can be quantified as plotted in Fig. 15. It reveals that the SR signal delay will increase the voltage gain. Fig. 16 shows that the peak value of i_m increases with t_{delay}. It can validate the analysis in Section II which demonstrates that the overcharge of L_m caused by the SR signal delay is the major reason for the voltage gain increment.

2) DCM: Similarly, the relationship between input and output voltage can be established. The output energy during a

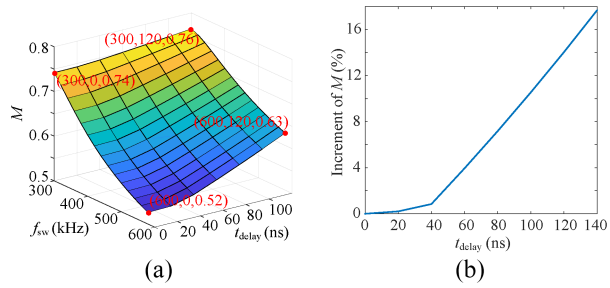

Fig. 15. Impact of the SR signal delay on the voltage gain of the *LLC* converter in CCM. (a) Voltage gain vs. t_{delay} under different f_{sw}. (b) Increment of voltage gain vs. $t_{\mathrm{delay}}, f_{\mathrm{sw}} = 480$ kHz. $t_{\mathrm{dead(OFF)}}$ is 37 ns.

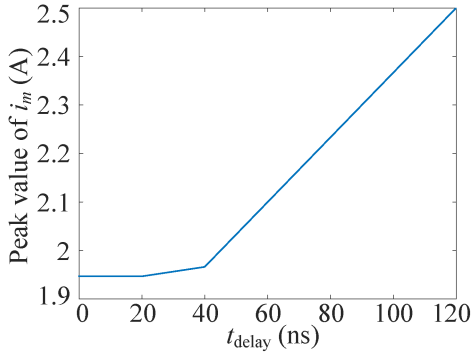

Fig. 16. Peak value of i_{m} vs. $t_{\mathrm{delay}}, f_{\mathrm{sw}} = 480$ kHz.

half-switching period is given as

$$E_o = \int_0^{\frac{1}{2f_{\mathrm{sw}}}} v_o i_o dt = \frac{v_o^2}{2R_L f_{\mathrm{sw}}}. \tag{51}$$

The input energy can be calculated as

$$E_{\mathrm{in}} = \int_0^{\frac{1}{2f_{\mathrm{sw}}}} v_i i_r dt. \tag{52}$$

Since $\eta E_{\mathrm{in}} = E_o$, the voltage gain M of the *LLC* converter can be calculated as

$$M = \frac{2\eta C_r f_{\mathrm{sw}} R_L \begin{pmatrix} -k_1 - k_3 - k_5 + k_5 \cos(\theta_4 - \theta_3) \\ +k_1 \cos\varphi_2 + k_3 \cos(\varphi_3 - \varphi_2) \\ +k_6 \sin(\theta_4 - \theta_3) \\ +k_2 \sin\varphi_2 + k_4 \sin(\varphi_3 - \varphi_2) \end{pmatrix}}{v_o} \tag{53}$$

where $\omega_m t_1 = \theta_1$, $\omega_m t_2 = \theta_2$, $\omega_m t_3 = \theta_3$, and $\omega_m t_4 = \theta_4$.

Coefficients k_1–k_6 can be obtained referring to the model driving process of DCM.

In DCM, the impact of SR signal delay on the voltage gain under different switching frequency can be calculated and depicted in Fig. 17. It reveals that the SR signal delay time is in negative correlation with the voltage gain, which means that the SR signal delay will reduce the voltage gain. It should be noted that this phenomenon is opposite to CCM. The reason is still the magnetizing inductor. The analysis of the operating principle of DCM in Section II revealed the energy stored in L_m from the load side during t_1 and t_2 is more than the energy feedback to the

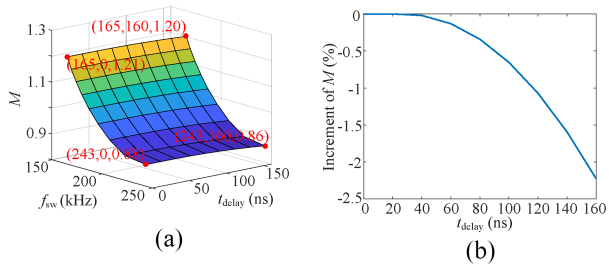

Fig. 17. Impact of the SR signal delay on the voltage gain of the *LLC* converter in DCM. (a) Voltage gain vs. t_{delay} under different f_{sw}. (b) Increment of voltage gain vs. $t_{\mathrm{delay}}, f_{\mathrm{sw}} = 180$ kHz. $t_{\mathrm{dead(OFF)}}$ is 37 ns.

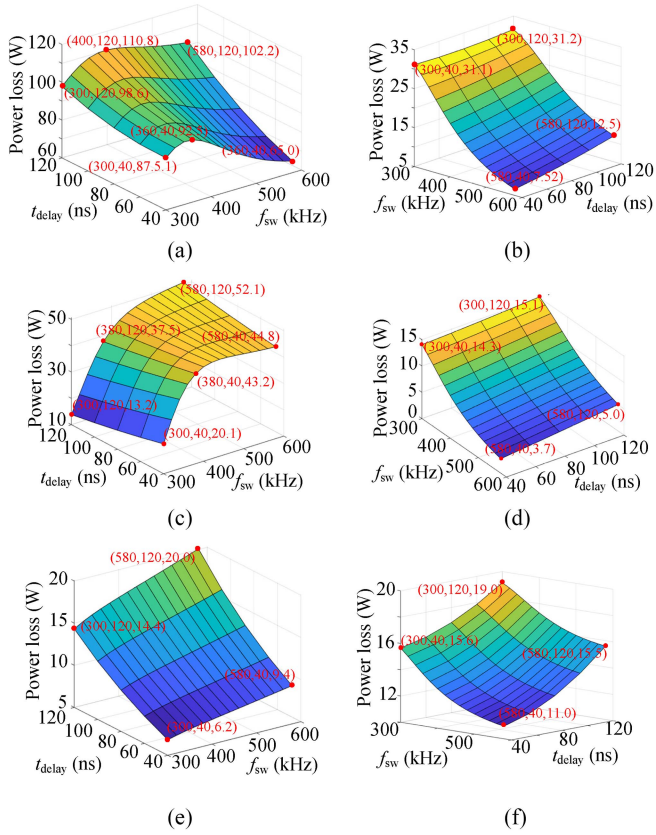

Fig. 18. Impact of SR delay on the power loss of MOSFETs under CCM. (a) Total power loss of MOSFETs. (b) Conduction loss of the primary-side MOSFETs. (c) Switching loss of the primary-side MOSFETs. (d) Conduction loss of the secondary-side MOSFETs. (e) Switching loss of the secondary-side MOSFETs. (f) Conduction loss of the secondary-side body diodes.

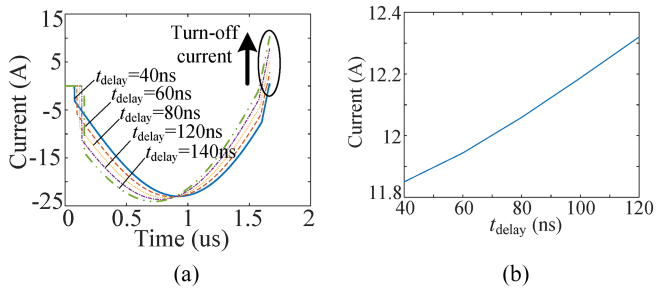

Fig. 19. Current of the secondary-side MOSFET in CCM. (a) Current waveforms under different t_{delay}. (b) RMS current vs. $t_{\mathrm{delay}}, f_{\mathrm{sw}} = 300$ kHz.

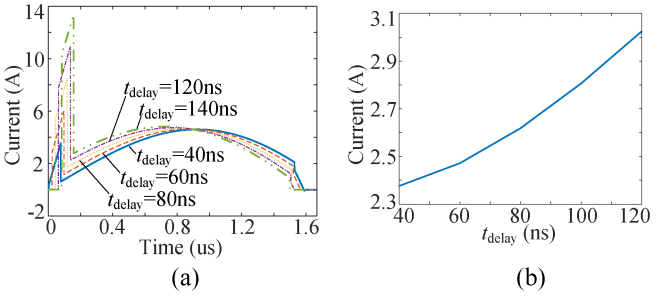

Fig. 20. Current of secondary-side body diode in CCM. (a) Current waveforms under different t_{delay}. (b) RMS current vs. $t_{\mathrm{delay}}, f_{\mathrm{sw}} = 300$ kHz.

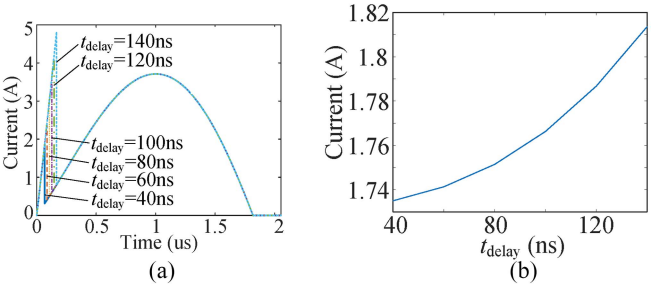

Fig. 23. Current of the secondary body diode in CCM. (a) Current waveforms under different t_{delay}. (b) RMS current vs. $t_{\mathrm{delay}}, f_{\mathrm{sw}} = 243$ kHz.

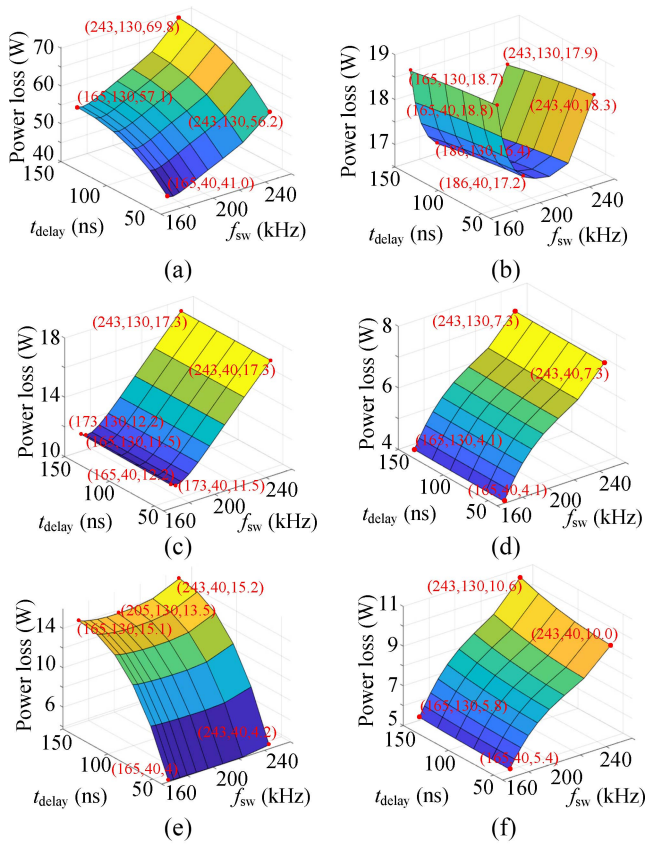

Fig. 21. Impact of SR delay on the power loss of MOSFETs under DCM. (a) Total power loss of MOSFETs. (b) Conduction loss of the primary-side MOSFETs. (c) Switching loss of the primary-side MOSFETs. (d) Conduction loss of the secondary-side MOSFETs. (e) Switching loss of the secondary-side MOSFETs. (f) Conduction loss of the secondary-side body diodes.

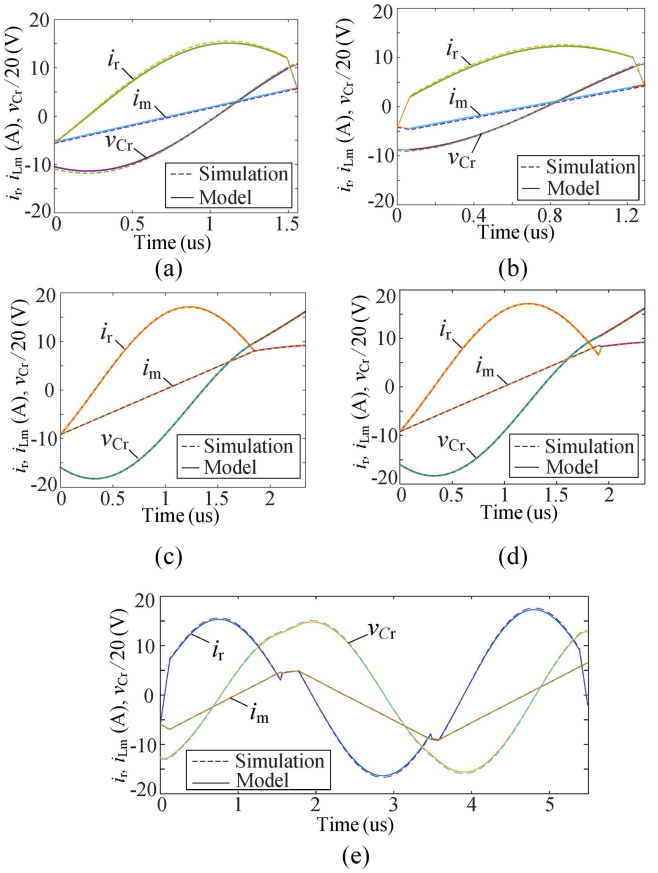

Fig. 24. Waveforms comparison between simulation and proposed model. (a) Under CCM, $t_{\mathrm{delay}} = 0$. (b) Under CCM, $t_{\mathrm{delay}} = 100$ ns. (c) Under DCM, $t_{\mathrm{delay}} = 0$. (d) Under DCM, $t_{\mathrm{delay}} = 100$ ns. (e) Under resonant frequency, $t_{\mathrm{delay}} = 100$ ns.

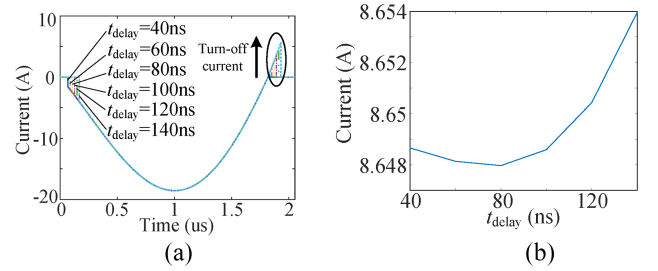

Fig. 22. Current of the secondary-side MOSFET in DCM. (a) Current waveforms under different t_{delay}. (b) RMS current vs. $t_{\mathrm{delay}}, f_{\mathrm{sw}} = 243$ kHz.

load side during t_2 and t_3. This energy is provided by the output filter capacitor. Without SR delay, the output filter discharges energy to load. In contrast, with SR signal delay, the output filter capacitor discharges energy to the load and resonant tank simultaneously. Hence, the voltage gain falls. Moreover, longer t_{delay} means that L_m extracts more energy from the output filter to the resonant tank and the voltage gain is reduced. However, according to the previous analysis, L_m will release a part of energy back to the load side under DCM, thus the impact of SR signal delay on the voltage gain in DCM is lower compared with CCM.

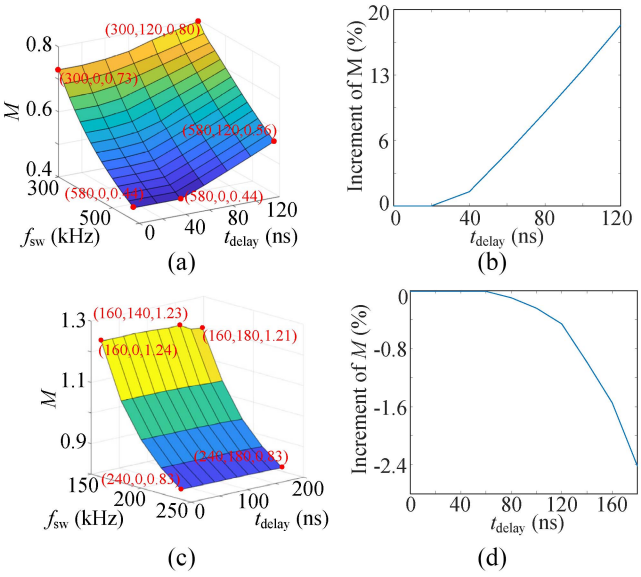

Fig. 25. Simulation results of the impact of the SR signal delay on the voltage gain of the *LLC* converter. (a) Voltage gain of CCM under different $f_{\rm sw}$. (b) Increment of voltage gain of CCM vs. $t_{\rm delay}$ at 320 kHz. (c) Increment of voltage gain of DCM under different $f_{\rm sw}$. (d) Voltage gain vs. $t_{\rm delay}, f_{\rm sw} = 167$ kHz.

TABLE III
PARAMETERS OF THE DESIGNED *LLC* CONVERTER PROTOTYPE

Parameters	Values
Input voltage	147 V
Output voltage	89–154 V
Output current	0–4.67 A
Load	23.33–55 Ω
Primary SiC-MOSFET Secondary SiC-MOSFET	C3M0060065D
Transformer ratio	13:10
Current transformer ratio	1:30
Resonant inductance	10 μH
Resonant capacitance	33 nF
Magnetizing inductance	50.26 μH

3) Operation at the Resonant Frequency: According to the previous analysis, the working mode of an *LLC*–DCX converter will bounce between CCM and DCM when the SR signal delay exists, thus it is hard to give the analytical solution of voltage gain. Since the impact of SR signal delay under CCM on the voltage gain is different from the DCM, the voltage gain will fluctuate, and the output voltage ripple increases. It is challenging for voltage closed-loop control implementation.

B. The Power Loss Calculation of mosfets

The power loss of the primary-side MOSFETs contains conduction and switching loss. Conduction loss is related to the ON-resistance of MOSFET and the current. Due to the zero-voltage switching of the primary-side MOSFETs, the turn-ON loss can be ignored while only turn-OFF power loss should be considered. Therefore, the power loss of the primary-side MOSFETs can be calculated as [38]

$$P_{\rm pri\_mos} = 4\left[E_{\rm off}\left(v_{\rm in}, i_{s\_{\rm off}}\right) f_{\rm sw} + I^2_{\rm rms\_mos} R_{\rm ds(on)}\right] \quad (54)$$

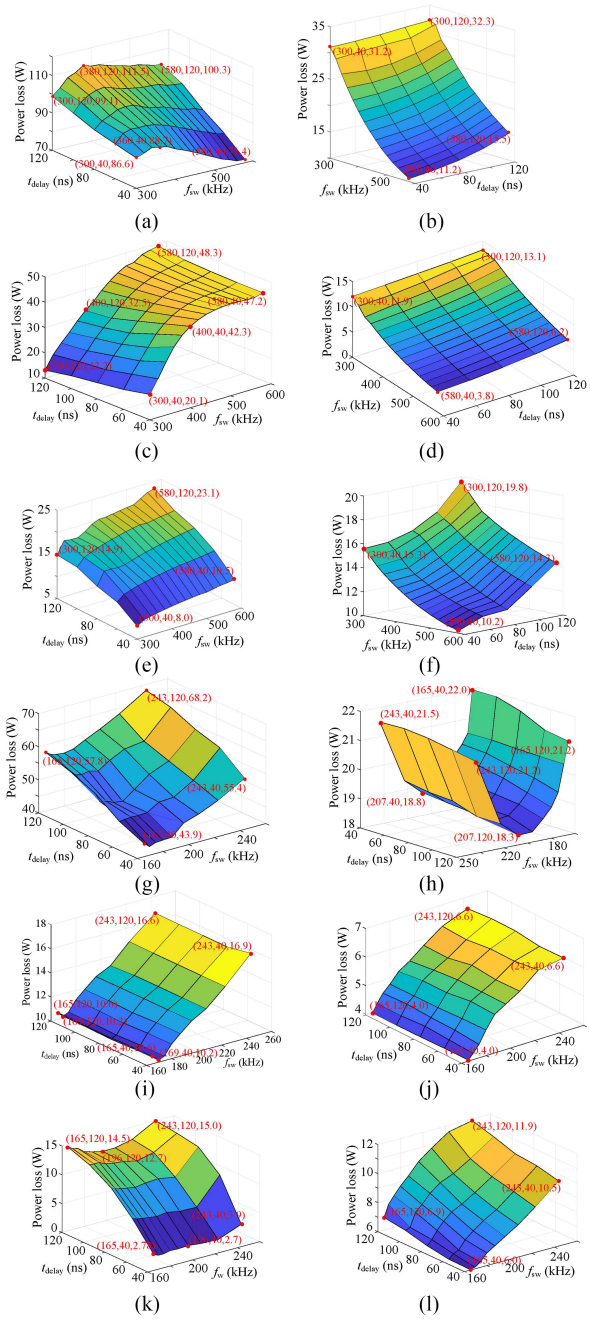

Fig. 26. Simulation results of power loss of MOSFETs. (a) Total power loss in CCM. (b) Conduction loss of primary-side MOSFETs in CCM. (c) Switching loss of primary-side MOSFETs in CCM. (d) Conduction of secondary-side MOSFETs in CCM. (e) Switching loss of secondary-side MOSFET in CCM. (f) Conduction loss of secondary-side body diodes in CCM. (g) Total power loss in DCM. (h) Conduction loss of primary-side MOSFETs in DCM. (i) Switching loss of primary-side MOSFETs in DCM. (j) Conduction of secondary-side MOSFETs in DCM. (k) Switching loss of secondary-side MOSFET in DCM. (l) Conduction loss of secondary-side body diodes in DCM.

where $E_{\rm OFF}(v_{\rm in}, i_{s\_{\rm OFF}})$ is the turn-OFF energy of MOSFET, which is related to the voltage $v_{\rm in}$ of MOSFET and turn-OFF current $i_{s\_{\rm OFF}}$. $f_{\rm sw}$ is the switching frequency; $I_{\rm rms\_mos}$ is the rms current of MOSFET; and $R_{\rm ds(ON)}$ is the ON-resistance of MOSFET.

For the secondary-side MOSFETs, the conduction loss of the body diode needs to be considered since the delay of SR will

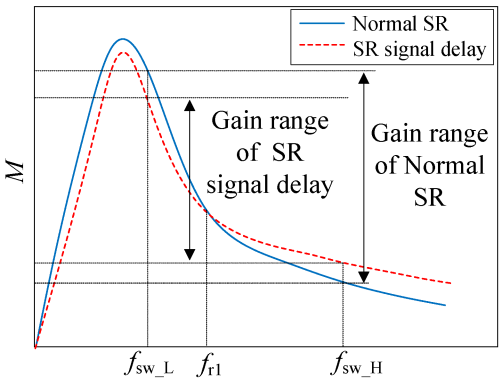

Fig. 27. Impact of the SR signal delay on the voltage gain characteristic of the *LLC* converter.

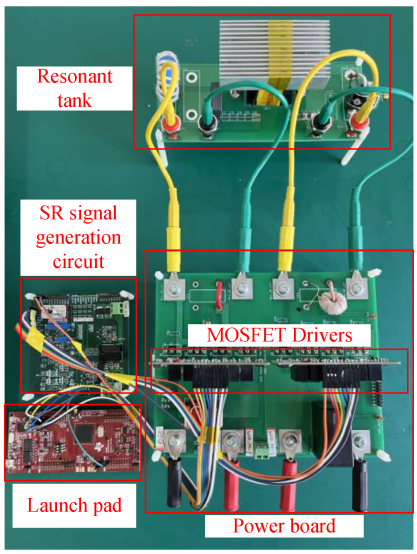

Fig. 28. *LLC* converter experimental prototype.

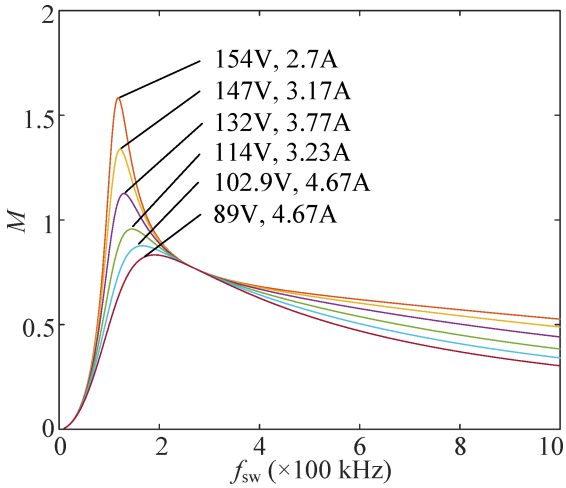

Fig. 29. Voltage gain curves of the designed *LLC* converter.

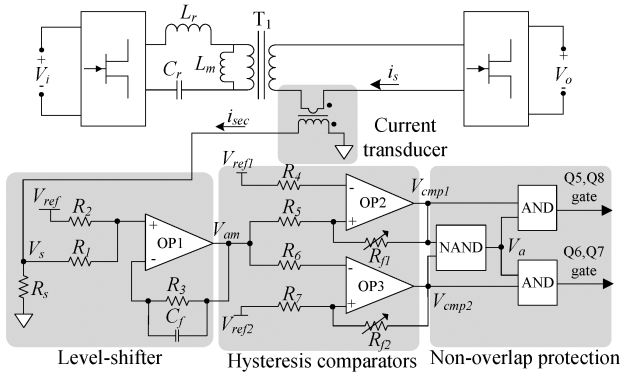

Fig. 30. Schematics of introduced SR signal generation module [39].

extend the conduction time of the body diode. Thus, the power loss of the body diode can be calculated as [38]

$$P_{\text{sec\_mos}} = 4\begin{bmatrix} E_{\text{off}}\left(v_{\text{in}}, i_{s\_\text{off}}\right) f_{\text{sw}} + I^2_{\text{rms\_mos}} R_{\text{ds(on)}} \\ + I^2_{\text{rms\_bd}} R_{\text{bd(on)}} \end{bmatrix} \quad (55)$$

where $I_{\text{rms\_bd}}$ is the rms current of the body diode; and $R_{\text{bd(ON)}}$ is the ON-resistance of the body diode.

C. The Analysis of mosfet Power Loss Under the SR Signal Delay

1) CCM: In CCM, the impact of SR signal delay on the power loss of MOSFETs under different f_{sw} is plotted in Fig. 18. As shown in Fig. 18, the power loss of the secondary-side MOSFETs is greatly influenced by the SR signal delay since the switching loss of MOSFETs and the conduction loss of body diodes also increase dramatically. For the switching loss of the secondary-side MOSFETs, the SR signal delay can make the secondary-side MOSFETs operate out of the zero-current switching (ZCS) range. Longer t_{delay} results in higher turn-OFF current, which is shown in Fig. 19(a), and higher switching power loss. For the conduction loss of the body diodes, SR signal delay results in the increment of rms current of the body diode, which is shown in Fig. 20(b). Thus, the conduction loss of the secondary-side body diodes increases. In contrast, the rms current of the secondary-side MOSFETs is not changed greatly, and the impact of SR signal delay on the conduction loss of secondary MOSFET is low if the SR delay time takes a small proportion of a switching period.

2) DCM: The impact of the SR signal delay on the power loss of MOSFETs under different f_{sw} is shown in Fig. 21. Similarly, the power loss of the secondary-side MOSFETs is influenced by the SR signal delay most significantly. For switching loss of secondary-side MOSFETs, Fig. 22(a) reveals that the turn-OFF current of secondary-side MOSFET rises with t_{delay}, thus the secondary-side MOSFETs are out of ZCS range now, and their switching loss increased dramatically. For the conduction loss of the secondary-side MOSFETs, Fig. 23(b) shows that the change of the secondary-side rms current is not critical, thus the delay has barely influence on the conduction loss. However, due to the lower output voltage when the *LLC* converter operates at DCM, the conduction loss of the body diode under DCM is less than in CCM.

D. Simulation Study

The waveforms of the *LLC* converter under CCM and DCM are shown in Fig. 24. It can verify the accuracy of the proposed

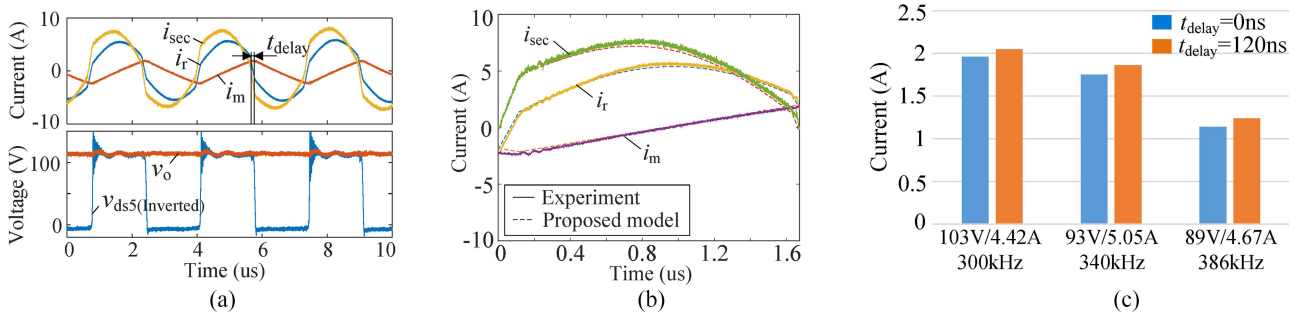

Fig. 31. Waveforms of the *LLC* converter which operates at CCM. (a) Experimental waveforms with SR signal delay, f_{sw} at 300 kHz. (b) Comparison between experimental waveforms and waveforms of proposed model. (c) Comparison of peak values of i_m between under normal SR and under SR signal delay.

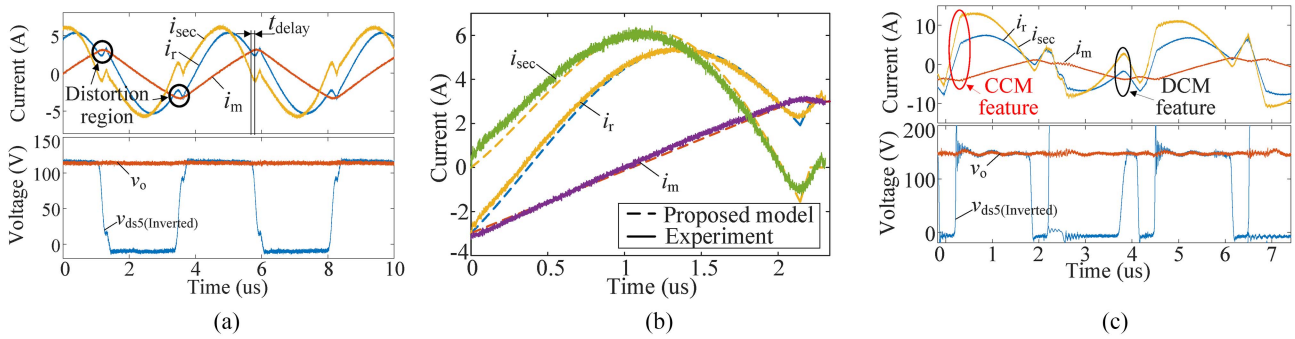

Fig. 32. Waveforms of the *LLC* converter which operates at DCM and at resonant frequency with SR signal delay. (a) Experimental waveforms, f_{sw} at 230 kHz, $t_{delay} = 120$ ns. (b) Comparison between experimental waveforms and waveforms of proposed model. (c) Experimental waveforms, f_{sw} at resonant frequency.

time-domain model since the predicted waveforms are matched with the simulation results under different t_{delay}.

The simulation results of voltage gain are shown in Fig. 25. Combined with Figs. 15, 17, and 25, the gain values given by the simulation and the constructed model are close and the trend is matched.

1) For CCM, the voltage gain is positively correlated with t_{delay} under different f_{sw}.
2) For DCM, the voltage gain is negatively correlated with t_{delay} under different f_{sw}.

The explanations can be given by analyzing the operating principle. The simulation results of the MOSFETs power loss under CCM and DCM are depicted in Fig. 26. It should be noted that there is a discrepancy between the simulation results and the theoretical analysis results, the reason is the simulation contains the change of junction temperature which will affect the R_{dsON}, E_{ON}, and E_{OFF} of the MOSFET. However, the time-domain model will be overcomplex if the junction temperature of the MOSFET is considered. Therefore, the proposed model uses the value of R_{dsON}, E_{ON}, and E_{OFF} of the MOSFET at $T_j = 25$ °C. However, it can be seen that the trends of the simulation and proposed model are matched. The impact of SR delay on the voltage gain and MOSFET power loss of an *LLC* converter can be summarized as follows.

1) For the operation of the *LLC* converter, in CCM and DCM, two new working stages will emerge. When the *LLC* converter operates at f_{r1}, the working mode of the converter will bounce between CCM and DCM.
2) For the voltage gain of the *LLC* converter, the impact of SR signal delay is different in CCM and DCM. For CCM, the delay will increase the voltage gain significantly. In contrast, the voltage gain of DCM will be decreased. Therefore, the gain curve of the *LLC* converter under SR signal delay is flatter as shown in Fig. 27. The output voltage range is narrower for the *LLC* converter if the frequency range is fixed. For the *LLC*–DCX converter, the unstable working mode can cause unstable voltage gain, thus the ripple of the output voltage will increase.
3) The SR MOSFETs are turned OFF after the zero-crossing point of the secondary-side current due to the SR signal delay, so ZCS cannot be achieved. Moreover, longer t_{delay} will increase the turn-OFF current of the SR MOSFETs.
4) The conduction loss of the body diode and the switching loss of SR MOSFET are significantly increased by SR signal delay. However, SR signal delay does not have a critical impact on the power loss of primary MOSFET.

IV. Experimental Validation

A. Introduction of the Experimental Prototype

To verify the aforementioned theoretical analysis, an experimental prototype using silicon carbide MOSFETs is built as shown in Fig. 28. The specs are listed in Table III. Its designed gain curves are plotted in Fig. 29. In this article, the SR MOSFETs are driven by measuring the secondary-side current. An analog/digital mixed signal circuit as shown in Fig. 30 is

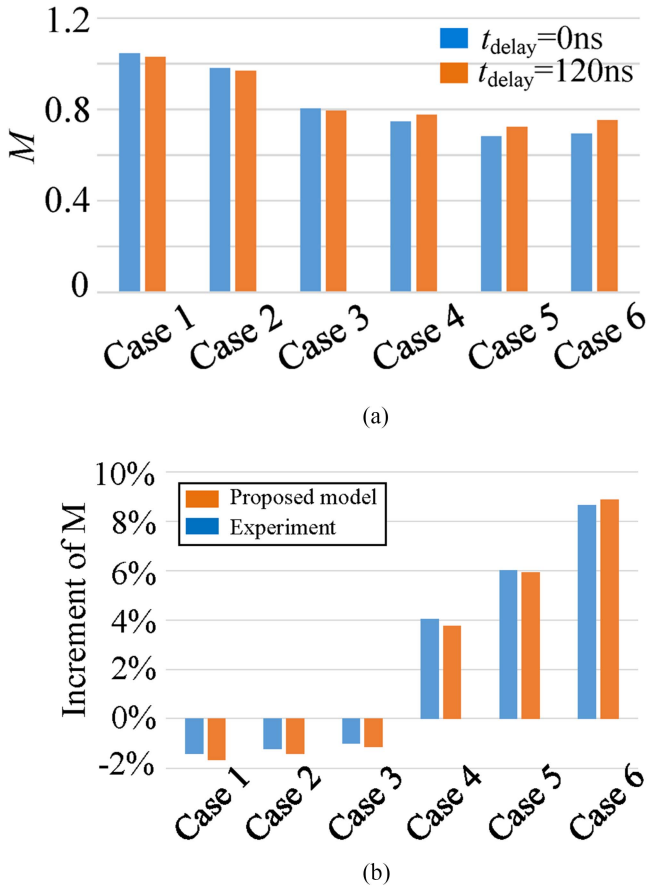

Fig. 33. Comparison of the voltage gain between normal SR and SR signal delay under different operating cases. (a) Voltage gain under different operating cases and different $t_{\rm delay}$. (b) Comparison of gain increment between proposed model and experiment under $t_{\rm delay}$ = 120 ns. Case 1: 154 V/2.70 A; case 2: 144 V/3.17 A; case 3: 114 V/3.23 A; case 4: 103 V/4.42 A; case 5: 93 V/5.05 A; case 6: 89 V/4.67 A.

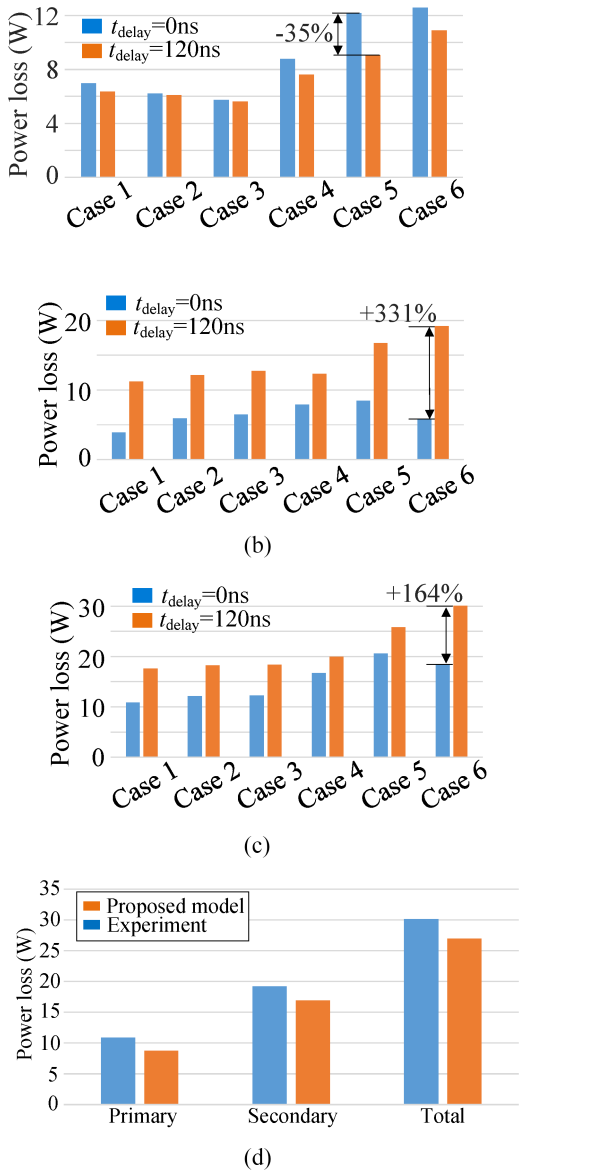

Fig. 34. The comparison of power loss of MOSFETs between normal SR and SR signal delay under different operating cases. (a) Power loss of the primary-side MOSFETs. (b) Power loss of the secondary-side MOSFETs. (c) Total MOSFETs power loss. (d) Comparison between experiment and proposed model at case 6. Case 1: 154 V/2.70 A; case 2: 144 V/3.17 A; case 3: 114 V/3.23 A; case 4: 103 V/4.42 A; case 5: 93 V/5.05 A; case 6: 89 V/4.67 A.

proposed to generate the SR gate signal [40]. The total SR signal delay time is around 120 ns, and the proportion of the delay time during the switching period is within 7%.

B. *The Impact of SR Signal Delay on the* LLC *Converter*

1) Operation Status: The experimental waveforms of the *LLC* converter operating in CCM with SR delay are shown in Fig. 31. It can validate the accuracy of the proposed time-domain model, and figure out that the SR signal delay can cause extra charge on L_m, thus the voltage gain is boosted.

The experimental waveforms of DCM and resonant frequency mode with SR signal delay are plotted in Fig. 32. Fig. 32(a) proves that the magnetizing inductor delivers energy from the load side to resonant rank, thus the voltage gain declines. The accuracy of the proposed time-domain model is proved by Fig. 32(b). Fig. 32(c) reveals that the working mode of the *LLC* converter bounces between CCM and DCM. Since the impact of SR signal delay on voltage gain in CCM is opposite to the impact in DCM, the voltage gain is unstable. Thus, the ripple of output voltage increases. It should be noted that when an *LLC* converter

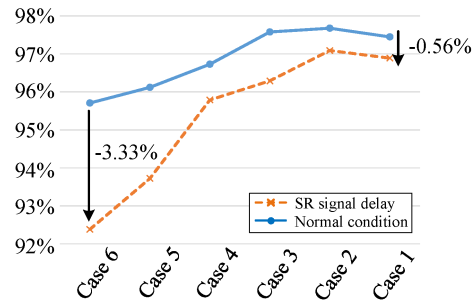

Fig. 35. Efficiency of the *LLC* converter under normal operating condition and the SR signal delay. Case 1: 154 V/2.70 A; case 2: 144 V/3.17 A; case 3: 114 V/3.23 A; case 4: 103 V/4.42 A; case 5: 93 V/5.05 A; case 6: 89 V/4.67 A.

TABLE IV
SUMMARY OF THE IMPACT OF THE SR SIGNAL DELAY ON THE *LLC* CONVERTER

Characteristics	Working mode		Impact
	CCM	DCM	
Working stage	Two new working stages will emerge.		The delay will cause the reverse power from the load side to the resonant tank and affect the voltage gain.
Voltage gain	Positive corelative with SR signal delay. SR signal delay will increase the voltage gain rapidly.	Negatively corelative with the SR signal delay. SR signal delay will decrease the voltage gain minorly.	The SR signal delay shrinks the output voltage range of the *LLC* converter.
Power loss of MOSFETs	Positively corelative with SR signal delay. The SR MOSFETs cannot achieve ZCS. The switching loss of secondary MOSFETs rises rapidly. The total power loss of MOSFETs rises.		Increase the pressure of junction temperature control

operates at DCM, there is an oscillation after the secondary-side MOSFETs turn OFF. It is caused by the parasitic capacitance of the transformer and the output capacitance of MOSFETs [41]. It can lead to repeated secondary-side current zero-crossing.

2) Voltage Gain: The impact of the SR signal delay on the voltage gain of the *LLC* converter is depicted in Fig. 33. When the t_{delay} on the switching period is within 7%, in DCM, SR signal delay only increases the voltage gain by 2% which is very low. However, in CCM, the SR delay causes voltage gain to increase rapidly, and the increment of voltage gain is positively correlated with the frequency when the SR signal delay time is constant. The results are consistent with theoretical analysis and the simulation. The discrepancy between the results of the proposed model and the results of the experiment is minor, which proves the accuracy of the proposed model.

3) The Power Loss of MOSFETs: The measured power loss is shown in Fig. 34 which reveals that the SR signal delay decreases the power loss of primary MOSFETs minorly; however, the power loss of the secondary-side MOSFETs increases greatly. In other words, the total power loss of MOSFETs is increased by the SR signal delay. The experimental results are consistent with the theoretical analysis and the simulation. Note that the power loss of the secondary-side MOSFETs under SR signal delay is three times of the normal operating conditions, which greatly raises the thermal stress of the secondary-side MOSFETs. Fig. 34(d) shows that the proposed model can estimate the power loss of the MOSFET when SR signal delay exists.

4) The Efficiency of the LLC *Converter:* The comparison of the converter efficiency between normal conditions and under SR signal delay is shown in Fig. 35. Since the SR signal delay will increase the total MOSFETs' power loss, the converter's efficiency is significantly decreased by the SR signal delay. Moreover, since the impact of the delay on the power loss of the MOSFET is more significant under the higher operating frequency of the converter, the efficiency at the minimum output voltage will be much worse.

C. Discussion

This article has comprehensively analyzed the impact of SR signal delay on the high-frequency *LLC* converter. The impact of SR signal delay can be summarized as follows.

1) SR signal delay can lead to two new working stages of the *LLC* converter. They will trigger reverse power from the load side to the resonant tank, which will affect the voltage gain of the *LLC* converter.
2) The influence of SR signal delay on the voltage gain is associated with the working mode, i.e., CCM, DCM, and DCX.
3) The voltage gain of CCM is significantly affected by the SR delay time, while that of DCM is barely impacted.
4) In all working modes of the *LLC* converter, the SR signal delay will increase the power loss of the secondary-side MOSFETs.

The details of the impact of the SR signal delay are summarized in Table IV.

V. CONCLUSION

Due to the input-to-output propagation delay of hardware, the gate driver signal of the rectifier can lag behind the secondary-side ac current. The SR signal delay will result in the turning-OFF lagging of the secondary-side MOSFETs, which can raise some abnormal working modes. This article comprehensively analyzes the operation process of the *LLC* converter and derives the time-domain model under SR signal delay. Then, the voltage gain and the power loss of MOSFETs are quantitively estimated for studying the impact of SR signal delay on the *LLC* converter. The correctness of the theoretical analysis results is verified by the simulation and experimental study.

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