Automatic Digital Optimization Design of Synchronous Rectification Buck Converter

Shufan Dong, Quanming Luo, *Member, IEEE*, Mengjia Wei, Guolin Lai, Jian Chen, Pengju Sun, *Member, IEEE*, and Xiong Du, *Member, IEEE*

***Abstract*—The loss and volume of the synchronous buck converter are influenced by various circuit parameters such as switching frequency, inductor, and dead time. However, their impact on the loss and volume has not been comprehensively analyzed and evaluated. To investigate and assess the loss and volume of synchronous buck converter over a wide load range, an automatic digital optimization design method is proposed in this article. First, the process established a complete circuit analytical model based on various operating conditions. Then, with the developed analytical model, the methodology is developed to comprehensively evaluate the loss and volume of the converter and investigate the impacts of the above-mentioned factors. Experimental results demonstrate that the proposed method can accurately predict the effects of switching frequency and inductor on the converter's efficiency and power density. Moreover, the method is effective in optimizing dead time. The proposed analysis and method provide guidance and a foundation for the parameter optimization and design of the synchronous buck converter.**

***Index Terms*—Dead time optimization, parameter design, synchronous buck converter.**

I. Introduction

THE synchronous buck converter, characterized by its high efficiency, high power density, and superior dynamic response [1], [2], [3], is extensively utilized in low-voltage and high-current applications such as data center power supply, rapid battery charging, and point of load converters [4], [5], [6], [7]. Although the structure of the synchronous buck converter is relatively simple, it is necessary to carefully design circuit parameters such as switching frequency, inductor, and dead time under different operating conditions to achieve high efficiency and power density. Moreover, to attain more compact and efficient converters, GaN devices characterized by fast switching speeds and low ON-resistances emerge as optimal selections for power applications.

Accurate time-domain models can predict circuit loss and provide a basis for optimizing and designing parameters. Most of the articles regard the power switch as an ideal switch, ignoring the switching transient process, establishing a steady-state model when the power switch is in ON-state or OFF-state [8], [9]. The model relying on an ideal switch simplifies analysis but results in imprecise loss calculation. Therefore, it is essential to establish a more refined model capable of describing the transient process of the power switch. In [10] and [11], an analytical model of low-voltage eGaN HEMTs when the power switch is in the process of turning ON or turning OFF is proposed, taking into account the parasitic inductor of printed circuit board (PCB) traces, nonlinear capacitors of switches, and nonlinear transconductance. However, since this model neglects inductor current ripple, it is only applicable when the converter operates in continuous conduction mode (CCM). In [12], a switching transient model under triangular current mode (TCM) is proposed, but only the transient processes after the main switch is turned OFF, which lacks completeness. In [13], a multitime-scale analytical model for zero-voltage switching (ZVS) synchronous buck converter is proposed, which merges the switching steady-state model and transient model based on the continuity of state variables. However, this model is only suitable for ZVS. This article proposes a comprehensive converter analytical model that is applicable to all operating conditions of the synchronous buck converter. A comparison between the proposed model and existing models is shown in Table I.

For the parameter design of synchronous buck converter, most research focuses on improving the converter's efficiency. The work in [14] and [15] investigated the impact of switching frequency and inductor on circuit loss of the CCM buck converter. In [16] and [17], the switching frequency has been optimized to improve the efficiency of the converter. In [18], the dead time has been optimized through an analysis of capacitor charging and discharging in the equivalent circuit. The range of inductance is calculated based on ripple constraints, which is a method commonly adopted in many studies. However, little attention has been given to the influence of inductance within ripple limits on the performance of the converter. The switching frequency has a significant impact on the converter, but it has not received more attention during the design phase. In addition to research focusing on dead time optimization, other research on parameter design does not pay special attention to dead time. Therefore,

Manuscript received 5 March 2024; revised 3 June 2024; accepted 17 July 2024. Date of publication 22 July 2024; date of current version 4 September 2024. This work was supported by the Natural Science Foundation of China under Grant 52177170. Recommended for publication by Associate Editor M. Hartmann. *(Corresponding author: Quanming Luo.)*

Shufan Dong, Quanming Luo, Mengjia Wei, Guolin Lai, Pengju Sun, and Xiong Du are with the State Key Laboratory of Power Transmission Equipment and System Security and New Technology, School of Electrical Engineering, Chongqing University, Chongqing 400044, China (e-mail: 20183509@cqu.edu.cn; lgm394@cqu.edu.cn; 202011021085t@cqu.edu.cn; 20193408@cqu.edu.cn; spengju@cqu.edu.cn; duxiong@cqu.edu.cn).

Jian Chen is with the School of Electrical Engineering, Southwest Jiaotong University, Chengdu 611756, China (e-mail: chenjian@swjtu.edu.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3431883.

Digital Object Identifier 10.1109/TPEL.2024.3431883

TABLE I
COMPARISONS OF THE EXISTING MODELS

Models	Available topology	Scale	Accuracy
Model in [8] and [9]	CCM buck	Switching steady-state	Low accuracy
Model in [10] and [11]	CCM buck	Switching transient	High accuracy but only for CCM
Model in [12]	TCM buck	Switching steady-state and switching transient	High accuracy but incompleteness
Model in [13]	TCM buck	Switching steady-state and switching transient	High accuracy but only for ZVS
The proposed model	CCM buck/TCM buck	Switching steady-state and switching transient	High accuracy and suitability for all operating conditions, with the capability for automatic operating condition recognition

for the efficiency optimization of synchronous buck converters, there is currently a lack of optimization and design that comprehensively considers switching frequency, inductor, and dead time. There are few studies on parameter design to improve the power density of converters. They mainly focus on using magnetic integration and planar inductor technology to reduce the inductor volume to achieve the purpose of increasing power density [19], [20]. In addition, some studies have optimized the volume of passive devices based on passive device energy storage [21], [22]. However, these articles did not consider the converter loss, so the power density cannot be evaluated.

Accordingly, this article proposes an automatic parameter optimization design method based on a complete circuit analytical model for the eGaN HEMT synchronous buck converter. The proposed method simultaneously considers the efficiency and power density of the converter, achieving automatic design of switching frequency and inductance, and automatic optimization of dead time. The main contributions of this article are reflected in the following three aspects.

1) Complete Circuit Analytical Model: An incomplete-zero voltage switching (inc-ZVS) transient model has been proposed, which has not been found in previous work based on hard switching (HS) and ZVS. Simultaneously, a complete circuit analytical model has been developed, including the switching steady-state model and various switching transient models, encompassing HS ZVS and inc-ZVS. This differs from previous methods that only included a single switching transient model.

2) Automatic Optimization of Dead Time: The proposed circuit analytical model accurately predicts switch transient waveforms, enabling precise anticipation of the optimal dead time under various operating conditions. It facilitates automatic dead time optimization under different working conditions when coupled with the current detect circuit.

3) Automatic Design of Parameters: Based on the proposed circuit analytical model, this article has developed a digital model for the loss and volume of the converter. The developed model can automatically output the impact of switching frequency and inductance on converter efficiency and power density according to input parameters and constraints, thereby achieving automated parameter design.

The rest of this article is organized as follows. Section II outlines the distinctions among HS, ZVS, and inc-ZVS, along with the modeling method of the complete circuit analytical model. Section III presents the dead time optimization method for the eGaN HEMT synchronous buck converter. Section IV demonstrates the evaluation methods for converter loss and volume and the rationale and outcomes of parameter automatic design. Section V validates the accuracy of the analytical model and the effectiveness of parameter optimization through experimental verification. Finally, Section VI concludes the article.

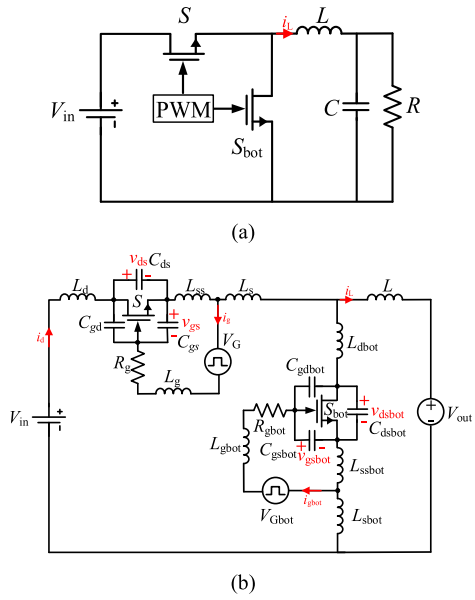

Fig. 1. (a) Single-phase synchronous buck converter. (b) Equivalent circuit of the synchronous buck converter.

II. COMPLETE ANALYTICAL MODEL OF SYNCHRONOUS BUCK CONVERTER UNDER WIDE LOAD RANGE

Fig. 1(a) illustrates the topology of the single-phase synchronous buck converter. The main switch S and the synchronous switch $S_{\rm bot}$ from a half-bridge structure. It is noteworthy that, although eGaN HEMTs have no P-N junctions, they can still conduct reversely when there is no gate-source voltage, similar to the body diode of MOSFETs. Therefore, we employ a body diode without a reverse recovery process to describe this characteristic for eGaN HEMTs.

Fig. 1(b) depicts the equivalent circuit of the synchronous buck converter with parasitic inductors and nonlinear capacitors. The output voltage can be considered akin to a constant voltage source, given the typically minimal magnitude of output voltage

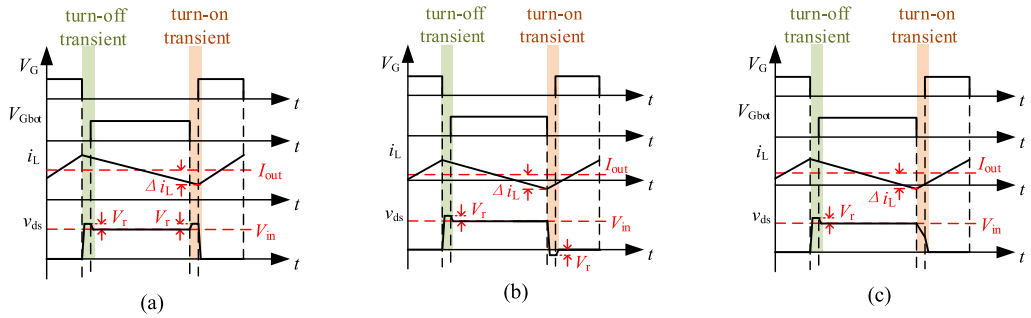

Fig. 2. (a) Ideal waveforms when S achieves HS. (b) ZVS. (c) inc-ZVS.

ripple. The power loop inductor includes the drain-source inductors L_d and $L_{d\mathrm{bot}}$, source inductors L_s and $L_{s\mathrm{bot}}$, and common source inductors L_{ss} and $L_{ss\mathrm{bot}}$.

The common source inductors and gate inductors L_g and $L_{g\mathrm{bot}}$ constitute the drive loop inductors. It is important to note that when applying Kelvin connections for the devices, common source inductors are equal to zero, and the parasitic inductor of the Kelvin source is included in the gate inductor. These parasitic inductors can be obtained through Maxwell Q3D simulation. The drain-source capacitor C_{ds}, gate-drain capacitor C_{gd}, and gate-source capacitor C_{gs} are nonlinear junction capacitors of the power transistor. The values of these nonlinear junction capacitors are estimated through curve fitting based on the power device's datasheet.

The analytical model of the converter comprises both the switching steady-state model and the switching transient model. The steady-state model is established when the power switch is in the ON-state or OFF-state. The steady-state model remains the same under different loads, as it possesses identical equivalent circuits and state variable equations. The switching-transient model can be divided into two parts: one is the turn-ON transient, specifically describing the process when S turns ON and S_{bot} turns OFF. The other is the turn-OFF transient, elucidating the process when S turns OFF and S_{bot} turns ON. The green and orange region in Fig. 2 displays the simplified waveforms of the switching transient process. Here, Δi_L represents the inductor current ripple, and V_r dnotes the reverse conduction voltage of the switch. Comparing the turn-OFF transient waveforms in Fig. 2, we can observe that during the dead time of the turn-OFF transient, the body diode of S_{bot} conducts freewheeling, implementing ZVS when S_{bot} turns ON. Therefore, under different loads, the turn-OFF transient model, which comprises a series of equivalent circuits and state variable equations, remains the same. The turn-OFF transient model is described in detail in [13] and will not be repeated here.

However, by observing the waveforms of the turn-ON transient in Fig. 2, noticeable differences can be found with varying loads. When the output current I_{out} exceeds Δi_L, the inductor current flows continuously in the forward direction throughout a switching cycle and the output capacitor of S is charged before S turns ON, the drain-source voltage v_{ds} of S is approximately $V_{\mathrm{in}}+V_r$ when S turns ON, S achieving HS. When I_{out} is less than Δi_L, there is a situation where the inductor current flows

TABLE II
SUBMODES OF TURN-ON TRANSITION WITH INCOMPLETE ZVS

Submode	Termination conditions
S_{bot} turn-off delay period (t_0–t_1)	$v_{\mathrm{gsbot}}=V_{\mathrm{gsbotth}}+(i_d-i_L)/g_{\mathrm{fs}}$
S_{bot} turn-off transition period (t_1–t_2)	$v_{\mathrm{gsbot}}=V_{\mathrm{gsbotth}}$
S_{bot} turn-off remaining transition period (t_2–t_3)	$t=t_{\mathrm{don}}$
S turn-on delay period (t_3–t_4)	$v_{\mathrm{gs}}=V_{\mathrm{gsth}}$
S turn-on transition period (t_4–t_5)	$v_{\mathrm{ds}}=0$
Gate charge remaining period (t_5–t_6)	$v_{\mathrm{gs}}=V_{\mathrm{G}}$

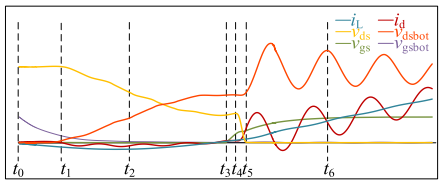

Fig. 3. Typical waveforms during the turn-ON transition of S with inc-ZVS.

reversely and discharges the output capacitor of S. If v_{ds} can drop to $-V_r$ when S turns ON, then S achieves ZVS. Otherwise, S cannot achieve ZVS, v_{ds} is less than $V_{\mathrm{in}}+V_r$ but greater than $-V_r$ when S turns ON. The authors refer to this scenario as inc-ZVS. When the load undergoes continuous variations, inc-ZVS is inevitable, yet it has not been considered in existing efforts. To address this gap, this article proposed the turn-ON transient model for S with inc-ZVS by dividing circuits and solving state variable equations. The detailed submodes and termination conditions are outlined in Table II, where V_{gsth} and V_{gsbotth} represent the forward threshold voltage, V_{G} is the drive voltage, t_{don} is the dead time before S turns on, g_{fs} is the slope of the forward transfer characteristic curve, obtained through curve fitting based on the datasheet. Typical waveforms during the turn-ON transition when S achieves inc-ZVS are shown in Fig. 3. Fig. 4 illustrates the equivalent circuits for the turn-ON transient process when S achieves inc-ZVS, which are described as follows.

Before t_0, S_{bot} is in ON-state and S is in OFF-state. The direction of the inductor current is opposite to the reference current direction illustrated in Fig. 4.

1) S_{bot} Turn-Off Delay Period (t_0–t_1): Fig. 4(a) shows the equivalent circuit of this submode. At t_0, the driving voltage

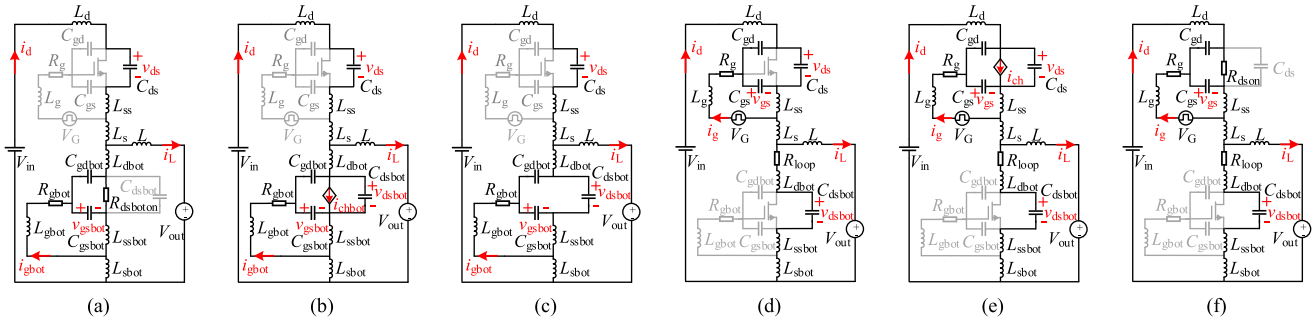

Fig. 4. Equivalent circuits during turn-ON transition of S with inc-ZVS.

$V_{G\text{bot}}$ is set to 0 V. C_{issbot} is discharged by the gate current $i_{g\text{bot}}$, leading to a decrease in gate-source voltage v_{gsbot}.

2) S_{bot} Turn-OFF Transition Period (t_1–t_2): Fig. 4(b) shows the equivalent circuit of this submodel. At t_1, the channel current i_{chbot} begins to be controlled by v_{gsbot}, and S_{bot} is treated as a voltage-controlled current source (VCCS), adhering to the forward transfer characteristic curve. During this period, the difference between i_d–i_L and i_{chbot} charges C_{ossbot}, leading to an increase in v_{dsbot}. Simultaneously, the reverse flow of i_d discharges C_{oss}, resulting in a decrease in v_{ds}.

3) S_{bot} Turn-OFF Remaining Transition Period (t_2-t_3): Fig. 4(c) shows the equivalent circuit of this submode. At t_2, the channel of S_{bot} ceases to conduct, indicating completely turned OFF. At the beginning of this submode, the inductor current flows in the reverse direction, and its absolute value continues to decrease. Consequently, i_d discharges C_{oss}, leading to a decrease in v_{ds}. If at the moment when the absolute value of i_L decreases to 0, the dead time has not yet ended (or the drive signal of S has not been loaded), i_L changes to forward flow and its absolute value continues to increase. Correspondingly, i_d charges C_{oss}, increasing v_{ds}.

4) S Turn-ON Delay Period (t_3–t_4): Fig. 4(d) shows the equivalent circuit of this submode. At t_3, $V_{G\text{bot}}$ is applied and v_{gsbot} rises.

5) S Turn-ON Transition Period (t_4–t_5): Fig. 4(e) shows the equivalent circuit of this submode. At t_4, i_{ch} begins to rapidly increase under the control of v_{gs}, following the forward transfer characteristic curve. During this period, S is treated as VCCS. The difference in current between i_{d} and i_{ch} discharges C_{oss}, leading to a decrease in v_{ds}.

6) Gate Charge Remaining Period (t_5–t_6): Fig. 4(f) shows the equivalent circuit of this submode. At t_5, S is entirely ON. The driving loop of S completes the remaining charging process.

The equivalent circuits and state equations for the turn-ON transient of S achieving HS and ZVS are extensively described in [11] and [13]. They are not reiterated in this article.

From the previous analysis, it can be seen that under different operating conditions, the steady-state model and the turn-OFF transient model remain the same, while the turn-ON transient model varies in three different ways. Although we have derived the turn-ON transient models for all scenarios, to develop a comprehensive converter model, it is necessary to establish a unified turn-ON transient model that integrates the ZVS, inc-ZVS, and

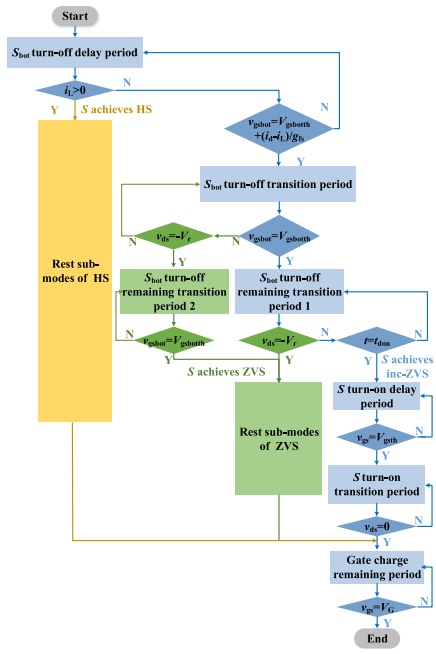

Fig. 5. Uniform model of turn-ON transient.

HS. As depicted in Fig. 5. At the end of the S_{bot} turn-OFF delay period, marked as t_1 in Fig. 3, if the current of the inductor is greater than zero, S achieves HS, otherwise, S is either ZVS or inc-ZVS. At the end of the S_{bot} turn-OFF remaining transition period, denoted as t_3 in Fig. 3, if the source-drain voltage v_{ds} of S drops to the reverse conduction voltage $-V_r$, indicating conduction of the S body diode, S achieves ZVS, otherwise, it is inc-ZVS. This differs from previous efforts based on a singular operating condition. For instance, the work in [11] is based on S with HS, while the work in [13] emphasizes S achieving ZVS.

To validate the accuracy of the proposed converter analytical model, experiments were conducted under the circuit parameters listed in Table III. Fig. 6 displays the comparison between the predicted and experimental waveforms under different loads. It can be observed that the predicted waveforms from the established analytical model closely match the experimental waveforms under various loads. The rising/falling rates of the predicted drain-source voltage v_{ds} and the rising rate of the drain current i_d are consistent with the experimental results. The article

TABLE III
KEY CIRCUIT PARAMETERS

Parameters	Values
Input voltage V_{in}	12 V
Output voltage V_{out}	3.3 V
Output current I_{out}	1 A/5 A/10 A
Switching frequency f_s	1 MHz
Output inductor L	180 nH
Turn-on dead time t_{don}	80 ns
Turn-off dead time t_{doff}	40 ns

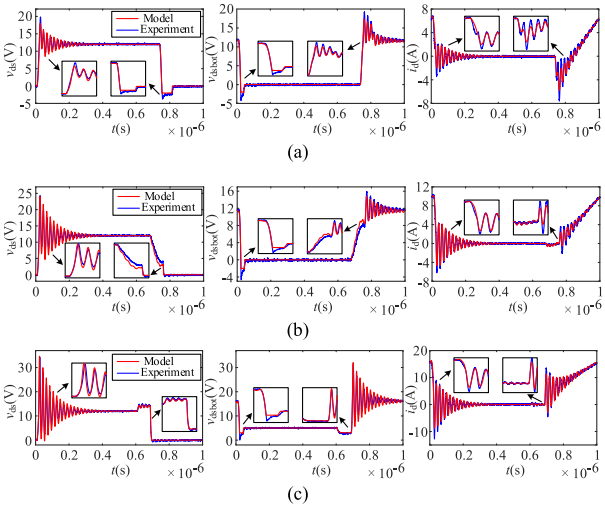

Fig. 6. Comparison of key waveforms between experiment and model at an output current of (a) 1 A, (b) 5 A, and (c) 10 A.

observes a slight difference in the oscillation amplitudes of voltage and current, which is attributed to the disparities between the actual parasitic inductors and junction capacitors compared to the model. Additionally, there is a minor phase deviation in the oscillation between the model and the experimental, primarily caused by differences in switching speeds.

III. DEAD TIME OPTIMIZATION BASED ON CIRCUIT ANALYTICAL MODEL

To prevent simultaneous conduction of the switches in the same bridge arm, a certain dead time needs to be set. However, due to the significant reverse conduction voltage in GaN devices, excessively long dead time can result in substantial reverse conduction loss.

In the modeling process described in Section II, the switching transient process is divided into several submodes. By using the MATLAB ode45 function to solve the state equations of these submodes, numerical solutions for the state variables as well as the start and end time of each submode can be obtained. The optimal dead time can be calculated from the start and end time of the relevant submodes.

Due to the three different turn-ON modes of S, the optimal turn-ON time varies under different loads. When the converter is in CCM, S achieves HS. Fig. 7(a) illustrates the simplified turn-ON transient waveform when S achieves HS. At t_0, the drive voltage of $S_{\rm bot}$ is removed. At t_2, the drain-source voltage of $S_{\rm bot}$ drops to the reverse conduction voltage $-V_r$, which means $S_{\rm bot}$ is completely turned OFF. Subsequently, during the time interval t_2–t_3, $S_{\rm bot}$ undergoes reverse conduction until the drive voltage to S is applied at t_3. At t_4, S starts turning ON. Therefore, to minimize reverse conduction loss, the control of the switch drive signal should be such that the moment when $S_{\rm bot}$ is completely turned OFF coincides with the moment when S starts turning ON. This yields the optimal turn-ON dead time when S achieves HS

$$\begin{aligned} t_{\rm odt\_on(HS)} &= t_2 - t_0 - (t_4 - t_3) \\ &= t_2 - t_0 + t_3 - t_4. \end{aligned} \tag{1}$$

Fig. 7(b) illustrates the simplified turn-ON transient waveform when S achieves ZVS. At t_0, the drive voltage of $S_{\rm bot}$ is removed. At t_3, the gate-source voltage of $S_{\rm bot}$ drops to $V_{\rm gsbotth}$, and the drain-source voltage of S drops to $-V_r$, indicating complete closure of $S_{\rm bot}$. At t_4, the drive voltage V_G is applied. At t_5, the gate-drain voltage of S rises to $V_{\rm gdth}$, signifying the commencement of S opening. To minimize reverse conduction loss, the optimal turn-ON dead time when S achieves ZVS is

$$\begin{aligned} t_{\rm odt\_on(ZVS)} &= t_3 - t_0 - (t_5 - t_4) \\ &= t_3 - t_0 + t_4 - t_5. \end{aligned} \tag{2}$$

Fig. 7(c) illustrates the simplified turn-ON transient waveform when S achieves inc-ZVS. At t_0, the drive voltage to $S_{\rm bot}$ is removed. At t_2, $S_{\rm bot}$ is completely turned OFF. Since the reverse inductor current is relatively small at this point, $v_{\rm ds}$ cannot drop to $-V_r$. At some point thereafter, the reverse inductor current will cross zero and start flowing positively. If the dead time is still ongoing at this moment, the positive inductor current will charge the output capacitor of S, causing the drain-source voltage $v_{\rm ds}$ to rise and increase the turn-ON loss of S. Therefore, the optimal end time for the turn-ON dead time should coincide with the moment when the inductor current is zero, and at this point, S starts to turn on. Thus, the optimal turn-ON dead time for incomplete ZVS is

$$\begin{aligned} t_{\rm odt\_on(in-ZVS)} &= t_{(i_L=0)} - t_0 - (t_4 - t_3) \\ &= t_{(i_L=0)} - t_0 + t_3 - t_4. \end{aligned} \tag{3}$$

As deduced from the analysis in Section II, $S_{\rm bot}$ defaults to achieving ZVS within the switching cycle. Hence, the optimal turn-OFF dead time remains consistent under different loads, similar to the case when S achieves ZVS. Wei et al. [13] provides specific analysis and expression for the optimal turn-OFF time, which will not be reiterated here.

It is worth noting that all the optimal dead time calculated above is based on the minimum dead time obtained from the analytical model. The actual dead time setting should be slightly larger than the calculated optimal dead time.

IV. PARAMETER AUTOMATIC OPTIMIZATION AND DESIGN FOR SYNCHRONOUS BUCK CONVERTER WITH DIFFERENT OPERATING CONDITIONS

Based on the circuit analytical model established in Section II and the optimal dead time calculation method proposed in

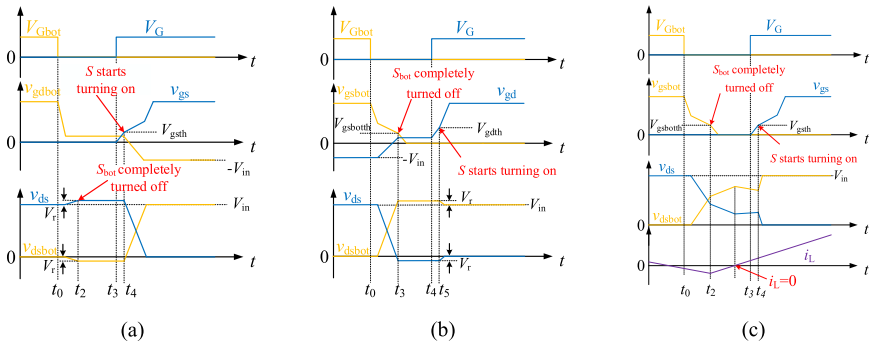

Fig. 7. Simplified turn-ON transient waveform when (a) *S* achieves HS. (b) *S* achieves ZVS. (c) *S* achieves inc-ZVS.

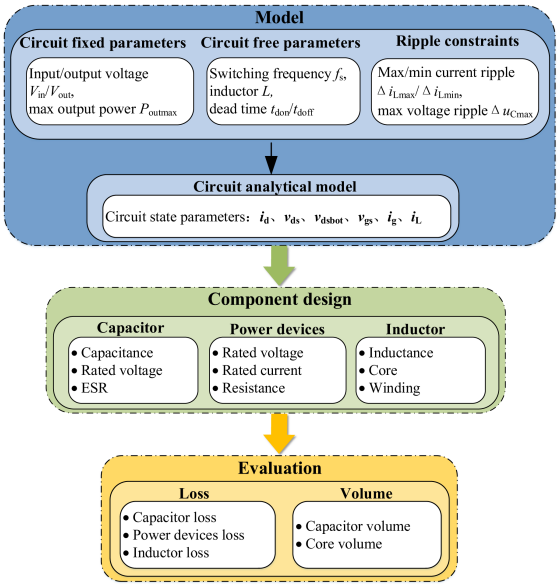

Fig. 8. Optimization and design approach for synchronous buck converter.

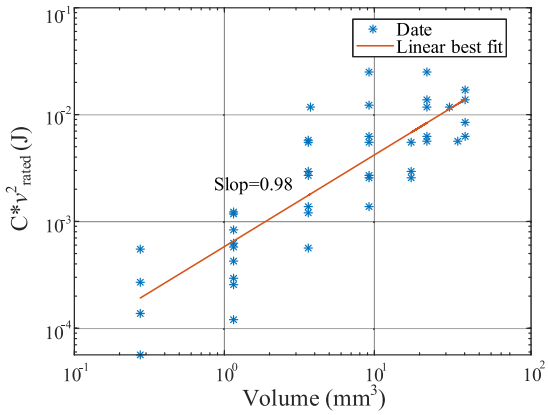

Fig. 9. Plot $C * v^2_{\text{rated}}$ product against the capacitor volumes.

Section III, this section will conduct parameter automatic optimization and design for the synchronous buck converter, as illustrated in Fig. 8. The circuit fixed parameters include input voltage V_{in}, output voltage V_{out}, and maximum output power P_{outmax}. The circuit-free parameters, or optimization parameters, encompass switching frequency f_s, output inductance L, and dead time t_{don}, t_{doff}. Ripple constraints consist of maximum/minimum inductor current ripple $\Delta i_{L\text{max}}$, $\Delta i_{L\text{min}}$, and maximum capacitor voltage ripple $\Delta u_{C\text{max}}$. It is noteworthy that although this article is based on fixed input and output voltages, the model is suitable for any variations in input and output voltages as it encompasses all possible operating conditions of the converter. Based on the provided fixed parameters and ripple constraints, the optimization design program automatically computes the ranges for the free parameters and sequentially performs circuit state solving, total loss, and volume evaluation, ultimately providing the results of parameter optimization and design. The next will first introduce the estimation methods for component loss and volume, followed by a detailed explanation of the parameter automatic design process and its results.

A. *Capacitor Design and Evaluation*

Due to the characteristics of small size, large capacitance, excellent high-frequency performance, and high reliability of multilayer ceramic capacitors (MLCC), this article chooses the TDK X7R series capacitors as the output capacitors. The equivalent series resistance provided in the datasheet was utilized to estimate the capacitor loss.

The volume of a capacitor can be represented by the product of $C * v^2_{\text{rated}}$ [21]. In this study, TDK MLCC from the X7R series were selected, including various sizes: 0402, 0603, 0805, 1206, 1210, and 1812, with rated voltages of 16, 25, 35, and 50 V. The $C * v^2_{\text{rated}}$ product and corresponding capacitor volume were plotted, as shown in Fig. 9. Linear fitting was performed on the obtained data, resulting in the best-fit line with a slope of 0.98.

In this article, considering the dc bias effect of MLCC, on the one hand, a total of n_p capacitors are connected in parallel to achieve the output capacitance determined by (4). On the other hand, The rated voltage $v_{i,\text{rated}}$ of a single capacitor should be selected to slightly larger the output voltage. n_p is not treated as an optimization parameter in this study but is set as a constant. This decision is based on the fact that variations in the values of n_p have a relatively small impact on the loss and volume of the converter. Additionally, the developed program supports examining the capacitor loss and volume resulting from different

values of n_p

$$C = \frac{\Delta i_{L\max}}{4\Delta u_{C\max} f_s}. \tag{4}$$

B. Inductor Design and Evaluation

This article adopts the area product (Ap) method for the design of the inductor, using the EE core structure with TDK PC47 [23]. The winding employs multistrand Litz wire. The core Ap is calculated using the formula

$$A_p = \frac{L I_{L\max}^2}{K_u J_m B_{\rm pk}}. \tag{5}$$

Here, L represents the inductance, $I_{L\max}$ is the peak current of the inductor, K_u is the effective utilization coefficient of the window, typically taken as 0.2–0.4 according to safety regulations, J_m is the current density factor, $B_{\rm pk}$ is the peak magnetic flux density when the magnetic core is operating.

Inductor loss consists of core loss and winding loss. The improved Steinmetz equation method is an approach for estimating nonsinusoidal excitation core loss [24]

$$P_c = \frac{\pi}{4} k_1 D \left(\frac{f}{2D}\right)^{\alpha 1} B_m^{\beta 1} + \frac{\pi}{4} k_2 (1-D) \left(\frac{f}{2(1-D)}\right)^{\alpha 2} B_m^{\beta 2}. \tag{6}$$

Here, k_1, α_1, and β_1 correspond to the Steinmetz parameters at the frequency $f_1 = f_s$ / 2D, while k_2, α_2, and β_2 correspond to the Steinmetz parameters at the frequency $f_2 = fs$ / 2(1-D). D represents the duty cycle of the converter, and the Steinmetz parameters at different frequencies can be obtained from the magnetic core data sheet.

The inductor winding loss includes dc resistance loss and ac resistance loss. The dc resistance can be calculated as l_w / ($\sigma * S_{\rm w}$), where l_w is the length of the winding, σ is the conductivity of the winding material, and S_w is the cross-sectional area of the winding coil. The alternating current resistance $R_{\rm ac}$ is expressed as $R_{\rm ac} = k_{\rm ac} * R_{\rm dc}$, where the alternating current winding factor $k_{\rm ac}$ is obtained through the following equation [25]:

$$k_{\rm ac} = \begin{cases} 1 + \dfrac{\left(\frac{r}{\sigma_0}\right)^4}{48 + 0.8\left(\frac{r}{\sigma_0}\right)^4} & \frac{r}{\sigma_0} < 1.7 \\ 0.25 + 0.5\frac{r}{\sigma_0} + \frac{2}{32}\left(\frac{r}{\sigma_0}\right)^2 & \frac{r}{\sigma_0} > 1.7 \end{cases}. \tag{7}$$

Here, r is the radius of the conductor. σ_0 is the skin depth, estimated by$1/\sqrt{\pi f_s \mu \sigma}$. μ *is* the permeability of the conductor.

The volume of the inductor is mainly determined by the core volume. As the actual Ap values of the series cores are discrete, and in comparison to the designed inductor results, the chosen cores often have a certain margin. To avoid the impact of discrete core margins on volume assessment, this article performs a linear fit on the actual core's window area A_w and effective cross-sectional area A_e to obtain a series of cores with continuously changing Ap values. The selected core structures include TDK Mn-Zn ferrite EE-type cores: EE8, EE10/11, EE13, EE16, EE19, EE19/16, EE20/20/5, EE22, EE25/19, and EE25.4. The fitting results of the cores are shown in Fig. 10, with the optimal fitting slope being 1.592.

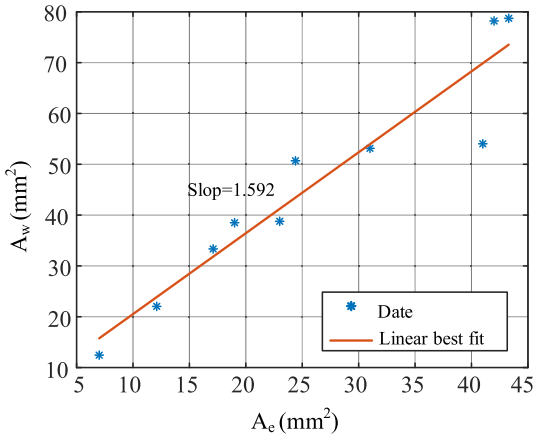

Fig. 10. Curve fitting of A_e and A_w.

C. Semiconductor Devices Design and Evaluation

For medium to small power applications, devices are typically cooled naturally through PCB vias. Therefore, when evaluating semiconductor devices, power loss is the main concern. This relies on the converter analytical model established in Section II, including conduction loss $P_{S\rm con}$, reverse conduction loss $P_{S\rm rec}$, switching loss $P_{\rm Sw}$, and parasitic parameter oscillation loss $P_{\rm ring}$.

The conduction loss $P_{\rm Scon}$ refers to the power dissipated when the power device is in a fully conducting state, resulting from the current flowing through the conduction resistance

$$P_{S\rm con} = \sum \left(f_s \times \int_{t_{\rm initial}}^{t_{\rm final}} i_d^2(t) \times R_{\rm dson} \cdot dt \right). \tag{8}$$

The reverse conduction loss $P_{S\rm rec}$ refers to the power dissipated when the current flows in the reverse direction through the equivalent body diode of the power device, without applying gate drive voltage

$$P_{S\rm rec} = \sum \left(f_s \times \int_{t_{\rm initial}}^{t_{\rm final}} i_d(t) \times (-V_r) \cdot dt \right). \tag{9}$$

The switching loss $P_{\rm Sw}$, including turn-ON loss $P_{S\rm on}$ and turn-OFF loss $P_{S\rm off}$, refers to the power generated when the current flows through the channel of the power device during the transition from fully off to fully on, and vice versa. Taking turn-ON loss $P_{S\rm on}$ as an example

$$P_{S\rm on(HSorinc-ZVS)} = \sum \left(f_s \times \int_{t_{\rm initial}}^{t_{\rm final}} i_{\rm ch}(t) \times v_{\rm ds}(t) \cdot dt \right)$$
$$P_{S\rm on(ZVS)} = \sum \left(f_s \times \int_{t_{\rm initial}}^{t_{\rm final}} i_{\rm ch}(t) \times v_{\rm sd}(t) \cdot dt \right). \tag{10}$$

In the power device's transient switching process, resonance occurs between the output capacitor of the power device and the parasitic inductor in the power loop, leading to high-frequency

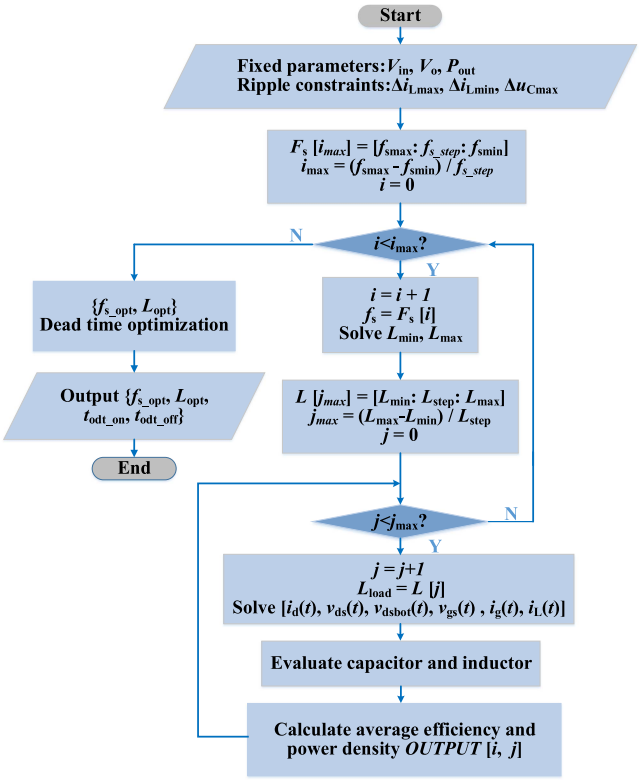

Fig. 11. Parameter optimization design process.

oscillations and parasitic effect loss P_{ring}. This can be represented by an equivalent ac resistance R_{loop}

$$P_{\text{ring}} = \sum \left(f_s \times \int_{t_{\text{initial}}}^{t_{\text{final}}} i_d^2 \times R_{\text{loop}} \cdot dt \right). \tag{11}$$

Since the volume of power devices is significantly smaller than that of passive components, this study neglects the volume of power devices.

D. Automatic Parameter Optimization and Design Based on Average Efficiency and Power Density

Fig. 11 illustrates the detailed flowchart of the parameter optimization and design process. The following will provide a detailed explanation of each step.

1) Input fixed parameters and ripple constraints. It is worth noting that the ripple in inductor current and capacitor voltage should be considered under the full load condition. The larger the set ripple range, the larger the subsequent range for traversing circuit parameters.

2) Set the range of the switching frequency f_s according to requirements. In this article, the minimum switching frequency is set to $f_{\text{smin}} = 100$ kHz, the maximum switching frequency is set to $f_{\text{smax}} = 1$ MHz, and the step size f_{s_step} is set to 100 kHz. Obtaining a one-dimensional array F_s [$i_{\max}$] = [f_{smin}: f_{s_step}: f_{smax}], where $i_{\max} = (f_{\text{smax}} - f_{\text{smin}}) / f_{s\_\text{step}}$ represents the number of elements in the array.

For any switching frequency f_s [i] in the F_s [$i_{\max}$] array, neglecting the voltage variation across the output inductor during the dead time, the range of inductance can be obtained from the volt-second balance. Taking the minimum inductance calculation as an example

$$L_{\min} = \frac{(V_{\text{in}} - V_{\text{o}})D}{2\Delta i_{L\max} f_s[i]}. \tag{12}$$

Similarly, the maximum inductance $L_{\max}$ for f_s [i] can be obtained. This yields a one-dimensional inductor array L [$j_{\max}$] =[$L_{\min}$: L_{step}: $L_{\max}$] for f_s [i], where $j_{\max}$ represents the number of elements in the inductance array. Considering that the difference between $L_{\min}$ and $L_{\max}$ varies for different switching frequencies, and to expedite the optimization design process, a variable step size L_{step} with a fixed number of elements $j_{\max}$ is employed to determine the discrete values of the output inductor for each f_s [i]. In this work, $j_{\max}$ is set to 10. Thus, by permuting and combining each f_s [i] with its corresponding L [$j_{\max}$], a {f_s, L} two-dimensional array, denoted as M [$i_{\max}$, $j_{\max}$], reflecting the range of values for the free parameters, can be obtained.

3) Each set of parameters from M [$i_{\max}$, $j_{\max}$] is then applied to the analytical model to solve for the circuit state variables [$i_d(t)$, $v_{\text{ds}}(t)$, $v_{\text{dsbot}}(t)$, $v_{\text{gs}}(t)$, $i_g(t)$, $i_L(t)$] under different load. This forms the basis for the subsequent design of inductors and capacitors, as well as the calculation of component loss. It is worth noting that, to avoid a secondary solution of the analytical model, a fixed dead time ($t_{\text{don}} = 80$ ns, $t_{\text{doff}} = 40$ ns) is used for each set of parameters in M [$i_{\max}$, $j_{\max}$]. Once the optimized values for {f_s, L} are determined, dead time optimization is then performed for the specific {f_s, L}.

4) For each set {f_s, L} in M [$i_{\max}$, $j_{\max}$], following the earlier content in this section, complete the design and evaluation of capacitors and inductors. And yields the circuit's average efficiency and power density for the corresponding parameters. Output the circuit's average efficiency and power density for each set in M [$i_{\max}$, $j_{\max}$], denoted as OUTPUT [$i_{\max}$, $j_{\max}$]. The average efficiency η_{ave} is defined as

$$\eta_{\text{ave}} = \frac{\sum_{k=1}^{m} a_k * \eta_k}{m} \tag{13}$$

where m represents the number of load points. In this study, the output current range is from 1 to 10 A with a step size of 1 A, thus $m = 10$. a_k denotes the efficiency weighting coefficients for different loads, and in this context, $a_{(k=12,3\ldots10)=1}$.

The power density is defined as the ratio of the output power under full load conditions to the sum of the volumes of all components.

5) Based on the OUTPUT [$i_{\max}$, $j_{\max}$], combined with practical requirements, the circuit parameter design results {f_{s_opt}, L_{opt}} can be obtained. Subsequently, the optimization of the dead time for {f_{s_opt}, L_{opt}} can be accomplished using the method described in Section III.

It is important to note that the optimal dead time is calculated based on the relevant modal duration. Therefore, any parameter affecting the circuit operating, such as V_{in}, V_{out}, I_o, f_s, and L can influence the optimal dead time. Since this study focuses on a converter with fixed input/output voltages (12 V/3.3 V) and the parameters f_s and L have been determined through the first

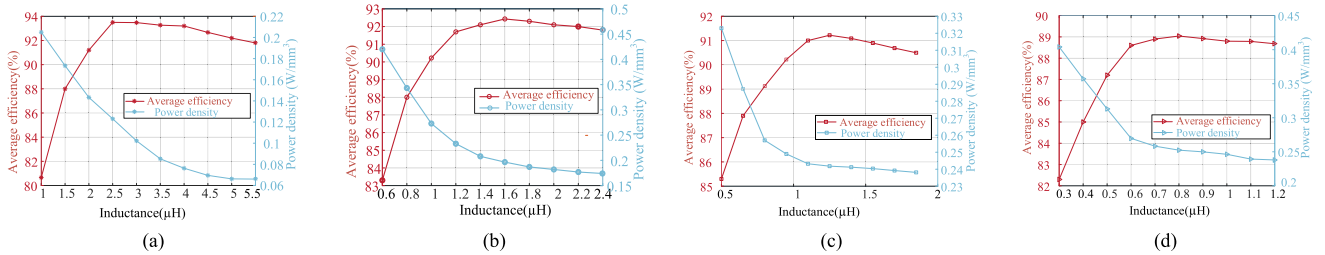

Fig. 12. Model-predicted efficiency and power density based on various inductances when (a) $f_s = 300$ kHz. (b) $f_s = 500$ kHz. (c) $f_s = 700$ kHz. (d) $f_s = 1$ MHz.

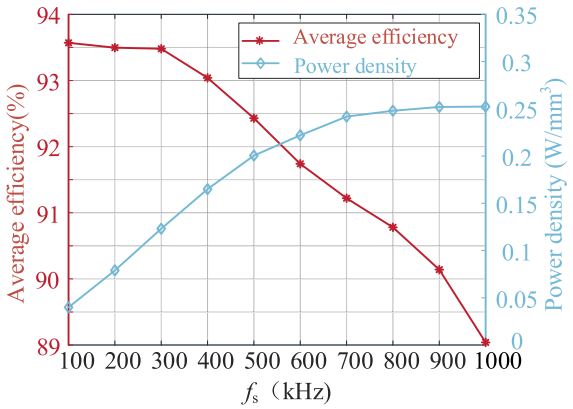

Fig. 13. Model-predicted efficiency and power density based on various frequencies.

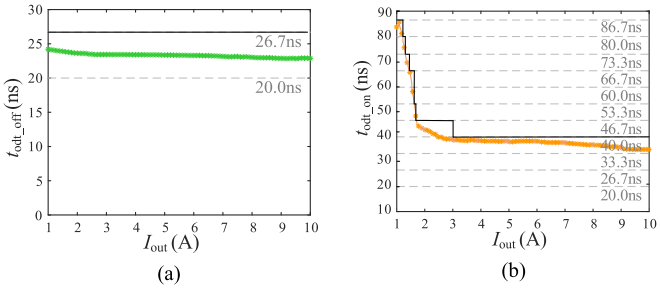

Fig. 14. Model-predicted optimal dead time based on various loads.

four optimization steps, only the changing output current will impact the optimal dead time.

Fig. 12 illustrates the model-predicted efficiency and power density based on various inductances under a fixed switching frequency. As depicted in Fig. 12, when the inductance increases, the circuit's average efficiency gradually rises to a peak and then decreases with further increases in inductance. This behavior is attributed to the fact that, with small inductance, the main switch S achieves ZVS in most operating conditions. While this reduces the switching loss of S, the presence of reverse currents leads to significant inductor current ripple, causing substantial inductor loss and resulting in lower overall efficiency. With the increase in inductance, the current ripple gradually decreases, leading to a reduction in inductor loss and an overall improvement in circuit efficiency. However, as the inductance continues to increase, the diminishing loss due to reduced current ripple cannot offset the increased loss associated with the larger inductor volume. This results in an increase in inductor loss and a gradual decrease in overall circuit efficiency. The circuit's power density decreases progressively with the increase in output inductance, exhibiting a monotonic trend.

Fig. 13 illustrates the model-predicted efficiency and power density based on various frequencies. As depicted in Fig. 13, the maximum average efficiency of the circuit decreases with an increase in switching frequency, sharply declining beyond 300 kHz. On the other hand, the power density shows a rapid increase with higher switching frequencies, with the growth rate gradually slowing down for frequencies exceeding 700 kHz. Considering both efficiency and power density, the converter demonstrates favorable performance in the range of 300 to 700 kHz. Since the focus of this study is on efficiency, a switching frequency of 300 kHz is chosen. Referring to Fig. 12(a), it is evident that the maximum circuit average efficiency at 300 kHz occurs in the range of 2 to 3 μH for the inductor value. Considering practical constraints on inductance, a value of 2.5 μH is selected as the circuit parameter design result.

Fig. 14 illustrates the relationship between the optimal dead time and the output current under the parameters $f_s = 300$ kHz and $L = 2.5$ μH. The green curve in Fig. 14(a) and the orange curve in Fig. 14(b) represent the optimal dead time obtained through the analytical model. The gray-dashed line represents the discrete dead time that the DSP can generate. In this study, a DSP TMS320F28335 is used to generate PWM drive signals, and its maximum operating frequency is 150 MHz. Therefore, the minimum achievable dead time is 6.67 ns. From Fig. 14, it can be observed that the optimal turn-OFF dead time remains nearly constant as the load varies between 1 and 10 A, with an actual value of 26.7 ns. However, the optimal turn-ON dead time exhibits noticeable variations. This phenomenon occurs because, under varying load currents, $S_{\rm bot}$ consistently achieves ZVS. The optimal turn-OFF dead time is primarily determined by the time for the output capacitor voltage $v_{\rm dsbot}$ of $S_{\rm bot}$ to vary from zero to $-V_r$. However, as the load current increases, S sequentially achieves ZVS, inc-ZVS, and HS. The optimal turn-ON dead time is determined by the time for the voltage $v_{\rm ds}$ of S to vary from zero to $-V_r$, the time for the inductor current to transition from negative to zero, and the time for the voltage $v_{\rm dsbot}$ of $S_{\rm bot}$ to vary from zero to $-V_r$, respectively. The actual dead time should be greater than the optimal dead time, as indicated by the black solid line.

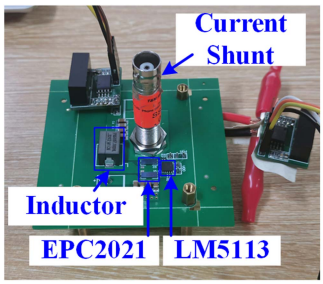

Fig. 15. Hardware prototype of the synchronous buck converter.

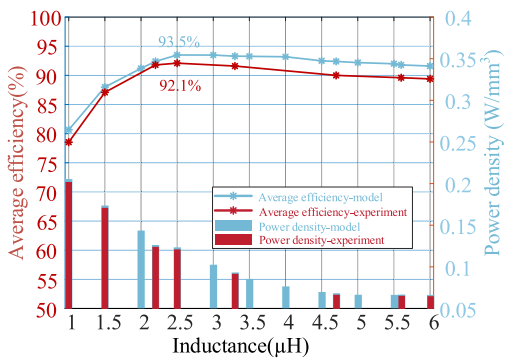

Fig. 16. Comparison of maximum average efficiency and power density between experiment and model with varying inductance.

TABLE IV
COMPARISON OF EXPERIMENTAL AND MODEL RESULTS WITH DIFFERENT INDUCTANCE

Inductance	Error of efficiency	Error of power density	Inductance	Error of efficiency	Error of power density
1 μH	2.12%	1.35%	3.3 μH	1.7%	0.9%
1.5 μH	0.92%	1.18%	4.7 μH	2.4%	1.5%
2.2 μH	0.6%	1.25%	5.6 μH	2.2%	1.2%
2.5 μH	1.4%	1.38%	6 μH	2.2%	1.17%

V. EXPERIMENTAL VALIDATION

This article built a hardware prototype as shown in Fig. 15. The main switch and synchronous switch used in the experiment is EPC2021, and the driver chip is LM5113. To verify the effectiveness of the parameter design, this article measured circuit average efficiency and power density with varying inductance at $f_s = 300$ kHz as shown in Fig. 16. The load range is from 1 to 10 A with a change step size of 1 A. The remaining circuit parameters are consistent with Table III. Table IV presents the error between the measured efficiency and power density and the model-predicted efficiency and power density under different inductances. As shown in Fig. 16, the trend of the measured efficiency curve is similar to that of the model-predict efficiency curve, both exhibiting a peak around 2.5 μH. The model predicts a maximum average efficiency of 93.5%, while the measured maximum average efficiency is 92.1%. The difference between measured and model-predicted efficiency for different inductance does not exceed 2.5%. The measured power density curve and the model-predicted power density curve exhibit the same trend, showing a monotonically decreasing pattern with increasing inductance. The difference between measured and model-predicted power density for different inductance does not exceed 1.5%.

TABLE V
COMPARISON OF EXPERIMENTAL AND MODEL RESULTS WITH DIFFERENT FREQUENCY

Switching frequency	Measured efficiency	Error of efficiency	Measured power density	Error of power density
100 kHz	92.83%	0.74%	0.043 W/mm^3	8.3%
300 kHz	92.1%	1.4%	0.121 W/mm^3	1.38%
500 kHz	91.96%	0.47%	0.191 W/mm^3	4.9%
700 kHz	89.84%	1.38%	0.232 W/mm^3	4.2%
1 MHz	89.89%	0.85%	0.247 W/mm^3	2.2%

Additionally, the experiment measured the maximum average efficiency and power density of the circuit at switching frequencies of 100, 500, 700, and 1 MHz. The actual measured results and errors are presented in Table V. The maximum average efficiency predicted by the model is consistent with the experimental result, indicating that the proposed loss model has a high level of accuracy. While there is some discrepancy between the measured power density and the model-predicted power density, it is attributed to the differences in the actual dimensions of the magnetic core and the model dimensions. However, the measured data aligns with the trend in the power density data presented in Fig. 13.

To verify the effectiveness of the dead time optimization, this article set $f_s = 300$ kHz, $L = 2.5$ μH, and varied the output current from 1 to 10 A in steps of 1 A while implementing fixed dead time ($t_{\rm don} = 80$ ns, $t_{\rm doff} = 40$ ns) and optimized dead time for the converter. The dead time optimization was automatically achieved through a current detect circuit, in conjunction with the optimized dead time table depicted in Fig. 14. The key steady-state experimental waveforms with fixed dead time are measured with an oscilloscope, as shown in Fig. 17. The load currents are 1, 1.2, and 2 A. From Fig. 17, it can be observed that with the increase in load current, the voltage $v_{\rm ds}$ at the instant when S turns ON rises from $-V_r$ (approximately -2 V) to $V_{\rm out}+V_r$. This indicates that S achieves ZVS, inc-ZVS, and HS, respectively. Meanwhile, the voltage $v_{\rm dsbot}$ at the moment when $S_{\rm bot}$ turns ON remains equal to $-V_r$, indicating that $S_{\rm bot}$ consistently achieves ZVS. The efficiency curves of the converter with varying loads before and after dead time optimization are illustrated in Fig. 18. When the load current is greater than 3 A, the efficiency of the converter due to dead time optimization is very significant, and the efficiency improvement for a single load can reach up to 2%. The average efficiency of the converter under all operating conditions has also increased from 92.1% before the dead time optimization to 93.8%.

This significant improvement in efficiency is mainly attributed to the reduction in the loss of switches, particularly sixth reverse conduction loss. Fig. 19 illustrates the model-predicted loss of switch before and after dead time optimization for output currents of 1, 5, and 10 A. As seen in Fig. 19, at different loads, reverse conduction loss $P_{\rm Srec}$ constitutes a significant portion. Through dead-time optimization, the reverse conduction loss

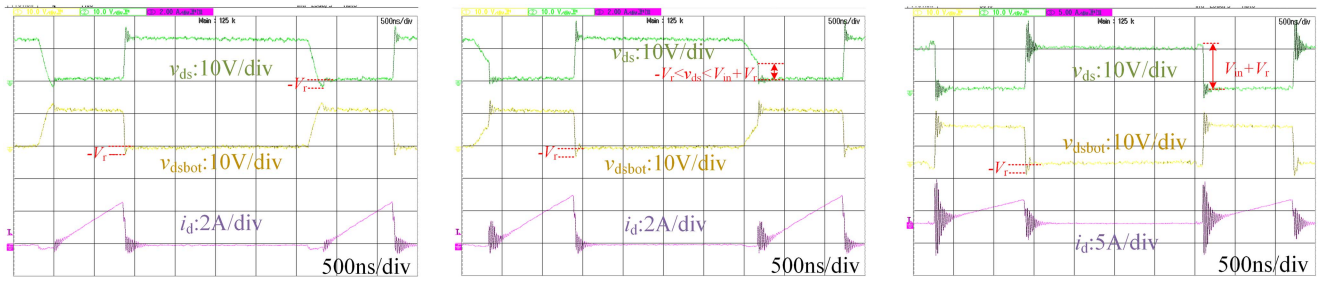

Fig. 17. Key experimental waveforms of the synchronous buck converter under different loads. (a) 1 A. (b) 1.2 A. (c) 2 A.

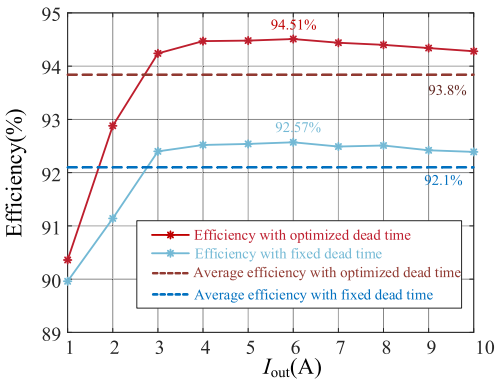

Fig. 18. Comparison of converter efficiency before and after dead time optimization.

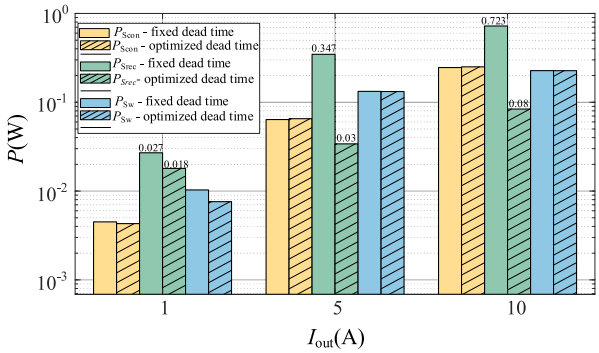

Fig. 19. Model-predicted loss of switch before and after dead time optimization for different output currents.

was reduced by 33%, 90%, and 88%, respectively. When the load current is 1 A, the optimization of reverse conduction loss is less pronounced compared to higher load currents. Furthermore, it can be observed that at a load current of 1 A, the switching loss P_{Sw} is significantly reduced after dead time optimization, compared to higher load currents. This is because the preset fixed turn-ON dead time ($t_{\mathrm{don}} = 80$ ns) is shorter than the optimal turn-ON dead time ($t_{\mathrm{odt\_on}} = 86.7$ ns). Although S can achieve ZVS, the shorter turn-ON dead time results in inc-ZVS instead. Therefore, during the turn-ON dead time, the body diode of S does not conduct, thereby avoiding reverse conduction loss but leading to additional turn-ON loss. At a load current of 1 A, increasing the turn-ON dead time significantly reduces the switching loss of S, while decreasing the turn-OFF dead time reduces the reverse conduction loss of S_{bot}. At higher load currents, S achieves HS, so decreasing the (turn-ON/turn-OFF) dead time does not significantly impact switching loss but primarily reduces the freewheeling time of S_{bot}, thereby decreasing reverse conduction loss.

VI. Conclusion

This article developed a methodology for evaluating the loss and synchronous buck converter under different operating conditions which is based on the proposed complete circuit analytical model. Using the developed method, the effects of switching frequency and inductance on converter efficiency and power density are comprehensively evaluated, and the dead time is optimized. The increase in the switching frequency is beneficial to improve the power density of the converter, but it will lead to a decrease in the average efficiency of the converter, and there is a tradeoff between the average efficiency of the converter and the power density. At a fixed switching frequency, the average efficiency of the converter increases first and then decreases with the increase of inductance. The power density of the converter decreases as the inductance increases. The optimal turn-ON dead time of the converter varies greatly depending on the load current, while the optimal turn-OFF dead time remains unchanged. Finally, the experimental results verify the feasibility and effectiveness of the proposed method and the analytical method.

References

[1] D. Díaz, O. García, J. A. Oliver, P. Alou, Z. Pavlovic, and J. A. Cobos, "The ripple cancellation technique applied to a synchronous buck converter to achieve a very high bandwidth and very high efficiency envelope amplifier," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2892–2902, Jun. 2014, doi: 10.1109/TPEL.2013.2272421.

[2] L. Karthikeyan and B. Amrutur, "Buck converter with load adaptive losses and 256x sub-mW load transient response time of 0.8 ms using synchronous control," *IEEE Trans. Power Electron.*, vol. 39, no. 5, pp. 5954–5966, May 2024, doi: 10.1109/TPEL.2024.3364145.

[3] R. Ramos, V. Repecho, and D. Biel, "Current-limited suboptimal sliding mode control for voltage-regulated synchronous buck converters," *IEEE Trans. Power Electron.*, vol. 37, no. 11, pp. 13081–13090, Nov. 2022, doi: 10.1109/TPEL.2022.3176022.

[4] M. Orabi and A. Shawky, "Proposed switching losses model for integrated point-of-load synchronous buck converters," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 5136–5150, Sep. 2015, doi: 10.1109/TPEL.2014.2363760.
[5] C. Fei, M. H. Ahmed, F. C. Lee, and Q. Li, "Two-stage 48 V-12 V/6 V-1.8 V voltage regulator module with dynamic bus voltage control for light-load efficiency improvement," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5628–5636, Jul. 2017, doi: 10.1109/TPEL.2016.2605579.
[6] B. N. Sanusi and Z. Ouyang, "Integrated inductor design for a highly compact embedded battery charger," *IEEE Trans. Power Electron.*, vol. 37, no. 8, pp. 8873–8885, Aug. 2022, doi: 10.1109/TPEL.2022.3156372.
[7] M. K. Hossain and M. R. Islam, "Power stage design of a synchronous buck converter for battery charger application," in *Proc. Int. Conf. Advance. Elect. Electron. Eng.*, 2018, pp. 1–4, doi: 10.1109/ICAEEE.2018.8642962.
[8] J. Sun, L. Yuan, Q. Gu, R. Duan, Z. Lu, and Z. Zhao, "Design-oriented comprehensive time-domain model for CLLC class isolated bidirectional DC-DC converter for various operation modes," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3491–3505, Apr. 2020, doi: 10.1109/TPEL.2019.2938312.
[9] O. M. Hebala, A. A. Aboushady, K. H. Ahmed, and I. Abdelsalam, "Generic closed-loop controller for power regulation in dual active bridge DC–DC converter with current stress minimization," *IEEE Trans. Ind. Electron.*, vol. 66, no. 6, pp. 4468–4478, Jun. 2019, doi: 10.1109/TIE.2018.2860535.
[10] K. Wang, X. Yang, H. Li, H. Ma, X. Zeng, and W. Chen, "An analytical switching process model of low-voltage eGaN HEMTs for loss calculation," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 635–647, Jan. 2016, doi: 10.1109/TPEL.2015.2409977.
[11] J. Chen, Q. Luo, J. Huang, Q. He, and X. Du, "A complete switching analytical model of low-voltage eGaN HEMTs and its application in loss analysis," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1615–1625, Feb. 2020, doi: 10.1109/TIE.2019.2891466.
[12] Y. Zhang et al., "Analysis of dead-time energy loss in GaN-based TCM converters with an improved GaN HEMT model," *IEEE Trans. Power Electron.*, vol. 38, no. 2, pp. 1806–1818, Feb. 2023, doi: 10.1109/TPEL.2022.3217456.
[13] M. Wei et al., "A multitime-scale analytical model of ZVS buck converter," *IEEE Trans. Power Electron.*, vol. 38, no. 9, pp. 11141–11151, Sep. 2023, doi: 10.1109/TPEL.2023.3283294.
[14] A. Hilal, M.-A. Raulet, C. Martin, and F. Sixdenier, "Power loss prediction and precise modeling of magnetic powder components in DC–DC power converter application," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 2232–2238, Apr. 2015, doi: 10.1109/TPEL.2014.2330952.
[15] V.-H. Bui et al., "Deep reinforcement learning-based optimal parameter design of power converters," in *Proc. Int. Conf. Comput., Netw. Commun.*, 2023, pp. 25–29, doi: 10.1109/ICNC57223.2023.10074355.
[16] K. B. stman and J. K. Jrvenhaara, "A rapid switch bridge selection method for fully integrated DCDC buck converters," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4048–4051, Aug. 2015, doi: 10.1109/TPEL.2014.2384915.
[17] X. Zhang and D. Maksimovic, "Multimode digital controller for synchronous buck converters operating over wide ranges of input voltages and load currents," *IEEE Trans. Power Electron.*, vol. 25, no. 8, pp. 1958–1965, Aug. 2010, doi: 10.1109/TPEL.2010.2043959.
[18] M. Asad, A. K. Singha, and R. M. S. Rao, "Dead time optimization in a GaN-based buck converter," *IEEE Trans. Power Electron.*, vol. 37, no. 3, pp. 2830–2844, Mar. 2022, doi: 10.1109/TPEL.2021.3116126.
[19] W. Huang and B. Lehman, "A compact coupled inductor for interleaved multiphase DC–DC converters," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 6770–6775, Oct. 2016, doi: 10.1109/TPEL.2016.2537832.
[20] Y. Dou, Z. Ouyang, and M. A. E. Andersen, "Design the high-frequency DC-DC converter with integrated coupled inductor and current-balancing-transformer," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2020, pp. 2610–2616, doi: 10.1109/APEC39645.2020.9124329.
[21] Y. Lei, W.-C. Liu, and R. C. N. Pilawa-Podgurski, "An analytical method to evaluate and design hybrid switched-capacitor and multilevel converters," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2227–2240, Mar. 2018, doi: 10.1109/TPEL.2017.2690324.
[22] Z. Ye, S. R. Sanders, and R. C. N. Pilawa-Podgurski, "Modeling and comparison of passive component volume of hybrid resonant switched-capacitor converters," *IEEE Trans. Power Electron.*, vol. 37, no. 9, pp. 10903–10919, Sep. 2022, doi: 10.1109/TPEL.2022.3160675.
[23] TDK, "Mn-Zn ferrites material characteristics PC47," [Online]. Available: https://product.tdk.com/system/files/dam/doc/product/ferrite/ferrite/ferrite-core/catalog/ferrite_mn-zn_material_characteristics_en.pdf
[24] S. Barg, K. Ammous, H. Mejbri, and A. Ammous, "An improved empirical formulation for magnetic core losses estimation under nonsinusoidal induction," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 2146–2154, Mar. 2017, doi: 10.1109/TPEL.2016.2555359.
[25] W. G. Hurley and W. H. Wolfle, *Transformers and Inductors for Power Electronics: Theory, Design and Applications*. Hoboken, NJ, USA: Wiley, 2013.

Shufan Dong was born in Sichuan, China, in 2000. She received the B.S. degree in 2022 in electrical engineering from the Chongqing University, Chongqing, China, where she is currently working toward the M.S. degree in electrical engineering.

Her current research interests include modeling and optimization of dc–dc converters and planar magnetics.

Quanming Luo (Member, IEEE) was born in Chongqing, China, in 1976. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Chongqing University, Chongqing, China, in 1999, 2002, and 2008, respectively.

Since 2005, he has been with the College of Electrical Engineering, Chongqing University, where he is currently a Professor. He has authored or coauthored of more than 80 papers in journal or conference proceedings. His current research interests include LED driving systems, communication power systems, power harmonic suppression, and power conversion systems in electrical vehicles.

Mengjia Wei was born in Anhui Province, China, in 1998. She received the B.S. degree in electrical engineering from the Anhui University, Hefei, China, in 2020. She is currently working toward the master's degree in electrical engineering with the Chongqing University, Chongqing, China.

Her current research interests include the analytical modeling and efficiency optimization of converters with wide bandgap devices.

Guolin Lai was born in Sichuan, China, in 2001. She received the B.S. degree in 2023 in electrical engineering from the Chongqing University, Chongqing, China, where she is currently working toward the M.S. degree in electrical engineering from the Chongqing University, Chongqing, China.

Her current research interests include digital twin of power converters.

Jian Chen was born in Hubei Province, China, in 1993. He received the B.S. degree in electrical engineering from the Qinghai University, Xining, China, in 2016, and the Ph.D. degree in electrical engineering from the Chongqing University, Chongqing, China, in 2021.

He is currently an Assistant Professor with the School of Electrical Engineering, Southwest Jiaotong University, Chengdu, China. His current research interests include wide bandgap device characteristics and models, active gate drivers, and power electronic integration.

Pengju Sun (Member, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from the Chongqing University, Chongqing, China, in 2005 and 2011, respectively.

Between 2009 and 2010, she was a Visiting Student with the University of California, Irvine, CA, USA. Since 2011, she has been with the College of Electrical Engineering, Chongqing University, where she is currently an Associate Professor. Her research interests include switching power converters, power quality control, and reliability of power converter.

Xiong Du (Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Chongqing University, Chongqing, China, in 2000, 2002, and 2005, respectively.

Since 2002, he has been with Chongqing University, where he is currently a Full Professor with the School of Electrical Engineering. He was a Visiting Scholar with Rensselaer Polytechnic Institute, Troy, NY, USA, from 2007 to 2008. His research interests include power electronics system reliability and stability.

Dr. Du was a recipient of the National Excellent Doctoral Dissertation of P.R. China in 2008.