Asymmetrical Level-Shifted PWM-Based Power Distribution Control of Single-Stage Multiport Inverter-Connected Islanded Microgrids

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***Abstract*—The single-stage multiport inverter (SSMPI) is a cost-effective and high-efficiency solution for multisource integration in islanded microgrids because the energy storage components can connect to the ac microgrid directly without intermediate dc-dc converters. However, it is challenging to design the modulation scheme for SSMPI due to the time-varying dc input voltages and requirement for power distribution between the energy storage components. To this end, this article proposes an asymmetric level-shifted pulsewidth modulation (ALSPWM) scheme for flexible power distribution of the SSMPI under time-varying dc input voltage. In the proposed ALSPWM scheme, proportional variation and asymmetric carriers are defined to ease system modeling under the time-varying dc input voltage in SSMPI. Besides, an instantaneous power model based on non-negative three-phase modulation waves is derived, and a zero-sequence voltage injection method is proposed for desired power distribution control. With the proposed ALSPWM, the flexible power distribution between the energy storage components and superior grid current control of the SSMPI under time-varying dc input voltages, along with reduced computational burden, are realized. Finally, the effectiveness of the proposed ALSPWM scheme is verified on an SSMPI-connected islanded microgrid platform.**

***Index Terms*—Carrier-based modulation, islanded microgrid, level-shifted pulsewidth modulation (LSPWM), multiport inverter, power distribution, zero-sequence injection.**

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I. Introduction

DUE to the environmental concerns and continuous decrease in the price, photovoltaic (PV) generation systems have been extensively installed in recent years [1], [2]. However, these systems lack the capability of frequency support, instantaneous reserve, and peak shaving provided by traditional synchronous generators, leading to stability challenges of grid frequency in islanded microgrids [3], [4]. The battery storage integration formed PV-battery hybrid system is an effective solution for these issues in islanded microgrids, which have achieved vigorous development over the past decades [5], [6], [7].

Single-stage multiport inverters (SSMPIs) have emerged as a promising solution for the integration of PV and battery to the ac microgrid because both sources can connect to the ac microgrid directly without intermediate dc-dc converters, featuring advanced merits of single-stage power conversion, simple configuration, and low cost [8], [9], [10]. Moreover, due to the removal of dc-dc converters with their bulky passive filters and capacitors, the power density of the whole system is also substantially increased [11], [12], [13]. The SSMPIs are also easy to implement and can be directly derived from some multilevel converters, such as neutral-point-clamped (NPC) multilevel converters [14], T-type multilevel converters [15], cascaded H-bridge converters [16], [17], [18], and modular multilevel converters [19].

Although the topology of SSMPI is similar to their counterparts of multilevel inverters in circuity, modulation and control strategies cannot be directly implemented [20], [21]. The main reason is that the port voltages of SSMPI are time-varying with the state of charge of the battery and light intensity for the PV, whereas those of the multilevel inverters are balanced. Moreover, power distribution control between PV and battery and the grid current control should be achieved simultaneously, which imposes difficulties in controller and modulation scheme design for SSMPIs.

In view of this, some research efforts have been conducted to achieve power distribution and ac current control of the SSMPIs by controller design. A control scheme beyond the specific pluse width modulation (PWM) modulation [22] was proposed for the power distribution of the SSMPIs. However, four interfaced proportional–integer (PI) loops were required in

this solution. Besides the linear controller-based solution, several papers design the controller of SSMPI with multiobjective control schemes. A model predictive control scheme with specified port power minimization is proposed in [23] to improve the power conversion efficiency of SSMPIs. A direct model-based controller was proposed for the power distribution between the dc sources in [24] to simplify the controller design of SSMPIs. A finite-control-set model predictive control (MPC) with flexible power distribution for SSMPIs was proposed in [25]. Although these strategies can realize the power distribution between the energy sources to some extent, the controller-based solution suffers from complex controller structure, heavy computational burden, and complicated control parameter tuning processes because of the strong nonlinearity and multivariable coupling in the SSMPIs.

In the last few years, several modulation schemes have been reported as an alternative solution to achieve power distribution and ac current control of the SSMPIs. A carrier-based PWM was proposed to simplify the modulation design under the asymmetrical dc-link voltages by modifying the magnitude of the carrier waves [26]. A two-stage modulation strategy is proposed to produce undistorted current even in the presence of unevenly distributed space vectors [27]. A hybrid PWM strategy composed of carried-based PWM and discontinuous PWM is proposed to generate high-quality ac voltages [28]. A modified space-vector PWM with coordination projection was proposed to generate the desired control performance under the unbalanced dc-link [29]. Although the above modulation strategies are effective under unbalanced dc input voltage and have presented benefits in system performance, these methods cannot be applied to SSMPI directly due to the lack of power distribution control capabilities.

Regarding power distribution issues of the SSMPI, several research efforts have been conducted recently. An SSMPI analytical model-based multiobjective vector modulation is proposed for regulating dc-port power and ac output voltage simultaneously [30]. However, complicated multiobjective-based calculations and coordinate transformation are unavoidable. An adaptive PWM is proposed for desirable power distribution by injecting the zero-sequence voltage into the common mode voltage [31]. An additional PI controller was employed for power flow control in the SSMPI by regulating the injected zero-sequence component [32]. A precise model of port power and the zero-sequence component was built in [33], and a deadbeat controller was proposed for the power distribution control of SSMPI. These works regulated the output power of the dc source by utilizing the extra control freedom provided by the zero-sequence components [31], [32], [33]. A virtual space-vector PWM-based flexible power control was proposed in [34] and [35], where power distribution between each port was regulated by adjusting the proportion of the positive and negative small vectors. However, the magnitude of positive and negative small vectors was not equal in SSMPIs, and adjusting the proportion of these vectors would affect the active voltage vector synthesis and deteriorate the ac current control performance. A decoupled circuit model by considering the SSMPI as upper and lower inverters was proposed in [36], and a simplified carrier-based PWM solution was derived based on this decoupled model for power distribution and current control in SSMPI. However, extra switching losses were introduced in this decoupled model, and deteriorated grid current was presented. Therefore, a simplified carrier-based modulation with a well-regulated grid current is still desired in the SSMPI.

The level-shifted pulsewidth modulation (LSPWM) provides an attractive solution for low switching losses and high-quality grid current. A carrier LSPWM strategy is proposed to balance the neutral-point voltage [37]. A modified LSPWM strategy is developed for realizing desired outputs under normal and switch open fault modes [38]. A novel LSPWM is investigated to reduce power losses and enhance the power quality at the grid side [39]. To balance dc input voltages and reduce voltage ripples, an enhanced LSPWM has been studied in [40]. Unfortunately, the aforementioned LSPWM strategies cannot be directly applied to SSMPIs due to flexible power distribution under time-varying dc input voltages not being addressed.

In view of this, this article proposes an asymmetric level-shifted pulsewidth modulation (ALSPWM) scheme for the SSMPI-connected islanded microgrid to deal with the time-varying dc input voltages and requirement for power distribution between the energy storage components. A unified expression of the modulation signals with adaptive magnitude is proposed to deal with pulse train generation under time-varying input voltages. In the proposed ALSPWM scheme, a direct and instantaneous power model based on three-phase modulation waves is derived, and a zero-sequence injection method is put forward for desired power distribution control. With the proposed ALSPWM, the flexible power distribution between the energy storage components with the desired grid current control performance of the SSMPI is realized under time-varying dc input voltages. Finally, the advantage of the proposed ALSPWM scheme for SSMPI is verified by a comparative experimental study of the islanded microgrid platform.

The rest of this article is organized as follows. The topology and control strategy of the SSMPI-connected PV-battery hybrid system is illustrated in Section II. Section III provides the proposed ALSPWM-based power distribution strategy. The simulation results are shown in Section IV. The experimental tests are conducted in Section V. Finally, Section VI concludes this article.

II. Topology and Control Strategy of SSMPI-Connected PV-Battery Hybrid System

In this section, the topology of the SSMPI-connected PV-battery hybrid system is introduced first. Then, the basic control scheme for the SSMPI-connected PV-battery hybrid system is reviewed.

A. Topology of SSMPI-Connected PV-Battery Hybrid System

The topology of the SSMPI-connected PV-battery hybrid system is depicted in Fig. 1. The high-voltage (HV) dc port is connected to the PV unit, and the low-voltage (LV) dc port is connected to the battery. The dc-port voltages are defined as V_H and V_L. And the currents of the PV-battery hybrid system

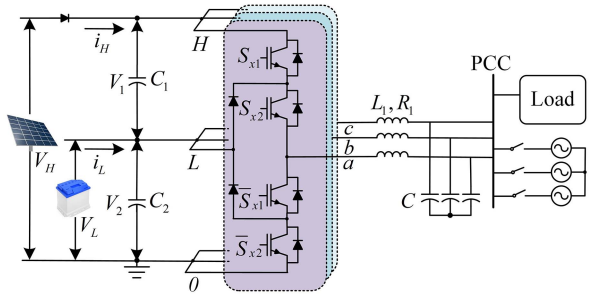

Fig. 1. Topology of SSMPI-connected PV-battery hybrid system.

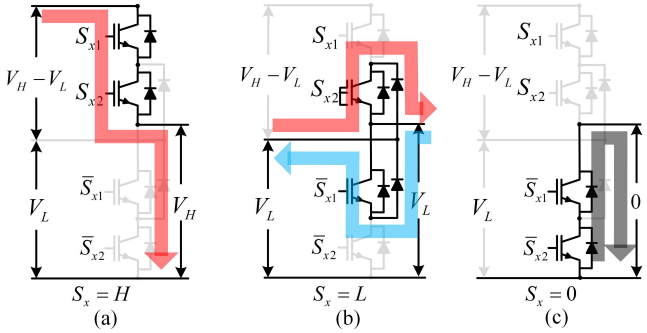

Fig. 2. Switching states and current paths in phase x. (a) $S_x = H$, the PV unit supports the AC grid. (b) $S_x = L$, the battery releases/absorbs power to/from the AC grid. (c) $S_x = 0$, fly-wheel mode.

TABLE I
SWITCHING STATES AND OUTPUT VOLTAGES OF THE SSMPI

$S_{x1}S_{x2}$	Switching state S_x	Output voltage
11	H	V_H
01	L	V_L
00	0	0

are i_H and i_L. The dc-side capacitors are assumed to be equal, i.e., $C_1 = C_2$. Then, the voltages of the dc-side capacitors can be expressed as $V_1 = V_H - V_L$ and $V_2 = V_L$. On the ac side, the SSMPI connects to the point of common coupling via an *LC* filter.

Each leg of the SSMPI has four active switches, i.e., S_{x1}, S_{x2}, $\bar{S}_{x1}$, and $\bar{S}_{x2}(x = a, b, c)$. Three different switching states S_x can be obtained as follows:

$$\begin{cases} S_x = H & S_{x1} = 1, S_{x2} = 1 \\ S_x = L & S_{x1} = 0, S_{x2} = 1 \\ S_x = 0 & S_{x1} = 0, S_{x2} = 0. \end{cases} \tag{1}$$

Fig. 2 shows the switching states and current paths in phase x: (a) $S_x = H$, the PV unit supports the ac grid, (b) $S_x = L$, the battery releases/absorbs power to/from the ac grid, and (c) $S_x = 0$, fly-wheel mode. The output voltages are V_H, V_L, and 0, respectively. The switching states and their corresponding output voltages are given in Table I.

B. Control of SSMPI-Connected PV-Battery Hybrid System

Fig. 3 shows the block diagram of the control strategy for the SSMPI-connected PV-battery hybrid system. On the dc side,

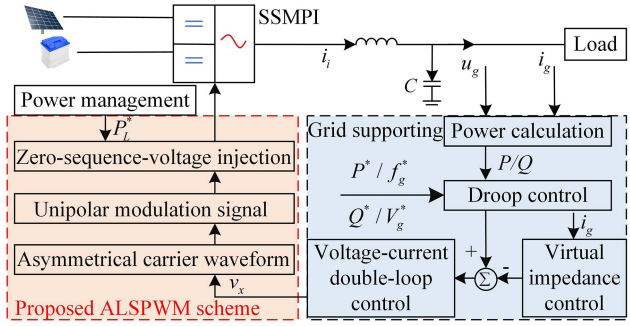

Fig. 3. Block diagram of control strategy for SSMPI-connected PV-battery hybrid system.

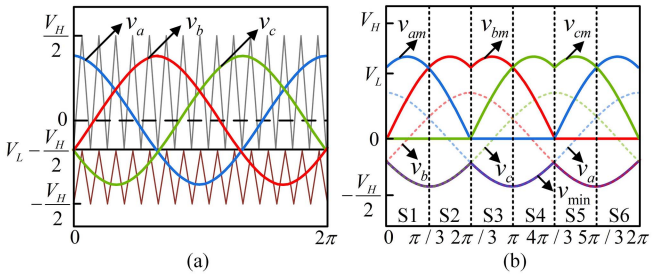

Fig. 4. Modulation signals for SSMPI. (a) Original three-phase modulation signals with asymmetrical carriers. (b) Non-negative modulation signals.

the reference output power of the battery P_L^* can be obtained according to the power management strategy [41]. The SSMPI is regulated as a grid-supporting power converter in this study. Detailed grid supporting control structure can be found in [42], including droop control, virtual impedance control, and voltage-current double-loop control. The contribution of this study is the proposed ALSPWM scheme, which will be detailed in Section III.

III. PROPOSED ALSPWM-BASED POWER DISTRIBUTION SCHEME

As shown in Fig. 3, the implementation process of the proposed ALSPWM includes three steps: asymmetrical carrier waveform definition, unipolar modulation signal generation, and zero-sequence-voltage injection. Detailed descriptions of each step are given in the following text.

A. Asymmetrical Carrier Waveform

As shown in Fig. 1, the topology of the SSMPI is similar to the traditional three-level neutral-point-clamped (3L-NPC) inverter. The carrier waveforms in the SSMPI are level-shifted, and both are in the same phase. However, unlike the symmetrically displaced carrier waveform with respect to the zero-axis in 3L-NPC inverters, the carrier waveforms are asymmetrical in SSMPI due to the time-variable dc input voltages. The amplitudes of the two carriers are proportional to the dc input voltages $(V_H - V_L)$ and V_L, respectively. The boundary line for the carrier waveform can be derived as $(V_L - V_H/2)$, as shown in Fig. 4(a). When

($2V_L < V_H$), the boundary line lies below the zero-axis, and the amplitude of the top carrier waveform is larger than that of the bottom one. When ($2V_L > V_H$), the situation is contrary to the former one. It is worth mentioning that when ($2V_L = V_H$), the boundary line is located on the zero-axis, and the amplitudes of two carrier waveforms are equal to each other, which means that the carrier waveform of the traditional three-level converter is only a special case of the SSMPI. Due to space constraints, only the detailed analysis of ($2V_L > V_H$) will be given in this article, and the other case can be studied in a similar manner.

B. Unipolar Modulation Signal-Based Instantaneous Power Model

As mentioned above, the modulation target of the SSMPI is to track the desired port power reference. To achieve the desired power distribution between the dc ports, the foremost step is to deduce the instantaneous port power model based on the modulation signals.

Assuming that the original three-phase modulation signals are sinusoidal and defined as v_a, v_b, and v_c, respectively, it can be written as follows:

$$\begin{cases} v_a = v_m \cos\theta \\ v_b = v_m \cos(\theta - 2\pi/3) \\ v_c = v_m \cos(\theta + 2\pi/3) \end{cases} \tag{2}$$

where v_m is the amplitude of the phase voltage, and θ is the phase angle.

In this model, three variables (v_a, v_b, and v_c) are determined for the power distribution control, which is complicated. To simplify the model, the unipolar modulation signal is derived in this article. The modulation signals can be normalized to a non-negative value as follows:

$$v_{xm} = v_x - v_{\min} \tag{3}$$

where $v_{\min} = \{v_a, v_b, v_c\}_{\min}$.

As shown in Fig. 4, the modulation signal can be categorized into six sections according to the value of v_{xm}. In each section, the power distribution control can be analytically realized.

C. Zero-Sequence-Voltage Injection

In the proposed ALSPWM, zero-sequence voltage can be properly injected into the modulation signal without affecting the output converter voltage. This degree of freedom can be employed for power distribution in SSMPI. After adding the zero-sequence voltage v_0, (3) is replaced by the following:

$$v'_x = v_{xm} + v_0. \tag{4}$$

The feasible span of the zero-sequence voltage that can be injected is $v_0 \in [0, V_H - v_{\max}]$ and $v_{\max} = \{v_{am}, v_{bm}, v_{cm}\}_{\max}$.

According to the results of v'_x, the analysis is performed in six sections (i.e., S1–S6) shown in Fig. 4(b). For instance in Section S1, the value of v'_x satisfies $v'_a\, v'_b\, v'_c$. Only the detailed analysis of the instantaneous power model in Section S1 is given here, and the other case can be studied in a similar manner.

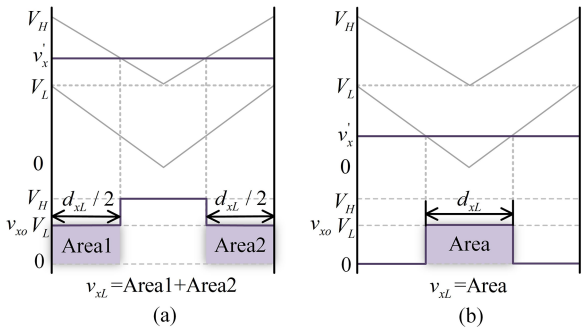

Fig. 5. Switching state and output voltage of phase x. (a) Case I: $v'_x \geq V_L$. (b) Case II: $v'_x < V_L$.

The ALSPWM technique is considered to generate the switching pulses for the SSMPI. Two triangular carriers with equal frequency are level-shifted above the zero-axis, whose amplitudes are proportional to dc-port voltages. In one switching cycle, the modulation signals with zero-sequence-voltage injection intersect with upper or lower level-shifted carriers according to the relationship of v'_x and V_L, as shown in Fig. 5. With the graphical method, duty cycles for the lower switching pairs can be derived as follows:

$$d_{xL} = \begin{cases} 1 - \dfrac{v'_x - V_L}{V_H - V_L} & \text{if } v'_x \geq V_L \\ \dfrac{v'_x}{V_L} & \text{if } v'_x < V_L. \end{cases} \tag{5}$$

Therefore, the output voltage of the LV dc port can be denoted as follows:

$$v_{xL} = V_L d_{xL} = \begin{cases} \varepsilon(V_H - v'_x) & \text{if } v'_x \geq V_L \\ v'_x & \text{if } v'_x < V_L \end{cases} \tag{6}$$

where $\varepsilon = V_L/V_H - V_L$. The area of shaded regions in Fig. 5 represents the output voltage of the LV dc port.

Generally, phase current contributes to the LV dc port if and only if this phase is connected to the LV dc port. Assuming that the frequency of the carrier waveform is much higher than that of modulation signals, the phase current can be considered as a fixed value in a switching cycle. The instantaneous output power of the LV dc port can be written as follows:

$$P_L = \sum_{x=a,b,c} v_{xL} i_x \tag{7}$$

where $i_x, x \in \{a, b, c\}$ is the phase current.

To be general, the modulation index is set to a small value for analysis. The modulation signals meet the relationship of $v'_a \geq v'_b \geq v'_c$ in Section S1. In this section, (4) can be rewritten as follows:

$$\begin{cases} v'_a = v_a - v_c + v_0 \\ v'_b = v_b - v_c + v_0 \\ v'_c = v_0. \end{cases} \tag{8}$$

Taking the value of V_L into consideration, the power distribution in SSMPI can be divided into four cases, as shown in Table II. In the following text, the four cases are analyzed one

TABLE II
MODULATION SIGNALS IN SECTION S1

Case	Condition	Port Power Distribution
I	$V_L \geq v'_a \geq v'_b \geq v'_c$	No available
II	$v'_a > V_L \geq v'_b \geq v'_c$	Yes
III	$v'_a \geq v'_b > V_L \geq v'_c$	Yes
IV	$v'_a \geq v'_b \geq v'_c > V_L$	No available

by one to clarify the idea of the proposed ALSPWM for power distribution.

1) Case I: In this case, the output voltage of the LV dc port v_{xL} can be denoted as follows:

$$\begin{cases} v_{aL} = v_a - v_c + v_0 \\ v_{bL} = v_b - v_c + v_0 \\ v_{cL} = v_0. \end{cases} \tag{9}$$

The instantaneous output power of the LV dc port can be written as follows:

$$\begin{aligned} P_L &= v_{aL}i_a + v_{bL}i_b + v_{cL}i_c \\ &= (v_a - v_c)i_a + (v_b - v_c)i_b + v_0(i_a + i_b + i_c). \end{aligned} \tag{10}$$

As $i_a + i_b + i_c = 0$ is satisfied in a three-phase three-wire system, P_L can be rewritten as follows:

$$P_L = (v_a - v_c)i_a + (v_b - v_c)i_b. \tag{11}$$

Therefore, the port power is not adjustable by regulating v_0 in Case I due to the lack of control freedom.

2) Case II: In this case, the output voltage of the LV dc port v_{xL} can be denoted as follows:

$$\begin{cases} v_{aL} = \varepsilon(V_H - v_a - v_0 + v_c) \\ v_{bL} = v_b - v_c + v_0 \\ v_{cL} = v_0. \end{cases} \tag{12}$$

The instantaneous output power of the LV dc port can be written as follows:

$$\begin{aligned} P_L &= v_{aL}i_a + v_{bL}i_b + v_{cL}i_c \\ &= \varepsilon(V_H - v_a + v_c)i_a + (v_b - v_c)i_b - (1+\varepsilon)v_0 i_a. \end{aligned} \tag{13}$$

The desired zero-sequence voltage v_0 for power distribution can be calculated by setting $P_L = P_L^*$

$$v_0 = \frac{\varepsilon(V_H - v_a + v_c)i_a + (v_b - v_c)i_b - P_L^*}{(1+\varepsilon)i_a}. \tag{14}$$

3) Case III: In this case, the output voltage of the LV dc port v_{xL} can be denoted as follows:

$$\begin{cases} v_{aL} = \varepsilon(V_H - v_a + v_c - v_0) \\ v_{bL} = \varepsilon(V_H - v_b + v_c - v_0) \\ v_{cL} = v_0. \end{cases} \tag{15}$$

The instantaneous output power of the LV dc port can be written as follows:

$$\begin{aligned} P_L &= v_{aL}i_a + v_{bL}i_b + v_{cL}i_c \\ &= \varepsilon(V_H - v_a + v_c)i_a + \varepsilon(V_H - v_b + v_c)i_b + (1+\varepsilon)v_0 i_c. \end{aligned} \tag{16}$$

The desired zero-sequence voltage v_0 for power distribution can be calculated by setting $P_L = P_L^*$

$$v_0 = \frac{\varepsilon(V_H + v_c)i_c + \varepsilon v_a i_a + \varepsilon v_b i_b + P_L^*}{(1+\varepsilon)i_c}. \tag{17}$$

4) Case IV: In this case, the output voltage of the LV dc port v_{xL} can be denoted as follows:

$$\begin{cases} v_{aL} = \varepsilon(V_H - v_a + v_c - v_0) \\ v_{bL} = \varepsilon(V_H - v_b + v_c - v_0) \\ v_{cL} = \varepsilon(V_H - v_0). \end{cases} \tag{18}$$

The instantaneous output power of the LV dc port can be written as follows:

$$\begin{aligned} P_L &= v_{aL}i_a + v_{bL}i_b + v_{cL}i_c \\ &= \varepsilon((-v_a + v_c)i_a + (-v_b + v_c)i_b) \\ &\quad + \varepsilon(V_H - v_0)(i_a + i_b + i_c). \end{aligned} \tag{19}$$

As $i_a + i_b + i_c = 0$ is satisfied in a three-phase three-wire system, P_L can be rewritten as follows:

$$P_L = \varepsilon\left((-v_a + v_c)i_a + (-v_b + v_c)i_b\right). \tag{20}$$

Therefore, the port power is also not adjustable by regulating v_0 in Case IV due to the lack of control freedom.

In conclusion, the instantaneous port power cannot be regulated in Cases I and IV due to the nonexistence of control freedom. The instantaneous port power can be regulated in Cases II and III via properly zero-sequence voltage injection. The process of the proposed method with zero-sequence-voltage injection is illustrated in Fig. 7.

D. Power Distribution Capability Analysis

According to the above discussion, the proposed power distribution method is achieved by injecting zero-sequence voltage in Cases II and III. Therefore, zero-sequence voltage v_0 should meet some constraints to avoid unavailable power distribution in Cases I and IV.

Considering Case I of the proposed scheme in Fig. 6, the maximum value of modulation signals $v_{\max}$ should exceed V_L via the zero-sequence-voltage injection so that Case I can turn into Case II. Therefore, the lower bound of v_0 can be calculated as follows:

$$v_0 \geq V_L - v_{\max}. \tag{21}$$

In Case IV of the proposed scheme, the modulation signals cannot intersect the lower carrier due to the zero-sequence-voltage injection, resulting in fixed output power of the LV dc port. To avoid this case, the upper bound of v_0 should be limited as follows:

$$v_0 \leq V_L. \tag{22}$$

Besides, in order to ensure the SSMPI operates in line modulation range, the range of v_0 can be written as follows:

$$0 \leq v_0 \leq V_H - v_{\max}. \tag{23}$$

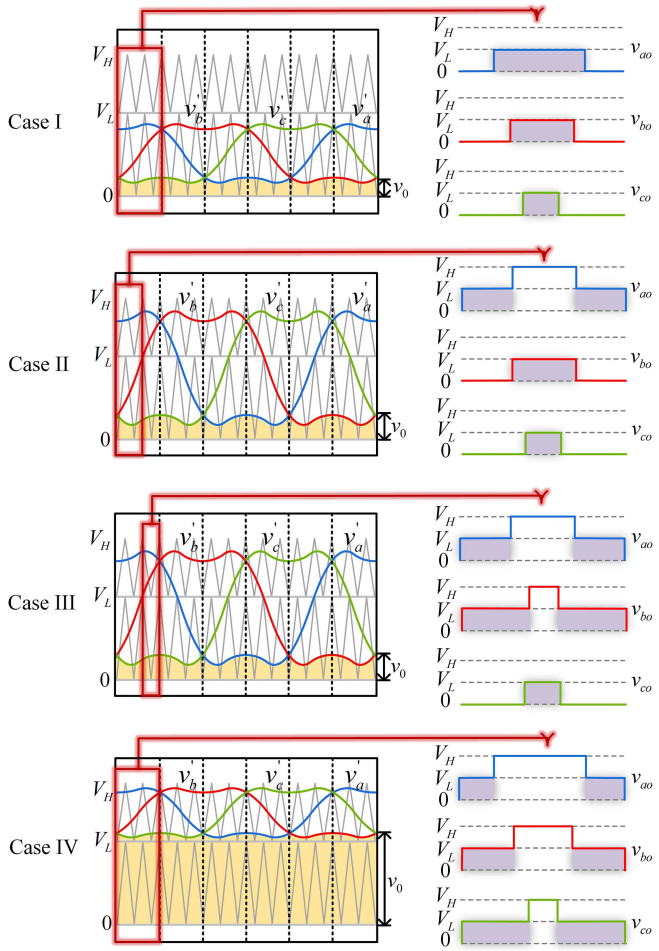

Fig. 6. Switching sequences of the SSMPI in Section S1 under four cases.

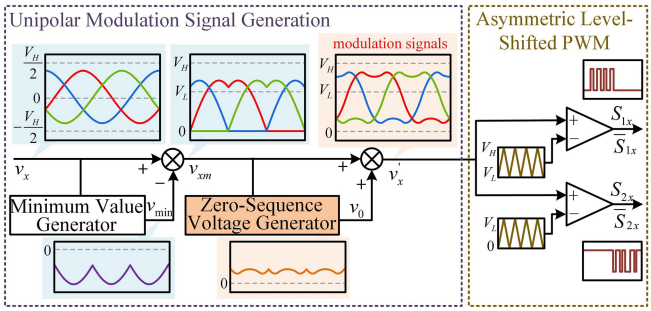

Fig. 7. Block diagram of the proposed ALSPWM with zero-sequence-voltage injection.

Combining (21) to (23), the range of v_0 is calculated as follows:

$$v_{0\min} \le v_0 \le v_{0\max} \tag{24}$$

where $v_{0\min} = \{0, V_L - v_{\max}\}_{\max}$ and $v_{0\max} = \{V_L, V_H - v_{\max}\}_{\min}$.

Substituting (24) into (13) and (16), the maximum and minimum output power of the LV dc port can be calculated and determines the power distribution range. The power distribution range of Cases II and III shares a boundary line, which is related to the condition that v_{bL} in (12) and (18) are equal, as shown in Fig. 8.

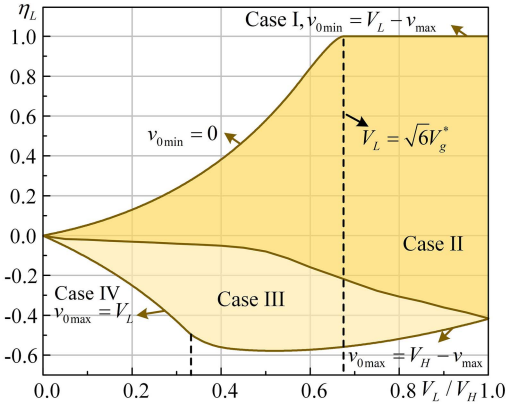

Fig. 8. LV DC port power ratio η_L versus different port voltage ratios V_L/V_H.

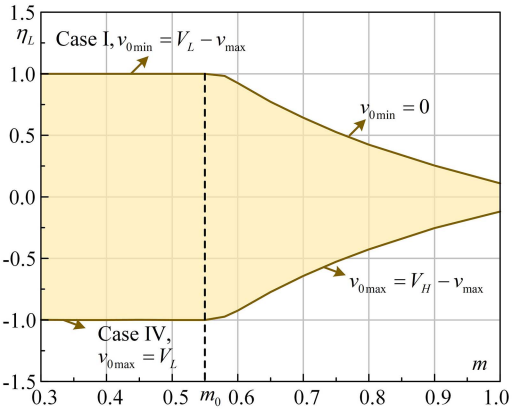

Fig. 9. LV DC port power ratio η_L versus different modulation index m.

The port power ratio is expressed as follows:

$$\eta_L = \frac{P_L}{P} \tag{25}$$

where P defines the total active power of the energy source system. Ignoring the power losses, P is equivalent to the active power on the ac side, which is calculated as follows:

$$P = v_a i_a + v_b i_b + v_c i_c. \tag{26}$$

Fig. 8 shows LV dc port power ratio η_L versus different port voltage ratios V_L/V_H. As shown in Fig. 8, the LV dc port is able to support the microgrid independently when $V_L = \sqrt{6}V_g^*$, i.e., $\eta_L = 1$ can be achieved. When ($V_L < \sqrt{6}V_g^*$), the range of the LV dc port power ratio increases with the rise in the port voltage ratio, which means an enhanced output power capability on the LV dc port. When ($V_L > \sqrt{6}V_g^*$), the power distribution range decreases with the increase of the port voltage ratio. In the SSMPI system, a wider power distribution range implies an expanded scope of applicability. Considering this, the port voltage ratio is recommended to be set at 0.6–0.8 for a wider power distribution range for the SSMPI.

TABLE III
PARAMETERS OF THE SSMPI-CONNECTED PV-BATTERY HYBRID SYSTEM

Low voltage	$V_L = 160-240$V
High voltage	$V_H = 400$V
DC-side capacitance	$C_1 = C_2 = 4920\ \mu$F
LC-Filter inductance	$L_1/R_1 = 3\ m$H/0.4 Ω
LC-Filter capacitance	$C = 15\ \mu$F
Sampling period/frequency	$T_s = 100\ \mu$s/$f_s = 10$ kHz
Rated ac-side voltage	$V_g^* = 110$ V
Rated ac-side frequency	$f_g^* = 50$ Hz
Rated ac-side active power	$P^* = 1000$W
Rated ac-side reactive power	$Q^* = 0$ var

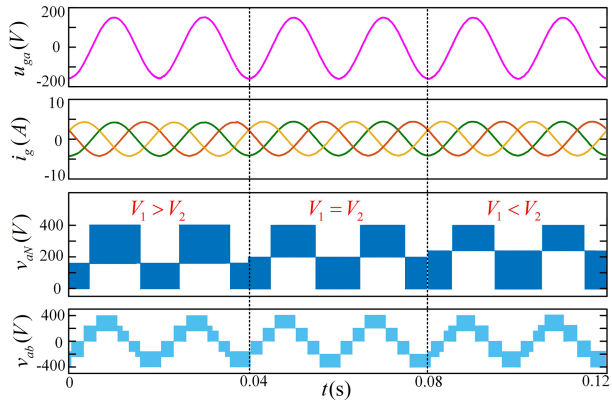

Fig. 10. Simulation results under asymmetrical DC-port voltages. From top to bottom, waveform is AC-side voltage u_{ga}, three-phase current i_g, phase voltage v_{aN}, and line-to-line voltage v_{ab}.

Fig. 9 shows LV dc port power ratio η_L versus different modulation index m. The modulation index is defined as $m = 2\sqrt{2}V_g^*/V_H$. The power ratio curves in Fig. 9 are obtained in the case of port voltage ratio $V_L/V_H = 0.5$. As the modulation index m increases, the port power distribution range decreases. The essential reason is that the degree of freedom provided by the zero-sequence voltage v_0 decreases with the increase of modulation index m. The system enjoys a large power distribution range when the modulation index is set to a small value. When $m < m_0$, the LV dc port is able to supply the ac side independently, i.e., $\eta_L = 1$ can be obtained. However, the utilization rate of dc-side voltage would be reduced with a small modulation index m. Hence, the tradeoff between power distribution range and utilization rate of dc-side voltage should be considered. In this study, the modulation index m is set as 0.78.

IV. SIMULATION RESULTS

Simulation tests have been conducted in the MATLAB/Simulink environment to validate the effectiveness of the proposed power distribution strategy. Table III shows the parameters of the SSMPI-connected PV-battery hybrid system. The dc-side capacitors are utilized to absorb the high-frequency components of dc-side current. The *LC* filter is adopted to improve the ac-side current quality, and the design rules can be found in [43] and [44]. The rated ac-side active/reactive power is set as $P^* = 1000$ W/$Q^* = 0$ var.

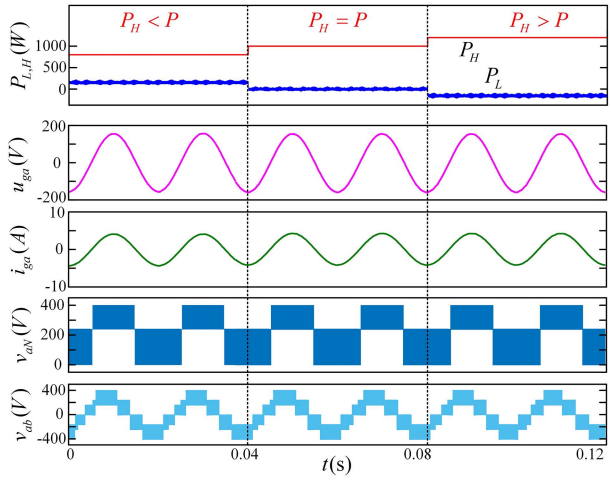

Fig. 11. Simulation results of the different power distribution cases under $V_1 < V_2$. From top to bottom, waveform is DC-port output power P_H/P_L, AC-side voltage u_{ga}, AC-side current i_{ga}, phase voltage v_{aN}, and line-to-line voltage v_{ab}.

Fig. 10 shows the simulation results under asymmetrical dc-port voltages. From top to bottom, waveform is ac-side voltage u_{ga}, three-phase current i_g, phase voltage v_{aN}, and line-to-line voltage v_{ab}. In Fig. 10, the voltages of the LV dc port are set as 160, 200, and 240 V, respectively. The phase voltage and line-to-line voltage are unbalanced under asymmetrical dc-port voltages. Though dc-port voltages are asymmetrical, high-quality ac-side voltage and current can be achieved.

Fig. 11 shows the simulation results of the different power distribution cases under $V_1 < V_2$. From top to bottom, waveform is dc-port output power P_H/P_L, ac-side voltage u_{ga}, ac-side current i_{ga}, phase voltage v_{aN}, and line-to-line voltage v_{ab}. In Fig. 11, the reference power of the HV dc port is set as 800, 1000, and 1200 W, respectively. Under different power distribution cases, the HV dc-port output power P_H is precisely controlled. Ripple power is concentrated in the LV dc port. In addition, desirable ac-side voltage and current have been obtained.

The simulation results in Figs. 10 and 11 indicate that the proposed strategy is effective for asymmetrical dc-port voltages and different power distribution cases.

V. EXPERIMENTAL RESULTS

A downscaled experimental test rig is established in the laboratory to verify the proposed ALSPWM strategy, which is depicted in Fig. 12. The system parameters are given in Table III. Two programmable dc sources are employed as the PV-battery hybrid energy storage components. The ac load is selected as a resistance box that is connected to the SSMPI via the *LC* filter. The SSMPI is implemented by three insulated-gate bipolar transistors power modules (Infineon F3L75R07W2E3). A dSPACE MicroLabBox DS1202 is used to implement the control algorithm and generate the switching signals. The sampling period/frequency is selected as $T_s = 100\ \mu$s/$f_s = 10$ kHz. The switching frequency of SSMPI is also set as 10 kHz. A multichannel oscilloscope is used to acquire the experimental waveform.

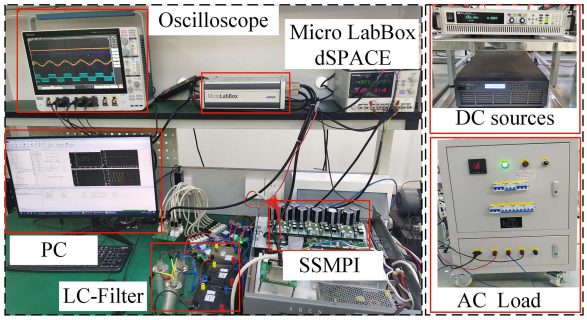

Fig. 12. Experimental test rig.

The steady-state results under asymmetrical dc-port voltages and different power distribution cases are given first. Then, the dynamic tests of variable dc-port power and ac-side power are carried out. Finally, the comparative tests between the previous strategy and the proposed strategy are presented.

A. Steady-State Results

The steady-state performance of the proposed strategy is investigated, including tests with asymmetrical dc-port voltages and variable power distribution. The experimental tests are conducted in the case of rated ac-side power.

1) *Steady-state performance under asymmetrical dc-port voltages:* Fig. 13 shows the steady-state performance under asymmetrical dc-port voltages: (a) in the case of $V_1 > V_2$, (b) in the case of $V_1 = V_2$, and (c) in the case of $V_1 < V_2$. From top to bottom, waveform is line-to-line voltage v_{ab}, phase voltage v_{aN}, ac-side voltage u_{ga}, and ac-side current i_{ga}. The voltage of the HV dc port is set to $V_H = 400$ V. And the voltages of the LV dc port are set to $V_L = 160, 200,$ and 240 V in Fig. 13(a), (b), and (c), respectively. The total harmonic distortions (THDs) of ac-side current are also given. The ac-side current THDs are 2.75%, 2.73%, and 2.73% in Fig. 13(a), (b), and (c), respectively. The high-quality ac-side currents indicate that the proposed strategy is effective for asymmetrical dc-port voltages.

2) *Results under different power distribution cases:* Fig. 14 shows steady-state performance of the different power distribution cases under $V_1 < V_2$: (a) $P_H = 800$ W, $P_L = 200$ W, (b) $P_H = 1000$ W, $P_L = 0$ W, and (c) $P_H = 1200$ W, $P_L = -200$ W. From top to bottom, waveform is dc-port output power P_H/P_L, ac-side voltage/current u_{ga}/i_{ga}, and phase voltage $v_{aN}/v_{bN}/v_{cN}$. In Fig. 14(a), the HV dc port tracks the reference power value 800 W as desired, and the output power of the LV dc port is 200 W. The ac-side power is supported by the HV dc port alone in Fig. 14(b). In Fig. 14(c), the HV dc port supplies power to the ac-side and charges to the LV dc port. Although power distribution conditions are different in Fig. 14, beneficial ac-side voltage/current and phase voltage can be achieved. From the zoom-in figure, the switching sequences of SSMPI are consistent with the theoretical analysis in Section III. The proposed ALPWM strategy outputs seven-segment PWM signals. It can be concluded that flexible power distribution can be achieved by the proposed strategy.

B. Dynamic Results

Apart from the steady-state tests, the dynamic tests are also carried out to verify the effectiveness of the proposed method. In this study, the variable dc-port power and ac-side power tests are investigated.

1) *Dynamic results of variable dc-port power with constant ac-side power:* Fig. 15 gives the dynamic results of variable dc-port power with P_H reference stepped from 800 W to 1200 W then stepped back to 800 W. From top to bottom, the waveform is dc-port output power P_H/P_L, ac-side voltage/current u_{ga}/i_{ga}, and phase voltage $v_{aN}/v_{bN}/v_{cN}$. The HV port power P_H changes from 800 W to 1200 W, then changes to 800 W. Accordingly, the LV port power P_L changes from 200 W to -200 W, then changes to 200 W. The dc-port power changes instantaneously as desired. This test is conducted in the case of rated ac-side power. Desirable ac-side voltage and current can be guaranteed, even in the dynamic moment. Hence, the proposed method has fast dynamic performance in the case of variable dc-port power.

2) *Dynamic results of variable ac-side power tests:* Fig. 16 shows the dynamic results of variable dc-port power with P_H reference stepped from 800 W to 1200 W then stepped back to 800 W. From top to bottom, the waveform is dc-port output power P_H/P_L, ac-side voltage/current u_{ga}/i_{ga}, and phase voltage $v_{aN}/v_{bN}/v_{cN}$. The HV dc port power is regulated as 1000 W to simulate the constant PV generation system. When the ac-side power changes from 1000 W to 375 W, the LV dc port is used to absorb the excess power. Similar results can be realized when the ac-side power changes from 375 W to 1000 W. Once the ac-side power increases or decreases, the ac-side current changes rapidly. Though ac-side power has changed, beneficial ac-side voltage and phase voltage can be ensured. Therefore, the proposed method has smooth dynamic performance under variable ac-side power.

C. Comparison Results

The comparative tests between the previous and the proposed strategies are presented, including the THD of ac-side current, computational burden, and power conversion efficiency.

1) *THD of ac-side current:* Fig. 17 gives the ac-side current fast Fourier transform (FFT) results: (a) Proposed method, (b) previous method [36]. From top to bottom, the waveform is ac-side current i_{ga} and its spectrum. The ac-side current THDs of the proposed method and the previous method [36] are 2.74% and 2.96%, respectively. Hence, the proposed method provides higher grid-side current quality than the previous method [36].

2) *Computational burden:* As shown in Fig. 18, the execution time of the proposed method and the previous method [36] are obtained by the dSPACE profiler 3.8. The proposed method and the previous method [36] have the same execution time of A/D and other calculation processes in the hardware layer. As for the execution time of the modulation and power control algorithm, it costs 10.01 μs and 11.32 μs to carry out the proposed method and the previous method. Therefore, 13.09%

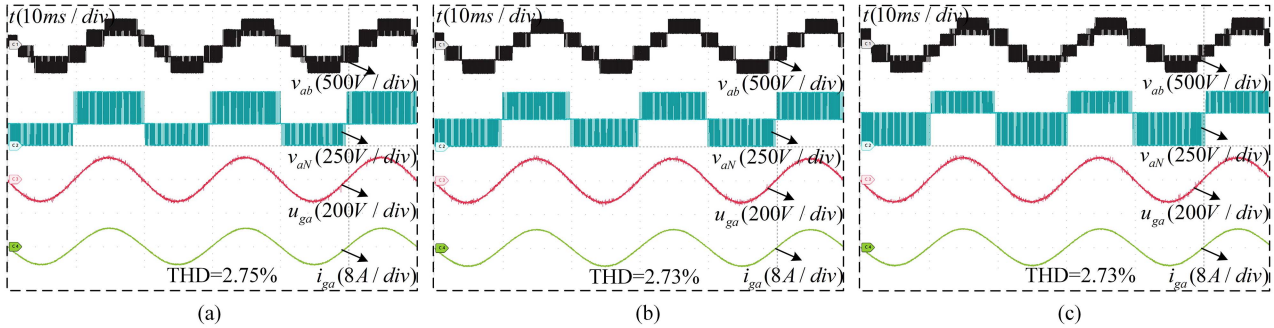

Fig. 13. Steady-state performance under asymmetrical DC-port voltages. (a) In the case of $V_1 > V_2$. (b) In the case of $V_1 = V_2$. (c) In the case of $V_1 < V_2$. From top to bottom, waveform is line-to-line voltage v_{ab}, phase voltage v_{aN}, AC-side voltage u_{ga}, and AC-side current i_{ga}.

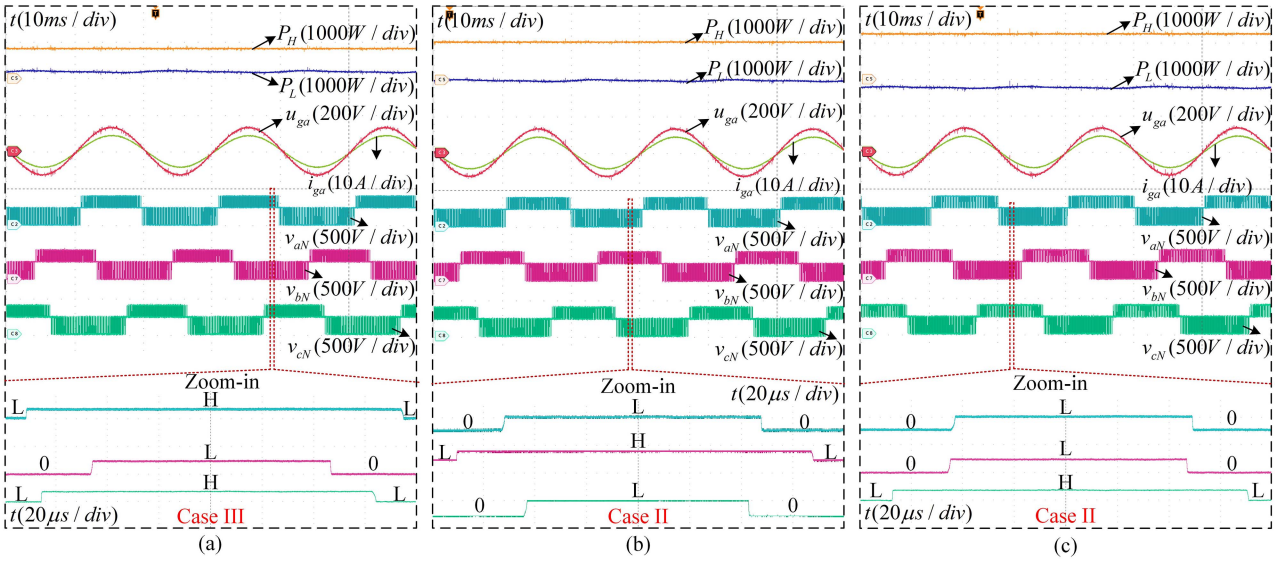

Fig. 14. Steady-state performance of different power distribution cases under $V_1 < V_2$. (a) $P_H = 800$ W, $P_L = 200$ W. (b) $P_H = 1000$ W, $P_L = 0$ W. (c) $P_H = 1200$ W, $P_L = -200$ W. From top to bottom, waveform is DC-port output power P_H/P_L, AC-side voltage/current u_{ga}/i_{ga}, and phase voltage $v_{aN}/v_{bN}/v_{cN}$.

computational burden reduction can be realized by the proposed method.

3) *Power conversion efficiency:* The power conversion efficiency is utilized to describe the power loss, which is calculated by the power analyzer YOKOGAWA WT1803E. The power conversion efficiency test circuit is shown in Fig. 19. Where W_1 and W_2 are the dc-side input power, W_3 and W_4 indicate the ac-side output power. Then, the system efficiency η_s can be calculated as follows:

$$\eta_s = \frac{W_3 + W_4}{W_1 + W_2}. \tag{27}$$

Fig. 20 gives the power conversion efficiency of the proposed method and the previous method [36] with different dc-port voltage ratios V_L/V_H. The results in Fig. 20 reflect the efficiency of SSMPI in the case of variable dc input voltages. As shown in Fig. 20, the power conversion efficiency of the proposed method (blue line) is about 0.5% higher than that of the previous method (red line). The reason is that the switching actions of the proposed method are fewer than those of the previous method.

4) *Dynamic response time:* Fig. 21 shows the dynamic response time of different methods: (a) previous method [36], (b) proposed method. These tests are carried out under the condition of HV dc-port power P_H changes from 1200 W to 800 W. As shown in Fig. 21(a), the dynamic response time of the previous method [36] is around 15 ms. In the proposed method, the HV dc-port power P_H instantaneously changes from 1200 W to 800 W due to power distribution being directly realized in the modulation layer.

D. Overall Comparison With the Previous Strategy

Table IV shows the comparison of the power distribution strategies for SSMPI, including current THD, computational burden, efficiency, and dynamic response. In [30], the computational burden is large due to complicated multiobjective-based

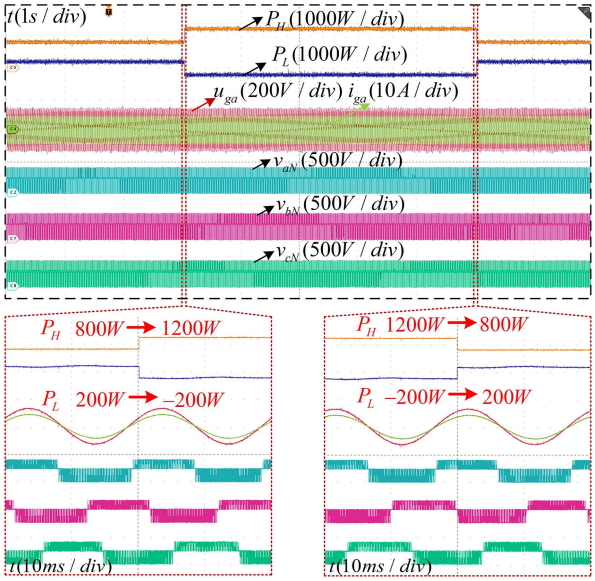

Fig. 15. Dynamic results of variable DC-port power with P_H stepped from 800 W to 1200 W then stepped back to 800 W. From top to bottom, the waveform is DC-port output power P_H/P_L, AC-side voltage/current u_{ga}/i_{ga}, and phase voltage $v_{aN}/v_{bN}/v_{cN}$.

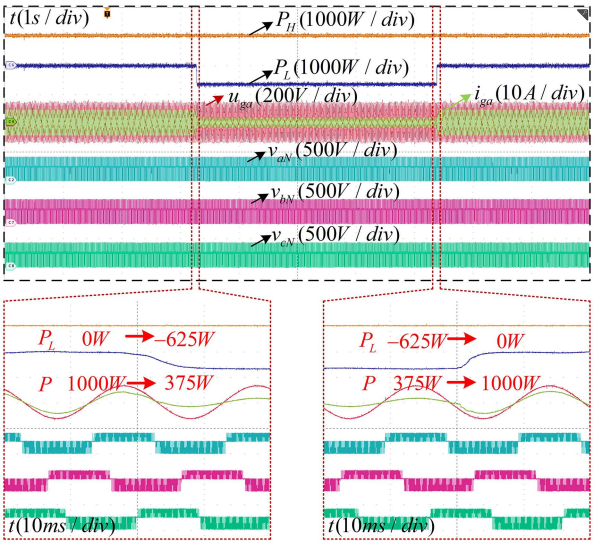

Fig. 16. Dynamic results of variable AC-side power with P stepped from 1000 W to 375 W then stepped back to 1000 W. From top to bottom, the waveform is DC-port output power P_H/P_L, AC-side voltage/current u_{ga}/i_{ga}, and phase voltage $v_{aN}/v_{bN}/v_{cN}$.

TABLE IV
COMPARISON OF THE POWER DISTRIBUTION STRATEGIES FOR SSMPI

REF	Current THD	Computational burden	Efficiency	Dynamic response
[26]	Good	Large	High	Fast
[27]–[29]	Good	Medium	High	Slow
[30], [31]	Medium	Large	High	Slow
[32]	Medium	Medium	Low	Slow
Proposed	Good	Small	High	Fast

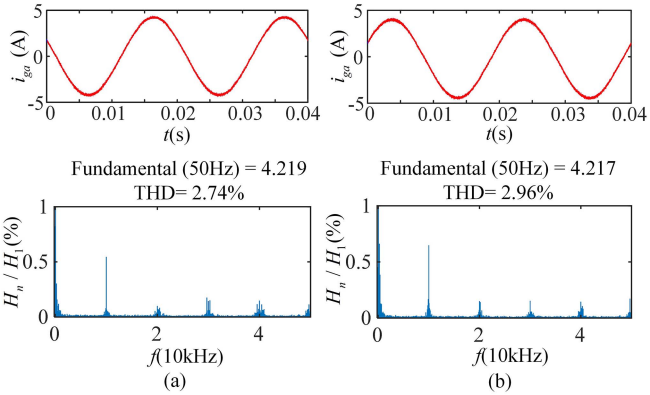

Fig. 17. AC-side current FFT results. (a) Proposed method. (b) Previous method [36]. From top to bottom, the waveform is AC-side current i_{ga} and its spectrum.

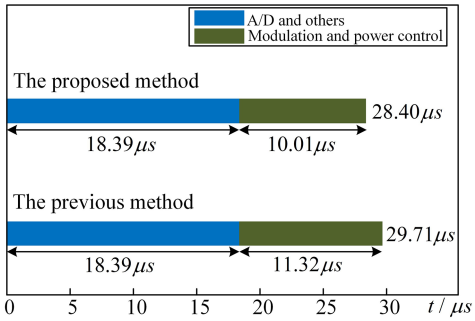

Fig. 18. Tested execution time of the proposed method and the previous method [36].

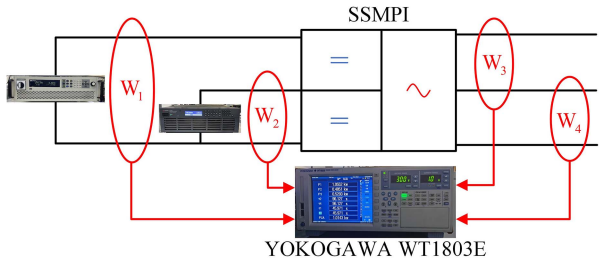

Fig. 19. Power conversion efficiency test circuit.

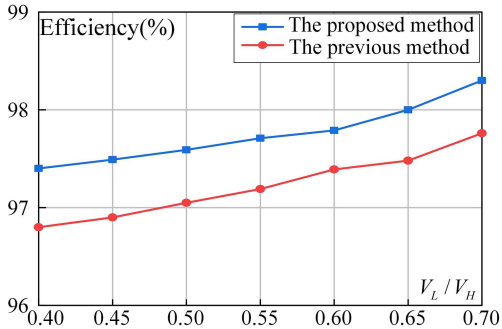

Fig. 20. Power conversion efficiency of the proposed method and the previous method [36] with different DC-port voltage ratios V_L/V_H.

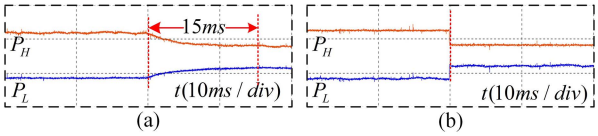

Fig. 21. Dynamic response time of different methods. (a) Previous method [36]. (b) Proposed method.

calculations being unavoidable. The dynamic response in [31], [32], and [33] is slow because of the outer power control loop. In [34] and [35], regulating redundant small vectors would deteriorate the ac current control performance and increase the computational burden. A power decoupled model is proposed in [36], which causes extra switching losses and reduces current quality. In the proposed ALPWM, good current THD and a small computational burden can be realized. The proposed strategy also offers high system efficiency. In addition, the dynamic response is fast due to power distribution being realized in the modulation layer.

VI. Conclusion

This article proposes an ALSPWM scheme for flexible power distribution of the SSMPI-connected islanded microgrid under time-varying dc input voltage. An instantaneous power model based on three-phase modulation waves is derived, and a precise zero-sequence injection method is put forward for desired power distribution control. Besides, a unified expression of the modulation signals with proportional variable magnitude is proposed to deal with pulse train generation under time-varying input voltages. As a result, the flexible power distribution between the energy storage components is realized with the desired grid current control performance under time-varying dc input voltage. Experimental results verified that the proposed ALSPWM scheme has the following advantages compared with the previous method [36].

1) The power conversion efficiency of the proposed scheme is 0.5% higher than that of the previous method.
2) The steady-state THD value is improved by 8.03% at the rated operating point.
3) The computational burden can be reduced by 13.09%.
4) The dynamic response time can be reduced by 15 ms.

However, the leakage current generated by the PV unit in SSMPI, which results in current distortion, electromagnetic interface, and safety issues, still calls for future work.

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