Letters

An Input-Coupling *LLC* Converter With Wide Input Voltage Range and High Efficiency

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***Abstract*—The *LLC* full-bridge converter is a highly efficient solution for high-power secondary power supply applications. It is known for its low stress operation and reduced electromagnetic radiation. However, it has a relatively narrow optimized switching frequency and is very sensitive to input voltage variations, particularly at low input voltage conditions. Achieving a balance between a wide input voltage range and high efficiency is challenging. This article proposes an input-coupling type *LLC* converter (IC-*LLC*) as a solution. The resonant converter shares the input voltage with a pre-stage. Power is transferred through the prestage during half of the switching cycle, while the resonant stage takes charge during the other half cycle. This results in an improvement in the efficiency of the converter. A 1.5-kW IC-*LLC* converter system was built and tested. Experimental results show that the input coupling mechanism significantly enhances the efficiency of the dual-stage conversion setup, overcoming the operational challenges associated with *LLC* converters.**

***Index Terms*—Dual-stage converter, input-coupling, *LLC* converter, wide step-up range.**

I. Introduction

RESONANT converters are widely used in various applications, such as electric vehicle battery chargers, distributed power grids, energy routers, solid-state transformers, and more. They are preferred due to their capability to achieve zero-voltage switching (ZVS) and zero-current switching (ZCS) [1]. However, fluctuations in the input voltage cause notable changes to the switching frequency, which would lead to the converter operating beyond the zero voltage or capacitive regions, resulting in lower conversion efficiency [2]. It is crucial to widen the voltage gain range in *LLC* resonant converters to handle input voltage fluctuations effectively.

Several improvements can be made to prevent the resonant converter from operating in the capacitive region, such as using advanced control algorithms, alternated topology structures, innovative power semiconductor technologies, and additional passive components [3], [4], [5], [6]. Integrating improved control strategies and topology structures makes it possible to narrow down the switching frequency range while maintaining a broad input voltage range. This approach can also increase the efficiency of conventional *LLC* resonant converters [3]. However, control strategies alone cannot fundamentally change the minimum operating frequency of the converter, which can limit its practical applications. Adjusting the resonant tank also helps enhance *LLC* converters' performance, as suggested in [4]. This method involves modifying certain parameters, such as resonant inductance, excitation inductance, or resonant capacitance. However, even after these adjustments, the lowest attainable input voltage is still limited, making it difficult to achieve a genuinely wide range of operation. This challenge needs to be addressed to improve the overall performance of *LLC* circuits. From the perspective of engineering practicality, adding a conversion stage to the existing resonant converter is more popular. In [5], a dual-phase interleaved boost converter is integrated to the primary *LLC* full-bridge converter to increase efficiency and reduce components. However, such an integration poses a challenge in achieving ZVS for switch devices located at the bottom of bridge arms. The boost current in the dead zone impedes ZVS and restricts the energy transfer range of the *LLC* stage. Using two boost inductors increases the system's volume and weight, thereby negating the advantage of high switching frequency. To increase the input voltage range of the *LLC* converter, one common approach is to cascade two stages: a nonisolated dc–dc converter and an isolated one (as stated in [6]). The second stage functions as a dc transformer, while the first stage acts as a front-end or back-end regulator. By regulating the output voltage, effective distribution of input voltage and output current is ensured. However, the cascading connection results in all power passing through the first-stage regulator before reaching the second-stage converter, which leads to increased losses.

A novel type of converter, namely, the input-coupling *LLC* converter (IC-*LLC*), is proposed in this article. This converter is unique in that only half of the power is supplied by the front-end regulator, while the remainder comes directly from the original power supply, which brings in the following advantages.

1) IC-*LLC* can operate near the quasi-resonant point even if the input voltage varies widely, while the single-*LLC* cannot.

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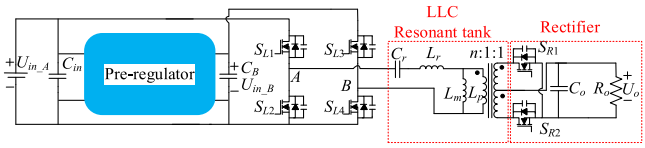

Fig. 1. Equivalent diagram of the proposed IC-*LLC* converter.

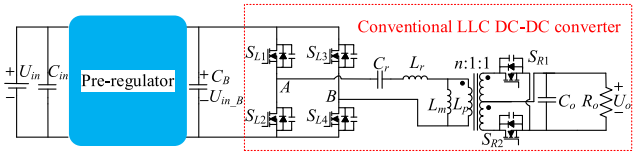

Fig. 2. Equivalent diagram of the common dual-stage DC–DC converter.

2) Compared with the dual-stage converters discussed in the literature [6], IC-*LLC* converter has lower power losses without any compromise on the operating range.

II. Proposed IC-*LLC* Converter

A. Input-Coupling Structure

Fig. 1 illustrates the proposed IC-*LLC* converter. It consists of a front-end regulator stage and an *LLC* resonant stage, which is the same as the common dual-stage dc–dc converter (see Fig. 2). The difference is that the input of the front-end stage is directly connected to one primary bridge (namely Bridge A) of the *LLC* stage. The input voltage of the front-end stage is denoted as $U_{\text{in\_}A}$, while the output voltage is $U_{\text{in\_}B}$. The output of the front-end stage is directly connected to another bridge of the *LLC* stage (namely, Bridge B). Both boost-type and buck-type converters are alternatives to the front-end regulator. The allowed operating frequency range determines the input voltage range. If the input voltage is lower than the minimum value allowed by a single *LLC* stage, a boost-type front-end converter should be used. Alternatively, a buck-type converter should be used.

B. Front-End Converter Modeling

In the continuous conduction mode (CCM) of the front-end converter, the relationship between $U_{\text{in\_}A}$ and $U_{\text{in\_}B}$ can be expressed as follows:

$$U_{\text{in\_}B} = \begin{cases} U_{\text{in\_}A} \cdot D_y & \text{buck} \\ U_{\text{in\_}A}/(1-D_y) & \text{boost} \end{cases} \tag{1}$$

where D_y represents the duty cycle of the preregulator. In the discontinuous conduction mode of the front-end converter, the relationship between $U_{\text{in\_}A}$ and the $U_{\text{in\_}B}$ is given as

$$U_{\text{in\_}B} = \begin{cases} U_{\text{in\_}A} - \frac{2I_{inb}L_B f_{sb}}{D_y^2} & \text{buck} \\ \frac{1}{\frac{1}{U_{\text{in\_}A}} - \frac{D_y^2}{2I_{inb}L_B f_{sb}}} & \text{boost} \end{cases} \tag{2}$$

where I_{inb} is the input current of the front-end converter, L_B is the buffering inductance, and f_{sb} is the switching frequency of the front-end converter.

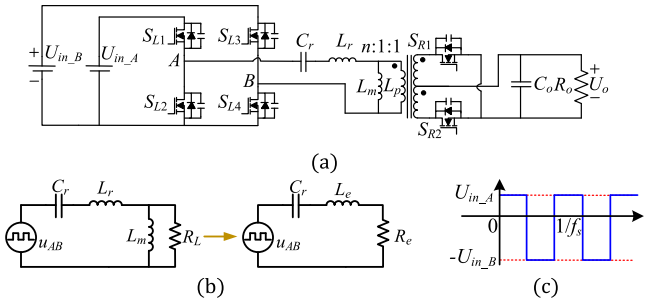

Fig. 3. IC-*LLC* resonant converter circuits. (a) IC-*LLC* resonant converter equivalent circuit. (b) Equivalent circuit of the IC-*LLC* resonant tank. (c) Voltage across the A/B terminals, u_{AB}.

C. IC-LLC Converter Modeling

Fig. 3 illustrates the equivalent circuit of the IC-*LLC* resonant converter. The pulse frequency modulation (PFM) is employed for the modulation of *LLC* here. Such a technique can alter the impedance of the *LLC* resonant circuit, thereby controlling the output voltage by modifying the voltage on the primary side of the transformer. The fundamental frequency analysis is used to scrutinize the operational principles of the *LLC* resonant converter

$$R_e = \frac{R_L \omega_s{}^2 L_m^2}{R_L^2 + \omega_s^2 L_m^2} \tag{3}$$

$$L_e = L_r + \frac{R_L^2 \omega_s L_m}{R_L^2 + \omega_s^2 L_m^2}. \tag{4}$$

where L_e and R_e are the equivalent resonant inductance and equivalent load resistance, respectively.

The front-end converter is assumed as a boost converter in the following analysis. The rated voltage of the boost converter is set as $U_{\text{in\_rated}}$. Fig. 3(a) shows that the converter's input is fed by two voltage sources i.e., $U_{\text{in\_}A}$ and $U_{\text{in\_}B}$. With PFM control, the switches on the same bridge are turned ON in a complementary way. Each of the switches conducts for half of a switching cycle. The equivalent input voltage of the positive half-cycle interval has an amplitude of $U_{\text{in\_}A}$. Within the negative half-cycle, it has an amplitude of -$U_{\text{in\_}B}$. The duration of both high and low levels takes half of a switching cycle. When the input voltage deviates from the rated point, the voltage across the AB terminals forms a square wave with a frequency of f_s and asymmetric plus/minus amplitudes, as depicted in Fig. 3(b) and (c). Further, the Fourier series expansion of the equivalent input voltage u_{AB} is expressed as

$$u_{AB} = -\frac{U_{\text{in\_}B} - U_{\text{in\_}A}}{2} + \frac{4}{\pi} \cdot \frac{U_{\text{in\_}A} + U_{\text{in\_}B}}{2} \sum_{n=1,3,5\ldots}^{\infty} \frac{\sin(n\omega_s t)}{n} \tag{5}$$

where ω_s is

$$\omega_S = 2\pi f_s. \tag{6}$$

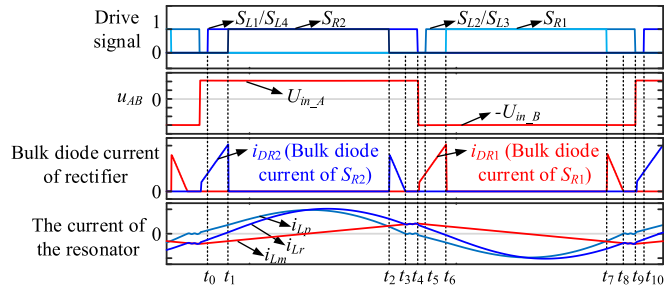

Fig. 4. Waveforms of each power level of the converter when $f_m < f_s < f_r$.

The rated input voltage is calculated as

$$U_{\text{in\_rated}} = \frac{U_{\text{in\_}A} + U_{\text{in\_}B}}{2}. \tag{7}$$

The expression for the fundamental component of the voltage u_{AB} is

$$u_{AB\_\text{BASE}} = \frac{4}{\pi} \cdot U_{\text{in\_rated}} \sin(\omega_s t). \tag{8}$$

Obviously, the fundamental component of u_{AB} remains the same as (7) is satisfied, no matter whether the input voltages U_{in_A} and U_{in_B} are balanced or not. Similarly, the imbalance in input voltages does not affect the resonant tank. Ensuring (7) is met maintains consistent switching frequency and operation at quasi-resonant frequency.

D. Operating Modes of IC-LLC

The first resonance is caused by the resonant inductor and resonant capacitor elements. Its frequency is given by

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}}. \tag{9}$$

The second one is caused by the resonance of the resonant capacitor, resonant inductor L_r, and excitation inductor L_m. The frequency is expressed as follows:

$$f_m = \frac{1}{2\pi\sqrt{(L_r + L_m)C_r}}. \tag{10}$$

The operating range of the *LLC* resonant converter is divided into four parts by the two resonant frequencies, i.e., $f_s < f_m$, $f_m < f_s < f_r$, $f_s = f_r$, and $f_s > f_r$. When $f_s < f_m$, the *LLC* resonant converter operates in the capacitive region where the primary-side switches cannot achieve ZVS. Hence, this frequency range will not be considered. This article focuses on the frequency range of $f_m < f_s < f_r$, where the *LLC* resonant converter operates in the inductive region. The primary-side switches achieve ZVS, and the secondary-side current is discontinuous, allowing for ZCS. The critical waveforms for comprehending the behavior of the converter within this frequency range are depicted in Fig. 4.

During t_0–t_4, the voltage across S_{L2} is U_{in_A}, while the voltage across S_{L3} is U_{in_B}. Throughout t_5–t_9, the voltage across S_{L1} is U_{in_A}, while the voltage across S_{L4} is U_{in_B}. Fig. 5 shows the resonance states of the resonant tank at different time intervals, assuming that the output voltage is stable.

The resonant tank states during t_0–t_3 and t_9–t_{10} are depicted in Fig. 5(a). In this phase, the excitation inductor L_m voltage is clamped at nU_o, while the excitation current i_{Lm} rises linearly. The secondary current flows through S_{R2}.

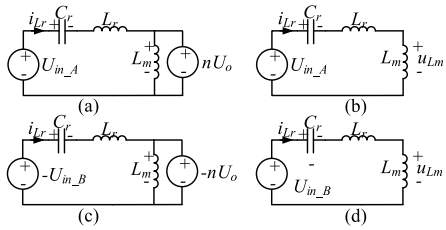

Fig. 5. Resonant tank states at different time intervals: (a)t_0–t_3 and t_9–t_{10}, (b) t_3–t_4, (c) t_4–t_8, and (d) t_8–t_9.

The resonant tank state during t_3–t_4 is depicted in Fig. 5(b). As shown, there is no energy transfer between the primary and secondary sides, with $|u_{Lm}| < nU_o$.

The resonant tank state during t_4–t_8 is depicted in Fig. 5(c). At this point, the voltage across the excitation inductor L_m is clamped at $-nU_o$, causing a linear decrease in the excitation current i_{Lm}. The secondary-side current flows through S_{R1}.

The resonant tank state during t_8–t_9 is presented in Fig. 5(d). Similarly to the states of Fig. 5(b), there is no energy transfer between the primary and secondary sides, and $|u_{Lm}| < nU_o$.

When $f_s = f_r$, the unit voltage gain is achieved. ZVS is realized by the primary-side switches, while the secondary-side rectifier switch current is exactly at the critical point between discontinuous and CCM. During this period, the efficiency of the converter generally reaches its peak.

In the case of $f_s > f_r$, ZVS is attained by the primary-side switches of the *LLC* resonant converter, but the secondary-side current remains in the continuous state, preventing ZCS. In this mode, the gain of the converter decreases with an increasing switching frequency, making it suitable for light-load conditions. However, the higher switching frequency results in increased switch losses, leading to a lower efficiency.

E. Converter Loss Modeling and Analysis

The losses of IC-*LLC* can be categorized into two parts: boost losses and *LLC* losses, which also apply to boost-*LLC*. For boost converters, the losses generally include magnetic and switching device losses. The magnetic losses comprise iron and copper losses. The inductor core loss can be calculated using the Steinmetz equation, as shown in the equation following:

$$P_{L\_Fe} = k_c f_{sb}^{\alpha} V_e B^{\beta} \tag{11}$$

where k_c is the loss constant of the iron core, V_e is the volume of the iron core, B is the magnetic induction intensity, and α and β are Steinmetz material coefficients

$$B = L\hat{I}_L/(n_p A_e). \tag{12}$$

In (12), L is the inductance (L_B for IC-*LLC*), $\hat{I}_L$ is the peak value of the inductor current, n_p is the number of winding turns, and A_e is the core cross-sectional area. The inductor copper loss is calculated as follows:

$$P_{L\_Cu} = I_{L\_\text{rms}}^2 R_{B\_ac} \tag{13}$$

where I_{L_rms} is the effective value of the current, and R_{B_ac} is the equivalent resistance of the inductor. The total conduction loss of the two switches on the boost stage (S_{B1} and S_{B2}, see Fig. 8) is

$$P_{cd\_SB} = R_{\mathrm{on}}\hat{I}_L^2(T_{SB1} + T_{SB2})f_{sb} \tag{14}$$

where R_{on} is the ON-resistance, T_{SB1} is the ON-time of S_{B1}, and T_{SB2} is the ON-time of S_{B2}. Since S_{B2} is turned ON with ZVS, the total switching loss is actually only contributed by S_{B1}, as expressed by the following:

$$P_{\mathrm{sw\_}SB1} = (E_{\mathrm{off}} + 0.5C_{\mathrm{DS}}V_{\mathrm{in}}^2)f_{sb} \tag{15}$$

where E_{off} is the dissipated energy when S_{B1} is turned OFF, C_{DS} is the drain–source capacitance, and V_{in} is the input voltage (U_{in_A} for IC-*LLC*). The diode conduction loss is

$$P_{fd\_SB} = V_{fd}\hat{I}_L t_{\mathrm{dead}} f_{sb}. \tag{16}$$

The magnetic loss $P_{L\_\mathrm{Fe}\_Lr}$ and copper loss $P_{L\_\mathrm{Cu}\_Lr}$ of the resonant inductor, the magnetic loss $P_{L\_\mathrm{Fe}\_T}$, primary-side copper loss $P_{L\_\mathrm{Cu}\_ps}$ and secondary-side copper loss $P_{L\_\mathrm{Cu}\_rs}$ of the transformer can also be calculated according to (11)–(13).

Since ZVS turning-ON is achieved for the primary side of *LLC*, only conduction loss and turn-OFF loss exist in the primary-side semiconductors. The conduction loss is

$$P_{\mathrm{con}\_SL} = I_{Lr\_\mathrm{rms}}^2 R_{\mathrm{DS}\_SL(\mathrm{on})} \tag{17}$$

where I_{Lr_rms} is the resonant current rms value and $R_{\mathrm{DS}\_SL(\mathrm{on})}$ is the ON-state resistance of the switching devices. The turn-OFF loss of the primary semiconductors is

$$P_{\mathrm{off}\_SL} = 0.5V_{\mathrm{in}}I_{Q\_\mathrm{off}}t_{\mathrm{off}}f_s \tag{18}$$

where I_{Q_off} is the current flowing through the semiconductor within the turning-OFF duration. And t_{OFF} is the turning-OFF time that can be obtained by looking up the semiconductor datasheet.

Since the synchronous rectification is adopted for the secondary side, there is only conduction loss on the secondary side. The secondary side loss can be expressed by

$$P_{\mathrm{con}\_SR} = I_{SR\_\mathrm{rms}}^2 R_{\mathrm{DS}\_SR(\mathrm{on})} \tag{19}$$

where I_{SR_rms} is the effective value of the current flowing through the secondary-side devices and $R_{\mathrm{DS}\_SR(\mathrm{on})}$ is the ON-state resistance.

With the analysis above, the boost stage loss of IC-*LLC* can be expressed by

$$P_{\mathrm{loss}\_b1} = P_{L\_\mathrm{Fe}\_1} + P_{L\_\mathrm{Cu}\_1} + P_{cd\_SB\_1} + P_{sw\_SB1\_1} + P_{fd\_SB\_1}. \tag{20}$$

The boost stage loss of the conventional boost-*LLC* can be derived with a similar manner. The loss can be expressed by

$$P_{\mathrm{loss}\_b2} = P_{L\_\mathrm{Fe}\_2} + P_{L\_\mathrm{Cu}\_2} + P_{cd\_SB\_2} + P_{\mathrm{sw}\_SB1\_2} + P_{fd\_SB\_2}. \tag{21}$$

Note that, for comparison convenience, the variables with subscript "_1" represent the losses for IC-*LLC*, while the ones with subscript "_2" are for boost-*LLC*.

Obviously, the loss of the boost stage is proportional to the average value of the inductor current. It can be seen from Fig. 4 that the time of two voltage sources, U_{in_A} and U_{in_B}, acting on the resonant tank is the same, i.e., $T_s/2$. Considering i_{Lr} is symmetrical, the average current values flowing through the two voltage sources, U_{in_A} and U_{in_B}, are, therefore, the same. Define P_A (P_B) as the power directly transmitted by voltage source U_{in_A} (U_{in_B}) to the resonant tank within one *LLC* switching cycle. P_A and P_B fulfil $P_A + P_B = P_{\mathrm{in}}$. The ratio of P_A to P_B is

$$\frac{P_A}{P_B} = \frac{U_{\mathrm{in}\_A}\cdot I_{\mathrm{avg}}}{U_{\mathrm{in}\_B}\cdot I_{\mathrm{avg}}} = \frac{U_{\mathrm{in}\_A}}{U_{\mathrm{in}\_B}} = 1 - D_y. \tag{22}$$

According to (22), where I_{avg} is average current of the two sources, the boost stage of IC-*LLC* transfers only a part of the total power. Hence, the average value of inductor current $i_{L\_\mathrm{avg}\_1}$ of IC-*LLC* is smaller than the average value of inductor current $i_{L\_\mathrm{avg}\_2}$ of boost-*LLC*. And the ripple of inductor current is calculated according to (23). It is obvious that, therefore, the peak inductor current $\hat{I}_{L\_1}$ of IC-*LLC* is also smaller than the one of boost-*LLC* ($\hat{I}_{L\_2}$)

$$\Delta i_L = U_{\mathrm{in}}D_y T_s/(2L). \tag{23}$$

As a result, the boost stage loss P_{loss_b1} of IC-*LLC* is smaller than that of boost-*LLC*, i.e., P_{loss_b2}. On the other hand, for both the *LLC* stages of IC-*LLC* and boost-*LLC*, the total loss $P_{\mathrm{loss}\_LLC\_1}$ and $P_{\mathrm{loss}\_LLC\_2}$ are the same, i.e., $P_{\mathrm{loss}\_LLC\_1} = P_{\mathrm{loss}\_LLC\_2}$. Both can be expressed by the following:

$$P_{\mathrm{loss}\_LLC\_1} = P_{L\_\mathrm{Fe}\_Lr} + P_{L\_\mathrm{Cu}\_Lr} + P_{L\_\mathrm{Fe}\_T} + P_{L\_\mathrm{Cu}\_ps} + P_{L\_\mathrm{Cu}\_rs} + P_{\mathrm{con}\_SL} + P_{\mathrm{off}\_SL} + P_{\mathrm{con}\_SR}. \tag{24}$$

The total loss of IC-*LLC* is $P_{\mathrm{loss}\_1} = P_{\mathrm{loss}\_b1} + P_{\mathrm{loss}\_LLC\_1}$ and the total loss of boost-*LLC* is $P_{\mathrm{loss}\_2} = P_{\mathrm{loss}\_b2} + P_{\mathrm{loss}\_LLC\_2}$. Therefore, it yields $P_{\mathrm{loss}\_1} < P_{\mathrm{loss}\_2}$, which means that the efficiency of the IC-*LLC* converter is larger than that of the boost-*LLC* converter.

For a more straightforward comparison, the losses of the proposed converter and the conventional boost-*LLC* are compared. The real sizes of the resonant tanks and semiconductors employed are listed in Table I.

The losses of boost converter for IC-*LLC* and boost-*LLC* at rated power are represented as P_{loss_b1} and P_{loss_b2}, respectively, in Fig. 6. Both converters have the same input voltage range. In order to ensure the system's efficiency, the loss of the boost stage must not exceed the maximum loss, which is taken as 30 W ($P_{\mathrm{loss}\_b\max}$). For boost-*LLC* converter, the input voltage (U_{in}) corresponding to $P_{\mathrm{loss}\_b2} = P_{\mathrm{loss}\_b\max}$ is 167 V, and for IC-*LLC* converter, the input voltage (U_{in_A}) corresponding to $P_{\mathrm{loss}\_b1} = P_{\mathrm{loss}\_b\max}$ is 126 V. Therefore, the minimum input voltage for IC-*LLC* converter is 126 V, while it is 167 V for boost-*LLC* converter. Since the input voltage limit is 290 V, the input voltage range for IC-*LLC* converter is [126 V, 290 V]. For boost-*LLC* converter, it is [167 V, 290 V]. It can be concluded that the input voltage range of IC-*LLC* converter is wider than that of boost-*LLC* converter for the same boost losses. In addition, the

TABLE I
LIST OF THE COMPONENTS USED FOR EFFICIENCY COMPARISON

Component	Models	Parameters
MOSFET (S_{B1},S_{B2},S_{L1}–S_{L4})	SC030N65H7 from Pingwei	On-Resistance: 30 mΩ Output capacitor: 180 pF ON Delay time: 14 ns Rise time: 15 ns OFF Delay time: 28 ns Fall time: 8 ns
MOSFET (S_{R1},S_{R2}) Three in parallel	HGT015N10S from Hunteck	On-Resistance: 1.3 mΩ Output capacitor: 2657 pF ON Delay time: 30 ns Rise time: 32 ns OFF Delay time: 48 ns Fall time: 18 ns
Boost inductor magnetic core	Magnetic core: ECIW37A from Dmegc	Effective volume: 10932.84 mm^3 Effective central column area: 206.67 mm^2
Resonant inductor magnetic core; Transformer magnetic core	Magnetic core: EC51A from Dmegc	Effective volume: 23842.56 mm^3 Effective central column area: 354.8 mm^2

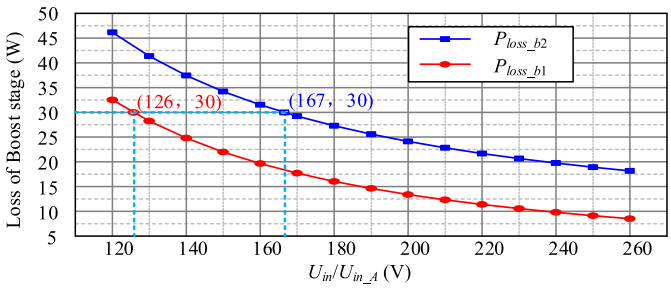

Fig. 6. Boost stage losses of IC-*LLC* and boost-*LLC* with the same input voltage range.

TABLE II
LLC PARAMETERS ALLOWING INPUT VOLTAGE RANGE 126–290V

$U_{\text{in\_min}}$	126 V	C_O	2500 μF
$U_{\text{in\_max}}$	290 V	C_r	202.897 nF
P_o	1.5 kW	L_r	12.48 μH
U_o	30.5 V	L_m	13.94 μH
f_r	100 kHz	n	5.364

efficiency of IC-*LLC* converter is higher than that of boost-*LLC* converter within a same input voltage range.

According to [7], the single-stage *LLC* can also be designed to operate with an input voltage range from 126 to 290 V. With the manner in [7], the corresponding *LLC* parameters can be derived as listed in Table II.

With a similar loss analysis procedure, the theoretical efficiency curve of the single-stage *LLC* converter, when the input voltage is 126–290V, is depicted in Fig. 7. It is evident that the maximum efficiency of the *LLC* converter reaches only 95.3%. This is a result of a tradeoff between a wide voltage range and high efficiency. Since the efficiency at the 126 V input voltage point is the lowest for IC-*LLC*, only the efficiency curve for the 126 V condition is provided in Fig. 7. It can be concluded that, in most operating conditions, the efficiency of the IC-*LLC* is higher than that of the *LLC* designed for accessing a wide range input voltage of 126–290V.

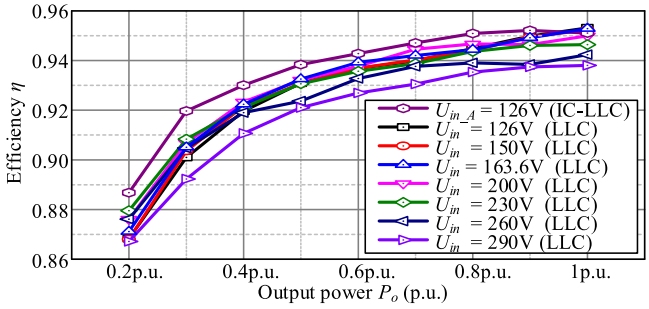

Fig. 7. Efficiency comparison of the wide input range *LLC* and the proposed IC-*LLC*.

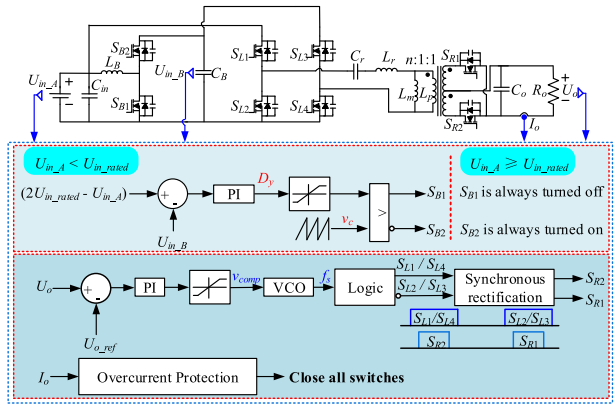

Fig. 8. Control strategy of IC-*LLC* converter.

III. CONTROL STRATEGY

The control strategy for the IC-*LLC* converter is shown in Fig. 8, where the front-end converter is considered as a boost converter. In the front-end converter, in case $U_{\text{in}\_A} < U_{\text{in\_rated}}$, the reference voltage is $2U_{\text{in\_rated}}$ - U_{in_A}. The difference between $2U_{\text{in\_rated}}$ - U_{in_A} and the feedback voltage U_{in_B} is fed into the PI controller to calculate the duty cycle D_y of the switch S_{B1}. After that, the drive signal for the switch S_{B1} is generated by comparing the duty cycle D_y with the carrier wave v_c. The drive signal for S_{B2} is the opposite of the one for S_{B1}. Otherwise, in case $U_{\text{in}\_A} \geq U_{\text{in\_rated}}$, S_{B1} is always turned OFF and S_{B2} is always turned ON.

The error between the output voltage and its reference value is then fed into a PI controller. The output of the PI controller is the voltage compensation v_{comp}. A limitation is applied to ensure that the IC-*LLC* converter remains outside the capacitive region. v_{comp} is utilized as the input to a voltage-controlled oscillator, generating a sine wave with a dynamically changing frequency. This sine wave is employed to produce the drive signals for the primary- and secondary-side switches, aligning with the IC-*LLC*'s switching frequency.

Concurrently, synchronous rectification is employed for the secondary-side switches. The drive signal for S_{L1}/S_{L4} or S_{L2}/S_{L3} is obtained through delayed turn-ON and advanced turn-OFF, subsequently serving as the drive signal for S_{R2} or S_{R1}. The collection of output current I_o is undertaken for overcurrent protection, preventing the occurrence of overcurrent or potential short-circuit conditions within the converter.

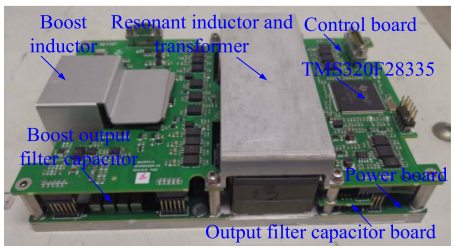

Fig. 9. Experimental prototype of the IC-*LLC* converter.

TABLE III
PARAMETERS OF THE IC-*LLC* PROTOTYPE

$U_{\text{in\_rated}}$	260 V	C_O	2500 μF
C_{in}	8 μF	C_r	300 nF
L_B	150 μH	L_r	8 μH
C_B	12 μF	L_m	80 μH
P_o / U_o	1.5 kW / 30.5 V	f_{sb}	100 kHz
f_r	102.73 kHz	n:1:1	17:2:2

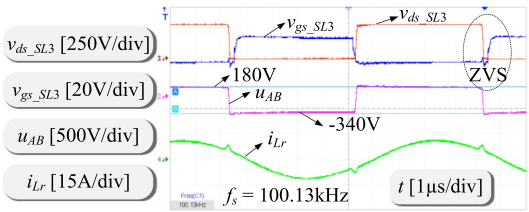

Fig. 10. Experimental result for the 180 V input voltage condition.

IV. EXPERIMENTAL VERIFICATION

This section provides the experimental results of the IC-*LLC* converter, as well as the two benchmarks, the dual-stage boost-*LLC* converter and the single-stage *LLC* converter. Fig. 9 shows the experimental prototype. Table III outlines the key parameters of the IC-*LLC* converter.

Fig. 10 depicts the experimental waveform with an input voltage of 180 V under full-load operating condition. As illustrated, the primary-side switch achieves ZVS. When S_{L3} is in a conducting state, the u_{AB} magnitude is equivalent to the boost output, which is -340 V. Conversely, when S_{L3} is turned OFF, the u_{AB} magnitude equals the input voltage, which is 180 V. The u_{AB} amplitude displays asymmetry, as shown by the resonant current i_L waveform. The switching frequency f_s is slightly lower than the resonant frequency f_r, indicating operation between the underresonance and quasi-resonance states.

In Fig. 10, it can be observed that the resonant current is still sinusoidal as the load condition is maintained at full load. At the same time, the switching frequency decreases as the load increases, indicating that the converter is functioning in a quasi-resonant mode interval before full load. As a result, the converter can operate at the quasi-resonant point even when the input voltage is low.

Fig. 11 shows the experimental waveform when the input voltage is 260 V. Fig. 11 presents the waveform at the full-load condition. At this point, when S_{L3} is conducting, the magnitude of u_{AB} aligns with the boost output, resulting in $u_{AB} = -260$ V. Conversely, when S_{L3} is turned OFF, u_{AB} matches the input voltage, yielding $u_{AB} = 260$ V. The voltage amplitude of u_{AB} remains symmetrical. As indicated by the resonant current waveform i_{Lr}, the switching frequency f_s is slightly lower than the resonant frequency f_r, indicating operation in a state between underresonance and quasi-resonance. As shown in Fig. 11, when the output power gradually decreases from full load, the resonant current exhibits a sinusoidal trend, and the converter operates in a quasi-resonant mode. Therefore, the converter operates at the quasi-resonant point under rated input conditions, achieving ZVS for the primary-side switch under the full-load condition.

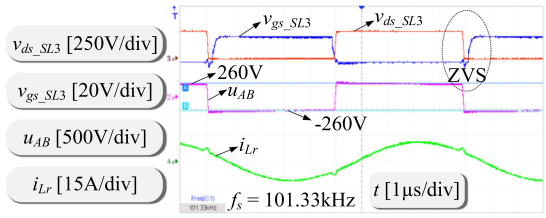

Fig. 11. Experimental result for the 260 V input voltage condition.

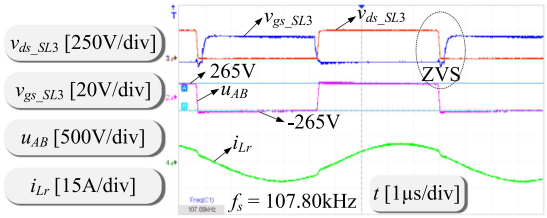

Fig. 12. Experimental result for the 265 V input voltage condition.

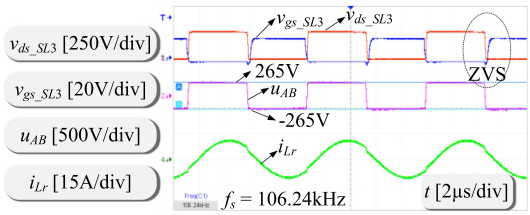

Fig. 13. Experimental result of *LLC* converter with input voltage of 265 V.

As shown in Fig. 12, when the input voltage is increased to 265 V that is higher than the rated level, the u_{AB} waveform becomes symmetric and has an amplitude of 265 V. This indicates that the boost converter has been bypassed and is no longer active. At full load, the converter operates in an overresonant mode, as can be observed from the corresponding curve of i_{Lr}. As the load intensifies, the converter reduces the switching frequency f_s to ensure output stability. When the load still gradually increases, i_{Lr} mainly exhibits a sinusoidal trend, which signifies the converter's operation will in a quasi-resonant mode.

In contrast, the experimental results of the single-stage *LLC* with different input voltage values, ranging from high to low, are presented in Figs. 13–15. It is important to note that the single-stage *LLC* used in the experiment is not the one designed in Section II. Instead, it is the back-end stage of IC-*LLC*, and its parameters can be found in Table III. Hence, the experiment results can also be regarded as a good supplement to the simulation results of Section II. Fig. 13 illustrates the scenario where

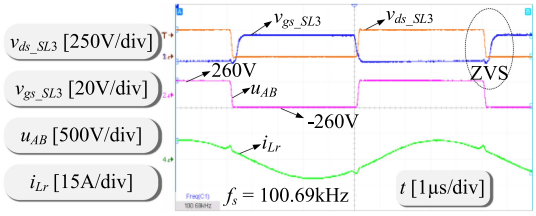

Fig. 14. Experimental result of *LLC* converter with input voltage of 260 V.

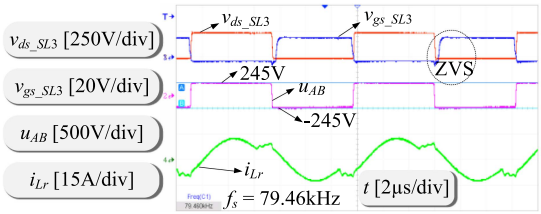

Fig. 15. Experimental result of *LLC* converter with input voltage of 245 V.

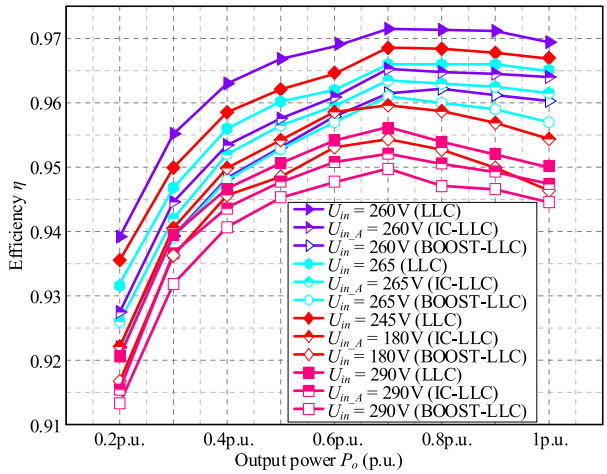

Fig. 16. Experimental results of single-stage *LLC* with input voltage 245–290 V and IC-*LLC* and boost-*LLC* with input voltage 180–290 V.

the input voltage is 265 V, and the output power is 1.0 per unit (p.u.). As seen in the figure, the switching frequency (f_s) is higher than the resonant frequency (f_r), indicating that the converter is operating in an overresonant state. The primary-side switches achieve ZVS. The waveform of the voltage u_{AB} is symmetrical, with an amplitude of 265 V.

When the input voltage decreases to the rated voltage of 260 V (the output power remains at 1.0 p.u.), the converter will operate in quasi-resonant mode, as illustrated in Fig. 14. It is worth noting that under this condition, the converter's efficiency theoretically reaches its highest value.

When the input voltage is further decreased to 245 V, the switching frequency drops to a relatively low value, i.e., 79.46 kHz. The result is shown in Fig. 15. If the input voltage is further decreased, the switching frequency will sharply decrease and eventually enter the capacitive region, which will cause damage to the converter and pose safety hazards. In contrast, the switching frequency of the *LLC* stage in IC-*LLC* is 100.13 kHz when the input voltage is 180 V (see Fig. 10), which is far from the capacitive region, proving a wider safe margin.

The curves displayed in Fig. 16 showcase the efficiencies of the single-stage *LLC*, IC-*LLC*, and boost-*LLC* converters at different load ranges between 0.2 and 1.0 p.u. It is important to note that the single-stage *LLC*'s input voltage range is limited to 245 to 290 V, which is permitted by the prototype hardware of the IC-*LLC*. Therefore, the experiment test takes into account four voltage points, 245, 260, 265, and 290V. In contrast, IC-*LLC* and boost-*LLC* are considered at input voltages of 180, 260, 265, and 290 V. For either of the three converters, the highest efficiency will be achieved at the voltage of 260 V. Voltage deviations, either increasing or decreasing, will result in lower efficiency. The single-stage *LLC* topology is a highly efficient method of power conversion, despite having a narrow switching frequency range. In other words, adding more conversion stages for both boost-*LLC* and IC-*LLC* in order to expand the operating range would result in a decrease in system efficiency. Thanks to the input voltage sharing mechanism, the efficiency of the proposed IC-*LLC* is superior to that of the boost-*LLC* converter. Therefore, it is clear that IC-*LLC* provides a better solution for balancing the tradeoff between operating range and system efficiency.

V. Conclusion

This article proposes an input-coupling type *LLC* converter capable of operating at the quasi-resonant point covering low input voltage conditions. Sharing of input voltage reduces losses in the preregulator stage, resulting in higher efficiency compared with the conventional dual-stage high-gain solutions. The experimental results validate the superior efficiency of IC-*LLC* over boost-*LLC* and demonstrate the wider operational range of IC-*LLC* compared to a single *LLC* converter. The proposed IC-*LLC* converter proves to be a promising solution to enhance the reliability and performance of high-power secondary power supplies in practical applications.

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