An Efficient Reduced Power Processing Single-Phase LED Driver Using Unidirectional PFC Converter

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***Abstract*—Recent advancements in LED technology have led to the popularity of reduced-power processing schemes owing to their ability to improve conversion efficiency. When LEDs are connected to the ac grid, they satisfy essential requirements, such as power factor correction, resulting in reduced input-current harmonics and maintenance of ac grid power quality. To achieve a high-quality light output with no flickering, the LED load was supplied with a constant output current, resulting in the elimination of flickering. To address these requirements, a novel reduced-power LED driver was introduced in this study. It employs a switching mechanism to divide the input power into two parts, with one part directly transferred to the load, resulting in greater efficiency. A simple control method was used to eliminate flickering in the light output by reducing ripples present in the output current. Reducing ripples can decrease the capacitance requirements, enabling the substitution of electrolytic capacitors with film capacitors, thus increasing the lifespan of the LED driver. A prototype with a power rating of 30 W was developed, and its performance was evaluated. The findings showed that the input power factor was 0.99 and the lower harmonic distortion was minimal. In addition, the driver efficiency was 94.4% at full power. The converter underwent extensive testing with universal input voltages and power levels to guarantee a reliable dimming functionality.**

***Index Terms*—Constant current, dimming, power control (PC), power factor (PF), reduced power processing.**

I. Introduction

SINCE their invention in the 1960s, LEDs have become the preferred lighting option due to their long lifespan, high efficacy, and other benefits, such as compact size and durability [1], [2]. Despite these advantages, connecting LEDs directly to their power supply is not possible due to the low internal impedance of the LEDs. Therefore, a current-controlled power supply is necessary to ensure proper operation and maximize the benefits of this technology. It is crucial to carefully design an electronic converter that meets the requirements of standards, such as IEC 61000-3-2 Class C [3], [4].

Industrial applications widely use LED drivers with power factor correction (PFC) converters owing to their high efficiency, compact size, and low cost. These single-stage drivers are popular in the market because of their ability to correct the power factor (PF), which results in a better power supply for LED lighting systems [5]. However, these drivers often produce high ripples when powering LEDs, requiring the use of significant capacitance to ensure flicker-free operation. This is typically achieved by using electrolytic capacitors (E-caps). Although, the main drawback of using E-caps in LED drivers is their limited lifespans. To overcome this issue, the use of long-lasting ceramic or film capacitors as replacements is recommended. However, their low energy density and high cost pose challenges for their practical application [6], [7], [8]. It is crucial to maintain a constant current supply to LEDs to avoid flickering.

A possible solution to this problem is to implement active buffering, as discussed in [9], [10], [11], and [12]. To achieve this, the rigid connection between the voltage ripple and capacitor energy storage is dissolved by transferring the ripple power to the buffer capacitor, which reduces energy storage requirements of the capacitor and enables the use of long-life capacitors without compromising cost or power density [13]. Fig. 1(a) depicts PFC-based two-stage LED drivers with active buffering. The first stage aims to provide a high PF while minimizing harmonics in the input current, whereas the second stage maintains a constant current to feed the LED load [14]. However, the requirement for an additional control circuit adds complexity and increases implementation costs, while using both converters for power processing leads to inefficiency, more components, larger size, and higher costs. A new approach has been proposed that combines both stages into one by utilizing shared components, notably, switches. However, this approach is limited by the high-voltage and current stresses on the switches, which ultimately restrict the output power [15], [16], [17], [18]. Minimizing the reprocessing power using bidirectional converter is illustrated in Fig. 1(b). In this configuration, a bidirectional converter is used to channel ripple power into a capacitor. However, the ripple power undergoes three processing cycles: once through the PFC converter and twice through the bidirectional converter. This involves charging the storage capacitor in one direction using the bidirectional converter and subsequently discharging the stored energy from the capacitor to the load through the bidirectional converter in another direction [19], [20], [21], [22].

An energy flow path analysis can be used to assess the effectiveness of the power processing stages in the converter [23]. A unidirectional converter-based LED driver was proposed in [24], [25], [26]. The dc–dc converter in parallel with the primary power route manages ripple power. The unidirectional converter-based solution is more efficient compared with the corresponding bidirectional setup because the ripple power is

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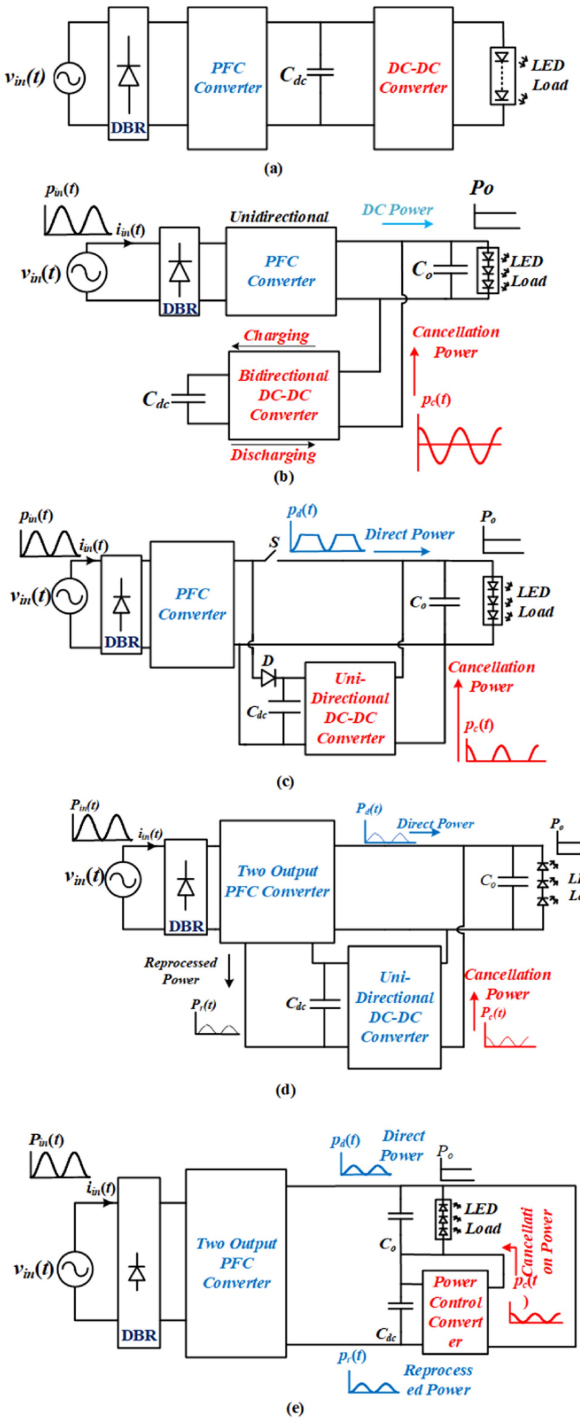

Fig. 1. LED driver with (a) two stages, (b) bidirectional converter, (c) unidirectional converter, (d) split inductor design, and (e) split capacitor design.

processed once by the unidirectional dc–dc converter, whereas with the bidirectional converter, the ripple power undergoes processing twice, as shown in Fig. 1(c). Nevertheless, with this technique, extra switches are required for proper input power distribution. Using a unidirectional converter, a unique design was developed in [27] to account for the ripple power, which is based on the split inductor concept. However, this approach for compensating the ripple power requires more energy storage

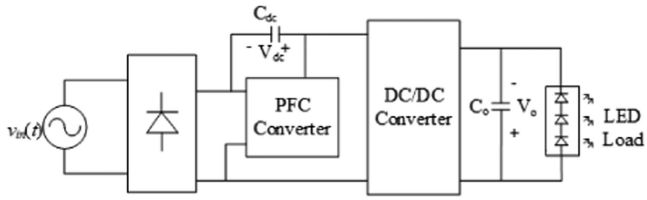

Fig. 2. LED driver with an efficient unidirectional PFC converter.

elements and semiconductor devices, which results in a reduction in efficiency and an increase in cost and size. In contrast to the earlier reduced power processing methods, a new driver architecture utilizing unidirectional power processing with fewer magnetic storage devices and semiconductors was introduced in [28]. In order to provide the necessary power from the dc-bus capacitor to keep the output power constant, a less accurate on-time analog controller is required in this method, as shown in Fig. 1(d). Integration of these analog controllers is essential to achieve higher accuracy without relying on preexisting designs. The use of converters connected in parallel with a single switch was proposed in [29]. The presence of 100 Hz ripple in the LED current causes greater stress across the switch due to the accumulation of excess current. A driver design that utilizes a split capacitor, as shown in Fig. 1(e), was proposed in [30], [31], and [32], which allows for the distribution of input power without the need for additional switches and can achieve high efficiency. However, the efficiency of the conversion process depends on the ratio of the voltages of the capacitors, which can limit reprocessing power. The novel LED driver introduced in this article offers several advantages, including the ability to distribute input power without additional switches, higher efficiency, and elimination of flickering in the LED current, as shown in Fig. 2. These benefits are achieved using a simple ripple cancelation technique that allows the replacement of E-caps with long-life film capacitors. The proposed driver also has a long lifespan, is cost effective, and highly efficient.

The rest of this article is organized as follows. Section II introduces the proposed converter, Section III elucidates its operational modes, Section IV emphasizes the design parameters, and Section V presents the experimental results. Finally, Section VI concludes this article.

II. Proposed LED Driver

The proposed design incorporates two buck–boost converters, as shown in Fig. 3. The first buck–boost converter is connected to the ac input by means of a bridge rectifier and operates as a PFC converter. This converter comprises S_{bbpfc}, L_{bbpfc}, and D_{bbpfc}, and the storage capacitor C_{dc}. The voltage across C_{dc} is V_{dc}. The second buck–boost converter, comprising S_{bbpc}, L_{bbpc}, and D_{bbpc}, functions as a power control (PC) converter. The output capacitor of PC converter is C_o, and it is connected to LED load. The voltage across C_o is V_o. The combined output of the rectifier and PFC converter is fed into the PC converter as an input. The input current is the sum of currents flowing through the PFC converter $i_{bb_{pfc}}(t)$ and current flowing through

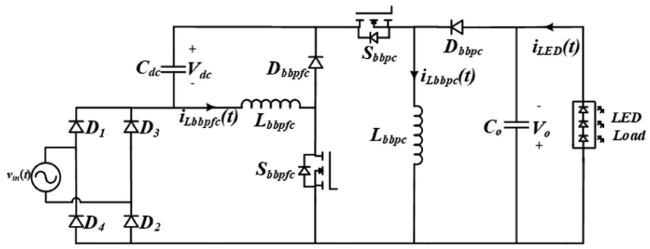

Fig. 3. Proposed LED driver schematic representation.

the PC converter $i_{bb_{\rm pc}}(t)$. Input power $P_{\rm in}(t)$ is separated into two parts: $Kp_{\rm in}(t)$ and $(1-K)p_{\rm in}(t)$. The input power $Kp_{\rm in}(t)$ is handled by both the PFC and PC converters and is referred to as the reprocessed power $p_r(t)$ because it is processed by two converters. The other portion of power $(1-K)p_{\rm in}(t)$ is sent to the load through the PC converter and is called the direct power $p_d(t)$. Power $p_r(t)$ is initially processed through a PFC converter and stored in a capacitor $C_{\rm dc}$. It is then transferred through a PC converter to the load, where it is transformed into cancelation power $p_c(t)$, which is added to the direct power $p_d(t)$ to yield constant output power P_o. The PFC converter is smaller and more efficient when compared with the PFC converter of the two-stage configuration because it is processing only portion of total input power, which is $Kp_{\rm in}(t)$. The total processing power in the proposed configuration is less when compared with two-stage configuration, where the total input power is processed through both PFC and dc–dc converter. The proposed configuration is categorized as single stage although it has two converters and their separate controllers, because the PFC converter is processing only half of the total input power.

III. Operating Modes

The PFC converter operates in discontinuous conduction mode (DCM) to achieve a high PF at the input side, because the current in the buck–boost converter in DCM tracks the input voltage, which can naturally lead to a high PF. A buck–boost converter is utilized for PC owing to its voltage-follower characteristics that maintain a constant output current and operate in the DCM. The converter operates in four distinct modes, as shown in Fig. 4, which presents the corresponding circuits for each mode. Fig. 5 illustrates the different waveforms for each mode.

The ac input voltage and current can be represented as

$$v_{\rm in}(t) = V_m \sin \omega t \tag{1}$$

$$i_{\rm in}(t) = I_m \sin \omega t. \tag{2}$$

The input power $p_{\rm in}$ is

$$p_{\rm in}(t) = V_m \sin \omega t \times I_m \sin \omega t \tag{3}$$

$$p_{\rm in}(t) = P_o(1 - \cos 2\omega t) = 2P_o \sin^2 \omega t \tag{4}$$

where P_o is the average value of the input power, and ω is the angular frequency of the input voltage.

Mode I: Switches $S_{bb_{\rm pfc}}$ and $S_{bb_{\rm pc}}$ are turned ON at time t_0. During this time, the supply voltage charges the PFC converter inductor, $L_{bb_{\rm pfc}}$, whereas the combined input and dc-bus voltages charge the PC converter inductor, $L_{bb_{\rm pc}}$. The output capacitor ensured that the load current was constant. According to Fig. 4(a), this mode terminates when the switching $S_{bb_{\rm pc}}$ is turned OFF at time t_1.

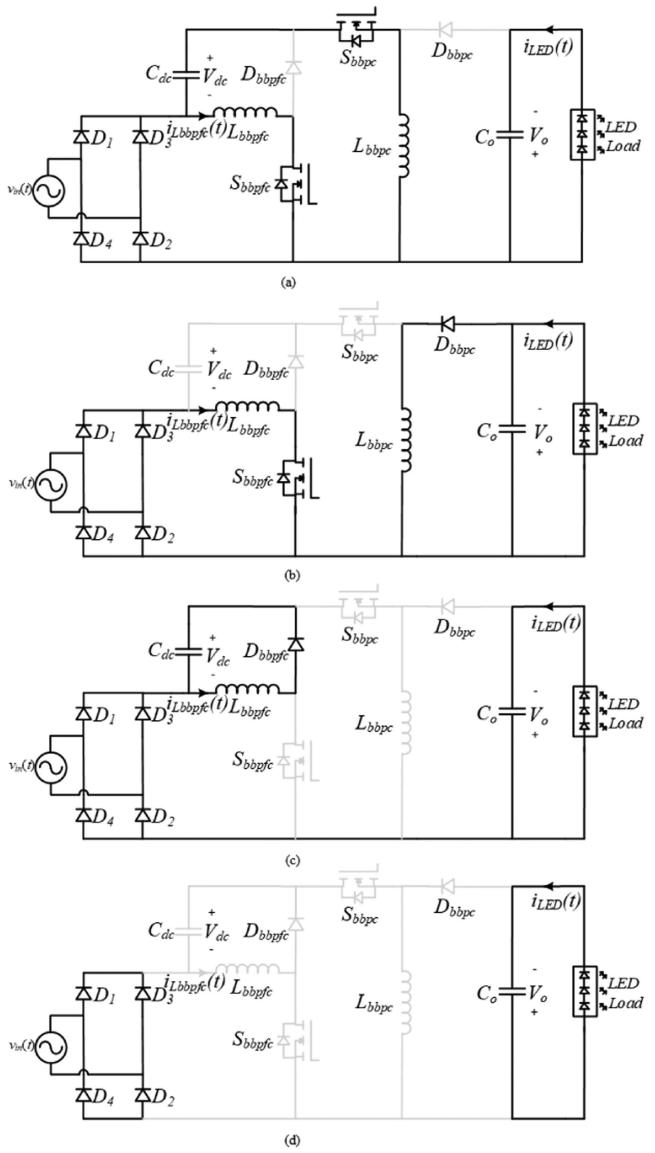

Fig. 4. Circuit operation for (a) Mode-I, (b) Mode-II, (c) Mode-III, and (d) Mode-IV.

Mode II: The switch $S_{bb_{\rm pfc}}$ of the PFC converter remains closed, and PFC inductor $L_{bb_{\rm pfc}}$ is continually charged. Simultaneously, at time t_1, the energy stored in the PC inductor $L_{bb_{\rm pc}}$ is redirected toward the output capacitor C_o via diode $D_{bb_{\rm pc}}$, as depicted in Fig. 4(b).

The maximum current flowing through the PC inductor $L_{bb_{\rm pc}}$ is represented by

$$i_{Lbbpc_{pk}}(t) = \frac{(V_m|\sin \omega t| + V_{\rm dc})\, d_2}{L_{bb_{\rm pc}} f_{\rm sw}} \tag{5}$$

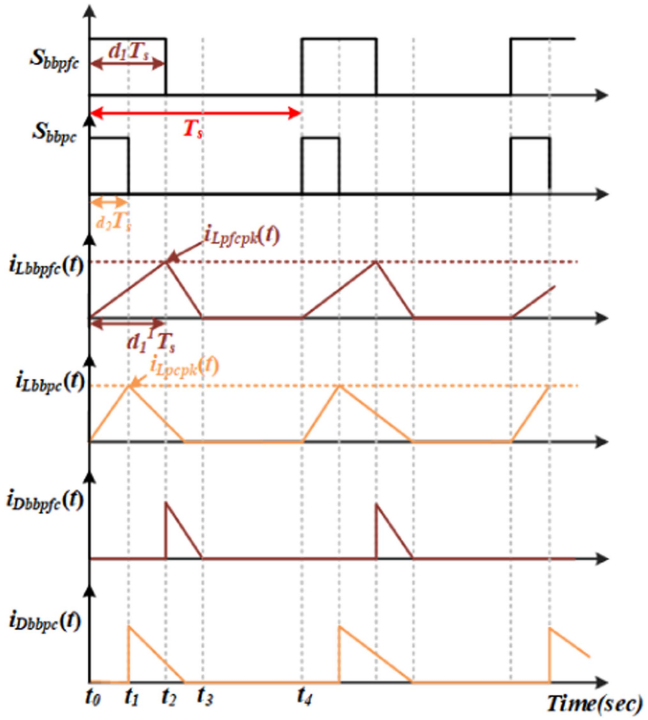

Fig. 5. Operating waveforms for each mode.

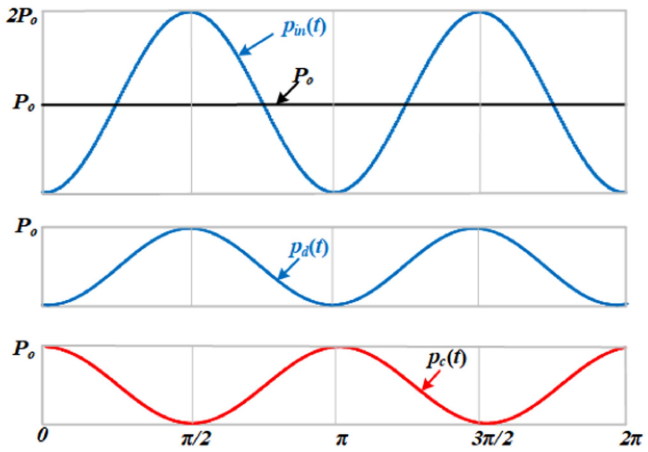

Fig. 6. Waveforms of $p_{\text{in}}(t)$, P_o, $p_d(t)$, and $p_c(t)$.

where d_2 is the duty cycle for $S_{bb_{\text{pc}}}$. The average value of PC inductor current during switch turn ON is

$$i_{Lbb\text{pc}_{\text{avg}}}(t) = \frac{(V_m|\sin\omega t| + V_{\text{dc}})d_2^2}{2L_{bb_{\text{pc}}}f_{\text{sw}}}. \tag{6}$$

The output power can be estimated as

$$P_o = \frac{d_2^2}{2\pi L_{bb_{\text{pc}}}f_{\text{sw}}}\int_0^{\pi}(V_m|\sin\omega t| + V_{\text{dc}})^2 dt \tag{7}$$

$$d_2 = \sqrt{\frac{2\pi P_o L_{bb_{\text{pc}}}f_{\text{sw}}}{\int_0^{\pi}(V_m|\sin\omega t| + V_{\text{dc}})^2 dt}}. \tag{8}$$

Mode III: The PFC buck–boost converter switch $S_{bb_{\text{pfc}}}$ is turned OFF at t_3. The energy stored in inductor $L_{bb_{\text{pfc}}}$ is discharged from $D_{bb_{\text{pfc}}}$ to C_{dc}, as shown in Fig. 4(c).

The peak value of PFC inductor current $L_{bb_{\text{pfc}}}$ during switch $S_{bb_{\text{pfc}}}$ ON is

$$i_{Lbb\text{pfc}_{pk}}(t) = \frac{V_m|\sin\omega t|d_1}{L_{bb_{\text{pfc}}}f_{\text{sw}}} \tag{9}$$

where d_1 is the duty cycle for $S_{bb_{\text{pfc}}}$. The average value of PFC inductor current during switch turn ON is

$$i_{Lbb\text{pfc}_{\text{avg}}}(t) = \frac{V_m|\sin\omega t|d_1^2}{2L_{bb_{\text{pfc}}}f_{\text{sw}}} \tag{10}$$

$$p_{o\text{pfc}} = \frac{V_m^2 d_1^2}{2L_{bb_{\text{pfc}}}f_{\text{sw}}} \tag{11}$$

$$d_1 = \frac{1}{V_m}\sqrt{2p_{o\text{pfc}}L_{bb_{\text{pfc}}}f_{\text{sw}}}. \tag{12}$$

The input current was determined by the average currents flowing through both inductors during the switch-ON period, which were added together

$$i_{\text{in}_{\text{avg}}}(t) = i_{Lbb\text{pfc}_{\text{avg}}}(t) + i_{Lbb\text{pc}_{\text{avg}}}(t) \tag{13}$$

$$i_{\text{in}_{\text{avg}}}(t) = \frac{V_m|\sin\omega t|d_1^2}{2L_{bb_{\text{pfc}}}f_{\text{sw}}} + \frac{(V_m|\sin\omega t| + V_{\text{dc}})d_2^2}{2L_{bb_{\text{pc}}}f_{\text{sw}}} \tag{14}$$

$$PF = \frac{P_{\text{in}}}{\frac{V_m i_{\text{in}_{\text{rms}}}}{\sqrt{2}}}. \tag{15}$$

At this time, the PF of the driver circuit was influenced by both converters. By decreasing the duty ratio d_2, a PF of approximately unity can be achieved. This can be achieved by raising the voltage across the storage capacitor to decrease the current in the PC converter.

Mode IV: Both the inductors have been discharged, and the output capacitor continues to deliver a constant output current to the load, as shown in Fig. 4(d).

A. Power Transfer Analysis

The value of K determines the division of the input power $p_{\text{in}}(t)$ into two halves, denoted as $p_r(t)$, half of which is routed to the PFC converter, stored in the storage capacitor, and then moved to the load via the PC converter. Denoted by $p_d(t)$, the second half was sent directly to the load via a PC converter, as shown in Fig. 6.

The reprocessing power can be estimated as

$$p_r(t) = Kp_{\text{in}}(t) = i_o(t) \times V_{\text{dc}}. \tag{16}$$

The power directly sending to the load is estimated as

$$p_d(t) = (1-K)p_{\text{in}}(t) = v_{\text{in}}(t) \times i_o(t) \tag{17}$$

$$p_{\text{in}}(t) = p_d(t) + p_r(t). \tag{18}$$

The conversion efficiency is the ratio of reprocessing power to total input power

$$\frac{p_{o_{\text{pfc}}}(t)}{p_{o_{\text{pc}}}(t)} = \frac{i_o(t) \times V_{\text{dc}}}{i_o(t) \times V_{\text{dc}} + V_{\text{in}} \times i_o(t)} \tag{19}$$

$$\frac{p_{o_{\text{pfc}}}(t)}{p_{o_{\text{pc}}}(t)} = \frac{K\eta_{bb_{\text{pfc}}}\eta_{bb_{\text{pc}}}}{K\eta_{bb_{\text{pfc}}}\eta_{bb_{\text{pc}}} + (1-K)\eta_{bb_{\text{pc}}}} \tag{20}$$

where $\eta_{bb_{\text{pfc}}}$ and $\eta_{bb_{\text{pc}}}$ are the efficiencies of PFC and PC converters, respectively. From (14) and (15)

$$K = \frac{V_{\text{dc}}}{V_{\text{dc}} + V_{\text{in}}\eta_{bb_{\text{pfc}}}}. \tag{21}$$

It is important to remember that the quantity of reprocessed power increases with storage capacitor voltage V_{dc} and that the efficiency benefit eventually becomes less significant. Selecting the voltage across the storage capacitor was the first step toward an efficient driver design.

The PFC converter voltage gain, denoted as $V_{bb_{\text{pfc}}}$, is expressed as

$$V_{bb_{\text{pfc}}} = \frac{V_{\text{dc}}}{V_{\text{in}}}. \tag{22}$$

The PC converter voltage gain, denoted as $V_{bb_{\text{pc}}}$, is expressed as

$$V_{bb_{\text{pc}}} = \frac{V_o}{V_{\text{dc}} + V_{\text{in}}}. \tag{23}$$

The LED driver overall voltage gain, denoted as $V_{g_{\text{driver}}}$, is expressed as

$$V_{g_{\text{driver}}} = V_{bb_{\text{pc}}}(1 + V_{bb_{\text{pfc}}}). \tag{24}$$

The value of K can be written in terms of voltage gains is

$$K = \frac{V_{bb_{\text{pfc}}}}{V_{bb_{\text{pfc}}} + \eta_{bb_{\text{pfc}}}}. \tag{25}$$

The overall efficiency of the driver circuit can be estimated as

$$\eta_{\text{driver}} = K\eta_{bb_{\text{pfc}}}\eta_{bb_{\text{pc}}} + (1-K)\eta_{bb_{\text{pc}}}. \tag{26}$$

Substituting K in (21)

$$\eta_{\text{driver}} = \eta_{bb_{\text{pfc}}}\eta_{bb_{\text{pc}}}\left(\frac{V_{bb_{\text{pfc}}} + 1}{V_{bb_{\text{pfc}}} + \eta_{bb_{\text{pfc}}}}\right). \tag{27}$$

From the above analysis, $p_r(t)$ and $p_d(t)$ can be represented as

$$p_r(t) = Kp_{\text{in}}(t) = 2KP_o\sin^2\omega t \tag{28}$$

$$p_d(t) = (1-K)p_{\text{in}}(t) = (1-K)2P_o\sin^2\omega t. \tag{29}$$

In order to get constant output power, the PC converter can be reshaped to reprocessing power $p_r(t)$ in to cancelation power $p_c(t)$. The required cancelation power $p_c(t)$ for obtaining constant output power can be estimated as

$$p_c(t) = P_o - p_d(t) \tag{30}$$

$$p_c(t) = P_o - p_d(t) = P_o - (1-K)2P_o\sin^2\omega t \tag{31}$$

$$p_c(t) = P_o - (1-K)2P_o(1-\cos^2\omega t) \tag{32}$$

$$p_c(t) = P_o(2K-1) + 2(1-K)P_o\cos^2\omega t. \tag{33}$$

To cancel ripple on output power, choose power splitting ratio K that produces enough $p_c(t)$. To achieve this, K must be equal to 0.5. To account for power losses during reprocessing, K needs to be

$$K \geq 0.5. \tag{34}$$

The output power P_o can be obtained by adding $p_d(t)$ and $p_c(t)$

$$P_o = p_d(t) + p_c(t) \tag{35}$$

$$= (1-K)2P_o\sin^2\omega t + P_o(2K-1) + 2(1-K)P_o\cos^2\omega t = P_o. \tag{36}$$

The input power splitting based on the value of K in the experimental work was chosen to be 0.52, and in this case, the reprocessing power was 52% to compensate for the losses in the PC converter.

IV. Design

The design of the converter focuses on decreasing the reprocessing power by enhancing the input PF, with the overall efficiency as the goal. This can be achieved by reducing d_2, which reduces the current through the PC inductor, while increasing the voltage across the storage capacitor. Reducing the reprocessing power managed by the PFC converter contributes to high efficiency. However, to attain a high PF, the voltage across the storage capacitor must be increased, which might reduce the efficiency. The balance between the PF and the efficiency depends on the voltage across the capacitor. To satisfy these requirements, the PFC converter functions in the DCM at an input power of 50%. The PFC converter output current is

$$i_{obb_{\text{pfc}}} = \frac{V_m|\sin\omega t|d_1(d_1' - d_1)}{2L_{bb_{\text{pfc}}}f_{\text{sw}}} \tag{37}$$

$$d_1' = \frac{2i_{obb_{\text{pfc}}}L_{bb_{\text{pfc}}}f_{\text{sw}} + V_m|\sin\omega t|d_1^2}{V_m|\sin\omega t|d_1}. \tag{38}$$

From inductor vol–sec balance

$$d_1' = \frac{(V_m|\sin\omega t| + V_{\text{dc}})d_1}{V_{\text{dc}}}. \tag{39}$$

From (28) and (29)

$$v_{\text{dc}} = \frac{V_m^2|\sin^2\omega t|d_1^2}{2i_{obb_{\text{pfc}}}L_{bb_{\text{pfc}}}f_{\text{sw}}}. \tag{40}$$

The power processed by PFC converter is

$$P_{bb_{\text{pfc}}} = \frac{V_m^2 d_1^2}{2L_{bb_{\text{pfc}}}f_{\text{sw}}} \tag{41}$$

$$L_{bb_{\text{pfc}}} = \frac{V_m^2 d_1^2}{2P_{bb_{\text{pfc}}}f_{\text{sw}}}. \tag{42}$$

The peak value of PC inductor $L_{bb_{\text{pc}}}$ current, when operating in DCM is

$$i_{bb_{\text{pc}}}(t) = \frac{(V_m|\sin\omega t| + V_{\text{dc}})d_2}{L_{bb_{\text{pc}}}f_{\text{sw}}}. \tag{43}$$

The average power processed by PC converter is estimated as

$$P_{bb_{\text{pc}}} = \frac{(V_m + V_c)^2 d_2^2}{4L_{bb_{\text{pc}}}f_{\text{sw}}} \tag{44}$$

$$L_{bb_{\text{pc}}} = \frac{(V_m + V_c)^2 d_2^2}{2P_o f_{\text{sw}}}. \tag{45}$$

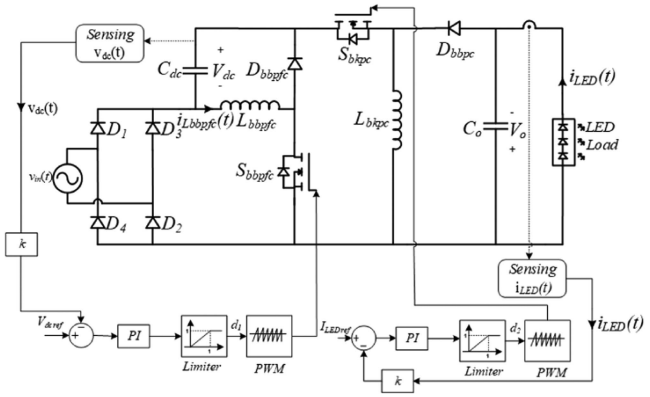

Fig. 7. Independent PI controllers for PFC and PC converters.

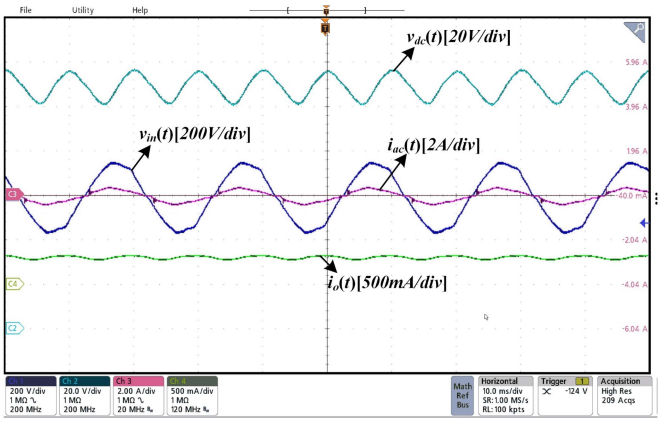

Fig. 8. Input voltage $v_{\text{in}}(t)$, input AC current $i_{\text{ac}}(t)$, output current $i_o(t)$, and storage capacitor voltage $v_{\text{dc}}(t)$ at 30 W power output.

The output current $i_o(t)$ is determined as

$$i_o(t) = \frac{(V_m|\sin\omega t| + V_{\text{dc}})d_2}{2L_{bb_{\text{pc}}}f_{\text{sw}}}(d_2' - d_2) \tag{46}$$

$$d_2' = \frac{V_m|\sin\omega t| + V_{\text{dc}}}{V_o} + 1 \tag{47}$$

$$V_o = \frac{(V_m|\sin\omega t| + V_{\text{dc}})^2 d_2^2}{2I_o L_{bb_{\text{pc}}}f_{\text{sw}}}. \tag{48}$$

A. Control Design

A ripple-cancelation method was implemented to maintain a constant output current, as shown in Fig. 7. The switch-triggering sequence does not require adjustment because of its straightforward power distribution. This is because both converters operate independently, requiring only a basic control scheme. The control variable d_1 was responsible for controlling the current of the PFC converter and ensuring its performance. It is crucial to balance the power input and output, and maintain a constant average dc voltage $v_{\text{dc}}(t)$ throughout each line period. The average value of $v_{\text{dc}}(t)$ is set to V_{dc} and used as a reference to maintain the voltage at a certain level. By comparing the actual voltage $v_{\text{dc}}(t)$ with the reference voltage $V_{\text{dc}}^{\text{ref}}$, an error signal was

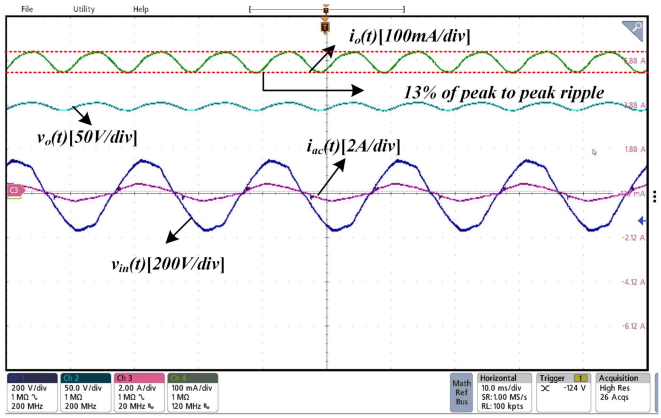

Fig. 9. Input voltage $v_{\text{in}}(t)$, input AC current $i_{\text{ac}}(t)$, output current $i_o(t)$, and output voltage $v_o(t)$ at 30 W power output.

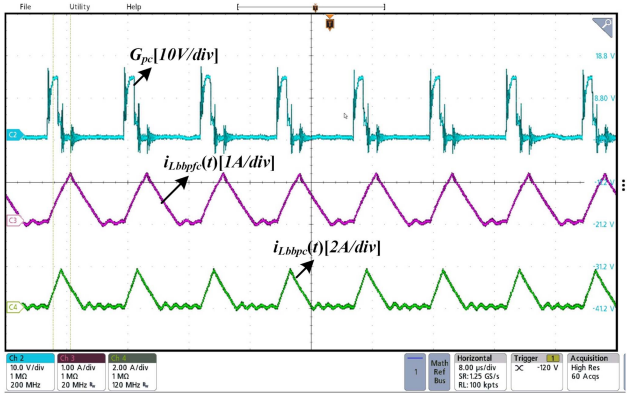

Fig. 10. Gate signal for $S_{bb_{\text{pc}}}$, PFC inductor current $i_{Lbb_{\text{pfc}}}(t)$, and PC inductor current $i_{Lbb_{\text{pc}}}(t)$.

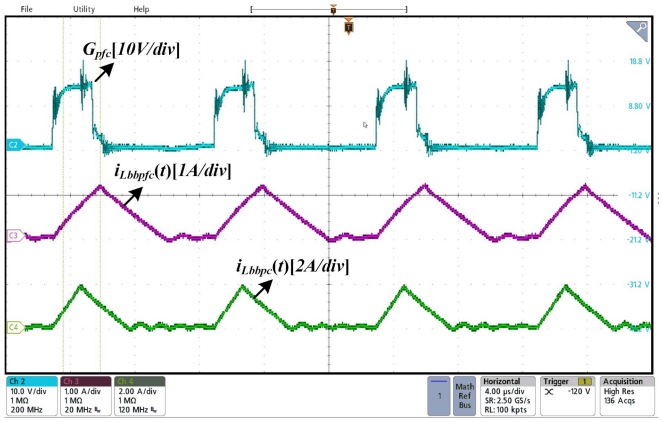

Fig. 11. Gate signal for $S_{bb_{\text{pfc}}}$, PFC inductor current $i_{Lbb_{\text{pfc}}}(t)$, and PC inductor current $i_{Lbb_{\text{pc}}}(t)$.

generated and sent to the proportional–integral (PI) controller. Consequently, as shown in Fig. 8, the controller generates signal d_1 for switch $S_{bb_{\text{pfc}}}$. A pulsewidth modulation (PWM) signal for $S_{bb_{\text{pfc}}}$ was generated using a (TMS320F28379D) DSP controller. The power necessary to remove the output ripples is determined

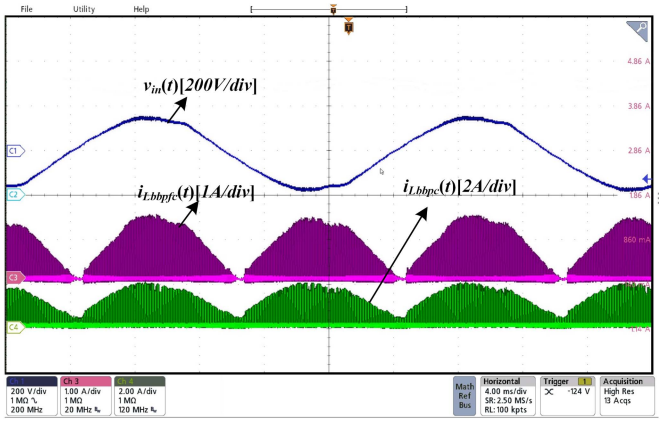

Fig. 12. Overview of PFC inductor current $i_{Lbb_{\text{pfc}}}(t)$, and PC inductor current $i_{Lbb_{\text{pc}}}(t)$, and input voltage $v_{\text{in}}(t)$.

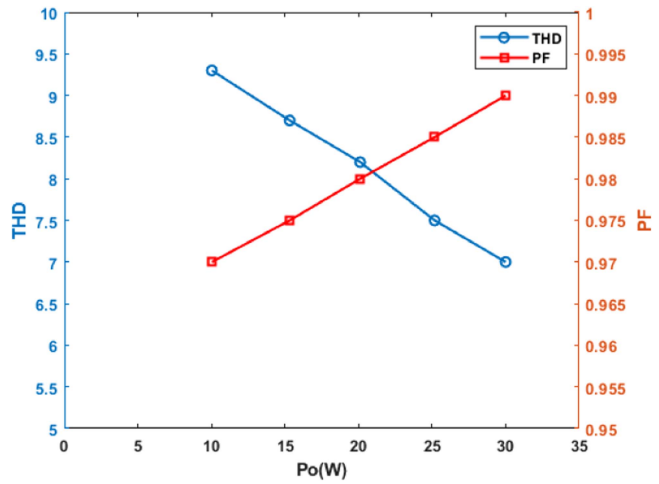

Fig. 13. THD and PF with respect to load variation.

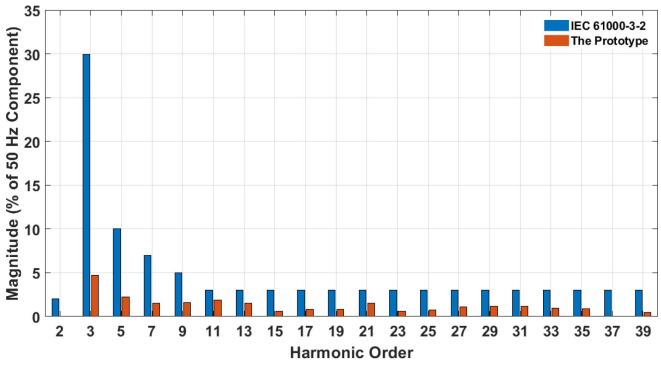

Fig. 14. Lower order input current harmonics.

using the control variable d_2. The average output current, $i_o(t)$, was used as a reference to maintain a constant current. An error signal was generated and sent to a PI controller after comparing the reference output (I_{oref}) with the actual output ($i_o(t)$). The controller then calculates d_2 for switch $S_{bb_{\text{pc}}}$, as shown in Fig. 7, and the PWM signal for $S_{bb_{\text{pc}}}$ is produced by

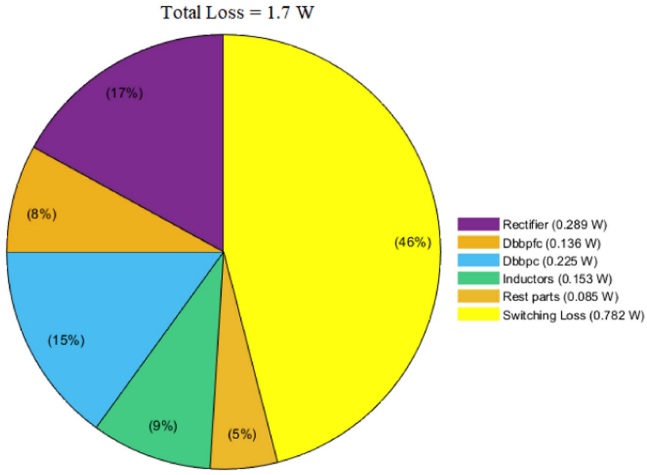

Fig. 15. Loss distribution.

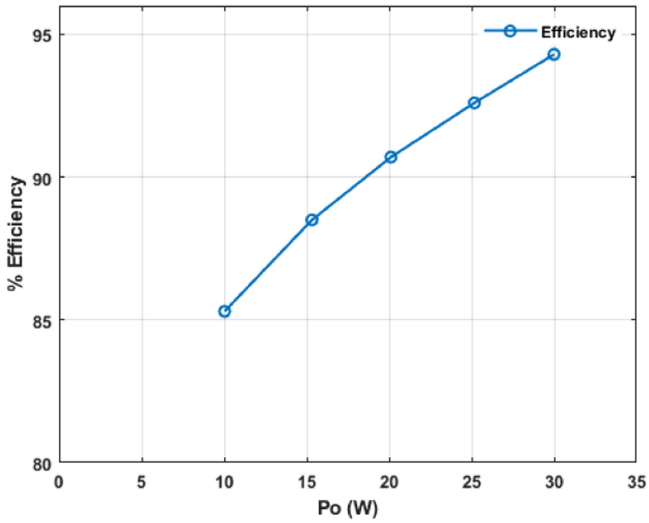

Fig. 16. Load versus efficiency graph.

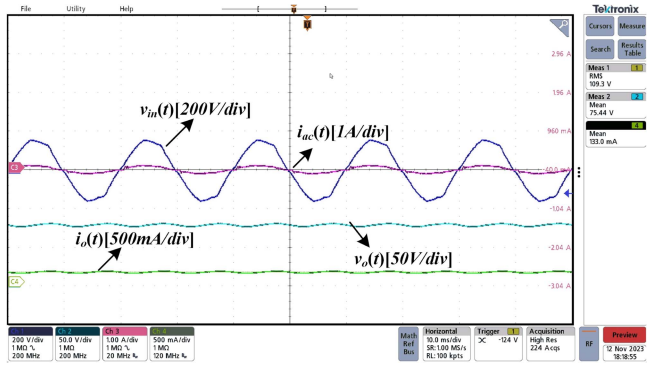

Fig. 17. Input and output voltage and current waveforms at 10 W.

the (TMS320F28379D) DSP controller. The output current was maintained con stant during each line period through the control variable d_2.

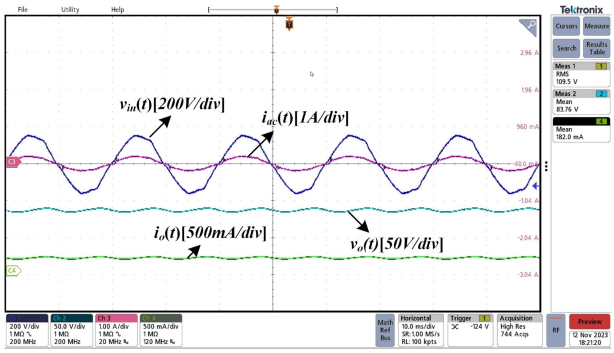

Fig. 18. Input and output voltage and current waveforms at 15 W.

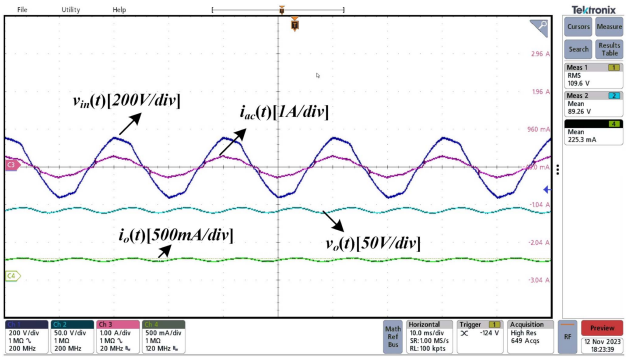

Fig. 19. Input and output voltage and current waveforms at 20 W.

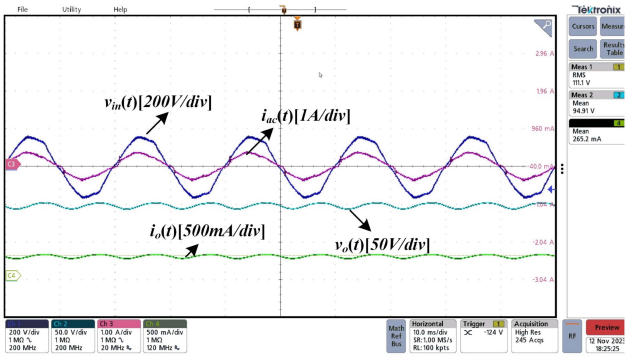

Fig. 20. Input and output voltage and current waveforms at 25 W.

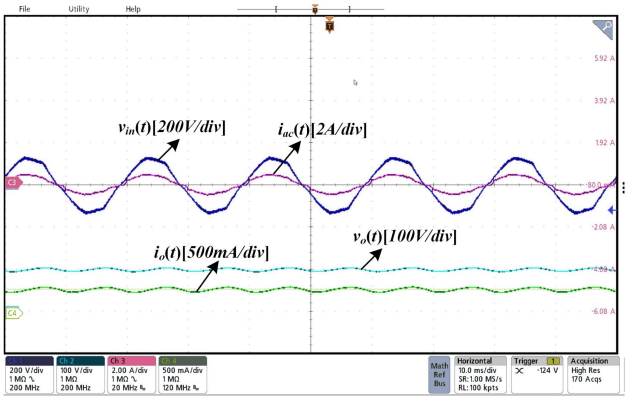

Fig. 21. Input and output voltage and current waveforms at 90 V.

TABLE I
PARAMETERS OF 30 W PROTOTYPE

Parameter	Specification
Input Voltage $v_{\text{in}}(t)$	110 V RMS AC
Supply Frequency, f	50 Hz
PFC Inductor, $L_{bb_{\text{pfc}}}$	306 μH
PC Inductor, $L_{bb_{\text{pc}}}$	147 μH
Output Capacitor (10K250), C_o	2 × 10 μF, 250 V
DC bus Capacitor (10K250), C_{dc}	2 × 10 μF, 250 V
Switches ($S_{bb_{\text{pfc}}}$ and $S_{bb_{\text{pc}}}$)	IRFP460
Diodes ($D_{bb_{\text{pfc}}}$ and $D_{bb_{\text{pc}}}$)	LTTH806DF
Output Current, I_o	0.3 A
Output Voltage, V_o	100 V
Switching Frequency, f_{sw}	100 kHz

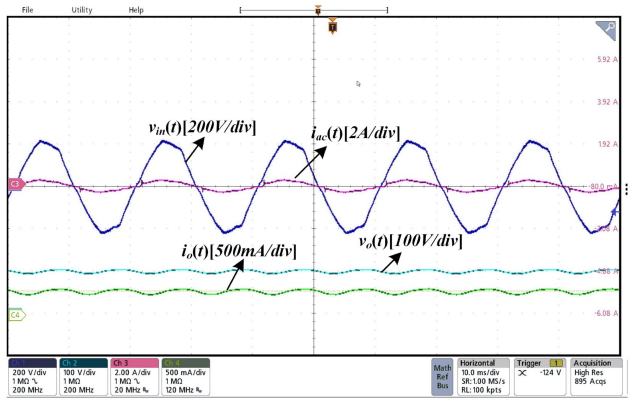

Fig. 22. Input and output voltage and current waveforms at 150 V.

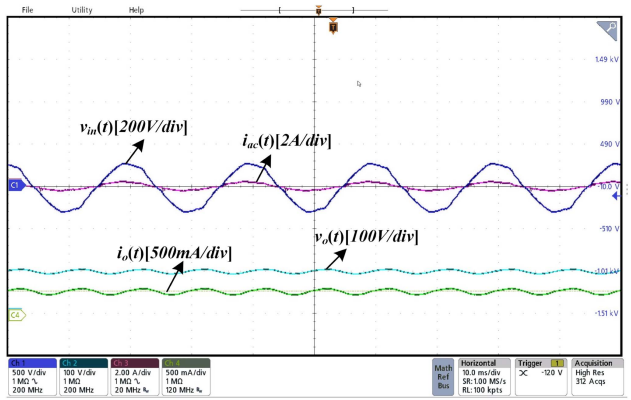

Fig. 23. Input and output voltage and current waveforms at 200 V.

V. EXPERIMENTAL RESULTS

A prototype of 30 W was designed and tested to prove the viability of the proposed driver circuit. The design parameters are presented in Table I.

The input current is proportional to the input voltage and produces the desired dc output, and the splitting of the power between two converters is depending on the voltage ratio of storage capacitor and input voltage, in the experimental work, the splitting ratio was chosen as 0.5, as shown in Fig. 8. The peak-to-peak ripple in the LED current is 13%, and ac current requirements are met with 0.99 input PF and less total harmonic distortion (THD), as per the results shown in Fig. 9. When switch

TABLE II
RESULTS OF PROTOTYPE COMPARED TO EXISTING REDUCED POWER PROCESSING SCHEMES

Parameter	[10]	[12]	[24]	[27]	[28]	[29]	[30]	[prototype]
Power Processing	8%	50%	32%	50%	50%	40%	50%	50%
Switches	3	2	3	2	2	1	2	2
Diodes	3	4	3	3	2	4	2	2
Magnetics	4	4	2	3	2	2	2	2
Capacitors	2	2	2	2	2	2	2	2
LED load current ripple	10%	-	-	5%	6%	19%	4%	13%
THD	-	7.388%	-	5%	11.75%	7%	10.64%	7%
Control Complexity	Increased	Decreased	Increased	Increased	Increased	Decreased	Decreased	Decreased
Peak efficiency	89.5%	81%	90%	85%	91.5%	92.4%	92.5%	94.4%
Power Rating	23 W	29.7 W	16 W	15 W	27 W	37.6 W	45 W	30 W

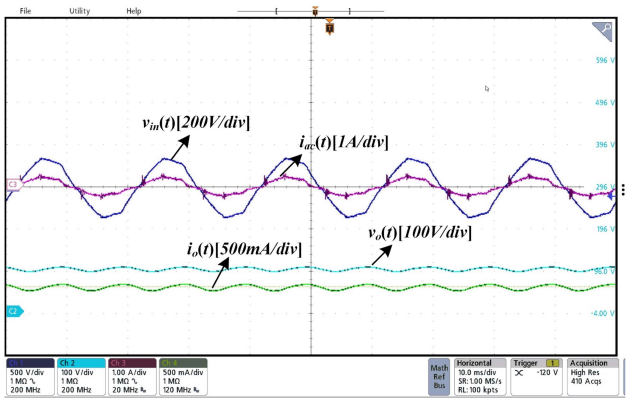

Fig. 24. Input and output voltage and current waveforms at 240 V.

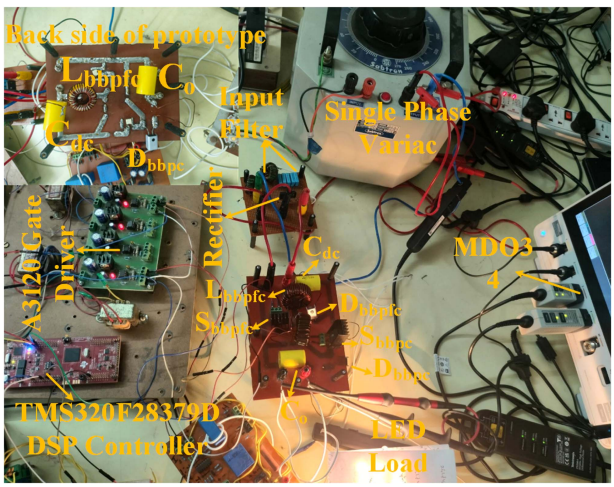

Fig. 25. Prototype design.

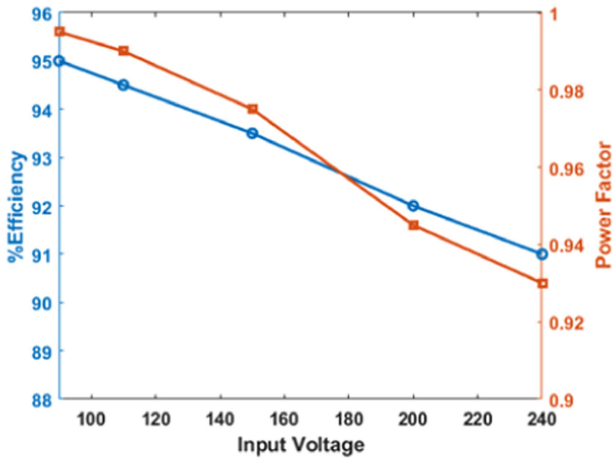

Fig. 26. % Efficiency and PF with universal input voltage.

$S_{bb_{pc}}$ is turned ON, it causes inductor $L_{bb_{pc}}$ to be charged, and when it is turned OFF, the inductor discharges from $D_{bb_{pc}}$ to C_o, as shown in Fig. 10. According to theoretical analysis, when switch $S_{bb_{pfc}}$ was turned ON, inductor $L_{bb_{pfc}}$ was charging, and when the switch was $S_{bb_{pfc}}$ turned OFF, the inductor $L_{bb_{pfc}}$ was discharged through $D_{bb_{pfc}}$ to C_{dc}, as shown in the Fig. 11. An overview of the inductor current is shown in Fig. 12.

The PF and THD with load variation are shown in Fig. 13. The input current's lower order harmonics are 7%, which comply with the IEC 61000-3-2 standard, as shown in Fig. 14. The loss analysis results are shown in Fig. 15. The efficiency with load variation is shown in Fig. 16. Table II gives the results of proposed LED driver, which is compared with existing reduced power processing LED drivers. The proposed driver, tested for dimming at different power levels, is shown in Figs. 17–20. The proposed driver, tested for universal input voltage range, and the results are shown in Figs. 21–24. The prototype of proposed LED driver is shown in Fig. 25. The variation of efficiency and PF with respect to universal voltage is depicted in Fig. 26. The results obtained from testing across a range of universal voltages show a decrease in efficiency and PF. In addition, the input current THD is significantly affected by these variations of input voltage.

VI. CONCLUSION

This article introduces an LED driver designed to enhance efficiency by reducing power processing. The driver circuit comprises two buck–boost converters that allow for an input PF near unity, a low-input-current THD, and a constant LED current in the output, which eliminates flickering in the LED current. The input-side buck–boost converter acts as a PFC converter operating in DCM to achieve a high PF by maintaining a constant duty ratio. The other buck–boost converter functions as a PC converter owing to its voltage follower characteristics. The ripple cancelation method enhances the driver's lifespan

by minimizing the output ripple and replacing the E-caps with film capacitors. The input power is split into two parts based on the value of K, which directly affects conversion efficiency. The power distribution on the input side does not require any additional switches or diodes, resulting in an improved efficiency and reduced size. The 30-W LED driver displayed consistent results, including a PF of 0.99, compliance with IEC 61000-3-2 standards for lower order harmonics of 7%, and a peak efficiency of 94.4% at full-load power. The driver's ability to function effectively with universal input voltage requirements, combined with its capacity to operate smoothly at various dimming levels, ensures its feasibility.

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