Letters

A Three-Switch AC–DC Converter With Buck/Boost Ability, Low Leakage Current, and Continuous Input/Output Currents

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***Abstract*—This letter proposes a three-switch ac–dc converter with buck/boost ability, low leakage current, and continuous input/output currents. Therefore, a wide output voltage range and no bulky electromagnetic interference filters can be achieved. Furthermore, the proposed topology can transfer pulsating power, reducing the demand for the output capacitance. Without a complex structure, the total component count is only nine and a high power density can be obtained. In addition, benchmarking is provided to compare various performance aspects with existing topologies. Finally, the validity of the topology is verified by the experimental results.**

***Index Terms*—Buck/boost, common ground, continuous input/output currents, high power density, three-switch.**

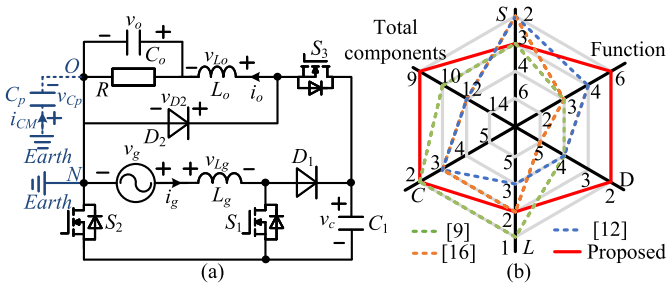

Fig. 1. Topology and comparisons. (a) Proposed three-switch AC–DC converter. (b) Categorization of single-phase AC–DC converters.

I. Introduction

TRADITIONAL ac–dc converters can only achieve buck or boost output, making it difficult to adapt to situations with a wide voltage output range [1], [2], [3]. To address this issue, some buck/boost ac–dc converters have been proposed [4], [5], [6], [7], [8]. Bridgeless ac–dc converters reduce conduction losses due to the elimination of the diode bridge, but they suffer from significant common-mode (CM) noise and leakage current [1], [8], [9], [10], [11]. To suppress the CM noise and leakage current in bridgeless converters, a scheme connecting the ac ground and dc ground has been proposed, which theoretically can completely eliminate CM voltage and leakage current [2], [3], [12], [13].

Existing ac–dc converters have discontinuous currents on the input or output side. The input side requires the design of bulky electromagnetic interference (EMI) filters [14], and the output side increases the effective value of the dc capacitor current, resulting in larger capacitor volume [2], [9]. An ac–dc converter with both continuous input and output currents has been proposed [3], [15]. To buffer the unbalanced power between the ac and dc sides, bulky and short-lived electrolytic capacitors are used, reducing the reliability of the system [1], [12], [15]. Some ac–dc converters with power decoupling capabilities have been proposed, which can reduce the demand for the output capacitance [2], [3], [16].

In summary, existing literature cannot simultaneously satisfy six functions as buck, boost, low leakage current, continuous input/output current (CIC and COC), and power decoupling, as shown in Fig. 1. Moreover, more functionalities would require more components, leading to a decrease in the system's power density and reliability. In this letter, a three-switch ac–dc converter that possesses the functionalities above is proposed. The structure is compact with only nine components. The advantages of the topology are summarized as follows.

1) The proposed topology possesses buck/boost output capabilities, making it adaptable to wide voltage scenarios.
2) The ac and dc ground are connected, eliminating CM voltage and leakage current, thereby obviating the need for bulky EMI filters.
3) The proposed topology features continuous input and output currents, simplifying the design of the filter and reducing the demand for output capacitance.
4) The proposed topology has power decoupling capabilities, eliminating the additional power decoupling circuits and reducing the requirement for output capacitance.

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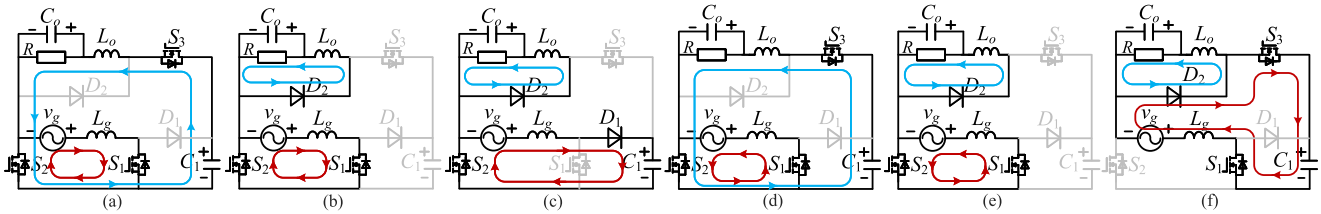

Fig. 2. Operation modes: (a)–(c) when $v_g > 0$, (d)–(f) when $v_g < 0$. (a) Mode1. (b) Mode2. (c) Mode3. (d) Mode4. (e) Mode5. (f) Mode6.

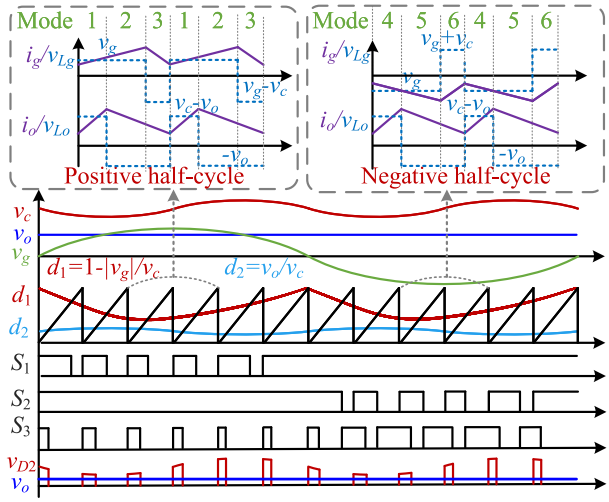

Fig. 3. Modulation strategy and drive signals.

5) The proposed topology only requires nine components in total with three switches, offering high power density.

II. Proposed Three-Switch AC–DC Converter

A. Operation Principle and Buck/Boost Characteristics

The proposed three-switch ac–dc converter is shown in Fig. 1. L_g, L_o, C_1, C_o, and R represent the input inductor, output inductor, intermediate capacitor, output capacitor, and load resistor, respectively. There is a parasitic capacitance C_p between the ac ground (N) and the dc ground (O). Fig. 2 presents the six modes of the proposed topology.

The pulse width modulation scheme is shown in Fig. 3, where $v_g, v_c, v_o, v_{D2}, v_{Lg}, v_{Lo}, i_g$, and i_o represent the input voltage, the voltage of C_1, the output voltage, the voltage of diode D_2, input inductor L_g and output inductor L_o, the current of input inductor L_g and output inductor L_o. The input/output current, i_g/i_o, are both in a continuous state.

Define two modulation signals, $d_1 = 1 - |v_g|/v_c$ for controlling v_c, and $d_2 = v_o/v_c$ for controlling v_o. The gain can be expressed as $d_2/(1-d_1)$ where $d_1 > d_2$. By appropriately setting d_1 and d_2, boost and buck output can be achieved.

The duty cycles for the six modes are defined as $d_{\text{mode}N}$ (N=6)

$$\begin{cases} d_1 = d_{\text{Mode1}} + d_{\text{Mode2}}, d_2 = d_{\text{Mode2}}; \text{when } v_g \geq 0 \\ d_1 = d_{\text{Mode4}} + d_{\text{Mode5}}, d_2 = d_{\text{Mode4}}; \text{when } v_g < 0 \\ 0 < d_2 < d_1 < 1. \end{cases} \quad (1)$$

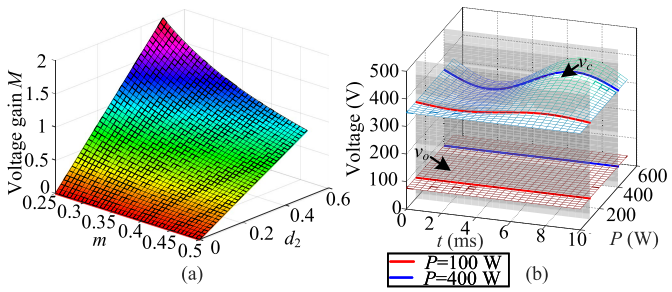

Fig. 4. 3-D diagrams. (a) Voltage gain varies with m and d_2. (b) v_c and v_o varying with P.

The duty ratio of S_1, S_2, S_3 in positive half-cycle can be derived as follows:

$$d_{s1} = d_{\text{Mode1}} + d_{\text{Mode2}},\ d_{s2} = 1,\ d_{s3} = d_{\text{Mode1}}. \quad (2)$$

Combining the relationships of d_1, d_2, v_g, v_c, and v_o, so (2) can be rewritten as follows:

$$d_{s1} = 1 - |v_g|/v_c, d_{s2} = 1, d_{s3} = v_o/v_c. \quad (3)$$

Similarly, the duty ratio of S_1, S_2, S_3 in a negative half-cycle can be derived as follows:

$$d_{s1} = 1, d_{s2} = d_{\text{Mode4}} + d_{\text{Mode5}}, d_{s3} = d_{\text{Mode4}} + d_{\text{Mode6}}. \quad (4)$$

Equation (4) can be rewritten as follows:

$$d_{s1} = 1, d_{s2} = 1 - |v_g|/v_c, d_{s3} = (|v_g| + v_o)/v_c. \quad (5)$$

Assuming $v_g = V_{gm}\sin(\omega t)$ where V_{gm} and ω represent the amplitude of grid voltage and angular frequency of the grid voltage, respectively. Define the modulation ratio $m = V_{gm}/v_c$ and the voltage gain $M = v_o/V_{gm} = d_2/m$. The 3-D diagram shows regions with $M \geq 1$ and $M \leq 1$, verifying the buck/boost ability as shown in Fig. 4(a).

Since all duty cycles are limited from 0 to 1, the voltage constraint is $|v_g| + v_o \leq v_c$. Introduce secondary pulsation into d_1 and d_2, making the output voltage ripple-free, achieving the decoupling of ac power and dc power, as shown in Figs. 3 and 4(b). A larger transmission power will lead to more pronounced secondary pulsations in d_1 and d_2. v_o is equal to the average value of v_{D2}, with no ripple.

B. Leakage Current Analysis

Fig. 5(a) shows the layout of a single-phase nonisolated ac–dc converter [17]. The capacitor voltage v_{C_p} is applied to C_p,

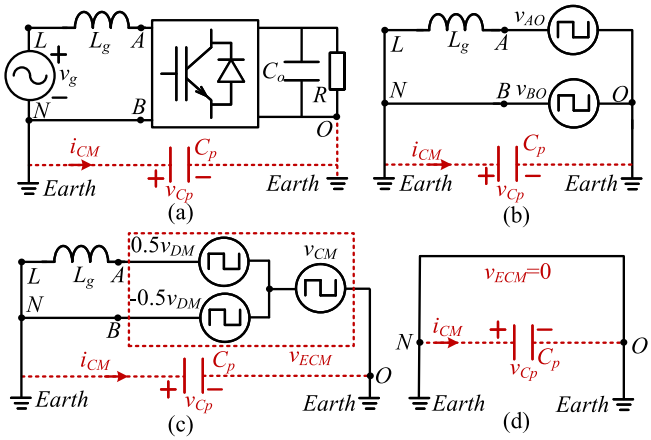

Fig. 5. CM model showing (a) General layout of a single-phase transformerless AC–DC converter. (b) Equivalent circuit for analyzing the CM current. (c) Equivalent CM circuit of the proposed converter. (d) Simplified single-loop CM model of the proposed converter.

resulting in the generation of a leakage current i_{CM}. Fig. 5(b)–(c) shows the CM equivalent circuit, and Fig. 5(d) shows the simplified CM equivalent circuit. v_{AO}, v_{BO}, v_{LO}, and v_{NO} represent the voltages at points A, B, L, and N with respect to point O. The expressions for v_{AO} and v_{BO} can be expressed based on CM voltage v_{CM} and differential-mode (DM) voltage v_{DM} are as follows:

$$\begin{cases} v_{AO} = v_{\mathrm{CM}} + 0.5 v_{\mathrm{DM}} \\ v_{BO} = v_{\mathrm{CM}} - 0.5 v_{\mathrm{DM}}. \end{cases} \tag{6}$$

The voltages v_{AO} and v_{BO} can be combined to form an equivalent CM voltage v_{ECM}, as shown in (7) and Fig. 5(c). v_{ECM} of the proposed converter is zero as shown in Fig. 5(d), so the leakage current can be eliminated

$$\begin{cases} v_{\mathrm{CM}} = 0.5(v_{AO} + v_{BO}),\ v_{\mathrm{DM}} = v_{AO} - v_{BO} \\ v_{ECM} = v_{\mathrm{CM}} - 0.5 v_{\mathrm{DM}} = v_{BO} = v_{NO} = 0. \end{cases} \tag{7}$$

C. Control Strategy for Output Voltage Ripple Suppression

To design a closed-loop controller and evaluate stability, it is necessary to analyze the small-signal model. In the proposed ac–dc converter, the inductor currents i_g and i_o, and the capacitor voltage v_c and v_o are defined as state variables [18]. Each variable contains steady-state components, such as V_g, V_c, V_o, I_g, I_o, D_1, D_2, and ac small-signal components, such as $\hat{v_g}$, $\hat{v_c}$, $\hat{v_o}$, $\hat{i_g}$, $\hat{i_o}$, $\hat{d_1}$, and $\hat{d_2}$. R_{eq} is defined as equivalent load resistance, as follows:

$$\begin{cases} v_g = V_g + \hat{v_g}; v_c = V_c + \hat{v_c}; v_o = V_o + \hat{v_o} \\ i_g = I_g + \hat{i_g}; i_o = I_o + \hat{i_o}; R_{eq} = R/D_2^2 \\ d_1 = D_1 + \hat{d_1}; d_2 = D_2 + \hat{d_2}. \end{cases} \tag{8}$$

Adding small perturbations to state variables and control variables, the small-signal model of the proposed ac–dc converter

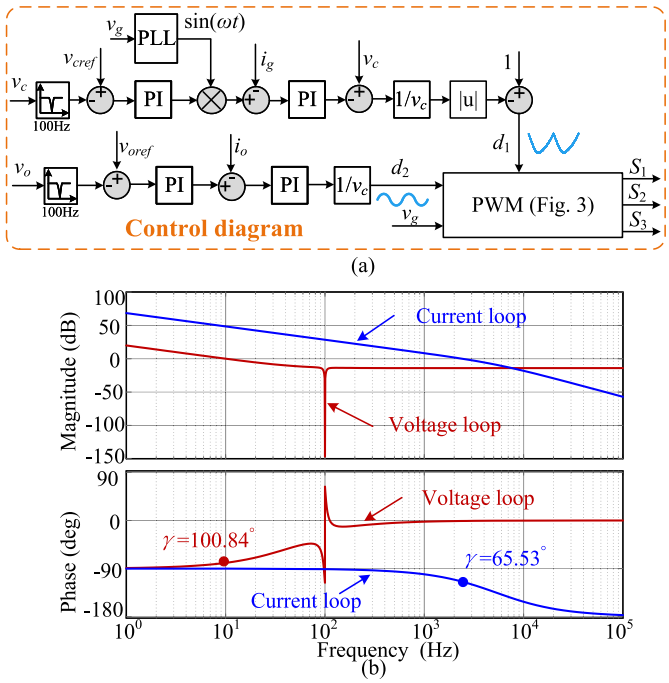

Fig. 6. Controller and stability analysis. (a) Control diagram. (b) Bode diagram.

can be expressed as follows:

$$\begin{cases} L_g \frac{d\hat{i_g}}{dt} = \hat{v_g} - (1 - D_1)\hat{v_c} + V_c \hat{d_1} \\ C_1 \frac{d\hat{v_c}}{dt} = (1 - D_1)\hat{i_g} - \frac{\hat{v_c}}{R_{\mathrm{eq}}} - I_g \hat{d_1} \\ L_o \frac{d\hat{i_o}}{dt} = -\hat{v_o} + D_2 \hat{v_c} + V_c \hat{d_2} \\ C_o \frac{d\hat{v_o}}{dt} = \hat{i_o} - \frac{\hat{v_o}}{R}. \end{cases} \tag{9}$$

From the small-signal model, control-to-output transfer functions $G_1(s)$ and $G_2(s)$ of the proposed converter can be derived as follows:

$$\begin{cases} G_1(s) = \frac{\hat{v_c}(s)}{\hat{d_1}(s)} = \frac{V_c[(1-D_1)R_{\mathrm{eq}} - sL_g/(1-D_1)]}{L_g R_{\mathrm{eq}} C_1 s^2 + sL_g + R_{\mathrm{eq}}(1-D_1)^2} \\ G_2(s) = \frac{\hat{v_o}(s)}{\hat{d_2}(s)} = \frac{V_c R}{L_o R C_o s^2 + sL_o + R}. \end{cases} \tag{10}$$

The duty ratios d_1 and d_2 can be obtained through the existing control scheme [3], without the need for redesign. As shown in Fig. 6(a), the first control loop is to control the voltage of C_1 and make the grid current sinusoidal. The second control loop is to control the output voltage and suppress the fluctuation of the output voltage. v_{cref} and v_{oref} represent the reference of v_c and v_o, respectively. Both control loops contain a current loop and a voltage loop. Taking the second control loop as an example, the bode diagram is shown in Fig. 6(b). It can be obtained that the harmonic component at twice the grid frequency in the output voltage is suppressed, and the phase margins of the voltage loop and current loop are $100.84°$ and $65.53°$, respectively, indicating that the system is stable.

III. Design Considerations

A. Semiconductors Rating

Similar to buck/boost ac–dc converter [16], the maximum value expression of v_c can be obtained as (11) where P and v_{cripple} represent the power and the fluctuation value of v_c

$$v_{c\max} \geq (V_{gm} + v_o) + v_{\text{cripple}}. \tag{11}$$

The voltage stress of the switches and diodes in the proposed topology is $v_{c\max}$. According to Fig. 2, the current stress of S_1 and D_1 is I_g, the current stress of S_2 and D_2 is $I_g + i_o$, and the current stress of S_3 is $\text{Max}\{I_g, I_o\}$ where I_g and i_o represent the amplitude of the grid current.

B. Passive Components Design

Since both the input and output currents are continuous, the design of the input and output filters is simple, only considering the ripple of the inductor current, without regard to power and switching frequency [3].

The nominal condition can be designed as $V_{gm} = 141$ V, $v_{c\max} = 380$ V, $v_o = 100$ V, $\lambda_{v_o} = 0.02$, $\Delta i_g = 1.05$ A, $\Delta i_o = 1$ A, $f_s = 50$ kHz, $\omega = 314$ rad/s, and $P = 500$ W, where λ_{v_o} represents the fluctuation coefficient of the output voltage, Δi_g and Δi_o represent the fluctuation values of the grid current and the output current, respectively, and f_s represents the switching frequency. The expression for input inductor L_g can be obtained as follows:

$$L_g = \frac{v_c - v_g}{\Delta i_g}\frac{v_g}{v_c f_s} \geq \frac{v_{c\max} - V_{gm}}{\Delta i_g}\frac{V_{gm}}{v_{c\max} f_s} = 1.7 \text{ mH}. \tag{12}$$

Similarly, the output inductor L_o can be obtained as follows:

$$L_o = \frac{v_c - v_o}{\Delta i_o}\frac{v_o}{v_c f_s} \geq \frac{v_{c\max} - v_o}{\Delta i_o}\frac{v_o}{v_{c\max} f_s} = 1.5 \text{ mH}. \tag{13}$$

According to (12) and (13), L_g and L_o are designed to be 3 and 2 mH, respectively. The capacitor C_1 buffers the unbalanced power between the ac input and the dc output [16]. Based on (11), the expression for C_1 can be derived as follows:

$$C_1 \geq \frac{P\sqrt{4L_g^2P^2/V_{gm}^2 + V_{gm}^2/\omega^2}}{V_{gm}(V_{gm} + v_o)(v_{c\max} - V_{gm} - v_o)} = 47.6\ \mu\text{F}. \tag{14}$$

Assuming that all the current ripple in L_o flows into the output capacitor C_o, the expression for C_o can be derived as follows:

$$C_o \geq \frac{(v_c - v_o)v_o}{8L_o\Delta v_o v_c f_s^2} = \frac{(v_{c\max} - v_o)}{8L_o\lambda_{v_o} v_{c\max} f_s^2} = 921 \text{ nF}. \tag{15}$$

According to (14) and (15), C_1 and C_o are designed to be 57 μF and 20 μF, respectively.

IV. Experimental Result

To validate the effectiveness of the proposed topology, a 500 W experimental prototype was constructed, as shown in Fig. 7. The voltage probe uses Tektronix P5210 A and the current probe uses Cybertek HCP8030. The power quality analyzer HIOKI3197 is used to measure the power factor (PF) and harmonic components of the grid current. The switches

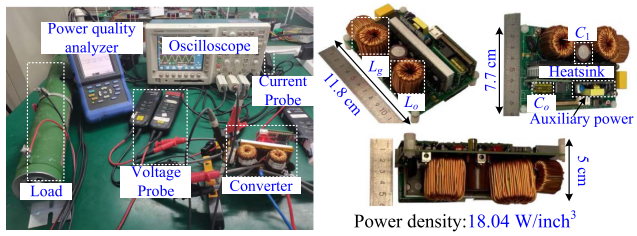

Fig. 7. Experimental prototype.

TABLE I
Parameters of the Proposed AC–DC Converter

Parameters	Values
Rated power, P	500 W
Switching frequency, f_s	50 kHz
Grid voltage (rms), v_g	100 V
Grid frequency, f_g	50 Hz
DC side voltage, v_o	72 V $\sim$ 150 V
Switches, S_1 ,S_2 and S_3	P3M12080K3 ($R_{DSon} = 80$ mΩ)
Diodes, D_1 and D_2	FFSH20120A
Inductors, L_g, L_o	3 mH, 2 mH
Capacitors C_1, C_o	57 μF, 20 μF

adopt P3M12080K3, with an on-resistance of 80 mΩ, and the diodes use SIC FFSH20120 A. The power density is as high as 18.04 W/in^3. The experimental parameters are listed in Table I.

The steady-state waveforms of the system are shown in Fig. 8, with the output voltage ranging from 72 to 150 V, demonstrating the capability of the buck/boost topology. The pulsating power is stored in the intermediate capacitor, with a peak-to-peak fluctuation of 88 V, whereas the fluctuation of the output voltage is less than 4 V, verifying the power decoupling function. The input current total harmonic distortion is less than 5%, and the PF is greater than 0.95, meeting the IEEE Standard 519–1992.

Fig. 9(a) validates the superiority of the common ground structure, with the root mean square (rms) of the leakage current being only 2.15 mA, far below the safety requirements of DIN VDE 0126-1-1 [17]. Fig. 9(b) and (c) shows the voltage waveforms of the three switches when the grid voltage is in the positive half-cycle and negative half-cycle, respectively. During the positive half-cycle, the converter transits from mode 1 to modes 2 and 3, and during the negative half-cycle, modes 4–6 are transited. This is consistent with the operation mode analysis in Fig. 2.

Figs. 10 and 11 present the dynamic waveforms and statistical graphs. The transition time is approximately 0.9 s, and the overshoot of the output voltage is less than 26 V, validating the system's stability. The maximum PF is 0.998, and the maximum efficiency is 96.54%. The harmonic components of the grid current all meet the IEC 6100-3-2 class C.

V. Quantitative Comparison

Tables II and III, and Fig. 12 present a comprehensive comparison between the existing topologies and the proposed ac–dc converter, taking into account the following factors.

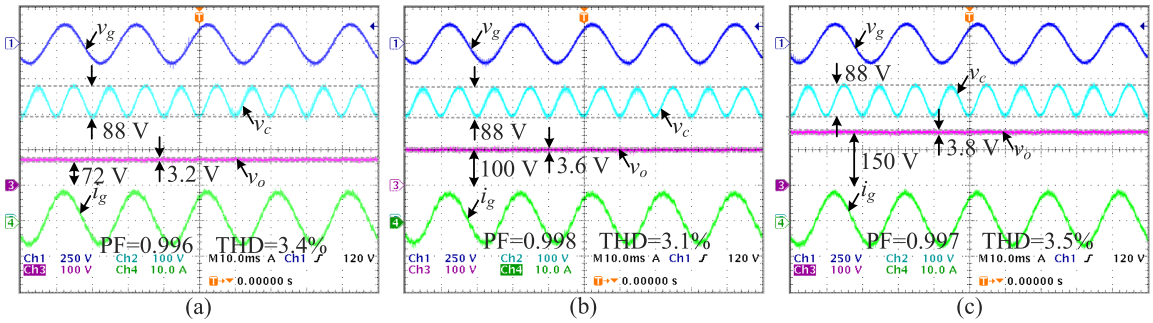

Fig. 8. Steady-state waveforms. (a) $v_o = 72$ V. (b) $v_o = 100$ V. (c) $v_o = 150$ V.

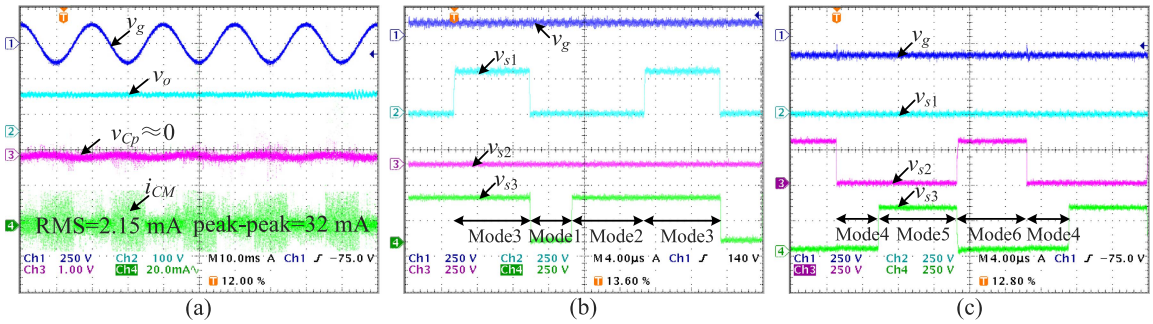

Fig. 9. CM voltage and switch voltage waveformes. (a) CM voltage and leakage current. (b) Switch voltages during the positive cycle. (c) Switch voltages during the negative cycle.

TABLE II
COMPARISON WITH EXISTING TOPOLOGIES BASED ON FUNCTIONS

Attributes	[1]	[9]	[12]	[15]	[16]	Proposed
Bridge	×	×	×	✓	✓	×
Buck/boost	✓/×	✓/✓	✓/✓	✓/✓	✓/✓	✓/✓
Power decoupling	×	×	×	×	✓	✓
Common ground	×	×	✓	×	×	✓
CIC/COC	✓/×	✓/×	✓/×	✓/✓	×/×	✓/✓
Extra input EMI filter	✓	×	×	×	✓	×

CIC/COC: Continuous input/output current.

TABLE III
COMPARISON WITH EXISTING TOPOLOGIES BASED ON QUANTITATIVE INDICATORS

Attributes	[1]	[9]	[12]	[15]	[16]	Proposed
Voltage stress	V_g+v_o	$2v_o$	V_g+v_o	V_g+0.5v_o	V_g+v_o	V_g+v_o
Current stress	I_g	I_g	$I_g + i_o$	I_g	$I_g + i_o$	$I_g + i_o$
Input L (mH)	0.16	1	1.5	3	3.5	3
Input L_{eq} (mH)	11.84	1.13	1.88	3	8.75	2.25
Input C (μF)	-	-	-	0.66	-	-
Output C (μF)	1410	1000	20000	1400	10	20
Number of S/D	8/0	3/4	2/4	1/6	2/5	3/2
Number of L/C	6/3	1/2	3/3	3/5	2/3	2/2
Components	17	10	12	15	12	9
$T_{\text{transition}}$ (s)	-	0.15	0.25	1.2	0.6	0.9
Power (W)	3700	1000	500	1000	100	500
f_s (kHz)	200	25	50	20	25	50
Efficiency	99.14%	98.03%	96.8%	95.3%	93.9%	96.54%

$T_{\text{transition}}$: Transition time; PD: Power density; -: Not provided.

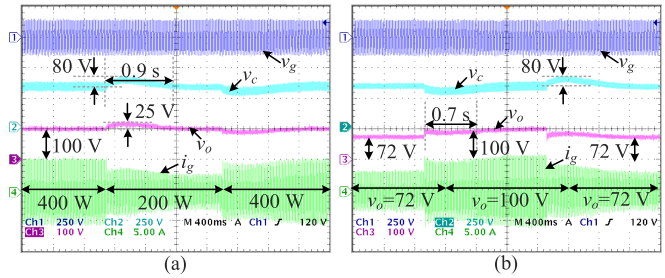

Fig. 10. Dynamic waveforms. (a) Power varies from 400 W to 200 W and then back to 400 W. (b) Output voltage varies from 72 to 100 V and then back to 72 V.

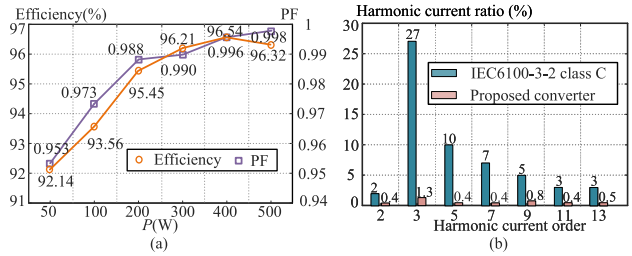

Fig. 11. Statistical graphs. (a) Curves of PF and efficiency. (b) Harmonic current ratio of grid current.

1) *Performance from functions:* Table II provides a functional comparison between the proposed topology and several recent similar literature. The proposed topology can achieve

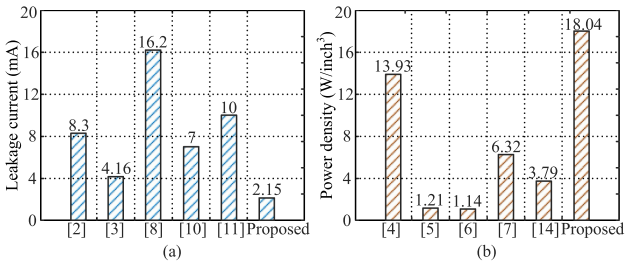

Fig. 12. Comparison of the leakage current and the power density. (a) RMS of the leakage current. (b) Power density.

buck/boost, common ground, power decoupling, continuous input/output current, and does not require a diode bridge, which will cause significant conduction loss and EMI filter. Functionally, the proposed topology is the most comprehensive.

2) *Number of quantitative indicators:* For fairness, the comparison results of quantitative indicators are presented in Table III. More functions often require more components. The proposed topology has the least number of components under the premise of having the most functions, showing significant advantages. The output capacitance in [1], [9], [12], and [15], all exceed 1 mF, necessitating the use of large-capacity electrolytic capacitors, which reduces the system's lifespan. However, the voltage stress and current stress of the proposed topology are higher, requiring higher components specifications. Moreover, the parameters of the filter are relatively large compared with the topologies in [1], [9], and [12], which can be further optimized in the future. For a fairer comparison of filter parameters, an equivalent inductance $L_{\text{eq}} = L * f_s * P *$ coe is defined, which is related to the switching frequency and power. coe is the coefficient used to evaluate EMI filters. When an additional EMI filter is needed, coe is equal to 1, otherwise, it is equal to 0.5. Although the efficiency is the highest in [1] due to soft switching, its output capacitance and equivalent inductance are as high as 1410 μF and 11.84 mH, and the number of components is 17, resulting in high cost.

3) *Comparison in Leakage current and power density:* As shown in Fig. 12, the leakage current of the ac–dc converter with a common-ground structure [2], [3] is usually lower than that of the noncommon-ground structure [8], [11]. Compared with the existing literature, the proposed topology has a lower leakage current and a higher power density.

In summary, the proposed topology can achieve the most functions with the fewest components, demonstrating high competitiveness.

VI. Conclusion

This letter proposes a high power density single-phase ac–dc converter with buck-boost capability, power decoupling, continuous input/output currents, and common ground. The output capacitance is only 20 μF, and the output voltage ripple is less than 4 V, demonstrating good load characteristics. Due to the common ground feature, the rms of the leakage current is only 2.15 mA, which is close to zero. In addition, the continuous input and output currents also alleviate the burden of EMI filter design. The total number of components is only nine, with a power density of up to 18.04 W/in^3.

References

[1] A. Tausif, A. F. Bakan, and S. Dusmez, "A high power density zero-voltage-switching Totem-pole power factor correction converter," *IEEE Trans. Power Electron.*, vol. 39, no. 1, pp. 837–849, Jan. 2024.

[2] H. Tian, Y. Cao, W. Han, and G. Liang, "Power decoupling rectifier with common-ground concept for lighting applications," *IEEE Trans. Power Electron.*, vol. 38, no. 3, pp. 2821–2826, Mar. 2023.

[3] X. Xu, M. Su, Y. Sun, B. Guo, H. Wang, and G. Xu, "Four-switch single-phase common-ground PV inverter with active power decoupling," *IEEE Trans. Ind. Electron.*, vol. 69, no. 3, pp. 3223–3228, Mar. 2022.

[4] Z. Chen, P. Davari, and H. Wang, "Single-phase bridgeless PFC topology derivation and performance benchmarking," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9238–9250, Sep. 2020.

[5] Z. Shan, X. Chen, J. Jatskevich, and C. K. Tse, "AC–DC LED driver with an additional active rectifier and a unidirectional auxiliary circuit for AC power ripple isolation," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 685–699, Jan. 2019.

[6] R. Patil and S. Prakash P, "A bridge-less Cuk-derived voltage doubler based power factor correction rectifier," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 38, no. 10, pp. 12278–12287, Oct. 2024.

[7] Z. Chen, B. Liu, Y. Yang, P. Davari, and H. Wang, "Bridgeless PFC topology simplification and design for performance benchmarking," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 5398–5414, May 2021.

[8] A. Anurag, N. Deshmukh, A. Maguluri, and S. Anand, "Integrated DC–DC converter based grid-connected transformerless photovoltaic inverter with extended input voltage range," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8322–8330, Oct. 2018.

[9] R. Patil and S. P P, "Performance enhancement of switched-capacitor-based bridgeless buck PFC rectifier," *IEEE Trans. Power Electron.*, vol. 39, no. 3, pp. 2938–2942, Mar. 2024.

[10] J.-S. Kim, J.-M. Kwon, and B.-H. Kwon, "High-efficiency two-stage three-level grid-connected photovoltaic inverter," *IEEE Trans. Ind. Electron.*, vol. 65, no. 3, pp. 2368–2377, Mar. 2018.

[11] S. Dhara and V. T. Somasekhar, "A nine-level transformerless boost inverter with leakage current reduction and fractional direct power transfer capability for PV applications," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 6, pp. 7938–7949, Dec. 2022.

[12] M. Pourmahdi, H. Heydari-doostabad, R. Ghazi, and T. O'Donnell, "Buck–boost common ground bridgeless PFC (CGBPFC) rectifies with positive/negative output," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1272–1282, Feb. 2022.

[13] M. Maghsoudi and H. Farzanehfard, "Fully soft-switched buck–boost bridgeless PFC converters with single-magnetic core," *IEEE Trans. Ind. Electron.*, vol. 71, no. 1, pp. 419–426, Jan. 2024.

[14] Z. Chen, J. Xu, X. Liu, P. Davari, and H. Wang, "High power factor bridgeless integrated buck-type PFC converter with wide output voltage range," *IEEE Trans. Power Electron.*, vol. 37, no. 10, pp. 12577–12590, Oct. 2022.

[15] J. Gupta and B. Singh, "A modified Luo PFC AC–DC converter with continuous input-output current feature for universal supply voltage range LVEV chargers," *IEEE Trans. Transport. Electrific.*, vol. 10, no. 2, pp. 4129–4141, Jun. 2024.

[16] S. Li, W. Qi, S.-C. Tan, and S. Y. R. Hui, "A single-stage two-switch PFC rectifier with wide output voltage range and automatic AC ripple power decoupling," *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 6971–6982, Oct. 2017.

[17] M. N. H. Khan, M. Forouzesh, Y. P. Siwakoti, L. Li, T. Kerekes, and F. Blaabjerg, "Transformerless inverter topologies for single-phase photovoltaic systems: A comparative review," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 805–835, Mar. 2020.

[18] R. W. Erickson and D. Maksimovi, *Fundamentals of Power Electronics. Fundamentals of Power Electronics*. Berlin, Germany: Springer, 2020.