A Series-Arm Modular Multilevel DC/DC Converter With Variable Duty Cycle Quasi-Square-Wave Modulation for ZVS Operation

Haozhe Jin, Wu Chen, *Senior Member, IEEE*, and Yueyin Wang

***Abstract*—A series-arm modular multilevel dc/dc converter is proposed in this article, which is suitable for dc transformer applications in medium-voltage (MV) dc systems. The proposed converter utilizes the series-arm configuration on the MV side, eliminating the MV terminal concentrated capacitors and reducing the number of submodules. Transmission power regulation can be achieved by adopting the variable duty cycle quasi-square-wave modulation and phase-shifted control with higher ac link frequency. A comprehensive analysis is conducted on the operational principle, and the soft switching characteristic of the converter is analyzed. Based on this, the parameter design procedure and output voltage control strategy are presented, which can effectively combat the degradation of soft switching characteristics caused by the inherent dc circulating current in modular multilevel structures. Hence, both MV-side SM and low-voltage-side full-bridge switches can realize zero voltage switching throughout the whole operating range. Finally, the theoretical analysis and control strategies of the proposed SAMMDC are verified by a 4kW SAMMDC prototype.**

***Index Terms*—DC/DC converter, dual-active-bridge (DAB), modular multilevel converter (MMC), soft switching.**

I. Introduction

THE medium-voltage (MV) dc system, featuring high power, high efficiency, and high flexibility, has received increasing attention in various applications, including renewable energy integration, data centers, and shipboard power systems [1], [2], [3], [4]. The dc transformer (DCT) is an essential equipment in MVDC systems, which is required to perform the crucial function of voltage conversion and galvanic isolation while also offering certain necessary protections and supplementary services [5], [6].

The DCT topologies that achieve high-voltage and high-power conversion in MVDC systems can be divided into three feasible solutions, including the input-series-output-parallel (ISOP) structure, the series-connected-device dc/dc converter, and the modular multilevel dc/dc converter (MMDC). For ISOP structure, numerous power modules are connected in series on MV side to reduce the voltage stress of devices with high modularization and redundancy [7], [8], [9]. Nevertheless, each power module can only transmit a portion of the overall power. Consequently, it must be designed considering insulation coordination for the MV terminal voltage, limiting the power density of DCT.

The other two solutions possess the capability of conducting bulk power processing. The series-connected-device dc/dc converters enable the attainment of high blocking voltage through a more straightforward configuration [10], [11]. However, dynamic voltage balancing and synchronous driver problems remain significant challenges for practical application.

The MMDC is a prospective candidate that combines the benefits of the modular multilevel converter (MMC) with traditional dc/dc converters [12], [13], [14]. With the modular multilevel structure on the MV side, the MMDC can scale up the voltage by increasing the number of submodules (SMs) while improving current capacity through the parallel arms, enabling high redundancy and flexible modulation patterns [15], [16]. The utilization of centralized high-power medium-frequency transformers (MFTs) simplifies the transformer insulation design. Furthermore, the MMDC can function as a dual-active-bridge (DAB) converter by employing quasi-square-wave (QSW) modulation and phase-shifted control, achieving bidirectional power transmission with an increased ac link frequency [17], [18]. In [18] and [19], the full-bridge and three-phase MMDCs with signal-phase-shifted (SPS) control are investigated to satisfy the different transmission power capacity requirements. The soft switching for MV-side switches can be realized under certain conditions. Besides, the half-bridge MMDC is proposed to reduce the number of SMs, thus decreasing the volume and capital cost [20], [21]. However, the half-bridge MMDC requires concentrated capacitors on MV terminal to carry the ac link current. Therefore, a sharing-branch modular multilevel DCT is introduced in [22] to eliminate the need for MV terminal concentrated capacitors while simultaneously reducing the number of SMs.

Benefiting from the modular multilevel structure, various modulation schemes and control strategies can be

Manuscript received 24 October 2023; revised 27 December 2023; accepted 18 January 2024. Date of publication 23 January 2024; date of current version 4 September 2024. This work was supported in part by the Science and Technology Project of State Grid—Research on Key Technologies of High-Quality Power Supply and in part by the Consumption Based on High-Performance Power Devices under Award 5108-202218280A-2-229-XG. Recommended for publication by Associate Editor J. Biela. *(Corresponding author: Wu Chen.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3357535.

Digital Object Identifier 10.1109/TPEL.2024.3357535

employed for MMDCs to improve performance over a wide transmission power and terminal voltage range. The dual-phase-shifted control, trapezoidal current control, and internal-phase-shifted control are investigated to broaden the soft switching operation range while also minimizing the current stress and power loss [18], [23], [24], [25], [26], [27], [28]. In addition, the constant inserted and bypassed SM number control is suggested in [22] and [29] to expand the voltage regulation range and improve overall efficiency. However, similar to MMC, the aforementioned MMDCs exhibit an inherent dc circulating current, leading to asymmetric soft switching characteristics of the upper and lower MV-side SM switches. As a result, soft switching is easily lost under light-load conditions, resulting in decreased efficiency.

In order to address the issues above, this article proposes a series-arm modular MMDC (SAMMDC) with variable duty cycle QSW modulation and SPS control. The adoption of the series-arm structure reduces the number of SMs. And the number of transformers and LV-side full bridges is further reduced compared to the topologies in [28]. To mitigate the impact of dc circulating current on soft switching of SM switches, the operation principle of SAMMDC employing variable duty cycle QSW modulation and SPS control is established and thoroughly analyzed. Thus, over the whole operating range, the zero voltage switching (ZVS) of MV-side SM switches and LV-side full-bridge switches can be realized.

The rest of this article is organized as follows. In Section II, the circuit configuration, operation principle, and the soft switching characteristic of SAMMDC are introduced. Section III provides the parameter design process and control strategy. In Section IV, experimental results are carried out. Finally, Section V concludes this article.

II. Topology and Operation Principle

A. Circuit Configuration

Fig. 1 illustrates the proposed SAMMDC, which consists of a filter inductor L_f, two modular multilevel arms, two dc blocking capacitors C_{di} ($i = 1, 2$), two transmission inductors L_{di}, a medium-frequency three-winding transformer T_r and a full bridge Q_1~Q_4 on LV side. Each modular multilevel arm comprises N half-bridge SMs. The filter inductor L_f and the two modular multilevel arms are connected in series on MV side. The upper and lower arms are connected to the MV-side windings of the three-winding transformer T_r through the dc blocking capacitor C_{di} and transmission inductor L_{di}. It should be noted that the two MV-side windings possess opposite dotted terminal positions. The V_M and V_L are the voltage across MV and LV terminals. The turns ratio of T_r is n:n:1.

B. Modulation

The SAMMDC utilizes a variable duty cycle QSW modulation scheme and SPS control, as depicted in Fig. 2. For MV-side half-bridge SMs, the driving signals of upper switches are denoted as g_{ij} ($i = 1, 2, j = 1, 2, \ldots, N$), and the driving signals of lower switches in each SMs are complementary to the corresponding upper switches with sufficient dead time. The duty cycle of the upper switch driving signals g_{ij} is D. Besides, an internal phase-shifted angle θ is introduced between two adjacent driving signals. In addition, the driving signals of the upper and lower arms are phase-shifted 180°. For LV-side full bridges, the duty cycle of switches is fixed at 50%, and the upper and lower switches are complementary with enough dead time.

Moreover, a phase-shifted duty cycle D_d is applied between the MV- and LV-side driving singles. In addition, the switching frequency of MV- and LV-side switches is f_s.

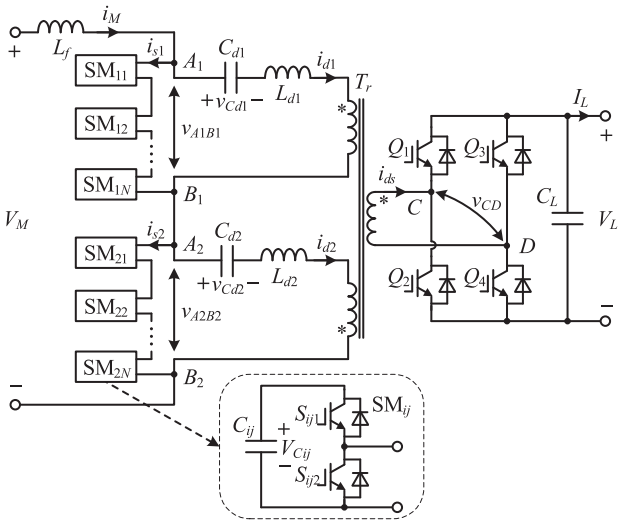

Fig. 1. Topology of SAMMDC.

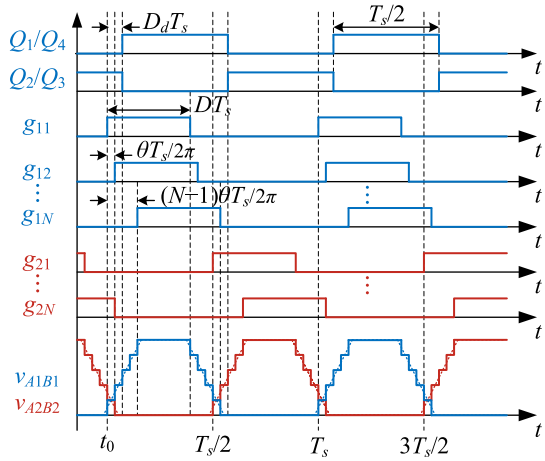

Fig. 2. Modulation scheme.

C. Operation Principle

With the above modulation strategy in Fig. 2, the arm voltages v_{A1B1} and v_{A2B2} are staircase waveforms with N+1 steps with the identical duty cycle D. The duty cycle of the arm voltage rising and falling process is denoted as d_N, $d_N = N\theta/2\pi$. In addition, v_{A1B1} and v_{A2B2} are phase-shifted 180°. The LV-side full-bridge output voltage is a two-level square-wave voltage with a duty cycle of 50%. The phase-shifted duty cycle D_d can be used to regulate the output voltage and transmission power of

SAMMDC, which is similar to the conventional DAB converter. The ranges of D_d, D, and d_N are set as [0, 1], [d_N, 1−d_N], and (0, 0.5), respectively. It should be noted that the lower limit of d_N needs to be greater than 0 for practical applications to reduce dv/dt.

In order to simplify the subsequent derivation, several assumptions are made as follows.

1) All of the components are ideal.
2) The terminal voltages V_M and V_L remain stable.
3) The inductances of L_{d1} and L_{d2} are identical and equal to L_d.
4) The voltage balancing method is adopted, and the SM capacitor voltages V_{Cij} are well balanced at V_C. Hence, the peak value of v_{A1B1} and v_{A2B2} is NV_C.

According to the voltage-second balance of L_f over one switching period T_s, (1) can be obtained, $T_s = 1/f_s$

$$V_M T_s - 2DNV_C T_s = 0. \tag{1}$$

According to (1), the SM capacitor voltage V_C can be determined as

$$V_C = \frac{V_M}{2DN}. \tag{2}$$

Therefore, with Fig. 1, the voltage across blocking capacitors C_{d1} and C_{d2}, which are denoted as V_{Cd1} and V_{Cd2}, respectively, can be calculated as

$$V_{Cd1} = V_{Cd2} = NDV_C = \frac{V_M}{2}. \tag{3}$$

The upper and lower arm current i_{s1} and i_{s2} consist of transmission inductor current i_{d1} and i_{d2}, respectively, and MV terminal current i_M, which can be written as

$$\begin{cases} i_{s1} = i_M - i_{d1} \\ i_{s2} = i_M - i_{d2} \end{cases}. \tag{4}$$

According to Fig. 1, the power conversion of the upper and lower arms in SAMMDC can be equivalent to the power exchange between voltage sources v_{A1B1}, v_{A2B2}, and v_{CD} through the transmission inductor L_{d1}, L_{d2}, and the MFT T_r. And the ac link equivalent circuit of the SAMMDC can be obtained as shown in Fig. 3(a). Therefore, the state equation of the circuit is obtained as

$$\begin{cases} L_{d1}\frac{\mathrm{d}i_{d1}}{\mathrm{d}t} = v_{A1B1} - V_{Cd1} - nv_{CD} \\ L_{d2}\frac{\mathrm{d}i_{d2}}{\mathrm{d}t} = v_{A2B2} - V_{Cd2} + nv_{CD} \end{cases}. \tag{5}$$

Besides, the LV-side full-bridge current i_{ds} can be expressed as

$$i_{ds} = n\left(i_{d1} - i_{d2}\right). \tag{6}$$

Then, (7) can be obtained by combining (3), (5), and (6)

$$L_d \frac{\mathrm{d}}{\mathrm{d}t}\left(\frac{i_{ds}}{n}\right) = v_{A1B1} - v_{A2B2} - 2nv_{CD}. \tag{7}$$

By adopting the variable duty cycle QSW modulation scheme along with the 180° phase-shifted between v_{A1B1} and v_{A2B2}, v_{A1B1}−v_{A2B2} is a bipolar QSW voltage with the amplitude of V_M/(2D). 2nv_{CD} is a two-level square-wave voltage with the amplitude of 2nV_L. Therefore, the ac link equivalent circuit can be further simplified, as shown in Fig. 3(b). According to Fig. 3(b), SAMMDC can be equivalent to two ac voltage sources v_{A1B1}−v_{A2B2} and 2nv_{CD} connected on both sides of an inductor L_d. The direction and amplitude of the transmission power can be controlled by regulating the phased-shifted angle between the two voltage sources.

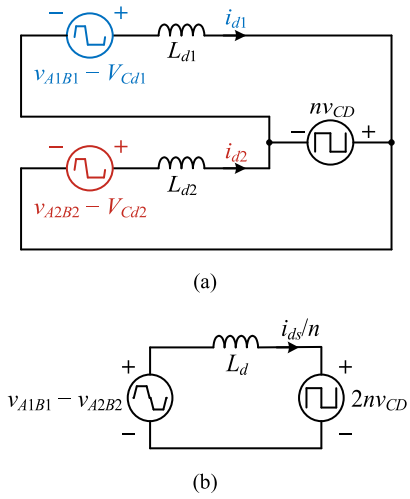

Fig. 3. AC link equivalent circuits of SAMMDC. (a) Equivalent circuit referred to MV side. (b) Simplest equivalent circuit.

Furthermore, similar to the traditional DAB converter, it is possible to decrease the current stress and extend the soft switching region of the LV-side full bridge when v_{A1B1}−v_{A2B2} and 2nv_{CD} are matched, namely V_M/(2D) = 2nV_L, which can be achieved by adjusting D under different terminal voltages.

The operation modes of SAMMDC can be characterized by the different sets of d_N, D, and D_d. The values of d_N and D will influence the shape and relative position of arm voltages v_{A1B1} and v_{A2B2}. The waveforms of v_{A1B1} and v_{A2B2} with different combinations of d_N and D are shown in Fig. 4. Staircase voltage during the rising and falling processes are simplified as diagonal lines to facilitate analysis and calculation in practical applications where a large number of SMs involved [20].

Fig. 4(a) shows the waveform of v_{A1B1} and v_{A2B2} when d_N≤D≤0.5−d_N. The duration of the arm voltage greater than zero is shorter than T_s/2. And v_{A1B1} and v_{A2B2} have a nonoverlapping under this condition. Fig. 4(b) shows the waveform of v_{A1B1} and v_{A2B2} under the circumstance where 0.5−d_N<D≤0.5+d_N. There are overlapping durations in the arm voltage rising and falling processes. Fig. 4(c) shows the waveform of v_{A1B1} and v_{A2B2} when 0.5+d_N<D≤1−d_N. The overlapping duration involves the entire arm voltage rising and falling process. Therefore, three operating regions are classified based on the different combinations of d_N and D for the upper and lower arms.

Taking d_N≤D≤0.5−d_N as an example, there are 8 cases when D_d varies from 0 to 1 based on the relative position of v_{A1B1} and v_{CD} as shown in Fig. 5. The operation modes when 0.5−d_N<D≤0.5+d_N and 0.5+d_N<D≤1−d_N can also be

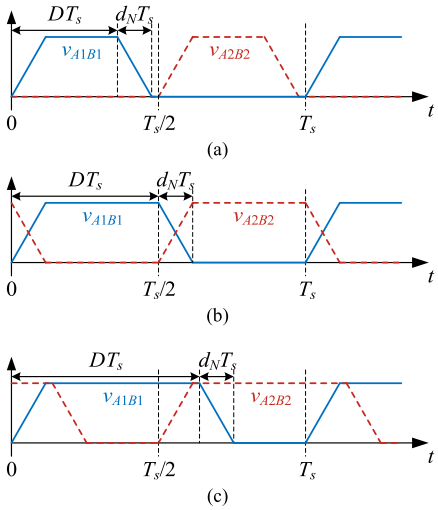

Fig. 4. Waveforms of v_{A1B1} and v_{A2B2} with different combinations of d_N and D. (a) $d_N \le D \le 0.5-d_N$. (b) $0.5-d_N < D \le 0.5+d_N$. (c) $0.5+d_N < D \le 1-d_N$.

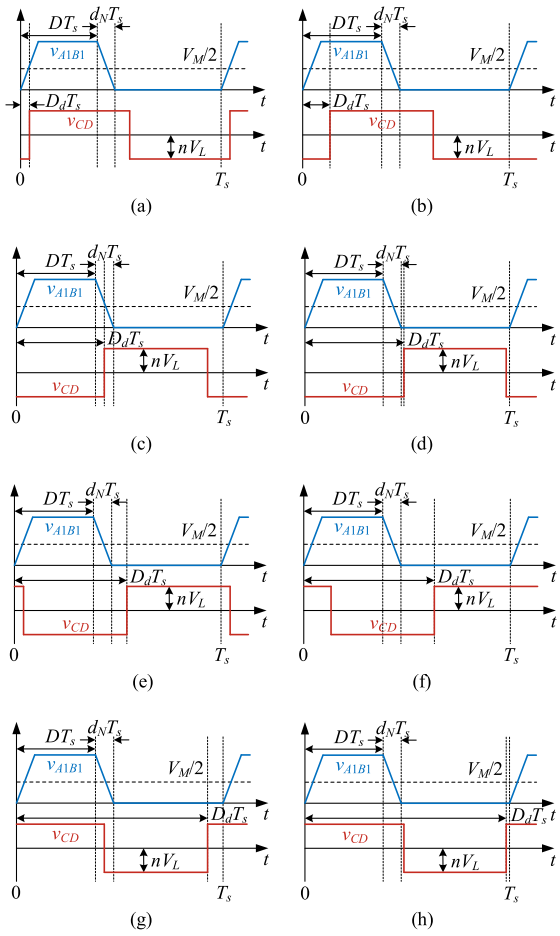

Fig. 5. Waveforms of v_{A1B1} and v_{CD} with different D_d when $d_N \le D \le 0.5-d_N$. (a) $0 \le D_d \le d_N$. (b) $d_N < D_d \le D$. (c) $D < D_d \le D+d_N$. (d) $D+d_N < D_d \le 0.5$. (e) $0.5 < D_d \le 0.5+d_N$. (f) $0.5+d_N < D_d \le 0.5+D$. (g) $0.5+D < D_d \le 0.5+D+d_N$. (h) $0.5+D+d_N < D_d \le 1$.

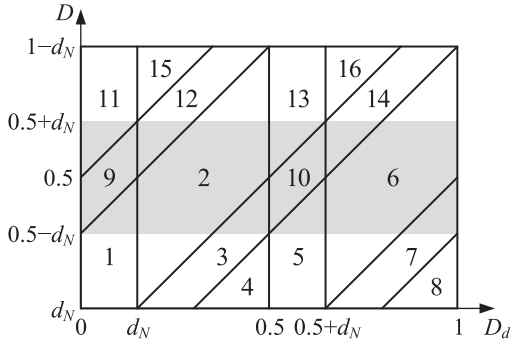

Fig. 6. Division of the operation modes.

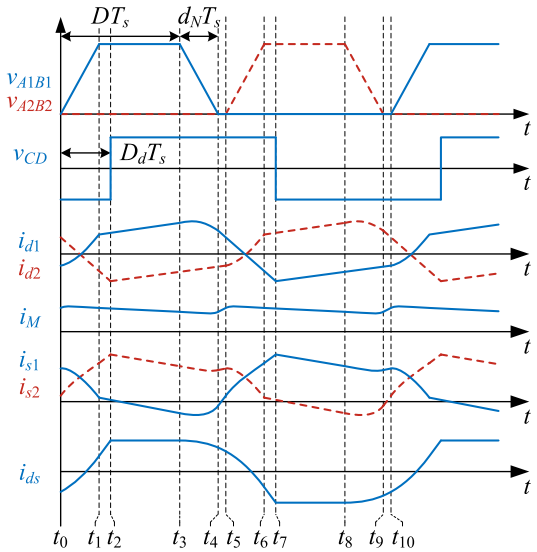

Fig. 7. Typical operating waveforms of SAMMDC in mode 2.

divided based on the set of D_d. In conclusion, SAMMDC has a total of 16 operation modes with various combinations of d_N, D, and D_d. The division is illustrated in Fig. 6. With different operation modes, SAMMDC possesses different transmission power, current stress, and soft switching characteristics.

The typical operating waveforms of SAMMDC in mode 2 are shown in Fig. 7, where $d_N \le D \le 1-d_N$, $d_N \le D_d < 0.5$, and $D+d_N-0.5 \le D_d < D$. The upper arm ($i = 1$) is used as an example in the following description. According to Fig. 7, v_{A1B1} and v_{CD} can be expressed as

$$v_{A1B1}(t) = \begin{cases} \frac{V_M}{2Dd_NT_s}(t-t_0), & t_0 \le t < t_1 \\ \frac{V_M}{2D}, & t_1 \le t < t_3 \\ \frac{V_M}{2D} - \frac{V_M}{2Dd_NT_s}(t-t_3), & t_3 \le t < t_4 \\ 0, & t_4 \le t < t_{10} \end{cases} \tag{8}$$

$$v_{CD}(t) = \begin{cases} -nV_L, & t_0 \le t < t_2 \\ nV_L, & t_2 \le t < t_7 \\ -nV_L, & t_7 \le t < t_{10} \end{cases}. \tag{9}$$

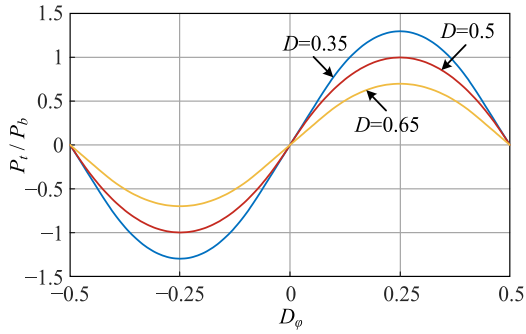

Fig. 8. Transmission power characteristic of SAMMDC.

Then, according to (5), (8), and (9), the transmission inductor current i_{d1} can be solved as

$$i_{d1}(t) = \begin{cases} i_{d1}(t_0) + \frac{1}{L_d}\left(\begin{array}{l}\frac{V_M}{4Dd_NT_s}(t-t_0)^2 \\ -\left(\frac{V_M}{2}-nV_L\right)(t-t_0)\end{array}\right), & t_0 \le t < t_1 \\ i_{d1}(t_1) + \frac{1}{L_d}\left(\frac{V_M}{2D}-\frac{V_M}{2}+nV_L\right)(t-t_1), & t_1 \le t < t_2 \\ i_{d1}(t_2) + \frac{1}{L_d}\left(\frac{V_M}{2D}-\frac{V_M}{2}-nV_L\right)(t-t_2), & t_2 \le t < t_3 \\ i_{d1}(t_3) + \frac{1}{L_d}\left(\begin{array}{l}-\frac{V_M}{4Dd_NT_s}(t-t_3)^2 \\ +\left(\frac{V_M}{2D}-\frac{V_M}{2}-nV_L\right)(t-t_3)\end{array}\right), & t_3 \le t < t_4 \\ i_{d1}(t_4) + \frac{1}{L_d}\left(-\frac{V_M}{2}-nV_L\right)(t-t_4), & t_4 \le t < t_7 \\ i_{d1}(t_7) + \frac{1}{L_d}\left(-\frac{V_M}{2}+nV_L\right)(t-t_7), & t_7 \le t < t_{10} \end{cases} \quad (10)$$

Based on the symmetry operating that $i_{d1}(t_0) = i_{d1}(t_{10})$, the initial value of the transmission inductor current $i_{d1}(t_0)$ in steady-state can be derivate as

$$i_{d1}(t_0) = \frac{V_M(d_N - 1 + D) + nV_L(1 - 4D_d)}{4L_d f_s}. \quad (11)$$

Therefore, according to (9)–(11), the transmission power of SAMMDC P_t that consists of the power conversion of two arms in mode 2 can be expressed as

$$\begin{aligned} P_t &= \frac{2}{T_s}\int_{t_0}^{t_{10}} nv_{CD}(t) i_{d1}(t)\mathrm{d}t \\ &= \frac{nV_LV_M}{12DL_df_s}\begin{pmatrix}12D_d(D+d_N-D_d) \\ -4d_N^2-6Dd_N+3D-6D^2\end{pmatrix}. \end{aligned} \quad (12)$$

The transmission power expression of SAMMDC in other modes can then be derived by applying a similar mathematical process. The results are presented in Table I. According to Table I, it can be proved that P_t reaches the maximum value $P_{\max}$ as (13) when $D_d = (D+d_N)/2$

$$P_{\max} = \frac{nV_LV_M}{12DL_df_s}\left(3D - 3D^2 - d_N^2\right). \quad (13)$$

The transmission power characteristic of SAMMDC with different D is shown in Fig. 8, where D_φ is the fundamental phase-shifted duty cycle, $D_\varphi = D_d - (D+d_N)/2 + 1/4$ and P_b is the reference power, $P_b = nV_LV_M/8L_df_s$. As shown in Fig. 8, P_t increases monotonically in the range $-0.25 \le D_\varphi \le 0.25$, similar to the conventional DAB converter. Therefore, the bidirectional transmission power regulation can be realized effectively by changing D_φ. Moreover, for the same D_φ, P_t decreases with the increase of D.

TABLE I
EXPRESSION OF THE TRANSMISSION POWER IN DIFFERENT MODES

Mode	Transmission power
1	$\frac{nV_LV_M}{12d_NDL_df_s}\left(3d_ND(1-2d_N-2D+4D_d)-4D_d^3\right)$
2	$\frac{nV_LV_M}{12DL_df_s}\left(12D_d(D+d_N-D_d)-4d_N^2-6Dd_N+3D-6D^2\right)$
3	$\frac{nV_LV_M}{12d_NDL_df_s}\begin{pmatrix}-D(4D^2+6Dd_N+6d_N^2-3d_N) \\ -12DD_d(D_d-d_N-D)-4(d_N-D_d)^3\end{pmatrix}$
4	$\frac{nV_LV_M}{4L_df_s}(2D+2d_N+1-4D_d)$
5	$\frac{nV_LV_M}{24d_NDL_df_s}\left(6d_ND(1+2d_N+2D-4D_d)+(2D_d-1)^3\right)$
6	$\frac{nV_LV_M}{12DL_df_s}\begin{pmatrix}-3(2D_d-1)(2D+2d_N-2D_d+1) \\ +4d_N^2+6Dd_N-3D+6D^2\end{pmatrix}$
7	$\frac{nV_LV_M}{24d_NDL_df_s}\begin{pmatrix}2D(4D^2+6Dd_N+6d_N^2-3d_N) \\ +6D(2D_d-1)(2D_d-1-2d_N-2D) \\ +(2d_N-2D_d+1)^3\end{pmatrix}$
8	$-\frac{nV_LV_M}{4L_df_s}(2D+2d_N+3-4D_d)$
9	$\frac{nV_LV_M}{24d_NDL_df_s}\begin{pmatrix}8D^3+12D^2d_N+12Dd_N^2-6Dd_N \\ +6D(2D_d+1)(2D_d+1-2D-2d_N) \\ +(2d_N-2D_d-1)^3-8D_d^3\end{pmatrix}$
10	$-\frac{nV_LV_M}{24d_NDL_df_s}\begin{pmatrix}2D(4D^2+6Dd_N-3d_N+6d_N^2) \\ +24DD_d(D_d-D-d_N) \\ +8(d_N-D_d)^3+(1-2D_d)^3\end{pmatrix}$
11	$\frac{nV_LV_M}{12d_NDL_df_s}\begin{pmatrix}3d_N(D-1)(2D+2d_N-4D_d-1) \\ +4(d_N-D_d)^3\end{pmatrix}$
12	$-\frac{nV_LV_M}{24d_NDL_df_s}\begin{pmatrix}6d_N(D-1)(4D_d+1-2D-2d_N) \\ +(2D_d+1-2D)^3\end{pmatrix}$
13	$-\frac{nV_LV_M}{24d_NDL_df_s}\begin{pmatrix}6d_N(D-1)(2D+2d_N-4D_d+1) \\ +(2d_N-2D_d+1)^3\end{pmatrix}$
14	$\frac{nV_LV_M}{12d_NDL_df_s}\begin{pmatrix}3d_N(D-1)(4D_d-1-2d_N-2D) \\ +4(D_d-D)^3\end{pmatrix}$
15	$\frac{nV_LV_M}{4DL_df_s}(D-1)(2D-4D_d+2d_N-1)$
16	$-\frac{nV_LV_M}{4DL_df_s}(D-1)(2D-4D_d+2d_N+1)$

D. Soft Switching

For SAMMDC, all of the power switches on MV and LV sides can achieve ZVS-ON by employing appropriate parameters design and control strategy over a wide variation range of transmission power and terminal voltages, significantly reducing switching loss. Mode 2 is still used to demonstrate the ZVS condition for SAMMDC.

1) Soft Switching for LV-Side Full Bridges: From Fig. 7, the ZVS condition of LV-side full-bridge switches can be expressed as (14), where I_{Qon} is the turn-ON current of LV-side full-bridge

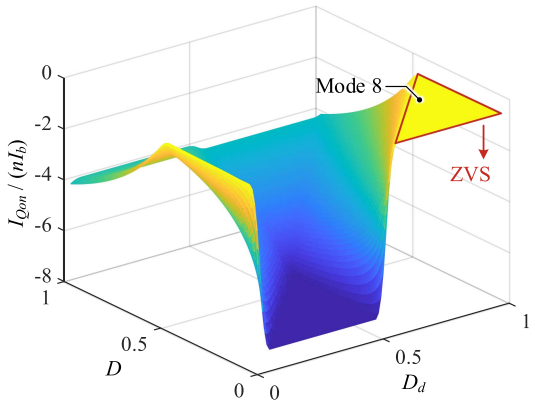

Fig. 9. Normalized turn-ON current of LV-side full-bridge switches $I_{Q\text{on}}/(nI_b)$ versus D_d and D when d_N=0.04.

switches

$$I_{Qon} = -i_{ds}\left(t_0 + D_d T_s\right) < 0. \tag{14}$$

According to (6), the LV-side full-bridge current i_{ds} can be expressed as (15), where i_{d2} is phase-shifted by 180° with respect to i_{d1}

$$i_{ds}(t) = n\left(i_{d1}(t) - i_{d2}(t)\right) = n\left(i_{d1}(t) - i_{d1}\left(t + \frac{T_s}{2}\right)\right). \tag{15}$$

The expression for I_{Qon} in mode 2 can be derivated as (16) from (10), (11), and (15)

$$I_{Q\text{on}} = -\frac{n\left(V_M\left(2D_d - d_N - D\right) + 2nV_L D\right)}{4L_d f_s D}. \tag{16}$$

The turn-ON current of LV-side full-bridge switches in other modes can be calculated similarly, and the normalized turn-ON current of LV-side full-bridge switches $I_{Q\text{on}}/(nI_b)$ is illustrated in Fig. 9, where I_b is the reference current, $I_b = nV_L/8L_d f_s$. From Fig. 9, $I_{Q\text{on}}$ reaches its maximum value in mode 8, which is independent of D and D_d. Therefore, the ZVS condition of LV-side full-bridge switches can be expressed as (17) from mode 8

$$I_{Q\text{on}} = -\frac{n\left(-V_M + 2nV_L\right)}{4L_d f_s} < 0. \tag{17}$$

According to (17), LV-side full-bridge switches can achieve ZVS-ON over the whole operating range when V_M<$2nV_L$. In addition, the ZVS boundaries of LV-side full-bridge switches is presented in Fig. 10 when $d_N = 0.04$, where M is the voltage gain, $M = 2nV_L/V_M$. According to Fig. 10, the ZVS region of LV-side full-bridge switches can be extended with a large M. When M≤1, D has a lower limit to ensure the ZVS-ON for any D_d, and the lower limit of D decreases with the increase of M. Besides, ZVS-ON can always be realized across the entire operating range when M>1. Therefore, the ZVS condition of LV-side full-bridge can also be obtained, which is the same as (17). In particular, D can be adjusted as (18), which can achieve the ZVS operation of LV-side full-bridge switches while ensuring the voltage matching of the equivalent DAB converter shown in

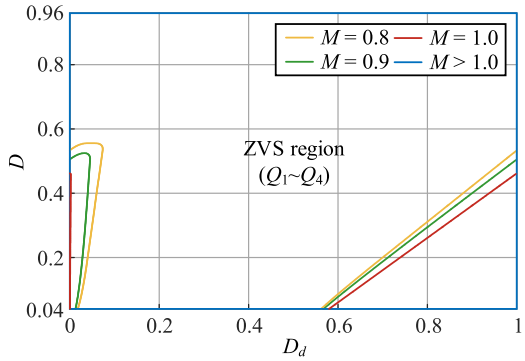

Fig. 10. ZVS boundaries of LV-side full-bridge switches.

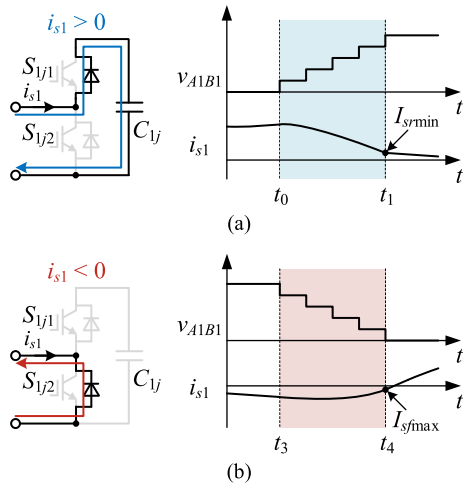

Fig. 11. Soft switching characteristic of SM switches. (a) Arm voltage rising process. (b) Arm voltage falling process.

Fig. 3(b)

$$D = \frac{V_M}{4nV_L} = \frac{1}{2M}. \tag{18}$$

With (18), D can be calculated as 0.625, 0.556, and 0.5, respectively, when M is set to 0.8, 0.9, and 1. Under these circumstances, ZVS-ON of LV-side full-bridge switches can be realized for arbitrary values of D_d according to Fig. 10.

2) Soft Switching for MV-Side Half-Bridge SMs: As shown in Fig. 11, the switching characteristics of the upper and lower switches behave differently, depending on the arm current and the transition process of the arm voltage. As depicted in Fig. 11(a), during the arm voltage v_{A1B1} rising process, the upper switch S_{1j1} achieves ZVS-ON with positive i_{s1}. Therefore, keeping the minimum value of i_{s1} within $[t_0, t_1]$, denoted as $I_{sr\min}$, greater than zero can ensure all upper switches realize ZVS-ON. During the falling process of v_{A1B1} shown in Fig. 11(b), ZVS-ON of the lower switch S_{1j2} is achieved when i_{s1}<0. As long as $I_{sf\max}$, the maximum value of i_{s1} within $[t_3, t_4]$, is guaranteed to be less than zero, all lower switches are capable of ZVS-ON. Therefore, the ZVS conditions of MV-side

upper and lower switches can be expressed as

$$\begin{cases} I_{sr\min} > 0 \\ I_{sf\max} < 0 \end{cases}. \tag{19}$$

When SAMMDC operates in different modes, the values of $I_{sr\min}$ and $I_{sf\max}$ are different. Therefore, the arm currents must be modeled separately for each mode to solve $I_{sr\min}$ and $I_{sf\max}$, obtaining the soft switching characteristic over the whole operating range. Similarly, mode 2 is utilized to illustrate the ZVS conditions of MV-side SM switches.

According to (4), i_{s1} comprises the transmission inductor current i_{d1} and MV terminal current i_M. In practice, the ripple of i_M is usually smaller than the average value of i_M. Therefore, the ripple of i_M is neglected in the following to simplify the analysis. Then, according to Fig. 7 and (4), $I_{sr\min}$ and $I_{sf\max}$ can be solved depending on the relationship between v_{A1B1} and v_{CD} as (20) and (21) in mode 2, where I_M is the average value of i_M, $I_M = P_t/V_M$

$$\begin{aligned} I_{sr\min} &= \min\left(i_{s1}\left(t_0\right), i_{s1}\left(t_0 + d_N T_s\right)\right) \\ &= I_M - \max\left(i_{d1}\left(t_0\right), i_{d1}\left(t_0 + d_N T_s\right)\right) \end{aligned} \tag{20}$$

$$\begin{aligned} I_{sf\max} &= \max\left(i_{s1}\left(t_0 + DT_s\right), i_{s1}\left(t_0 + (D + d_N) T_s\right)\right) \\ &= I_M - \min\left(i_{d1}\left(t_0 + DT_s\right), i_{d1}\left(t_0 + (D + d_N) T_s\right)\right). \end{aligned} \tag{21}$$

In other modes, the values of $I_{sr\min}$ and $I_{sf\max}$ can be solved in a similar manner. The results are shown in Fig. 12, which are normalized by I_b. According to Fig. 12(a), $I_{sr\min}$ increases and subsequently decreases with D and D_d, reaching a peak value near $D = D_d = 0.5$. When $I_{sr\min}>0$, the SM upper switches achieve ZVS-ON with a small D and heavy-load condition. Besides, as demonstrated in Fig. 12(b), the SM lower switches achieve ZVS-ON with negative $I_{sr\min}$ when D is small. Moreover, the ZVS boundaries of MV-side SM switches with different M are shown in Fig. 13. The ZVS region of MV-side SM switches narrows with the increase of M. For both upper and lower switches, a small D guarantees that ZVS is realized for any D_d, such as $D = 0.4$ when $M = 1.2$. However, ZVS-ON is more likely to be lost when D_d is close to 0 and 1. The ZVS conditions of the SM upper and lower switches can be found in mode 8 as

$$I_{sr\min} = \frac{\left(V_M\left(1 - d_N - D\right) - 2nV_L\left(D + d_N\right)\right)}{4L_d f_s} > 0 \tag{22}$$

$$I_{sf\max} = -\frac{\left(V_M\left(1 - d_N - D\right) - 2nV_L\left(D + d_N\right)\right)}{4L_d f_s} < 0. \tag{23}$$

From (22) and (23), it can be seen that $I_{sr\min} = -I_{sf\max}$. The ZVS conditions for upper and lower switches are determined by terminal voltages V_M and V_L, D, and d_N, but are independent of D_d. Besides, a smaller d_N can contribute to the realization of ZVS-ON. However, the limitations imposed by the dv/dt of arm voltage need to be considered when decreasing d_N. Then, the condition for ZVS-ON of MV-side SM switches can be simplified

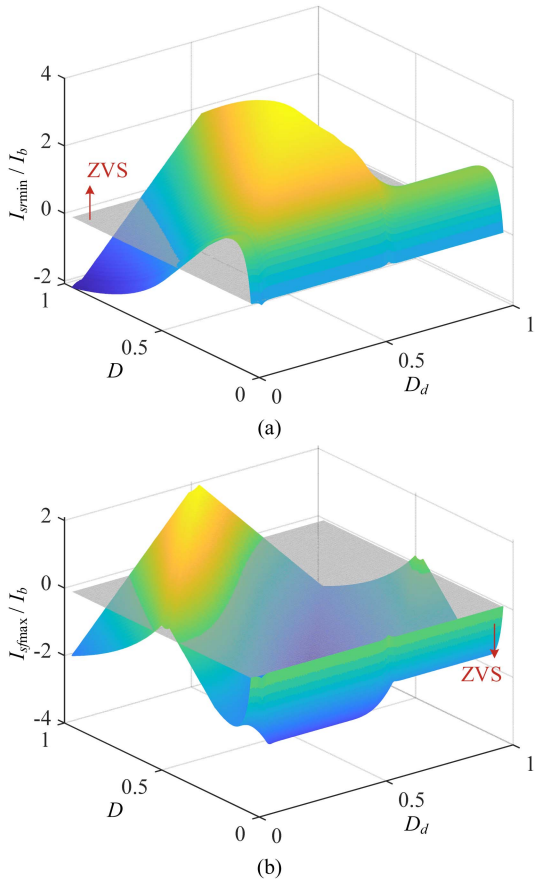

Fig. 12. Normalized maximum and minimum arm currents during arm voltage rising and falling process when d_N=0.04. (a) $I_{sr\min}/I_b$ versus D_d and D. (b) $I_{sf\max}/I_b$ versus D_d and D.

as

$$D < \frac{1}{1 + M} - d_N. \tag{24}$$

Combining (18), and (24), (25) can be obtained that achieves ZVS - ON of MV- and LV-side switches for any D_d while ensuring the voltage matches of the equivalent DAB converter

$$\begin{cases} \frac{1-2d_N-\sqrt{4d_N^2-12d_N+1}}{4d_N} < M < \frac{1-2d_N+\sqrt{4d_N^2-12d_N+1}}{4d_N} \\ 0 < d_N \le \frac{3-2\sqrt{2}}{2} \end{cases}. \tag{25}$$

It should be emphasized that the lower limit of d_N must account for the dv/dt requirements in practical applications. And when d_N exceeds $(3 - 2\sqrt{2})/2$, the MV-side SM switches cannot achieve ZVS-ON over the full operating range and will lose ZVS-ON under the light-load conditions. In addition, according to (18) and (24), D<0.5 when the MV- and LV-side switches can achieve ZVS-ON while maintaining the voltage matching. Thus, as shown in Fig. 7, the current ripple of i_M actually enlarges the ZVS regain of SM switches, ensuring the validity of the preceding analysis. Moreover, the decrease of D results in an increase in the number of SMs. Therefore, D should be maximized in order to achieve a relatively lower growth of SM number. According to (18) and (25), the maximum value of D

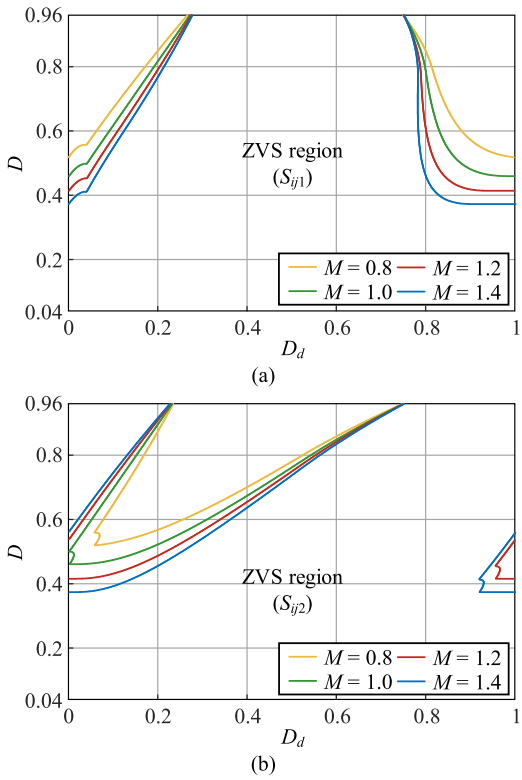

Fig. 13. ZVS boundaries of MV-side SM switches. (a) SM upper switches S_{ij1}. (b) SM lower switches S_{ij2}.

can be obtained as $1/2M_{\min}$ while M is set as its lower limit $M_{\min}$, and the minimum SM number can be calculated as $V_M M_{\min}/V_C$ with (2), realizing the ZVS-ON of both MV- and LV-side switches while ensuring the voltage matches of the equivalent DAB converter. The increased SMs can be used as redundant SMs that are usually configured in practical applications to improve reliability.

III. Parameter Design and Control Strategy

Based on the preceding analysis, the parameter design procedure for the key parameters is presented in this Section. Moreover, the control strategy of SAMMDC is also shown in this Section.

A. Parameters Design

First of all, to achieve ZVS-ON for all switches, M can be determined based on (25) and the dv/dt constraint in practice. Besides, according to (2) and (18), D decreases as M increases, thus increasing the number of SMs N. Therefore, to reduce the number of SMs, M is usually chosen to be slightly larger than the lower limit $M_{\min}$. Then, considering the fluctuation of the MV terminal voltage V_M, the turns ratio n can be selected as (26), where $V_{M\max}$ is the maximum value of V_M

$$n=\frac{M_{\min}V_{M\max}}{2V_L}=\frac{\left(1-2d_N-\sqrt{4d_N^2-12d_N+1}\right)V_{M\max}}{8d_NV_L}. \tag{26}$$

D under the rated terminal voltage can be calculated as

$$D=\frac{1}{2M}=\frac{V_M}{4nV_L}. \tag{27}$$

The number of SMs N_{total} can be expressed as (28) based on the modulation scheme of SAMMDC, which is determined by the device voltage stress and D

$$N_{\text{total}}=2N=\frac{V_M}{DV_C}. \tag{28}$$

With (12), the transmission power inductance L_d of L_{d1} and L_{d2} can be calculated as (29) under the rated terminal voltages and transmission power in mode 2, where P_N is the rated transmission power of SAMMDC

$$L_d=\frac{nV_LV_M}{12DP_Nf_s}\begin{pmatrix}12D_d\left(D+d_N-D_d\right)\\-4d_N^2-6Dd_N+3D-6D^2\end{pmatrix}. \tag{29}$$

According to Fig. 4, the current ripple ΔI_M of MV terminal current i_M can be expressed as (30), with the frequency of $2f_s$.

$$\Delta I_M=\begin{cases}\frac{(1-2D)(1-2d_N)V_M}{2L_ff_s}, & d_N\le D<0.5\\ \frac{(2D-1)(1-D)(1-2d_N)V_M}{2DL_ff_s}, & 0.5\le D\le 0.5-d_N\end{cases}. \tag{30}$$

Form (30), ΔI_M decreases with D and then increases, reaching the minimum value when $D=0.5$. And ΔI_M can also be reduced by increasing d_N. Thus, the value of L_f can be designed to meet the current ripple requirement of MV terminal, which is often a specified proportion of MV terminal average current I_M under the rated transmission power condition. Meanwhile, L_f can also be designed to meet the current limitation requirement to restrict the fault current when a fault occurs on MV side.

The dc blocking capacitance C_d of C_{d1} and C_{d2} can be designed as (31) under the rated operation conditions, where ΔV_{Cd} is the voltage ripple across C_{d1} and C_{d2} where t_{z1} and t_{z2} represent the moment of $i_{d1}(t_{z1})=i_{d1}(t_{z2})=0$. Using (10) and (31) C_d can be obtained as (A1)

$$C_d=\frac{1}{\Delta V_{Cd}}\int_{t_{z1}}^{t_{z2}}i_{d1}\left(t\right)\mathrm{d}t. \tag{31}$$

According to (31), C_d is increased with the decrease of ΔV_{Cd}. In addition, employing the dc blocking capacitor introduces LC resonant characteristics to SAMMDC, reducing phase-shifted duty cycle and current stress [33]. While this can improve the efficiency under heavy-load conditions, it can also lead to the loss of ZVS-ON under light-load conditions. And this phenomenon will become more evident with the decrease of C_d. Therefore, a tradeoff is needed when designing C_d.

The capacitance of SM capacitors C_{ij} can be selected based on the voltage ripple tolerance requirement. Fig. 14 shows the charging and discharging process of SM capacitors, where $i_{g11}\sim i_{g1N}$ are the SM capacitor currents of the SM driven by drive signals $g_{11}\sim g_{1N}$. According to Fig. 14, the voltage fluctuation of SM capacitors is influenced by the arm current i_{s1} and the internal phase-shifted angle of $g_{11}\sim g_{1N}$. According to Fig. 14, when all the SM switches achieve ZVS-ON, i_{s1} is positive during $[t_0, t_1]$ and negative during $[t_3, t_4]$. Therefore,

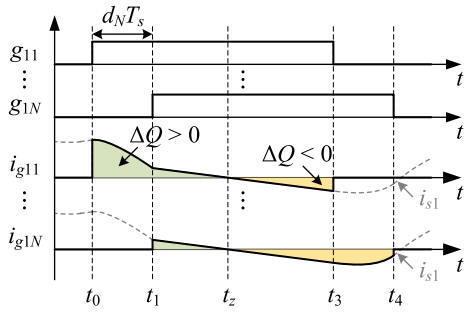

Fig. 14. Charging and discharging process of SM capacitors.

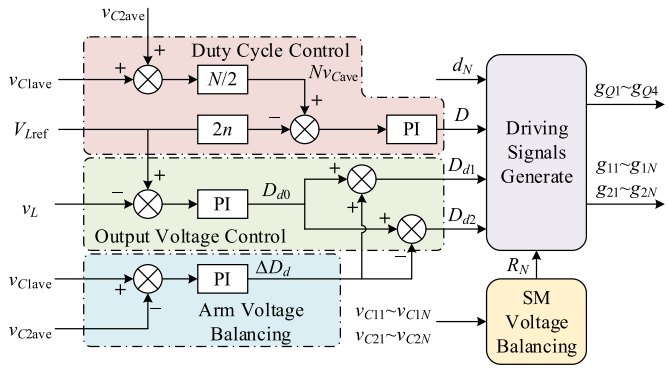

Fig. 15. Control block diagram for SAMMDC.

the first inserted SM in each switching period has the greatest capacitor charge increment, leading to the largest voltage increase ΔV_C. Therefore, the capacitance of SM capacitor C_{ij} can be calculated by (32) within the limitation of ΔV_C, where t_z is the time of $i_{s1}(t_z) = 0$

$$C_{ij} = \frac{1}{\Delta V_C}\int_{t_0}^{t_z} i_{s1}(t)\,\mathrm{d}t \approx \frac{1}{\Delta V_C}\int_{t_0}^{t_z} (I_M - i_{d1}(t))\,\mathrm{d}t. \tag{32}$$

According to (10) and (32), C_{ij} can be obtained as (A2).

Similarly, according to Fig. 14, the last inserted SM capacitor has the largest discharge, which also leads to the largest reduction in SM capacitor voltage. The capacitance of the SM capacitor can be designed to satisfy the voltage fluctuation limit during charging and discharging of the SM capacitor, namely, the larger value of the maximum SM capacitor voltage increment and decrement. Due to the higher ac link frequency, the SM capacitance requirement of SAMMDC is significantly lower than that of traditional MMCs [34].

B. Control Strategy

The control strategy of SAMMDC is illustrated in Fig. 15, which is mainly composed of duty cycle control, output voltage control, and arm voltage balancing control.

According to Fig. 3(b), the equivalent DAB converter suffers from increased current stress and loss of soft switching when $v_{A1B1}-v_{A2B2}$ and $2nv_{CD}$ are unmatched. Therefore, when terminal voltages change, the amplitude of $v_{A1B1}-v_{A2B2}$ can be regulated by changing D to achieve voltage matching, namely, $V_M/(2D) = 2nV_L$. According to (2), the aforementioned relationship can be further expressed as

$$2nV_L = \frac{V_M}{2D} = NV_C. \tag{33}$$

Based on (33), the duty cycle control can be obtained, as shown in Fig. 15 to achieve the voltage matching of the equivalent DAB converter. The average SM capacitor voltage $v_{C\mathrm{ave}}$ is calculated from the arm average SM capacitor voltages $v_{C1\mathrm{ave}}$ and $v_{C2\mathrm{ave}}$. In contrast, $2nV_{L\mathrm{ref}}$ is calculated with the referenced LV terminal voltage $V_{L\mathrm{ref}}$. Then, the Nv_{Cave} and $2nV_{L\mathrm{ref}}$ are compared to obtain D by a PI controller.

On account of the tolerance of passive parameters of two arms, the transmission power of two arms will be different for the same phase-shifted duty cycle, resulting in an imbalance of SM capacitor voltages in the upper and lower arms. Therefore, the arm voltage balancing control is adopted. According to Fig. 1, the absorbed power of the upper and lower arms can be established as

$$\begin{cases} P_1 = \frac{V_M I_M}{2} + \frac{1}{T_s}\int_{t_0}^{t_0+T_s} v_{A1B1}(t)\, i_{d1}(t)\,\mathrm{d}t \\ P_2 = \frac{V_M I_M}{2} + \frac{1}{T_s}\int_{t_0}^{t_0+T_s} v_{A2B2}(t)\, i_{d2}(t)\,\mathrm{d}t \end{cases}. \tag{34}$$

Taking mode 2 as an example, the exchange power between the upper and lower arms can be obtained as (35), where D_{d0} is the basic phase-shifted duty cycle, and ΔD_d is the compensation phase-shifted duty cycle for arm voltage balancing

$$\Delta P_{\mathrm{arm}} = P_2 - P_1 = \frac{nV_L V_M\,(D + d_N - 2D_{d0})}{DL_d f_s}\Delta D_d. \tag{35}$$

Therefore, based on (35), arm voltage balancing can be achieved by regulating ΔP_{arm} with ΔD_d. As illustrated in Fig. 15, the compensation phase-shifted duty cycle ΔD_d is obtained by comparing $v_{C1\mathrm{ave}}$ and $v_{C2\mathrm{ave}}$, achieving voltage balancing between two arms.

According to Fig. 8, the transmission power of SAMMDC can be regulated by D_d, which is similar to the conventional DAB converter. Therefore, the output voltage control can be realized by sampling the LV terminal voltage v_L and feeding back to generate the basic phase-shifted duty cycle D_{d0}. Then, the final phase-shifted duty cycle for each arm D_{d1} and D_{d2} can be obtained by combining D_{d0} and ΔD_d. SM capacitor voltage balancing control is adopted based on the SM capacitor voltage v_{C11}~v_{C1N} and v_{C21}~v_{C2N}, and N-dimensional rotating SM voltage balance sequences $\boldsymbol{R}_N$ can be obtained to achieve the SM capacitor voltage balancing in each arm [16], [32]. Finally, the driving signals for MV-side SMs and LV-side full-bridge are generated utilizing the carrier-phase-shifted modulation scheme based on d_N, D, D_{d1}, D_{d2}, and $\boldsymbol{R}_N$. It should be noted that the dc blocking capacitor voltages can be naturally balanced as long as the SM capacitor voltages and arm voltages are well balanced, since each MV-side SM has the same D obtained from the duty cycle control, thus simplifying the control strategy.

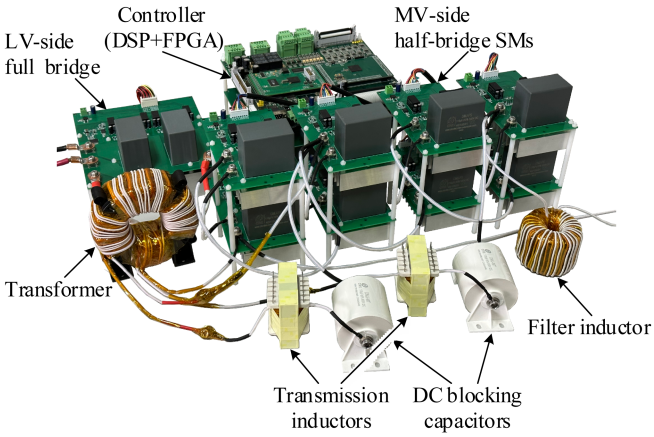

Fig. 16. Experimental prototype.

TABLE II
EXPERIMENTAL PARAMETERS

Parameters	Value
MV terminal voltage V_M/V	800~1000
LV terminal voltage V_L/V	200
Rated power P_N/kW	4
Switching frequency f_s/kHz	20
Number of SMs per arm N	4
SM capacitor C_{ij}/μF	110
Filter inductor L_f/mH	2.5
Transmission inductor L_d/μH	770
DC blocking capacitor C_d/μF	100
Transformer turns ratio n:n:1	3:3:1
LV-side capacitor C_L/μF	300

IV. EXPERIMENTAL VERIFICATION

A 4 kW prototype is constructed to verify the proposed topology and control scheme. The photograph of the experimental prototype is shown in Fig. 16. The detailed experimental parameters are given in Table II. The MV-side SM switches adopt WM2A060065L SiC MOSFETs, while the LV-side full-bridge switches employ WM2A030065L SiC MOSFETs. In addition, the control schemes are implemented by a TMS320F28346 DSP and a C6SLX16-2FTG256I FPGA. The duty cycle of arm voltage rising and falling process d_N is set as 0.04, and the dead time is set to 300 ns. The experimental results are shown in Figs. 17–25.

Fig. 17 illustrates the steady-state experimental waveforms of v_{A1B1}, v_{CD}, i_{d1}, and i_{ds} when $V_M = 900$ V under different load conditions. By implementing the variable duty cycle QSW modulation, the arm voltage v_{A1B1} is a five-step trapezoidal staircase waveform with a maximum value of 1.2 kV, and the duration of each step is 500 ns. The value of D is around 0.37 with different transmission power when $V_M = 900$ V. And v_{CD} is a 50% duty cycle square wave with a peak value of 200 V. As shown in Fig. 17(a), where $P_t = 4$ kW, the phase-shifted duty cycle D_d is 0.09. The peak values of i_{d1} and i_{ds} are 6.96 and 30.29 A, respectively. As presented in Fig. 17(b), D_d decreases to 0.01 when $P_t = 2$ kW. The peak values of i_{d1} and i_{ds} are -4.15 and 15.87A, respectively. In Fig. 17(c), where $P_t = 800$ W, D_d is -0.02. The peak values of

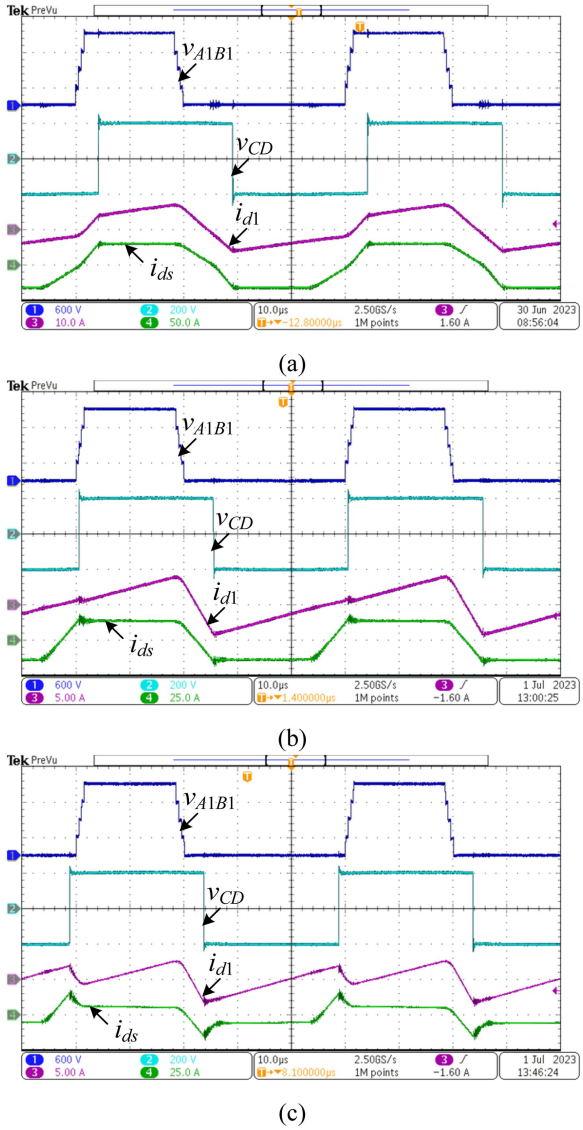

Fig. 17. Steady-state experimental waveforms of v_{A1B1}, v_{CD}, i_{d1}, and i_{ds} when V_M=900V. (a) P_t=4 kW. (b) P_t=2 kW. (c) P_t=800W.

i_{d1} and i_{ds} reduce to -3.25 and 15.38 A, respectively. Besides, the ZVS-ON of LV-side full-bridge switches can be achieved with the negative turn-ON current under different transmission power. These experimental results demonstrate that SAMMDC can achieve voltage matching of the equivalent DAB converter, low LV-side current stress, and ZVS turn-ON regardless under light- or heavy-load situations.

Fig. 18 shows the steady-state experimental waveforms of v_{A1B1}, v_{A2B2}, i_{s1}, and i_{s2} when $V_M = 900$ V under different load conditions. According to Fig. 18, the arm voltages v_{A1B1} and v_{A2B2} are phase-shifted by 180° to each other, as well as the arm currents i_{s1} and i_{s2}. The peak values of i_{s1} and i_{s2} are 12.11, 7.39, and 4.80A, respectively. Moreover, under the different transmission power conditions, all SM upper switches achieve ZVS-ON with positive i_{s1} and i_{s2} during v_{A1B1} and v_{A2B2} rising processes. i_{s1} and i_{s2} are both negative during the

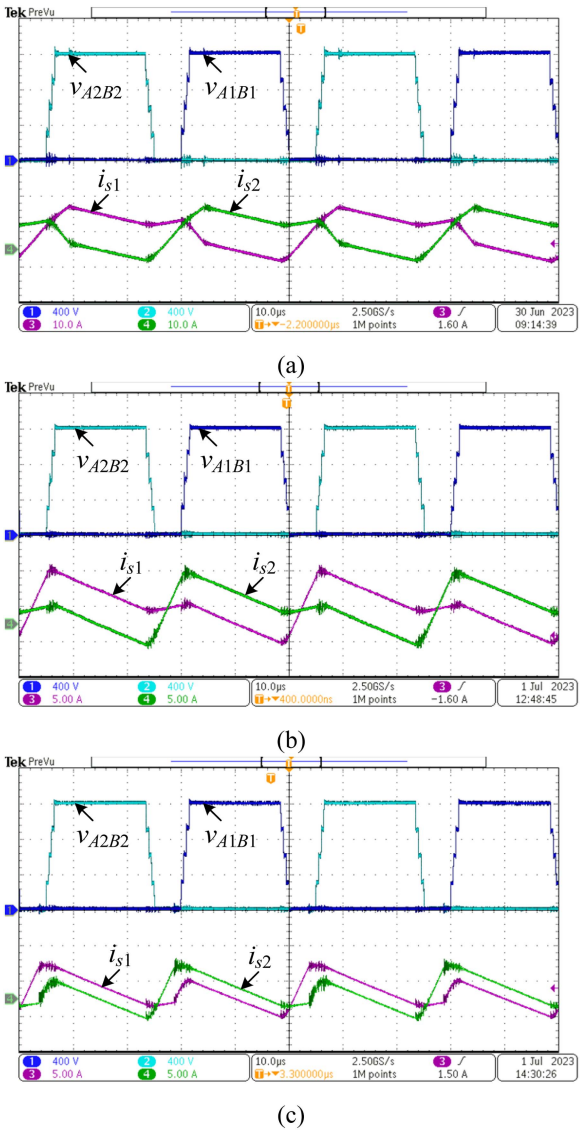

Fig. 18. Steady-state experimental waveforms of v_{A1B1}, v_{A2B2}, i_{s1}, and i_{s2} when V_M=900V. (a) P_t=4 kW. (b) P_t=2 kW. (c) P_t=800W.

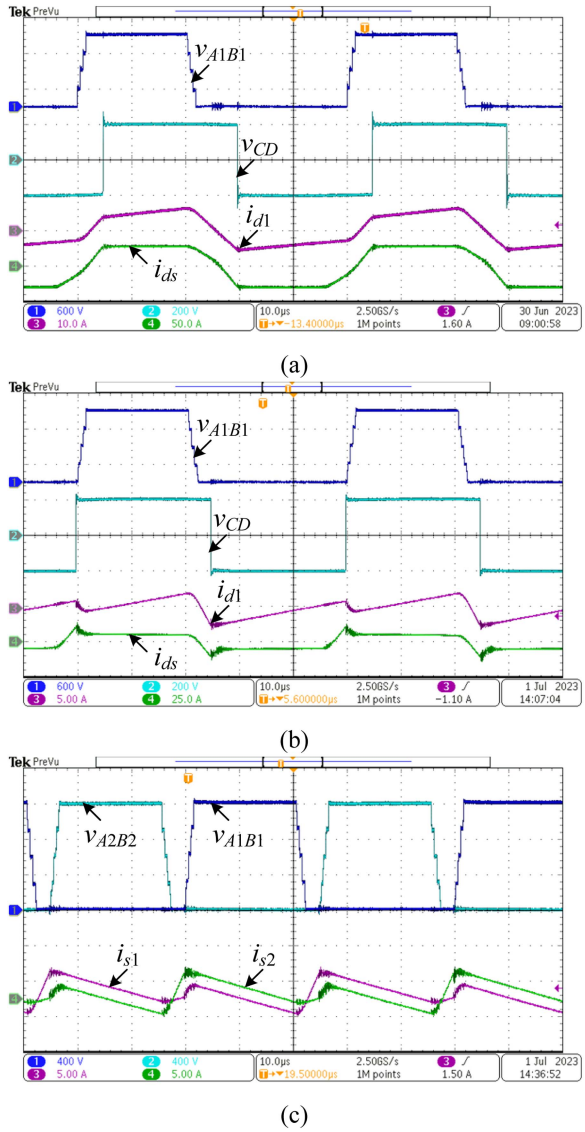

Fig. 19. Steady-state experimental waveforms when V_M=1 kV. (a) v_{A1B1}, v_{CD}, i_{d1}, and i_{ds} when P_t=4 kW. (b) v_{A1B1}, v_{CD}, i_{d1}, and i_{ds} when P_t=800 W. (c) v_{A1B1}, v_{A2B2}, i_{s1}, and i_{s2} when P_t=800 W.

arm voltages falling processes, which indicates that all SM lower switches are turned ON with ZVS.

Figs. 19 and 20 present the steady-state experimental waveforms when V_M = 1kV and V_M = 800 V, respectively. By utilizing the duty cycle control, D grows to 0.41 when V_M = 1kV and falls to 0.33 when V_M = 800 V. The peak values of v_{A1B1} and v_{A2B2} are maintained at 1.2 kV. Besides, both the LV-side full-bridge switches and the MV-side SM switches are turned ON with ZVS when $P_t = 4$ kW and $P_t = 800$ W.

The steady-state experimental waveforms in the reverse transmission power condition are shown in Fig. 21, where V_M = 900 V and $P_t = -4$ kW. The peak values of v_{A1B1} and v_{A2B2} are maintained at 1.2kV while D is 0.37 and D_d is -0.17. The ZVS-ON of LV-side full-bridge and MV-side SM switches can be realized under the reverse transmission power condition.

Therefore, it is concluded that the proposed SAMMDC can realize ZVS turn-ON for all switches over wide transmission power and terminal voltage range.

Fig. 22 shows the voltage waveforms of SM capacitors v_{C11}~v_{C14} and v_{C21}~v_{C24} when $V_M = 900$ V, which indicates that the SM capacitor voltages are well balanced around 300V.

The dynamic experimental waveforms is shown in Fig. 23. Fig. 23(a) shows the waveforms of v_M, v_L, v_{A1B1}, and i_{d1} when MV terminal voltage v_M increases from 800 to 1 kV in 40 ms, where $P_t = 4$ kW. Throughout the transition process, LV terminal voltage v_L and the peak value of v_{A1B1} are maintained at 200 V and 1.2 kV, respectively. The peak value of i_{d1} decreases from 7.92 to 6.23A and then stabilizes. Fig. 23(b) shows the experimental waveforms of v_L, v_{C11}, i_{d1}, and i_{ds} when V_M = 900 V with the P_t step changes from 2 to 4 kW. During the power step process, v_L has an undershoot and then stabilizes at 200V.

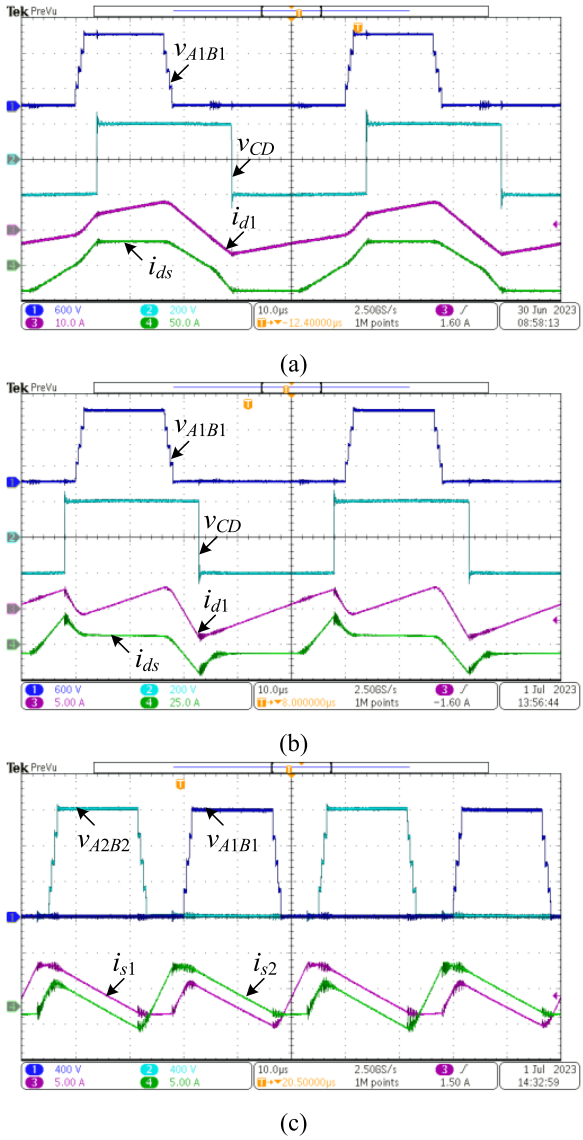

Fig. 20. Steady-state experimental waveforms when V_M=800 V. (a) v_{A1B1}, v_{CD}, i_{d1}, and i_{ds} when P_t=4 kW. (b) v_{A1B1}, v_{CD}, i_{d1}, and i_{ds} when P_t=800 W. (c) v_{A1B1}, v_{A2B2}, i_{s1}, and i_{s2} when P_t=800 W.

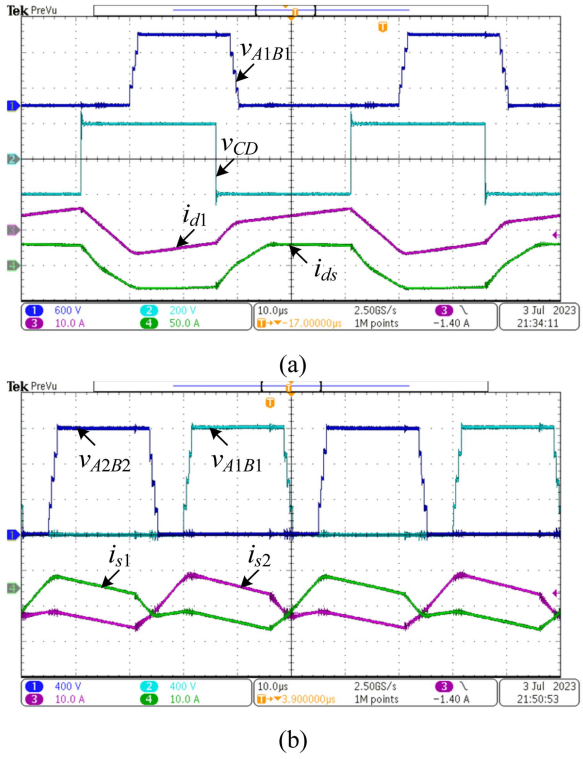

Fig. 21. Steady-state experimental waveforms in the reverse transmission power condition when V_M=900 V and P_t=−4kW. (a) v_{A1B1}, v_{CD}, i_{d1}, and i_{ds}. (b) v_{A1B1}, v_{A2B2}, i_{s1}, and i_{s2}.

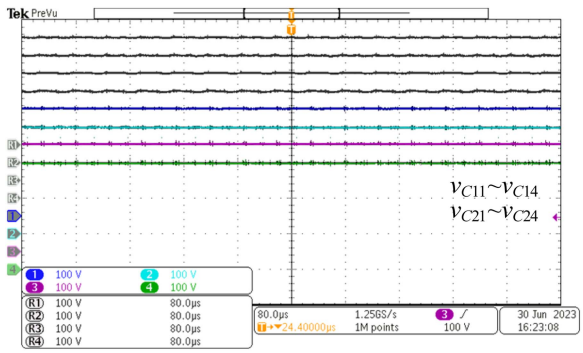

Fig. 22. Steady-state experimental waveforms of v_{C11}~v_{C14} and v_{C21}~v_{C24}.

And v_{C11} has a transient drop during the transmission power step process and is well balanced at 308 V with different P_t.

In addition, the power loss breakdown of the proposed SAMMDC is carried out, as shown in Fig. 24. The total power loss increases with the increase of P_t and the decrease of V_M. At the full-load condition (P_t = 4.0 kW), the total power loss is 155.28 W, 136.45 W, and 124.09 W when V_M is 800 V, 900 V, and 1 kV, respectively. The conduction loss is the major part of the total power loss under these conditions, accounting for about 50% of the total power loss, while the switching loss accounts for about 10% due to the soft switching operating. The magnetic components have about 30% power loss. The capacitors and other components produce about 10% power loss. At the light-load condition (P_t = 0.8 kW), the total power loss is 41.75, 34.31, and 29.43 W when the V_M is 800 V, 900 V, and 1 kV, respectively. The power loss of the magnetic components contributes to half of the total power loss and becomes the main part of the total power loss. The conduction loss takes about 15% of the total power loss, while the switching loss accounts for about 20% due to the ZVS current under light-load conditions.

Fig. 25 illustrates the measured efficiency of the proposed SAMMDC when transmission power P_t varies from 800 W to 4 kW with V_M of 800 V, 900 V, and 1 kV. The efficiency increases and then decreases with P_t. The efficiency is relatively low under light-load conditions because of the core loss and the ZVS current. Under heavy-load conditions, the efficiency declines due to the increase of the conduction loss and winding loss. The efficiency is higher than 91.15% under different operating

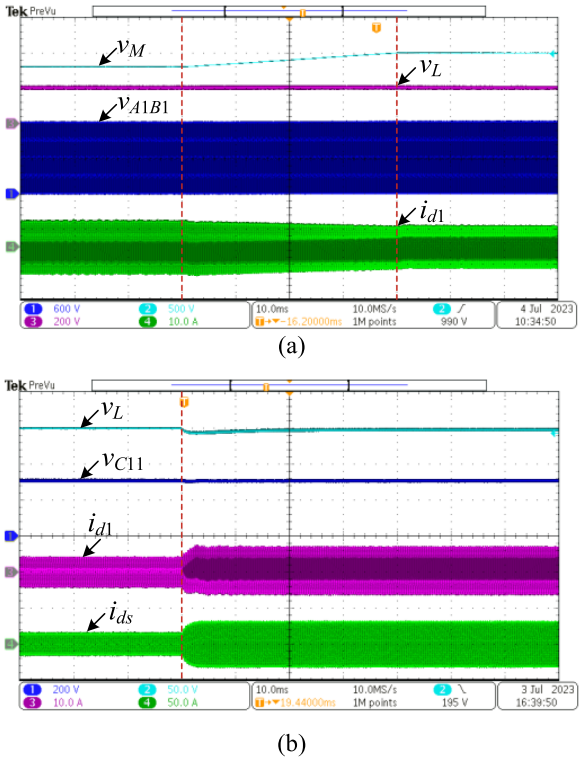

Fig. 23. Dynamic experimental waveforms. (a) v_M, v_L, v_{A1B1}, and i_{d1} with MV terminal voltage changes when P_t=4kW. (b) v_L, v_{C11}, i_{d1}, and i_{ds} with transmission power step changes when V_M=900 V.

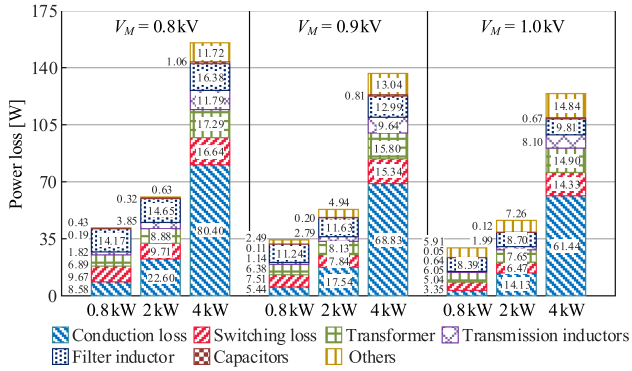

Fig. 24. Power loss breakdown with different transmission power P_t and MV terminal voltage V_M.

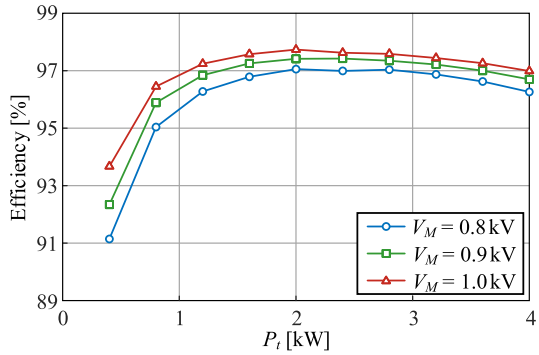

Fig. 25. Measured efficiency versus transmission power P_t.

conditions. The peak efficiency reaches 97.74% when $P_t = 2$ kW and $V_M = 1$ kV. The results illustrate that SAMMDC can achieve high efficiency throughout a wide range of terminal voltage and transmission power.

V. Conclusion

This article proposes a novel SAMMDC with a centralized transformer for MVDC to LVDC interconnection. With the series-arm structure, the MV terminal concentrated capacitors can be eliminated, and the number of SMs can be reduced. By employing the variable duty cycle QSW modulation and SPS control, the SAMMDC operates as a conventional DAB converter with bidirectional transmission power capability. Besides, rigorous derivation clearly identifies the ZVS constraints for both MV-side SM switches and LV-side full-bridge switches. On this basis, the output voltage control strategy and parameter design procedure are proposed to realize ZVS-ON for SAMMDC over the whole operating range. The operation principle and soft switching characteristics of SAMMDC are analyzed in detail. Finally, experiments with a 4kW prototype are carried out, and the results validate the theoretical analysis and control strategies of the proposed SAMMDC.

Appendix

With (10) and (31), the dc blocking capacitance C_d of C_{d1} and C_{d2} can be obtained as (A1) shown at the bottom of this page.

According to (10) and (32) the capacitance of SM capacitors C_{ij} can be obtained as (A2) shown at the bottom of this page.

References

[1] W. Chen, A. Q. Huang, C. Li, G. Wang, and W. Gu, "Analysis and comparison of medium voltage high power dc/dc converters for offshore

$$C_d = \frac{V_M \begin{pmatrix} 12D(D-1)^2 + 3DM\left((M+2)\left(8D_d\left(2d_N - 2D_d + 1\right) - 4d_N + 1\right) + 2\right) \\ +6D^2M\left(-6 + 8D_d - 4d_N + \left(M - 2\left(D - 2D_d + d_N\right)\right)^2\right) - 4d_N^2\left((M+1) + D\left(4M^2 + 6M - 1\right)\right) \end{pmatrix}}{192D\left(M+1\right)\left(D\left(M-1\right)+1\right)L_d f_s^2 \Delta V_{Cd}} \tag{A1}$$

$$C_{ij} = \frac{-V_M \begin{pmatrix} 9D^3\left(M+1\right)\left(\left(M+1\right)\left(D+2d_N\right) - 2\right) - 3D^2\left(\left(M+1\right)\left(12D_dM\left(D_d + d_N\right) + d_N\left(12 - d_N\left(7M+3\right)\right)\right) - 3\right) \\ -3D\left(2d_N\left(-3 + d_N + d_NM\left(3 + \left(M+1\right)\left(6D_d - 2d_N\right)\right)\right) - 12D_dM\left(d_N + \left(\left(M+1\right)d_N + 1\right)D_d\right)\right) \\ +4M\left(3D_d\left(D_d - d_N\right) + d_N^2\right)\left(M\left(3D_d\left(D_d - d_N\right) + d_N^2\right) - 3d_N\right) - 3d_N^2 \end{pmatrix}}{144D\left(D\left(M+1\right) - 1\right)L_d f_s^2 \Delta V_C} \tag{A2}$$

wind energy systems," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 2014–2023, Apr. 2013.
[2] Y. Chen, S. Zhao, Z. Li, X. Wei, and Y. Kang, "Modeling and control of the isolated dc–dc modular multilevel converter for electric ship medium voltage direct current power system," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 124–139, Mar. 2017.
[3] B. He, W. Chen, X. Li, L. Shu, Z. Zou, and F. Liu, "Unified frequency-domain small-signal stability analysis for interconnected converter systems," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 1, pp. 532–544, Feb. 2023.
[4] D. Rothmund, T. Guillod, D. Bortis, and J. W. Kolar, "99% efficient 10 kV SiC-based 7 kV/400 V dc transformer for future data centers," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 753–767, Jun. 2019.
[5] A. Q. Huang, "Medium-voltage solid-state transformer: Technology for a smarter and resilient grid," *IEEE Ind. Electron. Mag.*, vol. 10, no. 3, pp. 29–42, Sep. 2016.
[6] T. Guillod, D. Rothmund, and J. W. Kolar, "Active magnetizing current splitting ZVS modulation of a 7 kV/400 V DC transformer," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1293–1305, Feb. 2020.
[7] M. A. Hannan et al., "State of the art of solid-state transformers: Advanced topologies, implementation issues, recent progress and improvements," *IEEE Access*, vol. 8, pp. 19113–19132, 2020.
[8] B. Zhao, Q. Song, J. Li, W. Liu, G. Liu, and Y. Zhao, "High-frequency-link dc transformer based on switched capacitor for medium-voltage dc power distribution application," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4766–4777, Jul. 2016.
[9] D. Ma, W. Chen, and X. Ruan, "A review of voltage/current sharing techniques for series-parallel-connected modular power conversion systems," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 12383–12400, Nov. 2020.
[10] Z. Lu et al., "Medium voltage soft-switching dc/dc converter with series-connected SiC MOSFETs," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1451–1462, Feb. 2021.
[11] G. Ulissi, U. R. Vemulapati, T. Stiasny, and D. Dujic, "High-frequency operation of series-connected IGCTs for resonant converters," *IEEE Trans. Power Electron.*, vol. 37, no. 5, pp. 5664–5674, May 2022.
[12] S. Kenzelmann, A. Rufer, D. Dujic, F. Canales, and Y. R. de Novaes, "Isolated dc/dc structure based on modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 89–98, Jan. 2015.
[13] T. Lüth, M. M. C. Merlin, T. C. Green, F. Hassan, and C. D. Barker, "High-frequency operation of a dc/ac/dc system for HVDC applications," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4107–4115, Aug. 2014.
[14] M. Basić and D. Dujić, "Hybrid modular multilevel converter for variable dc link voltage operation," *CPSS Trans. Power Electron. Appl.*, vol. 6, no. 2, pp. 178–190, Jun. 2021.
[15] S. Cui, N. Soltau, and R. W. De Doncker, "A high step-up ratio soft-switching dc–dc converter for interconnection of MVDC and HVDC grids," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 2986–3001, Apr. 2018.
[16] S. Fan et al., "Inherent SM voltage balance for multilevel circulant modulation in modular multilevel dc–dc converters," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1352–1368, Feb. 2022.
[17] I. A. Gowaid, G. P. Adam, A. M. Massoud, S. Ahmed, D. Holliday, and B. W. Williams, "Quasi two-level operation of modular multilevel converter for use in a high-power dc transformer with dc fault isolation capability," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 108–123, Jan. 2015.
[18] Y. Wang, Q. Song, B. Zhao, J. Li, Q. Sun, and W. Liu, "Quasi-square-wave modulation of modular multilevel high-frequency dc converter for medium-voltage dc distribution application," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7480–7495, Sep. 2018.
[19] J. Zhang, Z. Wang, and S. Shao, "A three-phase modular multilevel dc–dc converter for power electronic transformer applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 140–150, Mar. 2017.
[20] Z. Xing, X. Ruan, H. You, X. Yang, D. Yao, and C. Yuan, "Soft-switching operation of isolated modular dc/dc converters for application in HVDC grids," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 2753–2766, Apr. 2016.
[21] X. Xiang, Y. Qiao, Y. Gu, X. Zhang, and T. C. Green, "Analysis and criterion for inherent balance capability in modular multilevel DC–AC–DC converters," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 5573–5580, Jun. 2020.
[22] H. Jin, W. Chen, K. Hou, S. Shao, L. Shu, and R. Li, "A sharing-branch modular multilevel dc transformer with wide voltage range regulation for dc distribution grids," *IEEE Trans. Power Electron.*, vol. 37, no. 5, pp. 5714–5730, May 2022.
[23] Y. Qiao, X. Zhang, X. Xiang, X. Yang, and T. C. Green, "Trapezoidal current modulation for bidirectional high-step-ratio modular dc–dc converters," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3402–3415, Apr. 2020.
[24] G. Zheng, Y. Chen, and Y. Kang, "Trapezoidal current modulation for a compact dc modular multilevel converter with ZVS of submodules and zcs of voltage-balancing circuits," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 10986–10992, Oct. 2021.
[25] C. Pineda, J. Pereda, F. Rojas, G. Droguett, C. Burgos-Mellado, and A. J. Watson, "Optimal ZCS modulation for bidirectional high-step-ratio modular multilevel dc–dc converter," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 12540–12550, Nov. 2021.
[26] J. Sheng et al., "High-efficient operation for modular multilevel resonant dc-dc converters in medium voltage applications with wide input range and wide load condition," *IEEE Trans. Power Electron.*, vol. 38, no. 10, pp. 12180–12194, Oct. 2023, doi: 10.1109/TPEL.2023.3295828.
[27] H. Jin, W. Chen, Y. Xie, L. Shu, and Y. Xu, "Asymmetric trapezoidal wave modulation of modular multilevel resonant dc/dc converter for current stress optimization," *IEEE Trans. Power Electron.*, vol. 38, no. 7, pp. 8499–8512, Jul. 2023.
[28] H. Jin, W. Chen, S. Shao, and L. Shu, "A quasi-square-wave modular multilevel resonant dc/dc converter with ZCS and current-shaping capacity for high step-ratio application," *IEEE Trans. Power Electron.*, vol. 38, no. 1, pp. 548–565, Jan. 2023.
[29] S. Shao et al., "A modular multilevel resonant dc–dc converter," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 7921–7932, Aug. 2020.
[30] J. Duan, D. Zhang, X. Wang, and R. Gu, "Modular multilevel resonant dc transformer with inherent balancing capability," *IEEE Trans. Power Electron.*, vol. 70, no. 6, pp. 5717–5727, Jun. 2023.
[31] Q. Zhou et al., "A step-down resonant modular multilevel dc/dc converter with extendable ZVS range based on asymmetric triangular current," *IEEE Trans. Ind. Electron.*, vol. 69, no. 11, pp. 11088–11099, Nov. 2022.
[32] S. Shao, M. Jiang, J. Zhang, and X. Wu, "A capacitor voltage balancing method for a modular multilevel dc transformer for dc distribution system," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 3002–3011, Apr. 2018.
[33] R. Lenke, F. Mura, and R. W. De Doncker, "Comparison of non-resonant and super-resonant dual-active ZVS-operated high-power dc-dc converters," in *Proc. Eur. Conf. Power Electron. Appl.*, 2009, pp. 1–10.
[34] J. Lan, W. Chen, X. Li, Y. Sun, L. Shu, and F. Deng, "A three-phase multiplexing arm modular multilevel converter with high power density and small volume," *IEEE Trans. Power Electron.*, vol. 37, no. 12, pp. 14587–14600, Dec. 2022.

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