A High-Bandwidth Parallel Active Balancing Controller for Current-Controlled Flying Capacitor Multilevel Converters

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***Abstract*—This work presents a capacitor voltage balancing controller for current-controlled flying capacitor multilevel converters. A small-signal model of the converter derived from state–space averaging informs the parallel controller structure. The proposed controller incorporates nonlinear actions to decouple flying capacitor control loops and prevent adverse interaction between the capacitor voltage balancing and inductor current controllers. Experimental results of closed-loop line and load transient responses demonstrate significant performance improvements with the proposed balancing architecture compared to a converter relying on natural capacitor balancing. These improvements are quantified with experimental measurements of switch voltage stress and load current disturbance as a response to line voltage perturbations at different frequencies. Limits to control bandwidths in balancing controllers based on averaged models are discussed. The closed-loop stability of the converter operating with the proposed active balancing architecture is discussed as a function of the operating point, controller gains, and hardware parameters, such as output filter inductance and inductor current ripple.**

***Index Terms*—Dynamical systems, DC-DC power converters, linear feedback control systems, multilevel converters.**

I. Introduction

THE flying capacitor multilevel (FCML) converter has been demonstrated as an attractive solution for applications targeting high power density and high efficiency [1]. It enables load regulation over a wide range of voltage conversion ratios, smaller magnetic elements in the output filter, and use of high-figure-of-merit switches rated for blocking voltages lower than the converter port voltages. [1], [2], [3], [4]. A generalized step-down N-level FCML converter, shown in Fig. 1, is capable of generating N distinct voltage levels at its switching node v_{sw}. The converter comprises $n_c = N - 1$ complementary switch pairs and $M = n_c - 1$ flying capacitors.

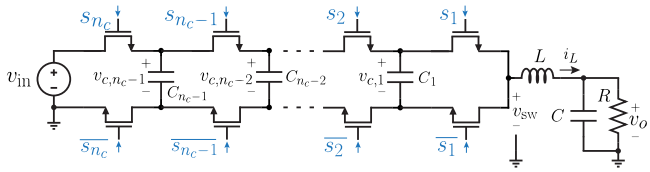

Fig. 1. Schematic of an N-level FCML converter with $n_c = N - 1$ complementary switch pairs and $M = N - 2$ flying capacitors.

In ideal operating conditions, the voltage of flying capacitor C_k is given by $v_{c,k} = \frac{k}{n_c} v_{\text{in}}$. This voltage distribution is termed *balanced* [5], [6], [7], and corresponds to equal blocking voltage stress of $\frac{1}{n_c} v_{\text{in}}$ on every switch. The balanced capacitor voltages are naturally achieved in steady-state when the switching signals for the n_c complementary switch pairs are generated with (circularly) symmetric phase-shifted pulse-width modulation (PS-PWM), shown in Fig. 2. In this switching scheme, neighboring switch pairs are driven by phase-shifted versions of a common PWM switching waveform [1], [8]. In balanced operation with switching signals generated by PS-PWM, the fundamental frequency of the inductor current ripple occurs at $n_c f_{\text{pwm}}$, where f_{pwm} is the switching frequency. This frequency-multiplication effect enables meeting a given current ripple specification with a reduced filter inductance, which corresponds to reduced converter mass and volume and faster current slew rates. Example waveforms of the switched-node voltage v_{sw} and inductor current i_L are also shown in Fig. 2.

Despite achieving *natural balancing* of capacitor voltages, open-loop operation with PS-PWM is unreliable in practice. As evident in the open-loop measurements of [5] and [8], the capacitor voltage responses to a step in the input voltage are typically slow, exhibiting long setting times and dominant underdamped behavior. Natural balancing is therefore an ineffective balancing strategy when the supply voltage varies quickly, such as during converter startup when the supply voltage is ramped, or if the supply varies at twice-line frequency as in the case of a rectifier-fed converter [9]. In these situations, the capacitor voltages deviate significantly from their respective nominal

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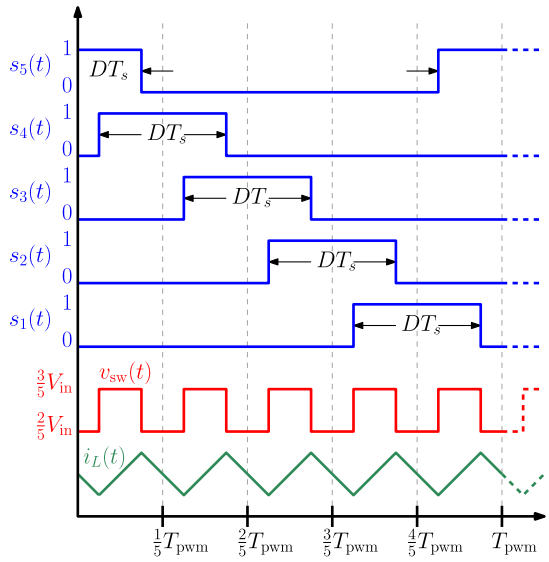

Fig. 2. Circularly symmetric PS-PWM example for a six-level FCML converter with $n_c = 5$ switching signals. In symmetric operation, all switching signals have equal duty ratio $D = 0.3$, and are shifted in time by $\frac{1}{n_c}T_{\text{pwm}}$. Assuming balanced capacitor voltages, the resultant switched-node voltage v_{sw} and inductor current waveform i_L are shown in the subplots below the switching signals.

fractions of the supply voltage, resulting in unequal voltage stresses across the switching devices that may surpass the device ratings. FCML converter solutions relying on natural balancing may therefore require excessively large filter and hold-up elements at the supply side to maintain safe operation, which detract from the overall system power density and efficiency. In addition, the natural balancing dynamics in open-loop operation vary significantly with underlying converter parameters, such as the filter inductor and flying capacitor values, the switching frequency, and parasitic elements in the converter [5], [6], [7], [8]. The steady-state capacitor voltages also depend on system parameters, such as the impedance of the supply, converter input capacitance [10], and loading impedance [5], [11]. As a result, natural balancing cannot broadly guarantee safe transient response across a wide range of converter designs and operating conditions.

Closed-loop *active balancing* control is desirable to ensure that the flying capacitor voltages remain at their nominal values relative to the input voltage. Several recent works have investigated active balancing controller design, however the presented closed-loop systems exhibit limitations arising from their structure and implementation. The works in [12], [13], [14], and [15] present balancing controllers which adjust switch duty ratios to regulate the average flying capacitor currents. These controllers do not properly decouple the control loops for different flying capacitors, forcing low-bandwidth operation in practice. Ghias et al. [16] propose a modification to the PS-PWM carriers to achieve natural balancing, but rely on a cost-function-minimizing control law that is computationally expensive and slow in practice. The controller in Stillwell et al.'s [17] work balances steady-state capacitor voltages by adjusting the duty ratios and phase shifts of switching signals, but the proposed feedback technique is slow and unable to track fast transients in the input voltage. The balancing controllers proposed for three-level FCML converters in [18] and [19] are designed for active balancing with fast current control response, but are not easily extended for converters with a greater number of levels. Wu and Lu [20] demonstrate a nonlinear controller for active balancing derived from the averaged model of the converter, but do not decouple the voltage balancing from the output current control. This ultimately limits the practical utility of the controller, as the inductor current may exhibit significant deviation from its steady-state value during supply transients. Tachon et al. [21] present a full-state-feedback controller to control both flying capacitor voltages and the inductor current with appropriate decoupling. However, the internal structure of the converter plant and proposed controller are not analyzed in detail. Furthermore, the controller only decouples the balancing and current control loops in the small-signal sense, implying mutual interaction in scenarios where capacitor voltages are significantly imbalanced, such as during balancing transients. The work in [21] also does not characterize the choice of controller gains and achievable closed-loop active balancing bandwidths, implying the dynamics of capacitor voltages can be assigned arbitrarily. Section V of the present work investigates limitations of balancing controllers based on averaging and discusses results that are also applicable to the controller in [21].

This work presents an active balancing controller implemented in parallel with a high-bandwidth current controller. The proposed balancing controller decouples the dynamics of every flying capacitor, and the presented current controller compensates large-signal mutual interactions between the control loops. The plant models, controller derivation, and experimental results are given for the buck-type FCML converter, but can be easily extended to the boost-type converter and other variants with the appropriate adjustments to dynamical equations. This work expands on a conference publication on the same topic [22], presenting additional theoretical foundation, experimental verification, and analysis of performance limits. The rest of this article is organized as follows. Section II derives a small-signal plant model of the converter, motivating the parallel controller structure. Section III details the active balancing and current control laws. Section IV presents experimental verification of the parallel controller, demonstrating high-bandwidth active balancing suitable for fast supply perturbations. Section V investigates the stability characteristics of the closed-loop system as a function of the converter operating point. Finally, Section VI concludes this article.

II. Averaged Plant Model

An N-level FCML converter with state variables labeled as shown in Fig. 1 is represented by the following dynamical equations:

$$C_k \dot{v}_{c,k} = i_L \cdot (s_{k+1} - s_k) \quad k \in 1, \ldots, M \tag{1}$$

$$L\dot{i}_L = v_{\text{in}} s_{n_c} + \sum_{k=1}^{M} v_{c,k} \cdot (s_k - s_{k+1}) - v_o \tag{2}$$

$$C_o \dot{v}_o = i_L - \frac{v_o}{R}. \tag{3}$$

The impact of switching on the state dynamics is captured by switching functions s_k corresponding to the switching signals applied to the converter. In this formulation, $s_1, \ldots, s_{n_c}$ are inputs to the system, and $v_{c,1}, \ldots, v_{c,M}$, i_L, and v_o are the N state variables. Application of state–space averaging [23] to the instantaneous dynamical equations describing the N-level FCML converter yields a system of N *averaged* equations. This averaged model captures the low-frequency dynamics of the state variables as functions of the averaged switching inputs, i.e., n_c duty ratios numbered $d_1, \ldots, d_{n_c}$. The averaged model is obtained via application of the averaging operator [23], [24], given by

$$\bar{x}(t) := \frac{1}{T_{\text{pwm}}} \int_{t-T_{\text{pwm}}}^{t} x(\tau) d\tau \tag{4}$$

to all state variables and inputs. In addition, as typical in averaged analysis [23], state variables are assumed to have small ripple with respect to their average values and averaged quantities are assumed to vary slowly with respect to the averaging interval $T_{\text{pwm}} = \frac{1}{f_{\text{pwm}}}$. The averaged dynamics of the FCML converter are given by the following nonlinear system:

$$C_k \dot{\overline{v_{c,k}}} = \overline{i_L} \cdot (d_{k+1} - d_k) \quad k \in 1, \ldots, M \tag{5}$$

$$L \dot{\overline{i_L}} = \overline{v_{\text{in}}} d_{n_c} + \sum_{k=1}^{M} \overline{v_{c,k}} \cdot (d_k - d_{k+1}) - \overline{v_o} \tag{6}$$

$$C_o \dot{\overline{v_o}} = \overline{i_L} - \frac{\overline{v_o}}{R}. \tag{7}$$

As a starting point for controller design, the nonlinear model in (5)–(7) is linearized at a quiescent dc operating point to obtain the small-signal dynamics of the averaged system. The quiescent state is vectorized as $[x_e] := [\, V_{c,1} \ \cdots \ V_{c,M} \ I_L \ V_o \,]^{\mathrm{T}}$ and the quiescent input is expressed as a vector of equal duty ratios $[d_e] := [\, D \ \ D \ \cdots \ D \,]^{\mathrm{T}}$. This choice of $[d_e]$ corresponds to the desired steady-state operating condition under symmetric PS-PWM. The small-signal dynamics are described by the following multiple-input multiple-output (MIMO) system where small-signal variables are denoted with tildes

$$\underbrace{\begin{bmatrix} \dot{\tilde{v}}_{c,1} \\ \vdots \\ \dot{\tilde{v}}_{c,M} \\ \dot{\tilde{i}}_L \\ \dot{\tilde{v}}_o \end{bmatrix}}_{[\dot{\tilde{x}}] \in \mathbb{R}^N} = \underbrace{\begin{bmatrix} \\ F \\ \\ \end{bmatrix}}_{[F] \in \mathbb{R}^{N \times N}} \underbrace{\begin{bmatrix} \tilde{v}_{c,1} \\ \vdots \\ \tilde{v}_{c,M} \\ \tilde{i}_L \\ \tilde{v}_o \end{bmatrix}}_{[\tilde{x}] \in \mathbb{R}^N} + \underbrace{\begin{bmatrix} \\ G \\ \\ \end{bmatrix}}_{[G] \in \mathbb{R}^{N \times n_c}} \underbrace{\begin{bmatrix} \tilde{d}_1 \\ \tilde{d}_2 \\ \vdots \\ \tilde{d}_{n_c} \end{bmatrix}}_{[\tilde{d}] \in \mathbb{R}^{n_c}} \tag{8}$$

where

$$[F] = \left[\begin{array}{ccc|cc} 0 & \cdots & 0 & 0 & 0 \\ 0 & \cdots & 0 & 0 & 0 \\ \vdots & \ddots & \vdots & \vdots & \vdots \\ 0 & \cdots & 0 & 0 & 0 \\ \hline 0 & \cdots & 0 & 0 & -\frac{1}{L} \\ 0 & \cdots & 0 & \frac{1}{C} & -\frac{1}{RC} \end{array}\right] \tag{9}$$

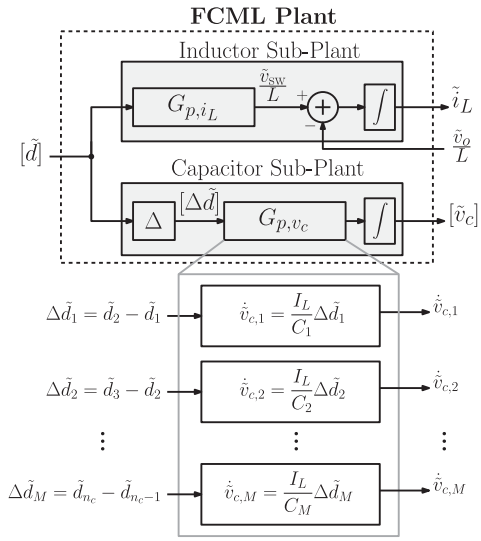

Fig. 3. Diagram of small-signal averaged plant model of the FCML converter, showing inner parallel plants. The flying capacitors are only controlled by the differences of neighboring duty ratios, Δd_k.

$$[G] = \begin{bmatrix} \frac{-I_L}{C_1} & \frac{I_L}{C_1} & 0 & \cdots & 0 & 0 \\ 0 & \frac{-I_L}{C_2} & \frac{I_L}{C_2} & \cdots & 0 & 0 \\ \vdots & \ddots & \ddots & \ddots & \vdots & \vdots \\ 0 & 0 & 0 & \cdots & \frac{-I_L}{C_M} & \frac{I_L}{C_M} \\ \frac{V_{c,1}}{L} & \frac{V_{c,2}-V_{c,1}}{L} & \frac{V_{c,3}-V_{c,2}}{L} & \cdots & \cdots & \frac{v_{\text{in}}-V_{c,M}}{L} \\ 0 & 0 & 0 & \cdots & \cdots & 0 \end{bmatrix}. \tag{10}$$

Although the averaged and small-signal models have been derived in [20] and [21], their internal structures have not previously been analyzed in detail. Specifically, the nature of the small-signal model reveals properties of the plant that may be used to derive the controller structure. From (10) it follows that the small-signal capacitor voltages, vectorized as $[\tilde{v}_c] := [\, \tilde{v}_{c,1} \ \cdots \ \tilde{v}_{c,M} \,]^{\mathrm{T}}$, and the small-signal inductor current $\tilde{i}_L$ are naturally decoupled, as the cross-coupling terms in $[F]$ are zero. Thus, $[\tilde{v}_c]$ and $\tilde{i}_L$ can be realized as the outputs of two separate subplants modeled as decoupled integrators, as shown in Fig. 3. Furthermore, the small-signal capacitor voltages are decoupled from each other, as the terms in the top-left block of $[F]$ are all zero. Thus, the capacitor subplant can also be modeled internally as a system of decoupled integrators, shown in the expanded view in Fig. 3. The standard assumptions of averaging underlie these claims about the plant behavior and the validity of the block diagram in Fig. 3—namely, the averaged analysis assumes that the ripple content of state variables do not significantly affect the dynamics of the averaged components. Section V of this work examines the extent to which this assumption is true, and consequently, presents the limitations of active balancing controllers designed from averaged models.

Linear manipulation of (8) reveals the capacitor subplant is modeled by the dynamical matrix equation

$$\underbrace{\begin{bmatrix}\tilde{v}_{c,1}\\ \tilde{v}_{c,2}\\ \vdots\\ \tilde{v}_{c,M}\end{bmatrix}}_{[\tilde{v}_c]\in\mathbb{R}^M} = \underbrace{\begin{bmatrix}\frac{I_L}{C_1} & 0 & \cdots & 0\\ 0 & \frac{I_L}{C_2} & \ddots & 0\\ \vdots & \vdots & \ddots & \vdots\\ 0 & 0 & \cdots & \frac{I_L}{C_M}\end{bmatrix}}_{[G_{p,v_c}]\in\mathbb{R}^{M\times M}} \underbrace{\begin{bmatrix}\Delta\tilde{d}_1\\ \Delta\tilde{d}_2\\ \vdots\\ \Delta\tilde{d}_M\end{bmatrix}}_{[\Delta\tilde{d}]\in\mathbb{R}^M} \tag{11}$$

where the difference variables Δd_k are defined as

$$\Delta d_k := d_{k+1} - d_k. \tag{12}$$

The inductor subplant is modeled by

$$\dot{\tilde{i}}_L = \underbrace{\begin{bmatrix}\frac{V_{c,1}}{L} & \frac{V_{c,2}-V_{c,1}}{L} & \cdots & \frac{v_{\text{in}}-V_{c,M}}{L}\end{bmatrix}}_{[G_{p,i_L}]\in\mathbb{R}^{1\times n_c}} \underbrace{\begin{bmatrix}\tilde{d}_1\\ \vdots\\ \tilde{d}_{n_c}\end{bmatrix}}_{[\tilde{d}]\in\mathbb{R}^{n_c}} - \frac{\tilde{v}_o}{L} \tag{13}$$

Each subplant responds to a different characteristic of the system inputs. The flying capacitor voltage dynamics are dependent on the differences of neighboring duty ratios, Δd_k, shown in Fig. 3 as the output of a difference operator Δ. The inductor current responds to a weighted sum of duty ratios.

A key observation motivates the controller presented in this work: a common offset applied to all duty ratios does not affect the capacitor voltage dynamics. This common offset—henceforth referred to as the *common mode* duty ratio—is always rejected by the capacitor subplant, as it is eliminated by the differences of duty ratios in (11). The following decomposition illustrates this point. Let

$$\begin{aligned}\tilde{d}_1 &= \tilde{d}_{\text{CM}} + \tilde{d}_{\text{DM},1}\\ \tilde{d}_2 &= \tilde{d}_{\text{CM}} + \tilde{d}_{\text{DM},2}\\ &\vdots\\ \tilde{d}_{n_c} &= \tilde{d}_{\text{CM}} + \tilde{d}_{\text{DM},n_c}\end{aligned} \tag{14}$$

where d_{CM} is the common mode (offset) variable, and $d_{\text{DM},k}$ indicates a *differential mode* variation added to it. Clearly

$$\begin{aligned}\Delta\tilde{d}_1 &= \tilde{d}_2 - \tilde{d}_1 = \tilde{d}_{\text{DM},2} - \tilde{d}_{\text{DM},1}\\ \Delta\tilde{d}_2 &= \tilde{d}_3 - \tilde{d}_2 = \tilde{d}_{\text{DM},3} - \tilde{d}_{\text{DM},2}\\ &\vdots\\ \Delta\tilde{d}_M &= \tilde{d}_{n_c} - \tilde{d}_{n_c-1} = \tilde{d}_{\text{DM},n_c} - \tilde{d}_{\text{DM},n_c-1}.\end{aligned} \tag{15}$$

Thus, the controller in this work uses the common mode duty ratio to control current and the differential mode duty ratios to regulate the capacitor voltages. The common mode duty ratio is a sensible choice for controlling the inductor current as it does not affect the capacitor voltages. At the same time, the balancing controller determines the differences of duty ratios Δd_k that should be applied to steer capacitor voltages. The differential mode duty ratios can be constructed from these difference variables recursively, as will be discussed in Section III. In this approach, both the capacitor balancing and output regulation objectives can be achieved independently.

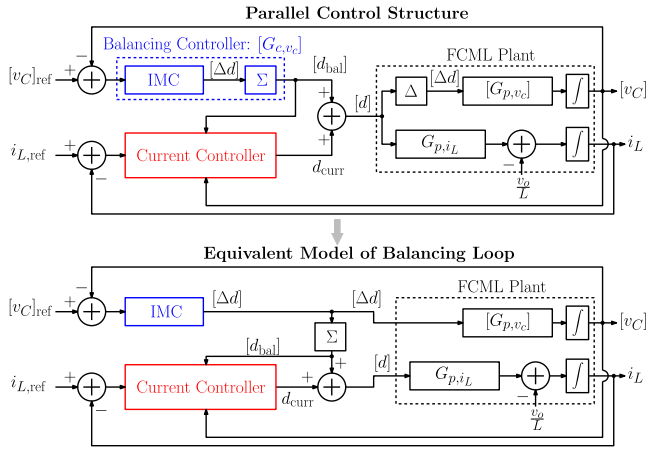

Fig. 4. Parallel control structure presented in this work and an equivalent model of the controller. The flying capacitor plant naturally rejects the common duty ratio term d_{curr} applied to all switches, as shown in the equivalent model.

One aspect of the control structure demands further study—from the perspective of the current controller, the difference variables set by the balancing controller add to the current control action as a disturbance. This disturbance will be studied and compensated in the design of the current controller.

III. Parallel Controller Structure

This work presents a control structure where a separate balancing and current controller operate in parallel and their outputs are summed. The balancing controller comprises an internal model controller (IMC) that sets differences of duty ratios Δd_k to balance each flying capacitor with a designed closed-loop bandwidth. Differences of neighboring duty ratios are summed to obtain a vector of the balancing contributions to each duty ratio, $[d_{\text{bal}}] = [d_{\text{bal},1}, \ldots, d_{\text{bal},n_c}]^{\text{T}}$. The current controller sets a scalar value d_{curr} applied equally to every duty ratio. Thus, the current controller computes the common mode duty ratio $d_{\text{CM}} = d_{\text{curr}}$ and the balancing controller computes the differential mode duty ratios $[d_{\text{bal}}] = [d_{\text{DM},1}, \ldots, d_{\text{DM},n_c}] = [d_{\text{DM}}]$. The net control action is $[d] = [d_{\text{bal}}] + d_{\text{curr}}$.

The proposed *parallel controller* is shown in Fig. 4. The Σ block in the balancing controller and the Δ block in the capacitor voltage path of the plant represent sum and difference operations on neighboring duty ratios, respectively. The common mode duty ratio computed for current control, $d_{\text{CM}} = d_{\text{curr}}$, is rejected by the capacitor subplant, so the closed-loop system can be represented by an equivalent model, also shown in Fig. 4. By contrast, the differential mode duty ratios computed for balancing, $[d_{\text{DM}}] = [d_{\text{bal}}]$, are not rejected by the inductor subplant, so the current controller must be designed to reject disturbances injected by the balancing controller.

A. Balancing Controller

Recalling that the small-signal capacitor subplant is a MIMO system that is already represented by decoupled integrators, the balancing controller should be designed such that the capacitor

dynamics remain decoupled in the closed-loop system. This ensures that the control action taken to steer one flying capacitor voltage does not disturb the others.

The principle of internal model control [25] is used to ensure this decoupling. In general, if the matrix description of a system is square and invertible, an IMC is designed by multiplying the inverse of the plant model by a diagonal system consisting of integrators. Application of the IMC design procedure detailed in [25] to the capacitor subplant in (11) results in a diagonal-matrix proportional controller where the bandwidths of the channels can be set independently via each channel's proportional gain. This controller is given by

$$[G_{\text{IMC}}] = \begin{bmatrix} \omega_1 \frac{C_1}{I_L} & 0 & \cdots & 0 \\ 0 & \omega_2 \frac{C_2}{I_L} & \ddots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & \omega_M \frac{C_M}{I_L} \end{bmatrix} \tag{16}$$

where ω_k is the designed bandwidth for capacitor k. The corresponding loop transfer matrix, obtained via the Laplace transform, is diagonal with integrator elements and given by

$$[L_{v_c}] = \begin{bmatrix} \frac{\omega_1}{s} & 0 & \cdots & 0 \\ 0 & \frac{\omega_2}{s} & \ddots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & \frac{\omega_M}{s} \end{bmatrix}. \tag{17}$$

The difference variables $[\Delta d]$ computed by the IMC must somehow be applied to the n_c differential mode duty ratios $[d_{\text{DM}}]$ such that the balancing actions for flying capacitors do not interfere with each other. Since there is one more control variable compared to the number of capacitors ($M = n_c - 1$) $d_{\text{bal},1} = 0$ is chosen, as it does not disturb the current control action. With the value for $d_{\text{bal},1}$ fixed, the balancing controller action $[d_{\text{bal}}]$ may be computed via back-substitution, which is computationally efficient and readily implemented in digital signal processors (DSPs). The small-signal balancing controller is given by

$$\underbrace{\begin{bmatrix} \tilde{d}_{\text{bal},1} \\ \tilde{d}_{\text{bal},2} \\ \vdots \\ \tilde{d}_{\text{bal},n_c-1} \\ \tilde{d}_{\text{bal},n_c} \end{bmatrix}}_{[\tilde{d}_{\text{bal}}] \in \mathbb{R}^{n_c}} = \underbrace{\begin{bmatrix} 0 & 0 & 0 & \cdots & 0 \\ \frac{\omega_1 C_1}{I_L} & 0 & 0 & \cdots & 0 \\ \frac{\omega_1 C_1}{I_L} & \frac{\omega_2 C_2}{I_L} & 0 & \cdots & 0 \\ \vdots & \vdots & \ddots & \ddots & \vdots \\ \frac{\omega_1 C_1}{I_L} & \frac{\omega_2 C_2}{I_L} & \frac{\omega_3 C_3}{I_L} & \cdots & \frac{\omega_M C_M}{I_L} \end{bmatrix}}_{[G_{c,v_c}] \in \mathbb{R}^{n_c \times M}} \underbrace{\begin{bmatrix} \tilde{e}_{v_{c,1}} \\ \tilde{e}_{v_{c,2}} \\ \vdots \\ \vdots \\ \tilde{e}_{v_{c,M}} \end{bmatrix}}_{[\tilde{e}_{v_c}] \in \mathbb{R}^{M}} \tag{18}$$

where the small-signal feedback error $[\tilde{e}_{v_c}]$ is

$$\begin{bmatrix} \tilde{e}_{v_{c,1}} \\ \tilde{e}_{v_{c,2}} \\ \vdots \\ \tilde{e}_{v_{c,M}} \end{bmatrix} = \begin{bmatrix} \tilde{v}_{c,1_{\text{ref}}} - \tilde{v}_{c,1} \\ \tilde{v}_{c,2_{\text{ref}}} - \tilde{v}_{c,2} \\ \vdots \\ \tilde{v}_{c,M_{\text{ref}}} - \tilde{v}_{c,M} \end{bmatrix}. \tag{19}$$

To illustrate the active balancing control action, a scenario with imbalanced capacitor voltages is shown in Fig. 5 over the timescale of a switching period T_{pwm}. Note the underlying

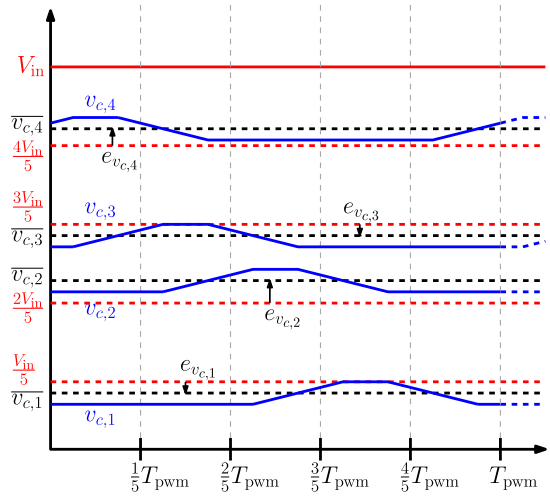

Fig. 5. Example imbalanced capacitor voltages, shown in a timescale of one switching period. The reference capacitor voltages are respective nominal fractions of the input voltage, $\frac{k}{n_c}V_{\text{in}}$, shown as red lines. The signed errors associated with imbalanced voltages are indicated by arrows.

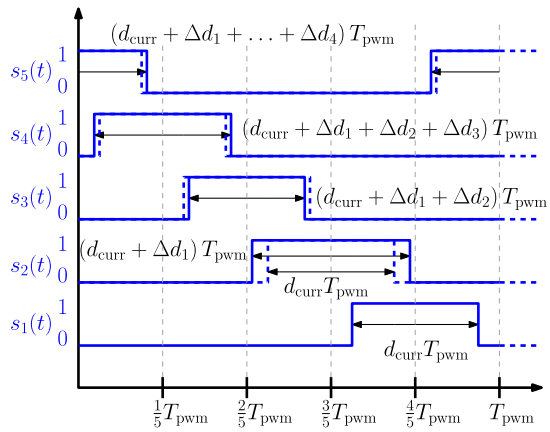

Fig. 6. Example duty ratios applied to each switch resulting from simultaneous current control and active balancing actions. The balancing actions appear as difference duty ratios Δd_k, applied recursively to each switch beginning with $d_1 = d_{\text{curr}}$. The pulse-width corresponding to the common-mode duty ratio d_{curr} is shown via dashed lines.

assumptions in this work: the average flying capacitor voltages vary slowly relative to the switching period, and the capacitor voltage ripples are small with respect to their average values. The errors associated with each flying capacitor voltage are indicated by arrows, where the reference values are the nominal fractions of the supply voltage V_{in}, indicated by the red lines. Fig. 6 shows the corresponding control action to steer these example capacitor voltage errors to zero. The difference variables Δd_k are applied recursively to each switching signal beginning with $d_1 = d_{\text{curr}}$.

In implementation, the balancing controller in (18) may be adapted to remove the quiescent-point dependence on I_L. In the prototype implemented in this work and demonstrated in Section IV, the denominator terms I_L are replaced with the current reference $I_{L,\text{ref}}$ to eliminate the dependence of the active balancing closed-loop bandwidth on the load current. In practice, the flying capacitor values can be expected to vary with dc

bias, temperature, and over lifetime. Thus, for a conservative design, the capacitance values in the control law of (18) may be chosen as the worst-case (smallest) capacitance expected due to derating. Further adaptive measures may be considered to remove the controller's dependence on converter parameters. For example, in converters incorporating Class II dielectrics for the flying capacitors, the capacitance values will change dramatically as a nonlinear function of the supply voltage. If the supply voltage is expected to have large-signal variations, the capacitance terms in (18) may be updated dynamically with a modeled voltage-controlled capacitance characteristic.

B. Current Controller

From inspection of (13), the inductor current dynamics clearly respond to a linear combination of the duty ratios, and the balancing controller action $[d_{\text{bal}}]$ couples into the current loop as a disturbance. To reject this disturbance and ensure high-bandwidth performance independent of the operating point, the current controller is designed via application of feedback linearization [24] to the nonlinear average current dynamics. Unlike a controller derived from the small-signal model, the proposed nonlinear current controller can reject the balancing disturbance effectively for large-signal variations in the capacitor voltages.

With the substitution $d_k = d_{\text{bal},k} + d_{\text{curr}}$, the dynamical system given by (6) can be re-expressed as

$$L\dot{\overline{i_L}} = \overline{v_{\text{in}}} d_{\text{curr}} + \alpha - \overline{v_o} \tag{20}$$

where

$$\alpha = \overline{v_{c,1}} d_{\text{bal},1} + \left(\overline{v_{c,2}} - \overline{v_{c,1}}\right) d_{\text{bal},2} + \cdots + \left(\overline{v_{\text{in}}} - \overline{v_{c,M}}\right) d_{\text{bal},n_c}. \tag{21}$$

The corresponding state feedback control law

$$d_{\text{curr}} = \frac{1}{\overline{v_{\text{in}}}} u - \frac{\alpha - \overline{v_o}}{\overline{v_{\text{in}}}} \tag{22}$$

linearizes the response of $\overline{i_L}$ with respect to a new input u. This input is then set by the feedback controller, yielding the full current control law

$$d_{\text{curr}} = \frac{1}{v_{\text{in}}} \left(K_p e_{i_L} + K_i \int_{-\infty}^{t} e_{i_L} d\tau \right) - \frac{\alpha - v_o}{v_{\text{in}}} \tag{23}$$

where

$$e_{i_L} = i_{L_{\text{ref}}} - i_L. \tag{24}$$

The balancing control actions appear as disturbances to the current controller, as evident in (20). To ensure that these disturbances are rejected effectively in practice considering delays and errors in sampling the capacitor voltages, the current controller should be designed for significantly higher bandwidth compared to the balancing controller. The combined balancing and current control action for any one duty ratio is constrained to the range [0,1]. Referring to (18), if any balancing control action $d_{\text{bal},k}$ saturates to 1, the capacitor dynamics become re-coupled and subsequent balancing actions $d_{\text{bal},k+1}, \ldots, d_{\text{bal},n_c}$ cannot compensate for positive error. Saturating the differences of duty ratios based on the current control action avoids this scenario. For example, if the saturation constraint $d_{\text{curr}} \leq 0.95$ is imposed for a six-level FCML converter, the constraint on balancing controller actions $\Delta d_k = \frac{\omega_{\text{bal}} C_k}{I_L} e_{v_{c,k}} \leq 0.01$ avoids saturation of any duty ratio.

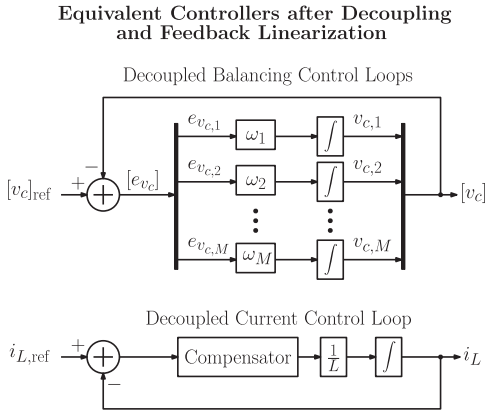

Fig. 7. Equivalent closed-loop system after feedback linearization of the current dynamics. To ensure the balancing disturbance is rejected in practice, the current controller bandwidth should be chosen to be significantly higher than the balancing control bandwidth.

Furthermore, saturation of the balancing control action prevents excessive disturbance of the inductor current during a line transient, so a tradeoff arises between balancing performance and current regulation. The worst-case expected capacitor voltage error can be used to define the balancing controller saturation limits. As an example, for a six-level FCML converter operating at $V_{\text{in}} = 100$ V, $\omega_{\text{bal}} = 2\pi \cdot 300$ rad/s, $I_L = 10$ A, and $C = 8.8$ μF, with worst-case expected error of 5 V, the maximum difference of duty ratios Δd_k used to control the capacitor voltage is $\Delta d_{k,\max} = \frac{\omega_{\text{bal}} C_k}{I_L} e_{v_{c,k}} = 0.008$. If the saturation limit is chosen to be more restrictive than this value, the balancing controller will saturate for lower capacitor errors when the converter is operating under the conditions specified. Note that if the operating point changes but the saturation limits are kept constant, the controller will saturate at a different value of the capacitor voltage error.

A PI compensator for the feedback control element u is chosen in this work to eliminate steady-state error for dc load current references, but the design of the current loop feedback compensator is arbitrary in general. Depending on the converter application and the expected forms of current references, the feedback terms in (23) can easily be replaced by other structures that offer improved performance.

The ideal decoupled balancing and current control loops resulting from feedback linearization of the current dynamics are shown in Fig. 7. As the proposed parallel controller takes into account the proper MIMO plant structure in order to realize a decoupled response in the averaged sense, it is simultaneously capable of high-bandwidth balancing and current control. By contrast, in [12] and [13], where the control laws are derived from qualitative reasoning, the resulting closed-loop system exhibits coupling between different flying capacitors due to improper controller structure. The corresponding coupled structure, combined with the uncompensated impact of the balancing

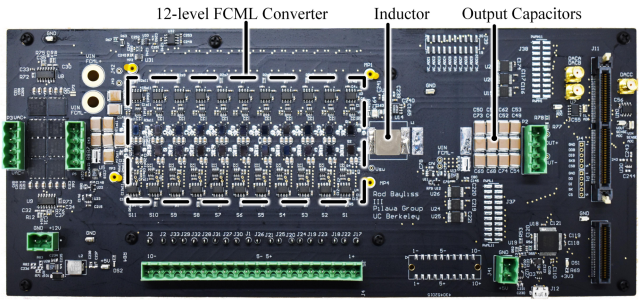

Fig. 8. 12-level FCML converter prototype used in this work. $L = 10\,\mu$H, $C_k = 8.8\,\mu$F, $f_{\text{pwm}} = 100$ kHz. The parallel controller is implemented on a Texas Instruments TMS320F28379D DSP. The hardware is reconfigured as a six-level FCML converter by shorting input-side switch pairs.

control on the inductor current, force the implementations in those works to be low-bandwidth.

The structure of the control laws presented in (18) and (23) are equivalent at the quiescent point to the MIMO controller derived in [21] further confirming the parallel controller properly decouples the capacitor voltages and inductor current. Unlike the controller in [21], which is derived directly from the MIMO representation of the averaged plant, the controller proposed in this work is derived from inspection of the small-signal plant structure. The capacitor voltages and inductor current are identified as separate decoupled plants, motivating the design of separate feedback loops that operate in parallel. This parallel implementation offers practical benefits—the coupling of control loops arising from practical nonlinearities such as duty cycle saturations is simpler to model and more easily addressed in the controller decoupling terms. Depending on the application, additional feedback or feedforward compensation terms can be readily incorporated into the parallel control loops. The closed-loop system modeled in this work may serve as the basis for future study into the impacts of sampling delays, measurement offset, noise propagation, and state estimator dynamics. In addition, the parallel control structure also serves as a foundation for balancing implementations where the capacitor voltages and inductor current are controlled at different rates. In practice, as verified in the experimental results in Section IV, the proposed controller can also be gain-scheduled to ensure high-bandwidth performance across a wide operating range.

To ensure the balancing action is rejected despite nonidealities such as control delays, capacitor voltage measurement error, and unmodeled plant dynamics, the bandwidth of the current controller must be significantly higher than the bandwidth of the balancing controller. The maximum balancing bandwidth that can be designed while maintaining closed-loop stability is explored in Section V, and is shown to be dependent on the load current.

IV. Experimental Results

A 12-level FCML converter hardware prototype, shown in Fig. 8 is constructed to verify the proposed parallel controller. Key component details and part numbers are given in Table I. The hardware is configured as a six-level FCML converter by shorting switch pairs on the input side. In this work, the flying capacitor voltages are measured directly using M on-board differential voltage sensors, however a capacitor voltage estimator, such as the one presented in [26] could be considered to simplify the hardware design and reduce cost. The inductor current is measured through a shunt resistor and amplifier circuit. To validate its practical utility, the parallel controller is implemented on a Texas Instruments TMS320F28379D DSP. The proposed implementation is similar in cost and complexity to [20] which relies on direct capacitor voltage sensing and TMS320x DSP implementation. Farivar et al. [13] present an implementation with a single sensor reducing component count, but the controller is implemented on expensive DSPACE FPGA hardware and its structure does not offer a decoupled response. The method presented in the work in [19] is only developed for three-level converters, and is not cost-effective for DSP implementation as it requires high-speed computation and positioning of switching edges. In this work, the controller is implemented on a single core of the DSP with single-sampled single-update PS-PWM [27]. The control law calculation for both the current controller and active balancing controller is timed in experiments and runs in approximately $7.5\,\mu$s. Thus, the proposed parallel controller can be executed once per switching period with $f_{\text{pwm}} = 100$ kHz.

TABLE I
Component Details

Component	Description	Part name
S_{1-5A}, S_{1-5B}	100 V, 1.8 mΩ GaN-FET	EPC2302
C_{1-4}	$4 \times 2.2\,\mu$F, X6S, 450V	C5750X6S2W225K250KA
C_o	$20 \times 2.2\,\mu$F, X6S, 450V	C5750X6S2W225K250KA
L	$10\,\mu$H	IHLP5050CEER100M01
Gate driver	5 V, 7.6 A / 1.3 A	LM5114
Isolator	Power and signal	ADUM5240
Cap. voltage sensor	Instrumentation amplifier	AD8429ARZ-R7
Current sensor	Current sense amplifier	LT1999IMS8-20

Three experiments—a supply transient measurement, a measurement of the converter response to periodic perturbation of the supply voltage, and a load transient measurement—are conducted to compare the performance of an FCML converter relying on natural balancing to one implementing the proposed parallel controller. The experiments verify that capacitor voltage tracking is significantly improved with active balancing for fast variations in the line voltage. In this work, a stiff output voltage generated by a large bulk output capacitance is used to simplify the current controller design, as the output voltage dynamics are not of interest. This setup is representative of an FCML converter feeding a stiff bus, as in the case of a rectifier in an electric vehicle onboard charger or first-stage dc/dc converter in a datacenter setting.

A. Supply Voltage Transient Response

The first experiment compares balancing responses for a damped-step transient in the supply voltage. The desired capacitor voltages—corresponding to nominal fractions of the input voltage—are overlaid as reference values alongside the measured results. A current controller designed for 10 kHz

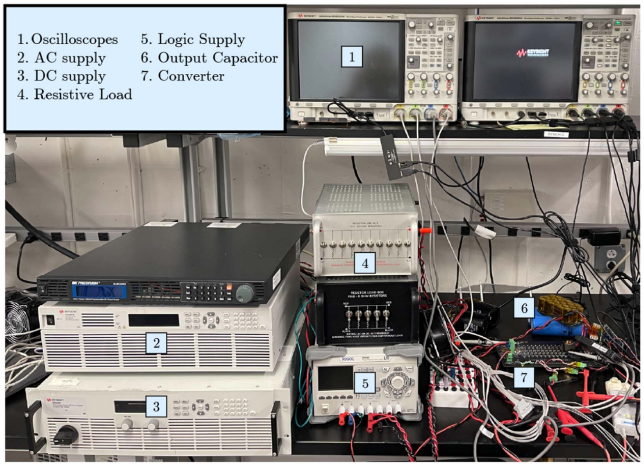

Fig. 9. Experimental setup used to characterize the proposed active balancing controller on the FCML converter prototype, with equipment annotated.

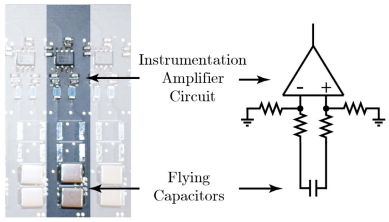

Fig. 10. Instrumentation amplifier circuit designed to measure flying capacitor voltages. The single-ended output of the circuit is interfaced to the analog-to-digital converter on the F28379D DSP.

control bandwidth regulates the output current to 3 A during an input voltage transient from 50 to 90 V. As seen in Fig. 11, when the controller relies on natural balancing, the flying capacitor voltages exhibit oscillations, which introduce unequal voltage stress across the switches in the converter. Capacitor voltage oscillations also couple into the current response in the form of increased harmonic content and peak-to-peak ripple. In contrast, active balancing designed for 600 Hz control bandwidth significantly improves voltage tracking, as seen in Fig. 12, and the inductor current is significantly less disturbed, exhibiting approximately 50% lower peak deviation during the balancing transient.

B. Periodic Supply Voltage Perturbation

The second experiment shows the improved voltage tracking with active balancing when the converter is subjected to large-signal periodic input voltage perturbations similar to the twice-line-frequency variations present in converters fed by a rectified single-phase ac supply [9]. A current controller with 10 kHz control bandwidth regulates the output current to 2 A during the periodic perturbation. Fig. 13 illustrates that the capacitor voltage tracking is poor when the system relies entirely on natural balancing, as the natural dynamics are too slow for capacitor voltages to track fast variations in the input voltage.

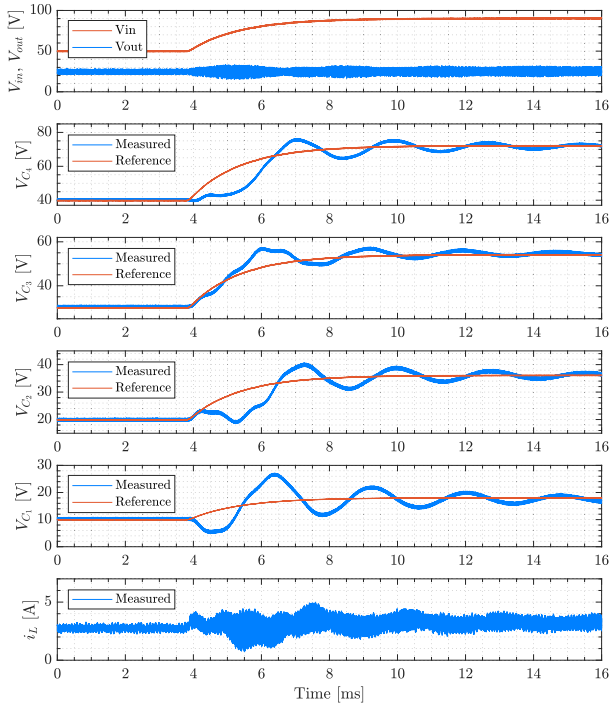

Fig. 11. Measured capacitor voltage and current response of a current-controlled converter relying on natural balancing when supply voltage is changed from 50 to 90 V. The capacitor voltages exhibit underdamped dynamics, resulting in unequal switch voltage stress. The current control bandwidth is set to 10 kHz, and the current reference $i_{L,\text{ref}} = 3$ A.

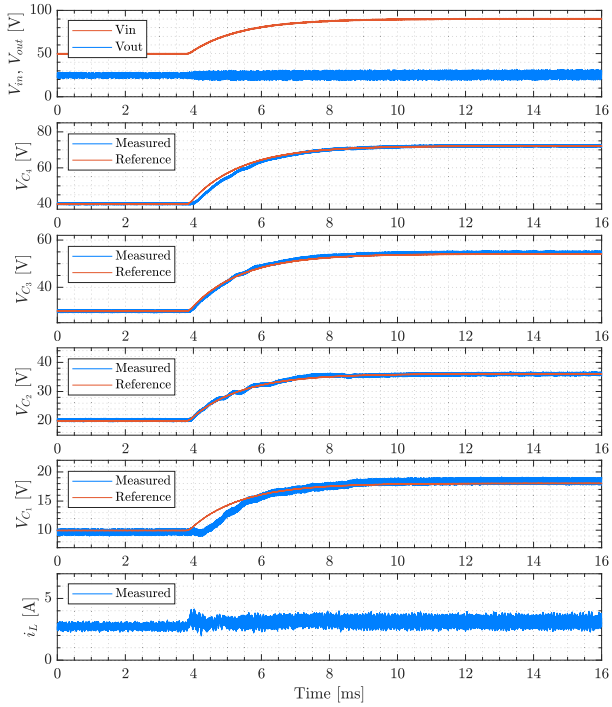

Fig. 12. Measured response of a converter implementing the proposed parallel active balancing controller when the supply voltage is changed from 50 to 90 V. The capacitor voltages track the reference values with negligible error compared to the natural balancing case. The current control bandwidth is set to 10 kHz, the flying capacitor active balancing control bandwidth is set to 600 Hz for each flying capacitor, and the current reference $i_{L,\text{ref}} = 3$ A.

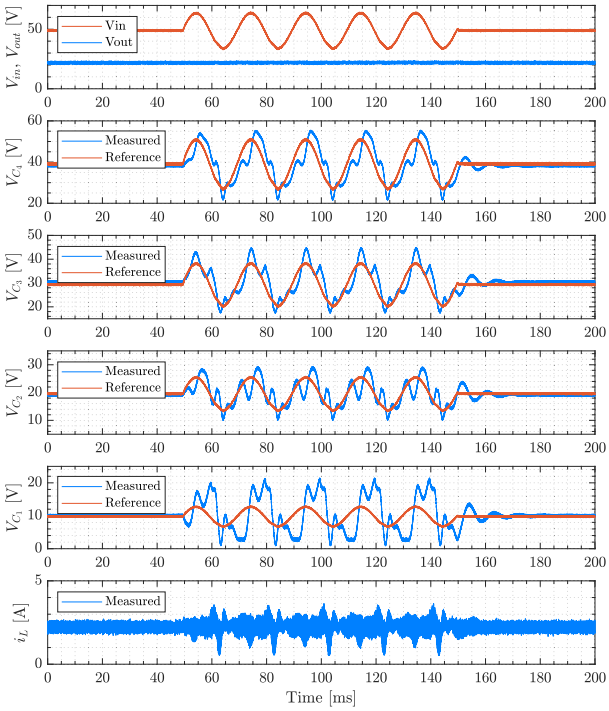

Fig. 13. Measured response of a current-controlled converter relying on natural balancing when a 50 Hz, 10 V_{RMS} ac perturbation is applied to the supply voltage. The capacitor voltages do not track their respective reference values as the natural balancing dynamics are not sufficiently fast. The current control bandwidth is set to 10 kHz, and the current reference $i_{L,\text{ref}} = 2$ A.

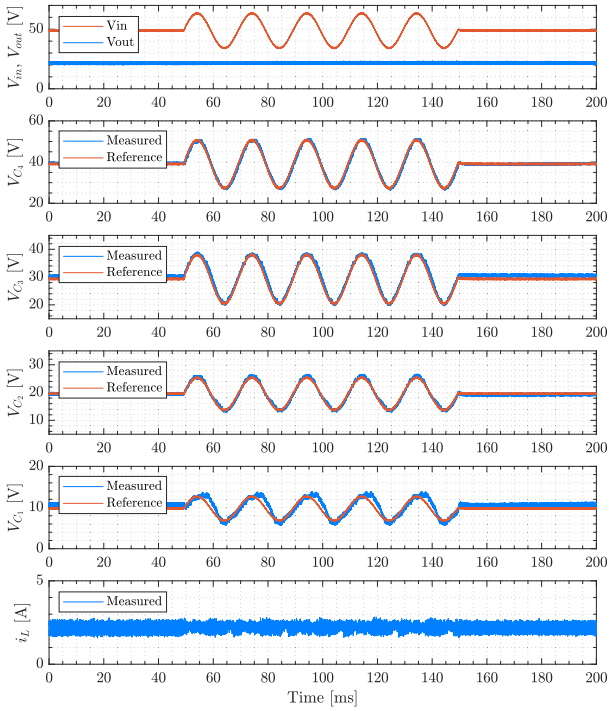

Fig. 14. Measured response of a converter implementing the proposed parallel active balancing controller when a 50 Hz, 10 V_{RMS} ac perturbation is applied to the supply voltage. The capacitor voltage tracking is significantly improved and the disturbance to the inductor current is reduced. The current control bandwidth is set to 10 kHz, the flying capacitor active balancing control bandwidth is set to 300 Hz for each flying capacitor, and the current reference $i_{L,\text{ref}} = 2$ A.

This finding is consistent with open-loop audiosusceptibility characterizations in [28]. Active balancing once again significantly improves voltage tracking, shown in Fig. 14. Here the specified balancing bandwidth is 300 Hz for all capacitors.

With active balancing, the maximum observed device voltage stress V_{ds} over the perturbation period decreases as a consequence of better capacitor voltage tracking. The maximum stress observed in the natural and active balancing cases is measured and characterized in Fig. 15 as a function of the supply perturbation frequency. The maximum measured voltage stress is normalized to the maximum stress expected at the peaks of the input perturbations to obtain a normalized stress metric defined in this work as

$$\max V_{\text{ds,norm}} := \frac{\max V_{\text{ds}}}{\max \frac{v_{\text{in}}}{n_c}}. \tag{25}$$

Two different active balancing bandwidths are studied and compared to the natural balancing case. For both active balancing designs, with perturbation frequencies within the controller bandwidths, the maximum observed device voltage stress is consistently smaller compared to the design relying on natural balancing. In the frequency ranges studied, the higher bandwidth active balancing design enables higher fidelity tracking of capacitor voltages, yielding the lowest normalized stress. The lower normalized stress with active balancing control indicates that in general, switching devices in FCML converters employing active balancing do not need to be significantly overrated relative

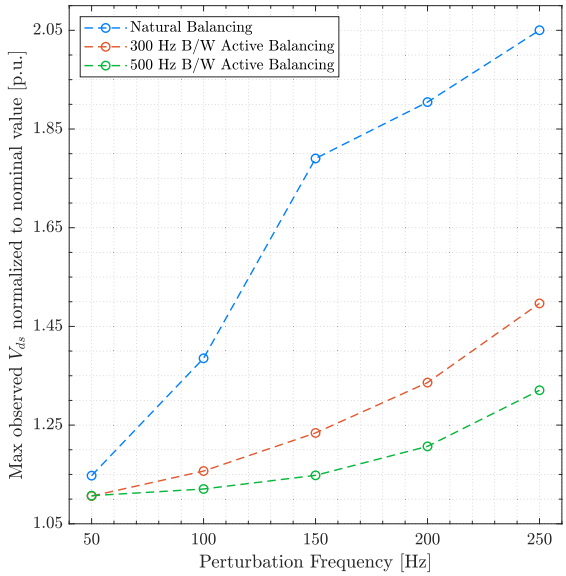

Fig. 15. Maximum measured device voltage stress V_{ds} and normalized stress given by (25), plotted against the supply perturbation frequency for a current-controlled converter relying on natural versus active balancing. A 10 V_{RMS} perturbation is applied on top of a nominal 50 V dc supply voltage. The current control bandwidth is set to 5 kHz and two different active balancing control bandwidths are studied, 300 and 500 Hz. The device voltage stress is consistently lower under active balancing.

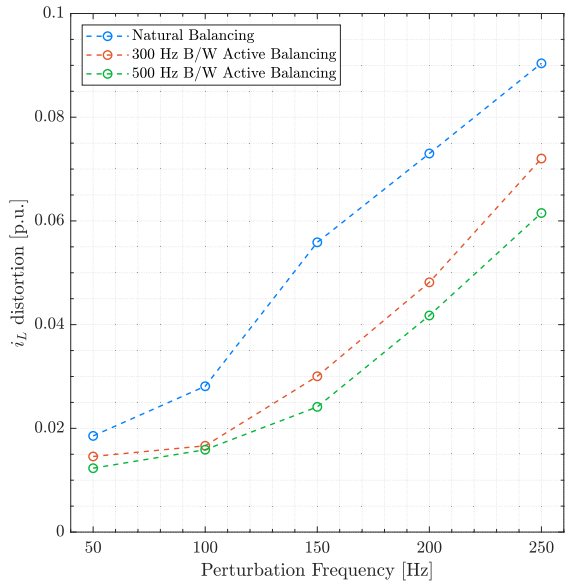

Fig. 16. Measured current distortion given by (26), plotted against the supply perturbation for a current-controlled converter relying on natural versus active balancing. A 10 V_{RMS} perturbation is applied on top of a nominal 50 V dc supply voltage. The current control bandwidth is set to 5 kHz. Under active balancing, the current distortion is consistently lower, indicating better decoupling of the capacitor voltages and inductor current with active balancing.

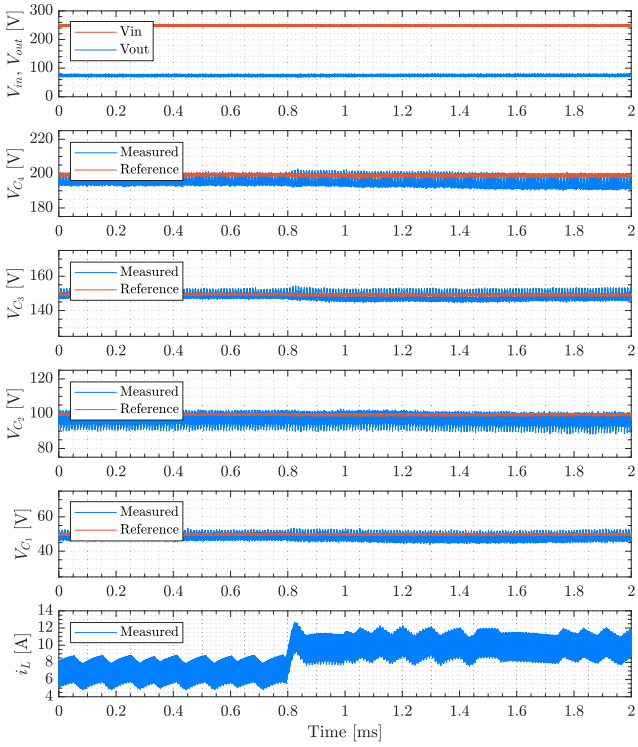

Fig. 17. Measured capacitor voltage and current response during a step change in the current reference i_{ref} from 7 to 10 A at $v_{in} = 250$ V. The current control bandwidth is set to 10 kHz. The flying capacitor voltages are undisturbed during the load current transient, verifying that the capacitor voltages naturally reject the common-mode duty ratio used to control current.

to the nominal blocking voltage stress. The proposed active balancing strategy therefore ensures safe operation of FCML converters designed with low-voltage switches.

Comparing the time-domain responses in Figs. 13 and 14, the inductor current response also improves with active balancing, as the input perturbation and capacitor voltage variations are visibly decoupled from the current ripple. The coupling between the line voltage variation and the inductor current waveform is analyzed via a harmonic distortion metric, defined in this work as

$$k_{\text{dist}} := \frac{\text{RMS}\left(i_L - I_{L,\text{ref}}\right)}{I_{L,\text{DC}}}. \tag{26}$$

This metric quantifies the power of the disturbed inductor current waveform relative to its dc value. This current distortion number is plotted in Fig. 16 as a function of the supply perturbation frequency. As the perturbation frequencies increase, the capacitor voltage tracking degrades, and the harmonic content in the inductor current generally increases due to nonidealities in the implemented feedback linearized current controller. In general, the current distortion is lower with the proposed active balancing controller compared to the current-controlled converter relying on natural balancing, indicating better decoupling in the actively balanced system compared to the naturally balanced one. For converters interfaced to dc buses with low-frequency voltage ripple such as those in single-phase inverter or rectifier systems, lower value of the distortion metric k_{dist} enables more efficient converter operation owing to lower RMS inductor current and consequently lower conduction loss. In ac applications, the reduced harmonic distortion in the inductor current improves power quality compared to the converter relying on natural balancing. This motivates active balancing control even when capacitor voltage deviations do not cause excessive switch voltages.

C. Load Transient Response

The third experiment investigates the load disturbance rejection of the proposed active balancing controller. Fig. 17 illustrates results corresponding to 1 kW peak power operation at 250 V input, with a current control bandwidth of 10 kHz. The common-mode duty ratio varies in response to the changing current reference, but does not visibly disturb the flying capacitor voltages. This experiment illustrates an operating point where the ripple in both the capacitor voltages and inductor current are low relative to their average values. Under these conditions, the averaged model given in (5)–(7) accurately predicts that variations in the common-mode duty ratio do not affect the capacitor voltages. This yields a similar load-transient response under natural balancing, and is not shown in this article for conciseness.

Experimentally measured converter responses to a large step in the current reference from 2 to 15 A are shown in Figs. 18 and 19 for the converter relying on natural balancing and active balancing respectively. In the high-current operating condition where the small-ripple approximation of capacitor voltages used to derive the averaged model is less accurate, the load transient

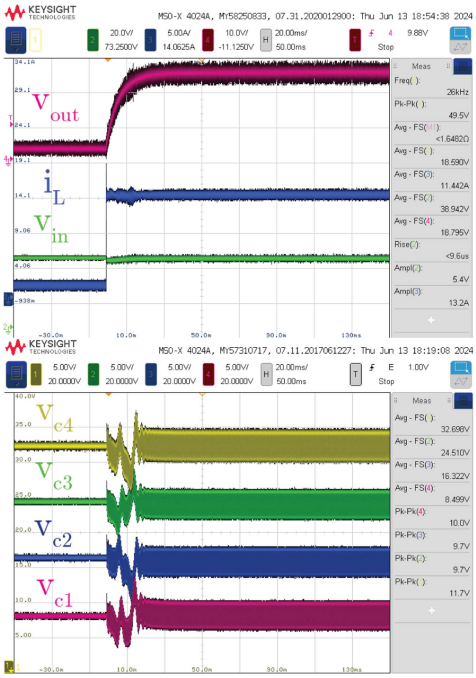

Fig. 18. Measured capacitor voltage response in the current-controlled converter relying on natural balancing during a large step change in the current reference from i_{ref} from 2 to 15 A. The load-transient is tested at $v_{\text{in}} = 40$ V with $L = 4.7\ \mu$H. For large output currents capacitor voltage ripple may significantly increase, affecting the small-signal approximation used to derive the averaged models. Hence, the load transient disturbs the capacitor voltages due to coupling between the voltage ripples and the inductor current. Large-signal nonlinearities not modeled in averaging, such as clamping between neighboring capacitor voltages are also observed.

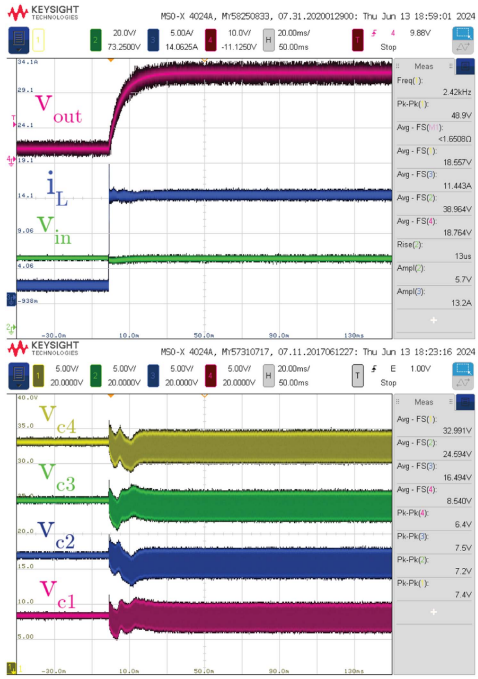

Fig. 19. Measured capacitor voltage response in the current-controlled converter implementing the proposed active balancing controller during a large step change in the current reference from i_{ref} from 2 to 15 A. The load-transient is tested at $v_{\text{in}} = 40$ V with $L = 4.7\ \mu$H. The capacitor voltage response to the load transient is improved with the proposed active balancing controller; however the capacitor voltages are still disturbed due to nonlinear coupling between the capacitor voltage ripple and the average inductor current. At the operating point shown, measurement errors from sampling the capacitor voltage ripple are significant relative to the average capacitor voltages and disturb capacitor voltage regulation during the transient.

disturbs the capacitor voltages due to nonlinear coupling between the capacitor voltage ripples and the average load current. Large-signal nonlinearities that are not captured by averaging such as clamping between neighboring capacitor voltages are also observed. The load transient response is improved with the active balancing controller as demonstrated in Fig. 19, however the average capacitor voltages are still disturbed due to coupling between the capacitor voltage ripples and the average load current. In addition, measurement errors arise from sampling the peaks and valleys of capacitor voltage ripples, which are significant relative to the average capacitor voltages. This measurement error also disturbs capacitor voltage regulation during the transient, further confirming that the accuracy of the proposed averaged converter model decreases as capacitor voltage ripples increase. The limitations of the averaged model are further studied in Section V, where the impact of current ripple on the closed-loop dynamics is experimentally characterized.

V. Characterization of Closed-Loop Performance

As shown in the experimental results in Section IV, the proposed controller enables improved capacitor voltage balancing in current-controlled FCML converters subjected to large signal variation in the input voltage. In the averaged sense (considering the model presented in Section III), the proposed control structure ideally realizes a stable decoupled system for arbitrary selections of capacitor balancing bandwidths and inductor current bandwidth. However in practice, delays in the control loop and the ripple content of the inductor current have significant impact on the small-signal stability of the closed-loop system. Furthermore, these practical considerations result in residual coupling between the balancing control action and the inductor current due to imperfect cancellation by the feedback linearizing control law. This section presents experimental results characterizing the closed-loop small-signal stability with the proposed controller as a function of the converter design and operating point.

The performance limits of the active balancing technique presented in this work may be characterized by the maximum designed balancing bandwidth ω_{bal} that can be chosen before the closed-loop system becomes unstable in the small-signal sense. In this work, small-signal instability corresponds to the capacitor voltages deviating from the dc reference values once the balancing controller is enabled. For small-signal-unstable designs, the nonlinearities of the closed-loop system typically cause capacitor voltages to exhibit steady-state limit cycle oscillations or saturated values depending on the operating point and controller parameters. For the purposes of evaluating closed-loop performance of the active balancing controller, this

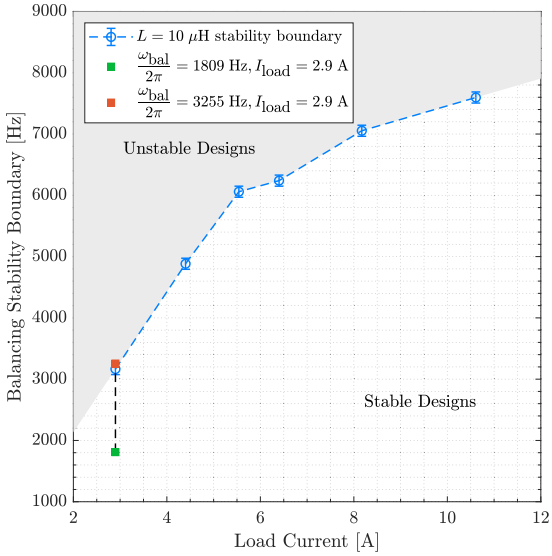

Fig. 20. Measured closed-loop stability boundary for the converter in Section IV with 10 μH filter inductance, 100 kHz switching frequency, 5 kHz designed current control bandwidth, and 80 V dc supply voltage. The maximum designed balancing bandwidth resulting in a stable system is plotted in blue as a function of the load current. Two points shown in green and red indicate examples of stable and unstable designs respectively, as shown in the time domain responses of Fig. 21. The error bars indicate tolerance arising from visual identification of the stability boundary.

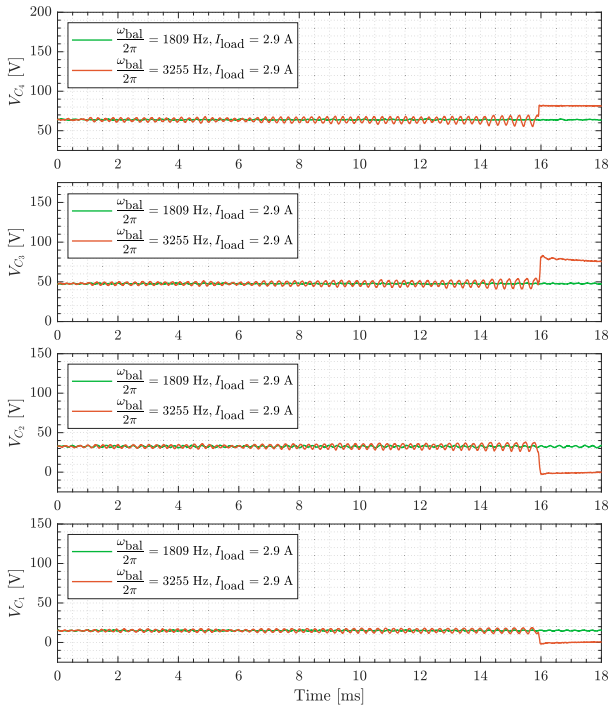

Fig. 21. Measured capacitor voltage responses for a stable design and unstable design at light load, indicated by the green and red plots, respectively. Unstable designs, resulting from large balancing gains, are characterized by exponentially growing time domain responses that either settle in limit cycle oscillations or, as in the case here, cause capacitor voltages to saturate.

large-signal behavior is regarded as unstable, since large deviations of capacitor voltages from the nominal balanced values results in excessive switch voltage stress.

Fig. 20 shows the experimentally measured maximum stable bandwidth as a function of the load current for the six-level converter with 10 μH filter inductance. For each load current condition, the balancing bandwidth is incremented in 100 Hz steps until the capacitor response becomes unstable. The stability boundary, indicated by the blue markers in Fig. 20, is defined as the designed balancing bandwidth for which measured oscillation amplitudes of any capacitor voltage grow to greater than one fourth the nominal switch blocking voltage $\frac{V_{in}}{n_c}$. The error bars in Fig. 20 indicate the 100 Hz resolution of the stability boundary characterization arising from the fixed step size. Note that the curve shown characterizes the system stability boundary and should not be interpreted as a reference design.

At low currents, the maximum stable bandwidth is significantly reduced compared to its value at greater loads. This suggests that a fixed balancing bandwidth that yields stable closed-loop operation at a given load current may not necessarily do so at lighter loads. Fig. 21 illustrates light-load measurements of the capacitor voltages over time for stable and unstable designs indicated by the green and red plots respectively. The time-axis is adjusted such that time $t = 0$ corresponds to the instant when the active balancing controller is enabled. For balancing bandwidths above the stability boundary, capacitor voltages are characterized by an oscillatory response with a growing amplitude that eventually saturate due to limits on the duty cycle applied and body-diode-induced clamping between neighboring capacitor voltages.

The load-dependence of the stability of the closed-loop system is not predicted by the averaged models used in this work. It is the result of the dynamics not modeled by the averaging procedure, namely the ripple content of the state variables [5], [6], [29], [30], [31]. To verify that the inductor current ripple is a primary contributor to the stability of the system for a designed balancing bandwidth, the stability boundary is recharacterized for a six-level converter with a smaller inductance and consequently larger current ripple. Fig. 22 shows this maximum stable bandwidth as a function of the load current for the six-level converter with 3.3 μH filter inductance, and Fig. 23 shows corresponding time domain measurements at light load. For a converter designed to have higher current ripple, the maximum stable bandwidth ω_{bal} for a given load current is consistently lower. This verifies that the inductor current ripple, unmodeled in the design process for the controller proposed in this work, impacts the stability of the closed-loop system.

The block diagram in Fig. 24 depicts how the plant modeling error generally affects the plant dynamics. Noting the high performance of the active balancing controller compared to the naturally balanced approach evident in the experimental results in Section IV, it is clear the unmodeled dynamics can be disregarded at heavy-load, but are nonnegligible at lighter loads. Furthermore, according to the natural balancing studies in [5], [6], and [7], the ripple content in the inductor has significant impact on the natural balancing dynamics. Since the ripple is purposefully ignored in the averaged modeling approach, the impact of the inductor current ripple is captured

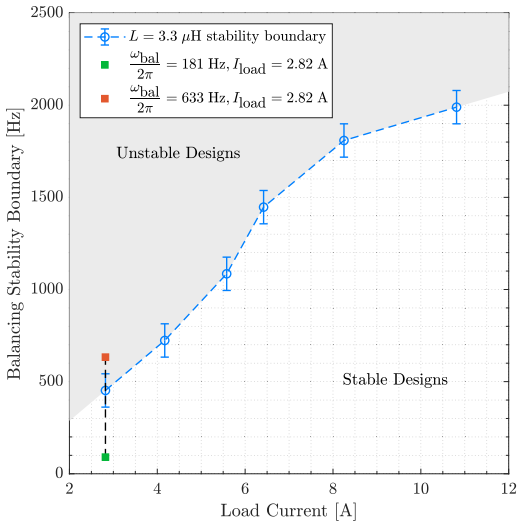

Fig. 22. Measured closed-loop stability boundary for the converter in Section IV with 3.3 μH filter inductance, 100 kHz switching frequency, 5 kHz designed current control bandwidth, and 80 V dc supply voltage. Two points shown in green and red indicate examples of stable and unstable designs respectively, as shown in the time domain responses of Fig. 23. Compared to the 10 μH inductance design, the stability boundary occurs at lower frequencies, implying the converter with a smaller filter inductor must be designed with a lower balancing bandwidth to remain stable.

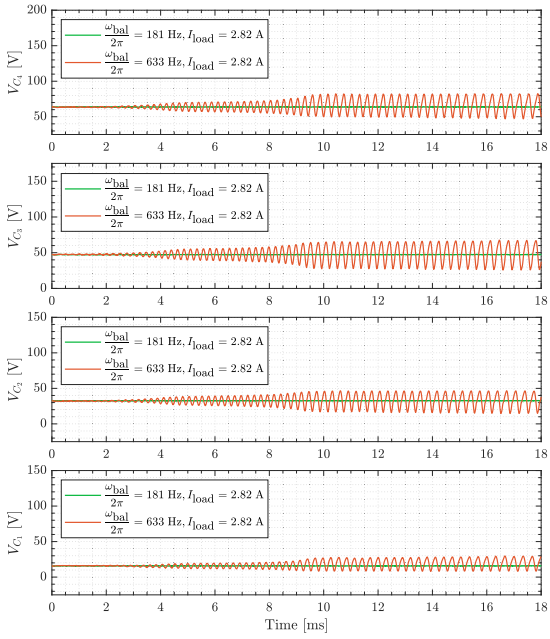

Fig. 23. Measured capacitor voltage responses for a stable design and unstable design at light load, indicated by the green and red plots respectively. Unstable designs, resulting from large balancing gains, are characterized by exponentially growing time domain responses that settle in limit cycle oscillations. Note that the onset of instability occurs at a lower balancing bandwidth for the design with a 3.3 μH filter inductor.

in Fig. 24 as a part of the unmodeled dynamics. This finding motivates future study into the exact impacts of inductor current ripple on the closed-loop behavior as a function of the converter design. It also motivates the design of controllers that shape the inductor current ripple or predict and complement the natural

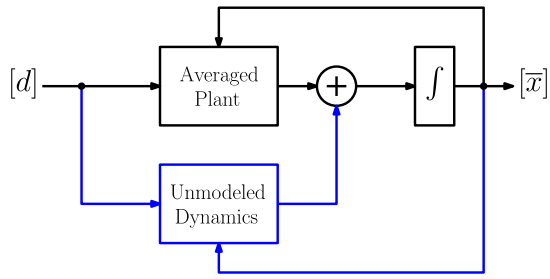

Fig. 24. Representation of averaged dynamics used as the plant model in this work and faster unmodeled dynamics. The unmodeled dynamics are insignificant at moderate to heavy loads, but become more relevant at light loads, contributing to closed-loop instability depending on the choice of active balancing controller gains. The unmodeled dynamics encompass the impact of inductor current ripple, sampling capacitor voltages, measurement and actuation delays, and other higher order phenomena.

balancing action to minimize this operating point dependence. Naturally, as the inductor current ripple evolves at significantly faster timescales compared to the averaged dynamics, such controllers will be more complex and difficult to implement on industry-standard DSPs compared to the solution proposed in this work.

VI. Conclusion

This work presents an active voltage balancing converter for FCML converters implemented in parallel with a high-bandwidth current control loop. The parallel controller structure is derived from the state–space averaged plant model of the FCML converter, and decoupled balancing and current controllers are presented. Experimental verification of the proposed controller on a six-level FCML converter shows improved voltage tracking compared to the same converter relying on natural balancing. The stability of the closed-loop system incorporating the proposed balancing and current controllers is analyzed and shown to depend on the converter operating point.

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