A General Modeling and Analysis of Impacts of Unbalanced Inductance on PWM Schemes for Two-Parallel Interleaved Power Converters

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***Abstract*—This article presents a comprehensive analysis of the impacts of inductor imbalance on the switching-related performance indicators (namely line-current ripple, high-frequency zero-sequence circulating current, and common-mode voltage) of two-parallel converters. It addresses this longstanding issue by presenting a general model that captures the dynamic behavior of the actual output voltages under imbalanced inductance. The central finding from our general model reveals that unbalanced inductances introduce additional voltages to the original common mode voltage, with the amplitude directly proportional to the imbalance degree. Those additional voltages cause the actual output voltages to deviate from the ideal ones under balance inductance, turning the traditional static vector plane into dynamic entities. Moreover, our general model reveals that these additional voltages deteriorate the switching-related performance indicators in both centralized and decentralized systems. However, due to their high-frequency characteristic, it is impossible to compensate for these additional voltages. Recognizing the unfeasible compensation, we have formulated a general analytical approach to identify general tolerance thresholds of inductance imbalance within which the switching-related performance indicators remain largely unaffected. Finally, the experimental results validate our theoretical evaluation of the unbalanced inductance's impact on switching-related performance indicators. The proposed general model and the analytical approach lay the foundation for future research into the impact of inductance imbalances on the switching-related performance indicators in parallel topologies.**

***Index Terms*—Common mode voltages, imbalanced inductance, line current ripples, two-parallel interleaved three-phase inverter, zero-sequence-circulating currents.**

I. Introduction

THE growing need for high power and scalability in areas such as grid connected wind power generation, electric vehicle chargers, and uninterruptible power supplies has spurred the implementation of parallel power inverters [1], [2], [3]. The two-parallel converter topology, with its paralleled dc links and ac terminals interconnected via filter inductors (see Fig. 1), has gained prominence, not least because proper control can provide both high full- and partial-load efficiency [4].

Manuscript received 11 February 2024; revised 22 March 2024; accepted 9 April 2024. Date of publication 12 April 2024; date of current version 4 September 2024. *(Corresponding author: Zhiyong Zeng.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3388024.

Digital Object Identifier 10.1109/TPEL.2024.3388024

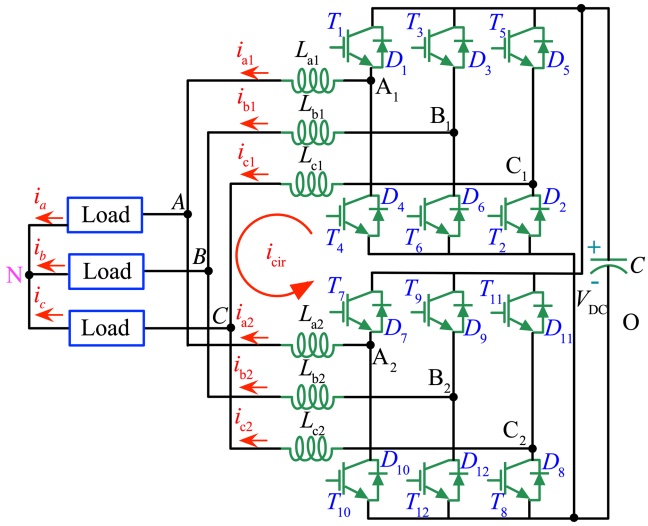

Fig. 1. Two interleaved paralleled three-phase two-level inverter.

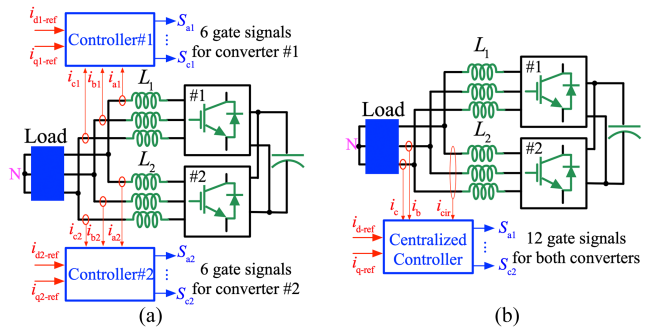

Fig. 2. Control architectures of (a) the decentralized and (b) the centralized.

Control architectures for two-parallel converters are generally classified into two categories: 1) decentralized and 2) centralized [5], [6]. In decentralized control, the individual converters regulate their respective output voltages and currents independently, as depicted in Fig. 2(a). Since each converter has its own controller, each converter applies the generic eight standard vectors known from space-vector modulation [see Fig. 3(a)]. We label modulation strategies for the decentralized architecture as *independent modulation* since it does not address the coordinated

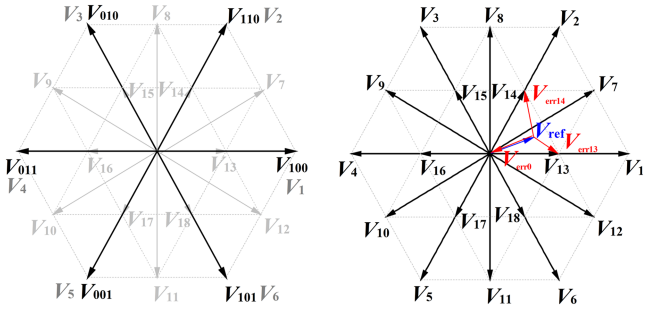

Fig. 3. Space-vector plane of (a) the individual converter and (b) the two-paralleled converter within the centralized architecture. With the assumption of the balanced inductances, the centralized architecture provides an equivalent vector plane including 19 vectors, resembling to a three-level converter.

switching states design between two parallel converters to target the optimization of switching-related indicators.

The switching-related indicators crucially affect the two-parallel converter's overperformance. For instance, a larger zero-sequence circulating current necessitates increased filter inductance, resulting in considerable energy losses; the common mode voltage presents significant challenges, potentially causing electromagnetic interference, damaging equipment insulation, inducing common mode currents, and posing safety hazards. Additionally, excessive line current ripple stresses power electronic components, decreases efficiency, and, in motor applications, leads to vibrations and noise.

The switching-related indicators are collectively determined by the vector combinations from two parallel converters, and the coordinated design of vector combinations maximizes the optimization potential for switching-related indicators. Notably, two parallel converters yield 64 ($= 8\times8$) vector combinations resulting from eight vectors of each converter, and with the assumption of balanced inductance ($L_{a1} = L_{a2} = L_{b1} = L_{b2} = L_{c1} = L_{c2} = L_1$, Fig. 1), these 64 switching states combinations result in 19 equivalent vectors. As illustrated by Fig. 3(b), those 19 equivalent vectors develop an equivalent vector plane, which is analogous to a three-level converter. These equivalent vectors and the resultant vector plane serve as foundational tools for developing pulse width modulation (PWM) schemes to optimize switching-related performance indicators in the centralized system, where all converters are collectively managed under a single central controller.

In contrast to the mere eight vectors applied by independent modulation schemes, the 64 vector combinations applied by coordinated schemes provide greater redundancy and flexibility, thereby offering enhanced opportunities for optimization. For clarity in expression, we label modulation strategies for the centralized control architecture as *coordinated modulation* due to the optimal coordinated switching states design between two-parallel converters.

Table I provides a comparative analysis of these crucial indicators across state-of-the-art coordinated PWM schemes. For example, Zeng et al.'s [6] line current ripple minimization PWM (LCPWM) and He et al.'s [7] modified DPWM (MMDPWM) focus on minimizing line current ripples. Quan and Li [8] proposed

TABLE I
CRITICAL INDICATORS COMPARISONS AMONG THE STATE-OF-THE-ART PWM METHODS

	Current ripple	ZSCC	Switching losses	CMV
Zero-CMV [11]	Largest	Large	Large	0
AZSPWM [9]	Large	Minimum	Large	$\pm V_{DC}/6$
3LSVM [8]	Large	Minimum	Medium	$\pm V_{DC}/6$
MDPWM [10]	Large	Minimum	Large	$\pm V_{DC}/2$
LCPWM [6]	Minimum	Minimum	Largest	$\pm V_{DC}/2$
ODPWM [12]	Medium	Minimum	Minimum	$\pm V_{DC}/2$
HPDPWM [13]	Medium	Minimum	Minimum	$\pm V_{DC}/2$
MMDPWM [7]	Medium	Minimum	Medium	$\pm V_{DC}/2$

a three-level space vector modulation (3LSVM) to suppress high-frequency zero-sequence circulating currents. At the same time, Gohil et al. [9] utilized active-zero-state-vector PWM (AZSPWM) and modified discontinuous PWM (MDPWM) [10] for the same purpose. Jiang et al. [11] introduced a zero common mode voltage (ZCMV) method to eliminate common mode voltages. Additionally, Zeng et al. [12] developed an optimal DPWM (ODPWM) and a high-performance DPWM (HPDPWM) [13] to balance the optimization of switching losses, line current ripples, and high-frequency zero-sequence circulating currents.

It is important to note that the assumption of identical inductances is foundational to all coordinated PWM schemes. However, in actual systems, inductors vary. Manufacturing tolerance renders perfectly matched inductors impossible while matching through measurement can drive the cost up. As this initial assumption is frequently challenged, the effectiveness of these coordinated modulation methods comes into question. Besides, the decentralized system successfully suppresses the low-frequency zero-sequence circulating current caused by the imbalance inductance [14], [15]. Still, the impact of the imbalance inductance on the switching-related indicators is not explored. This article addresses this longstanding issue by presenting a general model that captures the dynamic behavior of the actual vectors under imbalanced inductance. Without loss of generality, in this article, we will shift the inductance of Phase B out of balance to study imbalance inductance's effect, where $L_{a1} = L_{a2} = L_{c1} = L_{c2} = L_1$ and $L_{b2} \neq L_{b1} \neq L_1$ (L_1 is nominal inductance), as shown in Fig. 1.

The presented general model offers a novel perspective for understanding the impact of inductance imbalance on switching-related indicators. A key finding is that unbalanced inductance introduces additional voltages to the original common mode voltage. These additional common mode voltages experience rapid changes per carrier period and cause the amplitude and angle of actual vectors to oscillate, transforming what are initially static vectors into dynamically oscillating ones.

To quantitatively analyze the impact of the imbalance inductance, we developed a quantitative model that accurately predicts the additional common mode voltages for each carrier period. This quantitative model demonstrates that as inductance imbalances increase, the amplitudes of the additional common mode voltage and their rates of change (dv/dt) increase. These increased amplitudes cause the actual output voltages to deviate severely from the ideal ones, deteriorating line current ripples and high-frequency zero-sequence circulating currents.

Although the presented quantitative model successfully predicts these additional voltages, it is infeasible to compensate for them due to their high-frequency characteristics. Recognizing the unfeasible compensation, it is imperative to quantify the acceptable margin where the efficiencies of existing coordinated modulation schemes are not significantly impacted. Utilizing our quantitative model, we have formulated a general analytical approach to identify general tolerance thresholds of inductance imbalance within which the existing coordinated modulation schemes remain substantially effective. This identification is invaluable for engineers and designers since it offers a clearer understanding of the robustness and resilience of various coordinated PWM methods under real applications.

Furthermore, the decentralized systems often consist of converters from various manufacturers and this diversity typically results in larger inductance imbalances due to the differing manufacturing practices of different companies. Previous studies model the parallel converters with imbalanced inductance using the average values over each carrier period [16], [17], [18]. These models highlight how imbalanced inductance causes low-frequency zero-sequence circulating currents between parallel converters. Utilizing these models, earlier studies have established that decentralized systems can accommodate imbalances ranging from 50% to 70%, a limit directly influenced by their effectiveness in suppressing low-frequency zero-sequence circulating currents. However, this modeling approach overlooks the instantaneous behaviors within carrier periods, missing crucial insights into effects of inductance imbalance on switching-related performance indicators [16], [17], [18].

Contrary to the traditional approach, our general model captures the dynamic behavior of parallel converter under imbalanced inductance. In response, we have extended our general model to investigate how imbalanced inductance impacts the performance of the switching-related performance indicators in decentralized systems. Significantly, our model indicates that even at a 50% imbalance, decentralized systems experience increased common mode voltage and its rate of change (dv/dt). These findings challenge existing understanding and imply that decentralized systems may not be as tolerant of higher inductance imbalances as previously thought. Notably, our analysis underscores the importance of evaluating common mode voltages and their rate of changes (dv/dt) in decentralized systems.

Finally, the experimental results support our general model's predictions about the impact of unbalanced inductance on switching-related performance indicators, confirming the model's accuracy and practical relevance. Significantly, our analytical approach lays the foundation for future research into the impact of inductance imbalances on switching-related performance indicators in parallel topologies.

The rest of this article is organized as follows. Section II discusses the fundamentals of two parallel converters and highlights the reliance of coordinated PWM schemes on the assumption of balanced inductance. Section III introduces a general model for both decentralized and centralized systems with imbalanced inductance, revealing the extra high-frequency oscillating common mode voltages due to inductance imbalance. Section IV comprehensively investigates the impact of these additional oscillating common mode voltages on switching-related performance indicators and introduces a general analytical method for determining inductance imbalance tolerance thresholds. Section V presents experimental evidence supporting our theoretical analysis on the effects of inductance imbalance on switching-related performance indicators. Finally, Section VI concludes this article.

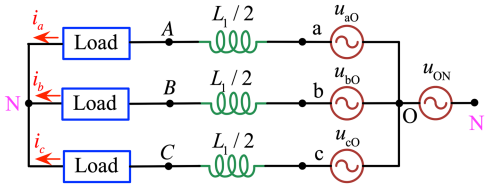

Fig. 4. Equivalent circuits of the two parallel converters with balanced inductances, where the parallel legs are equivalent to a single channel. $u_{aO,}$, u_{bO}, and u_{cO} denotes the output voltage of the equivalent single converter.

II. Basics of the Two Parallel Interleaved Three-Phase Power Converters

Fig. 1 depicts the topology of two parallel converters. Applying the Kirchhoff voltage theorem, the output voltages at the juncture points A, B, and C of the two converters follow:

$$\begin{cases} u_{AN} = u_{a1o} - L_{a1}\frac{di_{a1}}{dt} - u_{No} = u_{a2o} - L_{a2}\frac{di_{a2}}{dt} - u_{No} \\ u_{BN} = u_{b1o} - L_{b1}\frac{di_{b1}}{dt} - u_{No} = u_{b2o} - L_{b2}\frac{di_{b2}}{dt} - u_{No} \\ u_{CN} = u_{c1o} - L_{c1}\frac{di_{c1}}{dt} - u_{No} = u_{c2o} - L_{c2}\frac{di_{c2}}{dt} - u_{No}. \end{cases} \tag{1}$$

The voltage and current that the loads experience are the combined outputs from the two converters, and both converters can be treated as a single converter. Notably, if the balance inductance ($L_{a1} = L_{a2} = L_{b1} = L_{b2} = L_{c1} = L_{c2} = L_1$) is assumed, by averaging the corresponding terms in (1), we derive output voltages of this equivalent single converter (see Fig. 4) as

$$\begin{cases} u_{AN} = \underbrace{\frac{u_{a1o} + u_{a2o}}{2} - u_{No}}_{u_{aN}} - \frac{L_1}{2}\frac{di_a}{dt} \\ u_{BN} = \underbrace{\frac{u_{b1o} + u_{b2o}}{2} - u_{No}}_{u_{bN}} - \frac{L_1}{2}\frac{di_b}{dt} \\ u_{CN} = \underbrace{\frac{u_{c1o} + u_{c2o}}{2} - u_{No}}_{u_{cN}} - \frac{L_1}{2}\frac{di_c}{dt} \end{cases} \tag{2}$$

where u_{No} denotes the common mode voltage of a two-parallel converter, and the outputs of two parallel converters are represented by u_{a1o}, u_{a2o}, u_{b1o}, u_{b2o}, u_{c1o}, and u_{c2o}, respectively, as follows:

$$\begin{cases} u_{a1o} = S_{a1}V_{dc} - 0.5V_{dc} \\ u_{b1o} = S_{b1}V_{dc} - 0.5V_{dc} \\ u_{c1o} = S_{c1}V_{dc} - 0.5V_{dc} \end{cases}, \begin{cases} u_{a2o} = S_{a2}V_{dc} - 0.5V_{dc} \\ u_{b2o} = S_{b2}V_{dc} - 0.5V_{dc} \\ u_{c2o} = S_{c2}V_{dc} - 0.5V_{dc} \end{cases} \tag{3}$$

where the dc-link voltage is denoted by V_{dc}; S_{a1}, S_{b1}, S_{c1}, S_{a2}, S_{b2}, and S_{c2} denote the states of T_1, T_3, T_5, T_7, T_9, and T_{11} (see

TABLE II
TWO-PARALLELED INTERLEAVED CONVERTER'S ZSCC CHANGE RATES AND CMVS OF AVAILABLE VOLTAGE VECTORS

		VSC$_2$							
		V_{000}	V_{100}	V_{110}	V_{010}	V_{011}	V_{001}	V_{101}	V_{111}
VSC$_1$	V_{000}	$V_0(-V_{DC}/2, 0)$	$V_{13}(-V_{DC}/3, -1)$	$V_{14}(-V_{DC}/6, -2)$	$V_{15}(-V_{DC}/3, -1)$	$V_{16}(-V_{DC}/6, -2)$	$V_{17}(-V_{DC}/3, -1)$	$V_{18}(-V_{DC}/6, -2)$	$V_0(0, -3)$
	V_{100}	$V_{13}(-V_{DC}/3, 1)$	$V_1(-V_{DC}/6, 0)$	$V_7(0, -1)$	$V_{14}(-V_{DC}/6, 0)$	$V_0(0, -1)$	$V_{18}(-V_{DC}/6, 0)$	$V_{12}(0, -1)$	$V_{13}(V_{DC}/6, -2)$
	V_{110}	$V_{14}(-V_{DC}/6, 2)$	$V_7(0, 1)$	$V_2(V_{DC}/6, 0)$	$V_8(0, 1)$	$V_{15}(V_{DC}/6, 0)$	$V_0(0, 1)$	$V_{13}(V_{DC}/6, 0)$	$V_{14}(V_{DC}/3, -1)$
	V_{010}	$V_{15}(-V_{DC}/3, 1)$	$V_{14}(-V_{DC}/6, 0)$	$V_8(0, -1)$	$V_3(-V_{DC}/6, 0)$	$V_9(0, -1)$	$V_{16}(-V_{DC}/6, 0)$	$V_0(0, -1)$	$V_{15}(V_{DC}/6, -2)$
	V_{011}	$V_{16}(-V_{DC}/6, 2)$	$V_0(0, 1)$	$V_{15}(V_{DC}/6, 0)$	$V_9(0, 1)$	$V_4(V_{DC}/6, 0)$	$V_{10}(0, 1)$	$V_{17}(V_{DC}/6, 0)$	$V_{16}(V_{DC}/3, -1)$
	V_{001}	$V_{17}(-V_{DC}/3, 1)$	$V_{18}(-V_{DC}/6, 0)$	$V_0(0, -1)$	$V_{16}(-V_{DC}/6, 0)$	$V_{10}(0, -1)$	$V_5(-V_{DC}/6, 0)$	$V_{11}(0, -1)$	$V_{17}(V_{DC}/6, -2)$
	V_{101}	$V_{18}(-V_{DC}/6, 2)$	$V_{12}(0, 1)$	$V_{13}(V_{DC}/6, 0)$	$V_0(0, 1)$	$V_{17}(V_{DC}/6, 0)$	$V_{11}(0, 1)$	$V_6(V_{DC}/6, 0)$	$V_{18}(V_{DC}/3, -1)$
	V_{111}	$V_0(0, 3)$	$V_{13}(V_{DC}/6, 2)$	$V_{14}(V_{DC}/3, 1)$	$V_{15}(V_{DC}/6, 2)$	$V_{16}(V_{DC}/3, 1)$	$V_{17}(V_{DC}/6, 2)$	$V_{18}(V_{DC}/3, 1)$	$V_0(V_{DC}/2, 0)$

Fig. 1); for example, when $S_{b1} = 0$, T_3 is OFF; if $S_{b1} = 1$, T_3 is ON.

Typically, the balanced loads are assumed (see Fig. 1), and averaging the corresponding terms in (2) yields common mode voltages of two-parallel converter per

$$u_{No} = \frac{u_{a1o} + u_{a2o} + u_{b1o} + u_{b2o} + u_{c1o} + u_{c2o}}{6}. \quad (4)$$

Then, substituting (4) and (3) into (2) entails the equivalent output voltages u_{aN}, u_{bN}, and u_{cN} of the single converter (see Fig. 3)

$$\begin{cases} u_{aN} = [(2S_{a1} + 2S_{a2}) - (S_{b1} + S_{b2}) - (S_{c1} + S_{c2})]\, V_{dc}/6 \\ u_{bN} = [(2S_{b1} + 2S_{b2}) - (S_{a1} + S_{a2}) - (S_{c1} + S_{c2})]\, V_{dc}/6 \\ u_{cN} = [(2S_{c1} + 2S_{c2}) - (S_{b1} + S_{b1}) - (S_{a1} + S_{a2})]\, V_{dc}/6. \end{cases} \quad (5)$$

The output voltages of the equivalent single converter (see Fig. 4) dominate the performance of the switching-related indicators of the two parallel converters, which depends on the switching states combinations from two converters in parallel. Submitting all available 64 switching sates into (5) yields 19 distinct output voltages (vectors), constituting an equivalent vector plane, as Fig. 3(b) illustrates. This equivalent vector plane provides a basic tool for the design of coordinated PWM schemes. For example, illustrated in Fig. 3(b), three vectors $\boldsymbol{V_0}$, $\boldsymbol{V_{13}}$, and $\boldsymbol{V_{14}}$ are the nearest-three-vector for the given reference voltage, which minimizes the line current ripples. Indeed, assisted by this static vector plane, HBSVM, MMDPWM, and LCPWM optimize the output voltages of this equivalent single converter by applying the nearest-three vector, minimizing line current ripples.

Besides, the substitution of (3) into (4) yields the common mode voltage of the two-parallel converter as

$$u_{NO} = \frac{[(S_{a2}+S_{a1}) + (S_{c2}+S_{c1}) + (S_{b2}+S_{b1})]\, V_{dc}}{6} - \frac{V_{dc}}{2}. \quad (6)$$

In addition, the zero-sequence circulating current arises due to the common mode voltage differences between the two parallel converters, and its rate of change can be described by

$$\frac{\Delta i_{cir}}{\Delta t} = \frac{3\Delta u_{CMV}}{L_1 + L_1} = \frac{[(S_{a1} - S_{a2}) + (S_{c1} - S_{c2}) + (S_{b1} - S_{b2})]\, V_{dc}}{(L_1 + L_1)}. \quad (7)$$

Table II details the relationship among the rate of change of zero-sequence circulating current, common mode voltage, and the switching states (vectors), where the second item in parentheses denotes the normalized rate of change of the zero-sequence circulating current by $V_{dc}/(L_1+L_1)$, and the first item in parentheses denotes the common mode voltage. The zero-sequence circulating current's change rates can be divided into four grades: ±3, ±2, ±1, and 0, while the common mode voltage can be divided into four grades: $\pm V_{dc}/2$, $\pm V_{dc}/3$, $\pm V_{dc}/6$, and 0. It can be observed that each vector has multiple common mode voltages and zero-sequence circulating current' change rates. For example, $\boldsymbol{V}_0$ can be formed by the pair $\boldsymbol{V}_{000}/\boldsymbol{V}_{111}$—which produces the largest change rate (±3) and the zero common mode voltage, and the pairs $\boldsymbol{V}_{000}/\boldsymbol{V}_{000}$—which produces a zero-change rate but the largest common mode voltage ($\pm V_{dc}/2$). To mitigate zero-sequence circulating current, it is advantageous to use the vector with smaller rate of change (±1, 0), which forms the basis of 3LSVM [8], AZSPWM [9], and MDPWM [10]. Similarly, it is advantageous to use the vector with a smaller common mode voltage ($\pm\boldsymbol{V_{dc}}/6$, and 0), which is how the ZCMV suppresses the common mode voltage.

It is important to note that with the assumption of balanced inductances, output voltages (vectors) of the equivalent single converter can be predicted by (5), whose amplitudes and angles are fixed. These static vectors are foundational to coordinated PWM schemes. However, manufacturing tolerances undermine this assumption in real-world applications. When this assumption does not hold, the effectiveness of the coordinated modulation schemes becomes questionable.

III. IMPACT OF UNBALANCED INDUCTANCES ON THE BASIC VECTORS APPLIED BY COORDINATED PWM SCHEMES

To conduct a general analysis, we introduce six variables accounting for the discrepancies in the inductors through

$$L_{dev-x} = \frac{L_{x1} + L_{x2}}{2} - L_1, L_{diff-x} = \frac{L_{x1} - L_{x2}}{2} \quad (8)$$

where $L_{dev\text{-}x}$ ($x = $ a, b, and c) denotes the inductance's deviation of each phase from the nominal inductance L_1, and $L_{diff\text{-}x}$

denotes the inductance differences of each phase. Besides, we introduce four circulating currents as

$$\begin{cases} i_{\mathrm{cir-a}} = (i_{\mathrm{a1}} - i_{\mathrm{a2}})/2, i_{\mathrm{cir-b}} = (i_{\mathrm{b1}} - i_{\mathrm{b2}})/2, \\ i_{\mathrm{cir-c}} = (i_{\mathrm{c1}} - i_{\mathrm{c2}})/2, i_{\mathrm{cir-0}} = (i_{\mathrm{cir-a}} + i_{\mathrm{cir-b}} + i_{\mathrm{cir-c}})/3 = i_{\mathrm{cir}}/3. \end{cases} \tag{9}$$

Averaging the corresponding terms of (1) yields the common mode voltages with the unbalanced inductances

$$u_{\mathrm{No}} = \frac{u_{\mathrm{a1o}} + u_{\mathrm{a2o}} + u_{\mathrm{b1o}} + u_{\mathrm{b2o}} + u_{\mathrm{c1o}} + u_{\mathrm{c2o}}}{6} - \frac{\Delta V_{\mathrm{a}} + \Delta V_{\mathrm{b}} + \Delta V_{\mathrm{c}}}{3} \tag{10}$$

where ΔV_{a}, ΔV_{b}, and ΔV_{c} denote the voltage injection of each phase by the unbalanced inductance per

$$\begin{cases} \Delta V_{\mathrm{a}} = \frac{1}{2} L_{\mathrm{dev-a}} \frac{\mathrm{d}i_{\mathrm{a}}}{\mathrm{d}t} + L_{\mathrm{diff-a}} \frac{\mathrm{d}i_{\mathrm{cir-a}}}{\mathrm{d}t} \\ \Delta V_{\mathrm{b}} = \frac{1}{2} L_{\mathrm{dev-b}} \frac{\mathrm{d}i_{\mathrm{b}}}{\mathrm{d}t} + L_{\mathrm{diff-b}} \frac{\mathrm{d}i_{\mathrm{cir-b}}}{\mathrm{d}t} \\ \Delta V_{\mathrm{c}} = \frac{1}{2} L_{\mathrm{dev-c}} \frac{\mathrm{d}i_{\mathrm{c}}}{\mathrm{d}t} + L_{\mathrm{diff-c}} \frac{\mathrm{d}i_{\mathrm{cir-c}}}{\mathrm{d}t}. \end{cases} \tag{11}$$

As evidenced by (10), the unbalanced inductance adds extra voltages beyond the original common mode voltage described in (4). This extra voltage imposes extra voltage insulation stress on the two-parallel converters, which is a common challenge to both coordinated PWM and independent PWM schemes.

Submitting (10) into (1) yields actual output voltages of the equivalent single converter with unbalanced inductances

$$\begin{cases} u_{\mathrm{aN}} = \frac{[(2S_{\mathrm{a1}}+2S_{\mathrm{a2}})-(S_{\mathrm{b1}}+S_{\mathrm{b2}})-(S_{\mathrm{c1}}+S_{\mathrm{c2}})]V_{\mathrm{dc}}}{6} + \Delta V_{\mathrm{dev-a}} \\ u_{\mathrm{bN}} = \frac{[(2S_{\mathrm{b1}}+2S_{\mathrm{b2}})-(S_{\mathrm{a1}}+S_{\mathrm{a2}})-(S_{\mathrm{c1}}+S_{\mathrm{c2}})]V_{\mathrm{dc}}}{6} + \Delta V_{\mathrm{dev-b}} \\ u_{\mathrm{cN}} = \frac{[(2S_{\mathrm{c1}}+2S_{\mathrm{c2}})-(S_{\mathrm{b1}}+S_{\mathrm{b1}})-(S_{\mathrm{a1}}+S_{\mathrm{a2}})]V_{\mathrm{dc}}}{6} + \Delta V_{\mathrm{dev-c}} \end{cases} \tag{12}$$

where $\Delta V_{\mathrm{dev\text{-}a}}$, $\Delta V_{\mathrm{dev\text{-}b}}$, and $\Delta V_{\mathrm{dev\text{-}c}}$ denote the deviation of each phase's equivalent output voltages from their original ones

$$\begin{cases} \Delta V_{\mathrm{dev-a}} = (-2\Delta V_{\mathrm{a}} + \Delta V_{\mathrm{b}} + \Delta V_{\mathrm{c}})/3 \\ \Delta V_{\mathrm{dev-b}} = (-2\Delta V_{\mathrm{b}} + \Delta V_{\mathrm{a}} + \Delta V_{\mathrm{c}})/3 \\ \Delta V_{\mathrm{dev-c}} = (-2\Delta V_{\mathrm{c}} + \Delta V_{\mathrm{a}} + \Delta V_{\mathrm{b}})/3. \end{cases} \tag{13}$$

Equation (12) provides a generalized model of actual output voltages that the load experiences in two parallel converters, covering both balanced and unbalanced inductance scenarios. Under the assumption of balanced inductance, the 19 vectors applied by coordinated PWM schemes can be predicted by (5). However, unbalanced inductance introduces additional voltages to the original outputs, leading to deviations from the expected output based solely on switching states. Moreover, this model directly associates switching states with actual output voltages, thereby enabling the accurate prediction of actual output voltages for both coordinated and independent PWM schemes. Specifically, any PWM scheme's actual output voltage under imbalanced inductance can be predicted by inputting respective switching states into (12). Significantly, our general model reveals that inductance imbalance introduces additional common mode voltages in both decentralized and centralized systems, a key finding not previously reported.

To quantitatively investigate the effect of additional common mode voltages on the actual output voltages, it is essential to transform the three voltages in (13) into the static α-β coordinate. Applying Clarke transformation to (13) yields the projections of the voltage deviations on the static $\alpha-\beta$ coordinate as

$$\begin{cases} \Delta V_{\mathrm{dev}-\alpha} = -\left(2\Delta V_{\mathrm{a}} - \Delta V_{\mathrm{b}} - \Delta V_{\mathrm{c}}\right)/3 \\ \Delta V_{\mathrm{dev}-\beta} = -\left(\sqrt{3}\Delta V_{\mathrm{b}} - \sqrt{3}\Delta V_{\mathrm{c}}\right)/3 \end{cases} \tag{14}$$

where $\Delta V_{\mathrm{dev\text{-}}\alpha}$ and $\Delta V_{\mathrm{dev\text{-}}\beta}$ denotes the α-axis and β-axis projection of voltage deviations (see Fig. 5).

As indicated in Section I, without loss of generality, we shifted the inductance of Phase B out of balance

$$L_{\mathrm{dev-b}} \neq 0, L_{\mathrm{diff-b}} \neq 0, L_{\mathrm{dev-a}} = L_{\mathrm{diff-a}} = L_{\mathrm{dev-c}} = L_{\mathrm{diff-c}} = 0. \tag{15}$$

Submitting (15) and (13) into (14) yields

$$\begin{cases} \Delta V_{\mathrm{dev}-\alpha} = \frac{\Delta V_{\mathrm{b}}}{3} = \left(\frac{1}{6} L_{\mathrm{dev-b}} \frac{\mathrm{d}i_{\mathrm{b}}}{\mathrm{d}t} + \frac{1}{3} L_{\mathrm{diff-b}} \frac{\mathrm{d}i_{\mathrm{cir-b}}}{\mathrm{d}t}\right) \\ \Delta V_{\mathrm{dev}-\beta} = \frac{-\sqrt{3}\Delta V_{\mathrm{b}}}{3} = \left(-\frac{\sqrt{3}}{6} L_{\mathrm{dev-b}} \frac{\mathrm{d}i_{\mathrm{b}}}{\mathrm{d}t} - \frac{\sqrt{3}}{3} L_{\mathrm{diff-b}} \frac{\mathrm{d}i_{\mathrm{cir-b}}}{\mathrm{d}t}\right). \end{cases} \tag{16}$$

The differential terms in (16) can be derived from (2)

$$\begin{cases} L_{\mathrm{dev-b}} \frac{\mathrm{d}i_{\mathrm{b}}}{\mathrm{d}t} = \frac{3(L_{\mathrm{b1}}+L_{\mathrm{b2}}-2L_1)(L_{\mathrm{b1}}+L_{\mathrm{b2}})(u_{\mathrm{bN}}-u_{\mathrm{BN}})}{L_1L_{\mathrm{b1}}+L_1L_{\mathrm{b2}}+4L_{\mathrm{b1}}L_{\mathrm{b2}}} \\ \quad + \frac{(L_{\mathrm{b1}}+L_{\mathrm{b2}}-2L_1)(L_{\mathrm{b2}}-L_{\mathrm{b1}})(S_{\mathrm{b1}}-S_{\mathrm{b2}})V_{\mathrm{dc}}}{L_1L_{\mathrm{b1}}+L_1L_{\mathrm{b2}}+4L_{\mathrm{b1}}L_{\mathrm{b2}}} \\ L_{\mathrm{diff-b}} \frac{\mathrm{d}i_{\mathrm{cir-b}}}{\mathrm{d}t} = \frac{3(L_{\mathrm{b1}}-L_{\mathrm{b2}})(L_{\mathrm{b1}}-L_{\mathrm{b2}})(u_{\mathrm{BN}}-u_{\mathrm{bN}})}{2(L_1L_{\mathrm{b1}}+L_1L_{\mathrm{b2}}+4L_{\mathrm{b1}}L_{\mathrm{b2}})} \\ \quad + \frac{(L_{\mathrm{b1}}-L_{\mathrm{b2}})(L_{\mathrm{b2}}+L_{\mathrm{b1}}+L_1)(S_{\mathrm{b1}}-S_{\mathrm{b2}})V_{\mathrm{dc}}}{2(L_1L_{\mathrm{b1}}+L_1L_{\mathrm{b2}}+4L_{\mathrm{b1}}L_{\mathrm{b2}})}. \end{cases} \tag{17}$$

Then, submitting (17) into (16) yields the voltage deviations

$$\begin{cases} \Delta V_{\mathrm{dev}-\alpha} = \frac{\lambda_1(u_{\mathrm{bN}}-u_{\mathrm{BN}})+\lambda_2(S_{\mathrm{b1}}-S_{\mathrm{b2}})V_{\mathrm{dc}}}{3} \\ \Delta V_{\mathrm{dev}-\beta} = \frac{-\sqrt{3}(\lambda_1(u_{\mathrm{bN}}-u_{\mathrm{BN}})+\lambda_2(S_{\mathrm{b1}}-S_{\mathrm{b2}})V_{\mathrm{dc}})}{3} \end{cases} \tag{18}$$

where u_{BN} denotes the output voltage of the parallel points (see Fig. 4); u_{bN} refers to the ideal output voltage of phase-B assuming the balanced inductance

$$u_{\mathrm{bN}} = \left[(2S_{\mathrm{b1}} + 2S_{\mathrm{b2}}) - (S_{\mathrm{a1}} + S_{\mathrm{a2}}) - (S_{\mathrm{c1}} + S_{\mathrm{c2}})\right] V_{\mathrm{dc}}/6 \tag{19}$$

and the coefficients λ_1 and λ_2 are

$$\begin{aligned} \lambda_1 &= -\frac{3(L_1L_{\mathrm{b2}} + L_1L_{\mathrm{b1}} - 2L_{\mathrm{b1}}L_{\mathrm{b2}})}{(L_1L_{\mathrm{b1}} + L_1L_{\mathrm{b2}} + 4L_{\mathrm{b1}}L_{\mathrm{b2}})}, \\ \lambda_2 &= -\frac{3L_1(L_{\mathrm{b2}} - L_{\mathrm{b1}})V_{\mathrm{dc}}}{2(L_1L_{\mathrm{b1}} + L_1L_{\mathrm{b2}} + 4L_{\mathrm{b1}}L_{\mathrm{b2}})}. \end{aligned} \tag{20}$$

Equation (18) reveals that the voltage deviations consist of two components. The first is determined by phase B's instantaneous output voltage u_{bN}, which is the projection on phase B of the original vectors; the second component further specifies the effects of circulating current on voltage deviations for the same vector. For example, both $\boldsymbol{V_{101}}/\boldsymbol{V_{110}}$ and $\boldsymbol{V_{110}}/\boldsymbol{V_{101}}$ form the ideal vector $\boldsymbol{V_{13}}$, but they introduce the circulating current in opposite directions in Phase B, resulting in two different voltage deviations. Thus, each original vector potentially introduces two

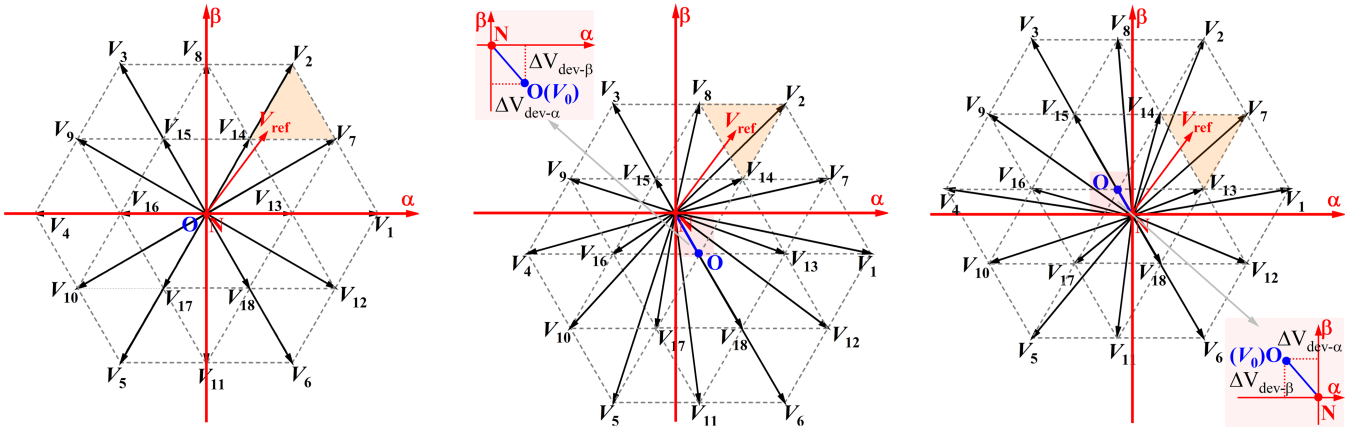

Fig. 5. Actual output vectors for the two-parallel converter in different scenarios: (a) under the assumption of balanced inductance, (b) when the original vector V_u is activated with $S_{b1}-S_{b2}=1$ under imbalanced inductance, and (c) when the original vector V_u is activated with $S_{b1}-S_{b2}=-1$ under imbalanced inductance.

different voltage deviations. For a given ideal vector $\boldsymbol{V_u}$, the resultant two voltage deviations are

$$\begin{cases}\Delta V_{b-u-}=\lambda_1(u_{bN}-u_{BN})+\lambda_2 V_{dc}\\ \Delta V_{b-u+}=\lambda_1(u_{bN}-u_{BN})-\lambda_2 V_{dc}\end{cases} \tag{21}$$

where the positive and negative subscript specifies states difference $S_{b1}-S_{b2}=1$ and $S_{b1}-S_{b2}=-1$.

Typically, the static $\alpha-\beta$ coordinate's origin aligns with the three-phase system's neutral point **N**, where the reference voltage is defined. The zero-voltage vector $\boldsymbol{V_0}$ that represents zero-output voltage ideally overlaps with neutral point **N**, and the vectors' amplitudes and angles are referred to the zero vector $\boldsymbol{V_0}$, as depicted in Fig. 5(a). Using (18) and (21), Fig. 5(b) and (c) shows the voltage deviations on the vector plane caused by a given ideal vector and the resulting actual vectors. The imbalanced inductance causes an instantaneous shift of the vector $\boldsymbol{V_0}$ from $\boldsymbol{N}$, altering the actual vectors' positions from the original locations defined by (5).

Moreover, each voltage deviation leads to a distinct set of 19 actual vectors, and three vectors are applied to synthesize the reference result in six different sets of 19 actual vectors per period. As a result, the vector plane undergoes dynamic oscillation six times each carrier period, with variations in the vectors' amplitudes and angles. Furthermore, as the entire vector plane encompasses numerous carrier periods, the amplitudes and angles of the actual vectors continuously oscillate when reference voltages change across all modulation indexes. Therefore, imbalanced inductance transforms the static vector plane into dynamic ones, posing significant challenges to existing coordinated PWM schemes that are based on static vectors with fixed angles and amplitudes.

Though the case study focuses on an unbalanced inductance of Phase B, the methodology introduced in this section is applicable to the imbalanced inductance of other phases as well. Other scenarios are not detailed in this section due to space constraints, but can be addressed using the corresponding models and equations presented in this section.

IV. Impact and Limits of Unbalanced Inductance on Line Current Ripples and CMV

While the instantaneous voltage deviations caused by the imbalanced inductance can be predicted by (18), it is unfeasible to compensate for those deviations since they experience rapid changes per carrier period. Recognizing the unfeasible compensation of instantaneous deviation voltages, it becomes essential to investigate how those instantaneous deviations affect the switching-related indicators. Importantly, it is imperative to quantify the acceptable margin where existing modulation schemes' efficiencies are not significantly impacted, offering a clearer understanding of their robustness and resilience under real applications.

A. Impact of Unbalanced Inductances on Common Mode Voltage Peak

According to (10), the additional common mode voltage injected by the imbalanced inductances can be expressed as

$$\Delta u_{No}=\frac{-(\Delta V_a+\Delta V_b+\Delta V_c)}{3}. \tag{22}$$

Substituting (11) and (17) into (22) yields the additional common mode voltages

$$\Delta u_{No}=-\frac{1}{3}\Delta V_b=-\frac{1}{3}\lambda_1(u_{bN}-u_{BN})-\frac{1}{3}\lambda_2(S_{b1}-S_{b2})V_{dc}. \tag{23}$$

Equation (23) is proportional to the voltage deviations defined by (18). Therefore, similar to the instantaneous voltage deviations, there are six different additional common mode voltages per carrier period. It is important to note that the existing ZCMV method serves as an ideal benchmark for investigating this additional common mode voltage, since any observed common mode voltage in the ZCMV scheme corresponds to this additional common mode voltage under the unbalanced inductance. By submitting the three vectors $\boldsymbol{V_7}$ ($\boldsymbol{V_{100}/V_{110}}$), $\boldsymbol{V_{12}}$($\boldsymbol{V_{101}/V_{100}}$), and $\boldsymbol{V_0}$ ($\boldsymbol{V_{111}/V_{000}}$) applied by ZCMV to (23), we have the six

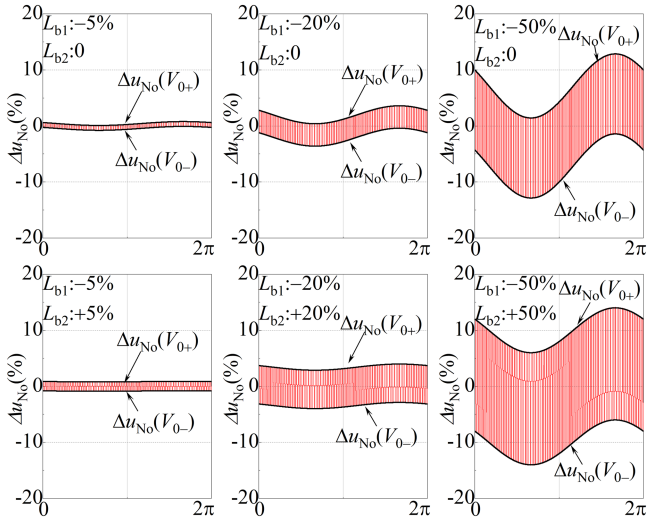

Fig. 6. Simulation results of common mode voltage for the existing ZCMV method with two typical types of unbalanced inductance at three imbalance percentages.

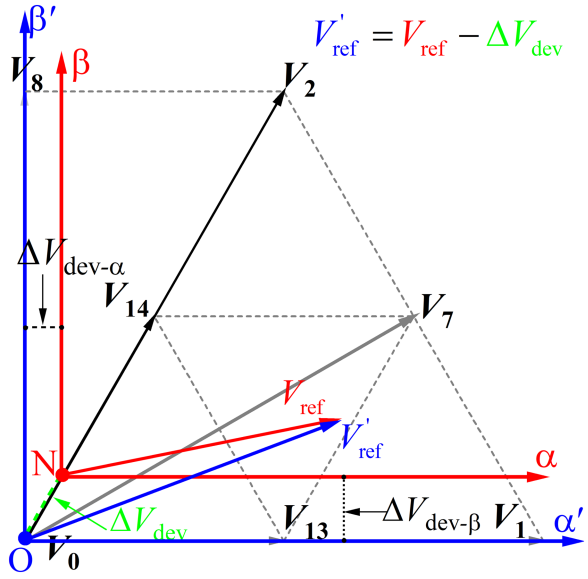

Fig. 7. Static $\alpha-\beta$ coordinates and the dynamically oscillating $\alpha'-\beta'$ coordinate under imbalanced inductance.

additional common mode voltages and then categorized them into three different expressions based on their amplitudes as

$$\begin{cases} \Delta u_{No}(V_{0+})=\Delta u_{No}(V_{7+})=\frac{V_{dc}}{3}\lambda_1\left[\frac{1}{2}M\cos\left(\theta-\frac{2\pi}{3}\right)\right]-\frac{V_{dc}}{3}\lambda_2 \\ \Delta u_{No}(V_{0-})=\Delta u_{No}(V_{7-})=\frac{V_{dc}}{3}\lambda_1\left[\frac{1}{2}M\cos\left(\theta\right)\right]+\frac{V_{dc}}{3}\lambda_2 \\ \Delta u_{No}(V_{12+})=\Delta u_{No}(V_{12-})=\frac{V_{dc}}{3}\lambda_1\left[\frac{1}{2}+\frac{1}{2}M\cos\left(\theta\right)\right] \end{cases} \tag{24}$$

where the positive and negative subscripts specify the states $S_{b1}-S_{b2}=1$ and $S_{b1}-S_{b2}=-1$, respectively.

Our investigation shows that the peaks and valleys of additional common mode voltages correspond to the first and second equations in (24), respectively. Fig. 6 illustrates common mode voltage peaks and valleys under three levels of inductance imbalance. We examined two unbalanced inductance types: the first involves a single inductor (L_{b1}) deviating from its nominal value (L_1), and the second involves deviations in both inductors of a phase (L_{b1} and L_{b2}). Fig. 6 shows simulated common mode voltages using the ZCMV method, which closely matches the analytical findings.

For minor inductance imbalances, additional common mode voltages are negligible. However, at a 20% imbalance, common mode voltage amplitudes noticeably increase, reaching up to 10% of V_{dc}. This 10% increase is the threshold for the effectiveness of coordinated PWM schemes under imbalanced inductances. In centralized architectures, where converters are from the same manufacturer, inductance imbalance typically arises from manufacturing tolerances, around 20%. Our analysis confirms that within these tolerances, existing coordinated PWM schemes ensure less than a 10% increase in common mode voltage, almost maintaining their original levels under balanced inductance.

Furthermore, we extend our analysis to decentralized architectures, which often involve converters from various manufacturers. This potentially leads to larger inductance imbalances due to differences in the manufacturing practices of different manufacturers. Previous research has shown that decentralized systems can tolerate inductance imbalances of 50% to 70%, based on their ability to suppress low-frequency circulating currents [16], [17], [18]. However, as depicted in Fig. 6, our analysis reveals that at a 50% imbalance level, the additional common mode voltage notably increases to 20% of V_{dc}, with a significant dv/dt. These findings challenge the existing understanding and suggest that decentralized systems may not be as tolerant of higher inductance imbalances as previously thought. Significantly, it emphasizes the need to consider common mode voltage and dv/dt in independent PWM schemes.

B. Impact of Unbalanced Inductances on the Line Current Ripples

In the static vector plane, applying the nearest-three-vector scheme is straightforward. As illustrated in Fig. 5(a), the whole vector plane is divided into 24 equilateral triangles, each of which uses the vertex vectors to synthesize the reference voltage. For example, for the given reference in Fig. 5, three vectors $\boldsymbol{V_2}$, $\boldsymbol{V_7}$, and $\boldsymbol{V_{14}}$ are the nearest three vectors. However, Fig. 5(b) and (c) demonstrates that voltage shifts caused by unbalanced inductances make the original three vectors no longer the nearest. Thus, it is essential to assess how well the nearest-three-vector scheme works under imbalanced inductances.

To facilitate the analysis, we introduce a dynamically oscillating coordinate $\alpha'-\beta'$ aligning with the zero-voltage vector $\boldsymbol{V_0}$, contrasting the static $\alpha-\beta$ coordinates aligned with neutral point N, as Fig. 7 illustrates. Under balanced inductance, these two coordinates coincide. However, unbalanced inductance shifts $\alpha'-\beta'$ from $\alpha-\beta$ due to instantaneous voltage deviations (see Fig. 7). Despite this shift, actual vector positions within $\alpha'-\beta'$ remain constant, essentially forming another static plane. Hence,

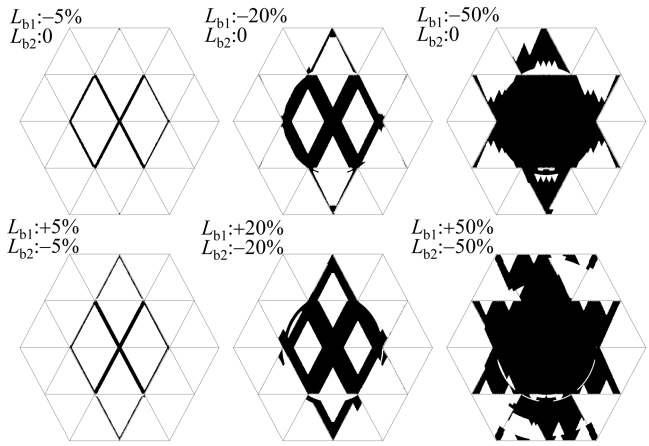

Fig. 8. Impact of the unbalanced inductance on the applicability of the near-three vector scheme with two types of unbalanced inductance at three uneven percentages.

it is more practical to evaluate the nearest-three-vector scheme in $\alpha'-\beta'$. Since the reference voltage is set in the static $\alpha-\beta$, it is essential to transform the reference voltage to the dynamically oscillating coordinate $\alpha'-\beta'$. Fortunately, voltage deviations can be predicted by (14), and the transformation can be facilitated by accounting for the dynamic voltage deviation per

$$\begin{cases} V'_{\mathrm{ref}-\alpha} = V_{\mathrm{ref}-\alpha} - \Delta V_{\mathrm{dev}-\alpha} \\ V'_{\mathrm{ref}-\beta} = u_{\mathrm{ref}-\beta} - \Delta V_{\mathrm{dev}-\beta} \end{cases} \tag{25}$$

where the voltage deviation $\Delta \boldsymbol{V}_{\text{dev-}\alpha}$ and $\Delta \boldsymbol{V}_{\text{dev-}\beta}$ of each original vector can be predicted by (18).

Fig. 7 shows the transformation of the original reference voltage $\boldsymbol{V}_{\mathbf{ref}}$ to the modified $\boldsymbol{V'}_{\mathbf{ref}}$ in $\alpha'-\beta'$ when activating specific vectors. Within each carrier period, three vectors result in six different voltage deviations, leading to six modified reference voltages $\boldsymbol{V'}_{\mathbf{ref}}$ in $\alpha'-\beta'$ coordinate per period. The nearest-three-vector scheme holds only if all six transformed references fall within the area of the original nearest-three vectors. As illustrated in Fig. 7, if the original reference applies $\boldsymbol{V_{13}/V_{14}/V_7}$, only when all six transformed references simultaneously meet

$$u'_{\mathrm{a}} - u'_{\mathrm{b}} \le 1/2, u'_{\mathrm{b}} - u'_{\mathrm{c}} \le 1/2, u'_{\mathrm{a}} - u'_{\mathrm{c}} \ge 1/2 \tag{26}$$

will the nearest-three-vector scheme be maintained in the presence of unbalanced inductances.

With the proposed coordinate transformation, we implemented a comprehensive MATLAB analysis to methodically examine the transformed reference voltages across the entire vector plane. Based on the analysis, Fig. 8 examines the impact of two types of unbalanced inductance at different percentages, and the regions shaded in black denote areas where the nearest-three-vector scheme is not applicable. The findings show that a minor discrepancy in inductance allows the nearest-three-vector scheme to be largely applicable across the vector plane. However, as this imbalance increases, the applicable region shrinks significantly. Specifically, when the unbalanced inductance reaches the typical manufacturing tolerances (20%), almost 10% of the vector plane fails to satisfy the nearest-three-vector scheme, which means 10% performance degrading. The analysis confirms that within typical manufacturing tolerances, the existing coordinated PWM schemes still maintain their original line current ripples, ensuring less than a 10% performance degradation when compared to that in the balanced inductance.

It is also crucial to understand that the nearest-three vector's applicability quantitatively indicates how much the vectors' angles and amplitudes deviate from their original one under the balanced inductance, reflecting the deviation of actual output voltages from the ideal. Therefore, this measure can also assess the overall output voltage in independent PWM schemes. Previous research suggested that decentralized architecture can handle inductance imbalances of 50% to 70% due to their suppression of low-frequency circulating currents. Yet, as shown in Fig. 8, our findings demonstrate that a 50% imbalance leads to significant deviations from ideal output voltages and consequently deteriorates the current quality that the loads experience. Significantly, the presented analysis emphasizes the need to consider the line current qualities in the decentralized system.

C. Impact of Unbalanced Inductances on Zero-Sequence Circulating Currents

In centralized control, both converters share the same modulation signal, the voltage difference remains zero ($u_{\text{diff-d}} = u_{\text{diff-q}} = 0$), and the averaged zero-sequence circulating current per carrier period is generalized as

$$\begin{aligned} i_{\mathrm{cir}} = &-\frac{3(L_{\mathrm{a1}}-L_{\mathrm{a2}})\cos\omega t + 3(L_{\mathrm{b1}}-L_{\mathrm{b2}})\cos(\omega t - 2\pi/3)}{2(L_{\mathrm{a1}}+L_{\mathrm{b1}}+L_{\mathrm{c1}}+L_{\mathrm{a2}}+L_{\mathrm{b2}}+L_{\mathrm{c2}})} i_{\mathrm{d}} \\ &- \frac{3(L_{\mathrm{c1}}-L_{\mathrm{c2}})\cos(\omega t + 2\pi/3)}{2(L_{\mathrm{a1}}+L_{\mathrm{b1}}+L_{\mathrm{c1}}+L_{\mathrm{a2}}+L_{\mathrm{b2}}+L_{\mathrm{c2}})} i_{\mathrm{d}}. \end{aligned} \tag{27}$$

It becomes evident that the uneven inductors lead to the low-frequency zero-sequence circulating current, which is consistent with the scenarios observed in the decentralized architecture. The suppression of the low-frequency zero-sequence circulating current lies in adjusting the averaged common mode voltage difference.

Since this article aims to investigate the effect of the imbalanced inductance on the switching frequency-related indicators, it is essential to investigate how the imbalanced inductance affects the high-frequency circulating current per carrier period. The zero-sequence circulating current amounts to the sum of circulating currents between parallel legs of each phase [12], [13]

$$\begin{aligned} \frac{\mathrm{d}i_{\mathrm{cir}}}{\mathrm{d}t} = &\frac{S_{\mathrm{a1}} - S_{\mathrm{a2}}}{2(L_1 + L_{\mathrm{dev-a}})} V_{\mathrm{dc}} + \frac{S_{\mathrm{b1}} - S_{\mathrm{b2}}}{2(L_1 + L_{\mathrm{dev-b}})} V_{\mathrm{dc}} \\ &+ \frac{S_{\mathrm{c1}} - S_{\mathrm{c2}}}{2(L_1 + L_{\mathrm{dev-c}})} V_{\mathrm{dc}}. \end{aligned} \tag{28}$$

It is evident that the unbalanced inductance primarily affects rates of change of the high-frequency zero-sequence circulating currents. Given the unbalanced inductances of Phase B ($L_{\text{dev-a}} = L_{\text{dev-c}} = L_{\text{diff-a}} = L_{\text{diff-c}} = 0$), we have

$$\frac{\mathrm{d}i_{\mathrm{cir}}}{\mathrm{d}t} = \left[S_{\mathrm{a1}} - S_{\mathrm{a2}} + \frac{(S_{\mathrm{b1}} - S_{\mathrm{b2}})L_1}{(L_1 + L_{\mathrm{dev-b}})} + S_{\mathrm{c1}} - S_{\mathrm{c2}} \right] \frac{V_{\mathrm{dc}}}{2L_1}. \tag{29}$$

Equation (29) reveals that the coefficient defined by $L_1/(L_1+L_{\text{dev-b}})$ affects the rate of change of zero-sequence circulating current. Similarly, we consider two types of unbalanced inductance with three different uneven percentages. In the first type of unbalanced inductance, a hypothetical scenario of 50% imbalance—far exceeding the usual 20% manufacturing tolerance—results in only a 10% increase in the rate of change of the zero-sequence circulating current since the second type of unbalanced inductance has $L_{\text{dev-b}} = 0$, it theoretically does not affect the rate of change of zero-sequence circulating current. It is evident that the unbalanced inductance has a less significant impact on the rate of change for high-frequency zero-sequence circulating currents compared to its effects on common mode voltage and line current ripples.

Finally, to eliminate any potential confusion, we highlighted several key points from the presented comprehensive analysis.

1) Inductance imbalance introduces additional common mode voltage proportional to the imbalance degree, primarily affecting the performance of switching-related indicators in both centralized and decentralized systems.
2) Imbalances below 20% lead to minor additional common mode voltages, allowing coordinated PWM schemes to remain effective within the typical 20% manufacturing tolerance of centralized systems.
3) The additional common mode voltage becomes significant at inductance imbalances of 50% and above, which intensifies the rate of change (dv/dt) of common mode voltage and the resultant EMI issues. Our analysis reveals that the decentralized system is not as tolerant of higher inductance imbalances (60%–70%) as previously thought [16], [17], [18].
4) Inductance imbalance has a minimal impact on high-frequency zero-sequence circulating currents, which slightly increase with higher imbalances.
5) Despite challenges from inductance imbalance, coordinated PWM schemes outperform independent PWM schemes in managing switching-related performance indicators.

Note that all the presented analyses focus on two major types of unbalanced inductances, which represent typical scenarios. Although actual applications may present more complex variations across the three-phase inductors, our analytical model and approach provide a foundational framework for tackling such complexities. Besides, our analytical approach lays the foundation for future research into the impact of imbalances on the effectiveness of PWM schemes across various parallel topologies. Another key contribution is identifying general tolerance thresholds for inductance imbalance. This identification is invaluable for engineers and designers, as it offers a clearer understanding of the robustness and resilience of various modulation methods used in two parallel converters under real-world conditions.

V. Experiments

As Fig. 9 illustrates, we developed an experimental setup to validate the presented analysis. The assembly includes a

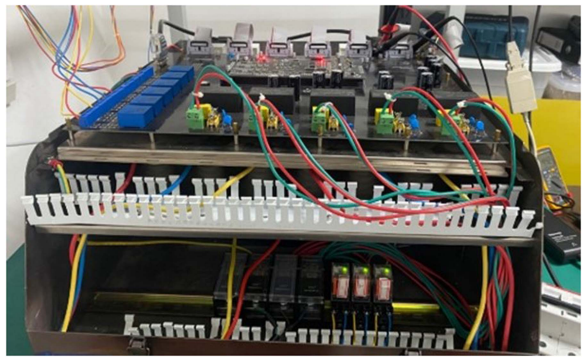

Fig. 9. Photograph of experimental setup.

TABLE III
System Parameters

R_L	L_1	V_{DC}	P
10 Ω	5 mH	400 V	6 kW
	T_s	f	C
	0.0002 s	5 kHz	1500 μF

TMS320F2808 DSP-based controller interface board, a power supply board using RECOM ac–dc power modules, Concept insulated gate bipolar transistor (IGBT) gate drivers (2SP0115T2C), Infineon IGBTs (FF300R17ME4), LEM current sensors and voltage sensors, SBE dc-link capacitors (700D158911-590), and filter inductors. We conducted tests on the prototype in the inverter mode. It sources its dc link from a three-phase diode rectifier and uses three resistors (R) as ac loads. The main parameters are listed in Table III. We used Tektronix current probes (TCP303) for current measurements and recorded waveforms with a Tektronix MSO58B oscilloscope. Experiment data were processed and visualized using Origin for clearer representation.

In an experimental study, we considered typical unbalanced inductance scenarios, where both inductances within a single-phase deviate (L_{b1} negatively and L_{b2} positively). We considered three different imbalance ratios: ±50% ($L_{\text{b1}} = -50\%$, $L_{\text{b2}} = 50\%$), ±20% ($L_{\text{b1}} = -20\%$, $L_{\text{b2}} = 20\%$), and ±5% ($L_{\text{b1}} = -5\%$, $L_{\text{b2}} = 5\%$). As discussed in Section IV, centralized systems typically face up to 20% inductance imbalance, whereas decentralized systems are believed to handle imbalances between 50% and 70%. However, our findings suggest decentralized systems may not withstand high imbalances as previously assumed. To test this, we included a 50% imbalance scenario in our experiments for a decentralized scheme. Although the 50% imbalance inductance is not typically encountered in the centralized system, we also included this imbalance rate in the coordinated PWM schemes tests. By maintaining uniform testing conditions as the independent PWM schemes, we facilitate a comprehensive comparison between coordinated and independent PWM schemes, offering another valuable reference for real applications.

Given the variety of coordinated PWM schemes for two-parallel converters, it is crucial to choose representative schemes for experimental studies. The ZCMV method is particularly

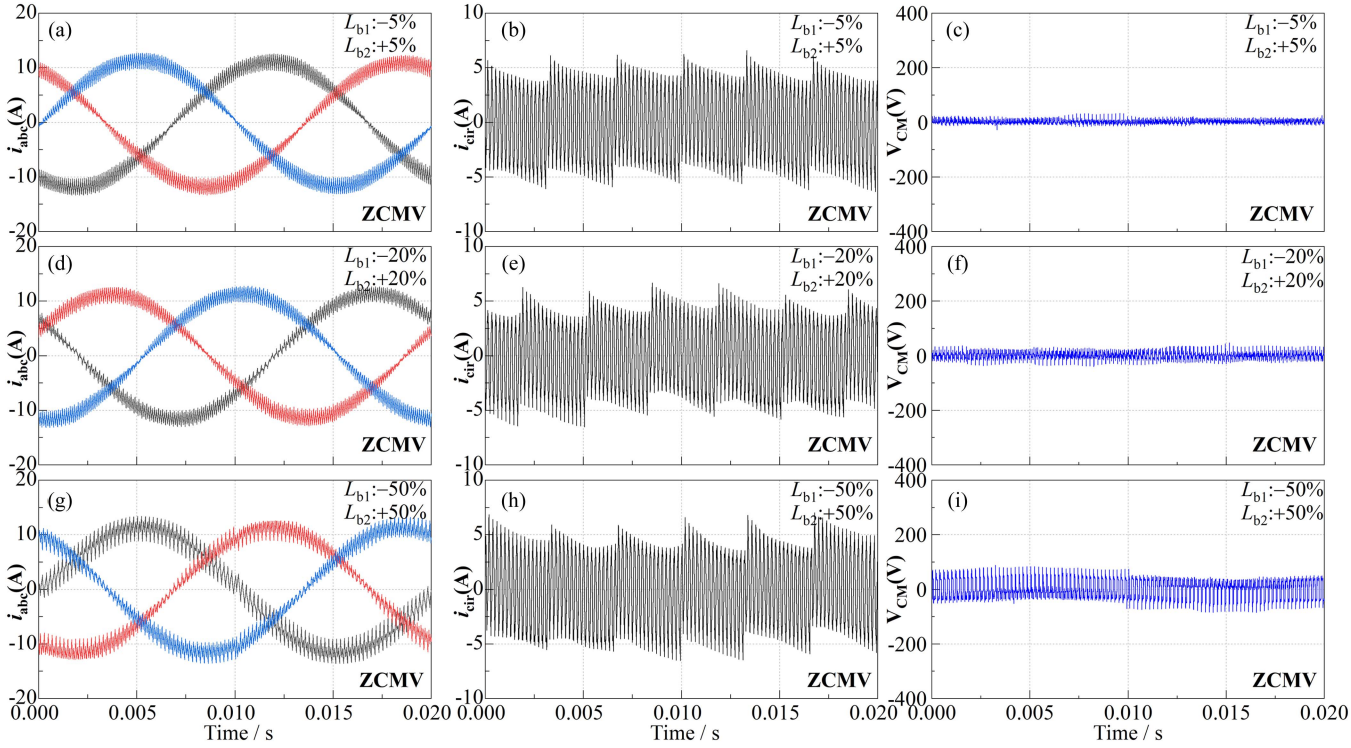

Fig. 10. Experimental output currents, zero-sequence circulating current and common mode voltage of the existing **ZCMV** at $M = 0.6$ and $f = 5$ kHz. (a)–(c) $L_{b1} = -5\%/L_{b2} = 5\%$. (d)–(f) $L_{b1} = -20\%/L_{b2} = 20\%$. (g)–(i) $L_{b1} = -50\%/L_{b2} = 50\%$.

suitable as a benchmark to investigate the additional common mode voltage resulting from imbalanced inductance, where any detected common mode voltage directly reflects this additional voltage. Furthermore, the HPDPWM scheme is more susceptible to actual vectors' oscillations resulting from imbalanced inductance since HPDPWM primarily relies on the nearest three vectors to minimize line current ripples. Consequently, we selected two representative coordinated modulation schemes (ZCMV and HPDPWM) along with an independent PWM scheme interleaved space vector modulation (ISVM) for the experimental validation of our general analysis.

The low-frequency zero-sequences circulating current occurs in both centralized and centralized systems, which can be sup pressed by adjusting the averaged common mode voltage differences among two parallel converters [16], [17], [18]. Our paper primarily focuses on investigating the impact of unbalanced inductance on switching-related performance indicators. Due to space constraints, we prioritized presenting the experimental results after low-frequency zero-sequence circulating current suppression to ensure that our main findings are detailed thoroughly. It is essential to clarify that Figs. 10–13 are the experimental results after the low-frequency zero-sequence circulating current suppression.

Fig. 10 demonstrates the impacts of inductor imbalance (±5%, ±20%, and ±50%) on the line current, zero-sequence circulating current, and common mode voltage using the ZCMV method. As discussed in Section IV, unbalanced inductance adds extra voltages to the original common mode voltage, with the amplitude directly proportional to the imbalance degree. Indeed, Fig. 10 shows that the additional common mode voltage amplitudes increase with higher imbalance rates. Particularly, at a 50% imbalance, which is a hypothetical scenario for coordinated PWM schemes, a significant increase in common mode voltage is observed. Significantly, as illustrated in Fig. 10(f), within typical manufacturing tolerances (20%), the ZCMV scheme maintains optimal common mode voltage, which is less than a 10% performance degradation. Moreover, any observed common mode voltage in the ZCMV scheme corresponds to the additional common mode voltage injected by the imbalance inductance. Therefore, Fig. 10(c) and (f) validates that within the typical manufacturer tolerances, despite some impact, existing coordinated PWM schemes ensure less than a 10% increase in common mode voltage, almost maintaining their original levels under balanced inductance.

Additionally, Fig. 10(a), (d), and (g) shows that line current quality deteriorates with increasing imbalance. A significant ripple in line current is observed at 50% imbalance, a hypothetical extreme for coordinated schemes. However, the impact of unbalanced inductance on the high-frequency zero-sequence circulating current is relatively marginal, as evidenced by Fig. 10(b), (e), and (h), zero-sequence circulating current peaks increase marginally across all imbalance levels.

Fig. 11 presents experimental results for HPDPWM with different inductor imbalances (±5%, ±20%, and ±50%). Higher imbalances lead to significant deviations in actual vectors from their ideal ones, exacerbating line current ripples. Since HPDPWM primarily relies on the nearest three vectors to minimize line current ripples, it is more susceptible to actual vectors'

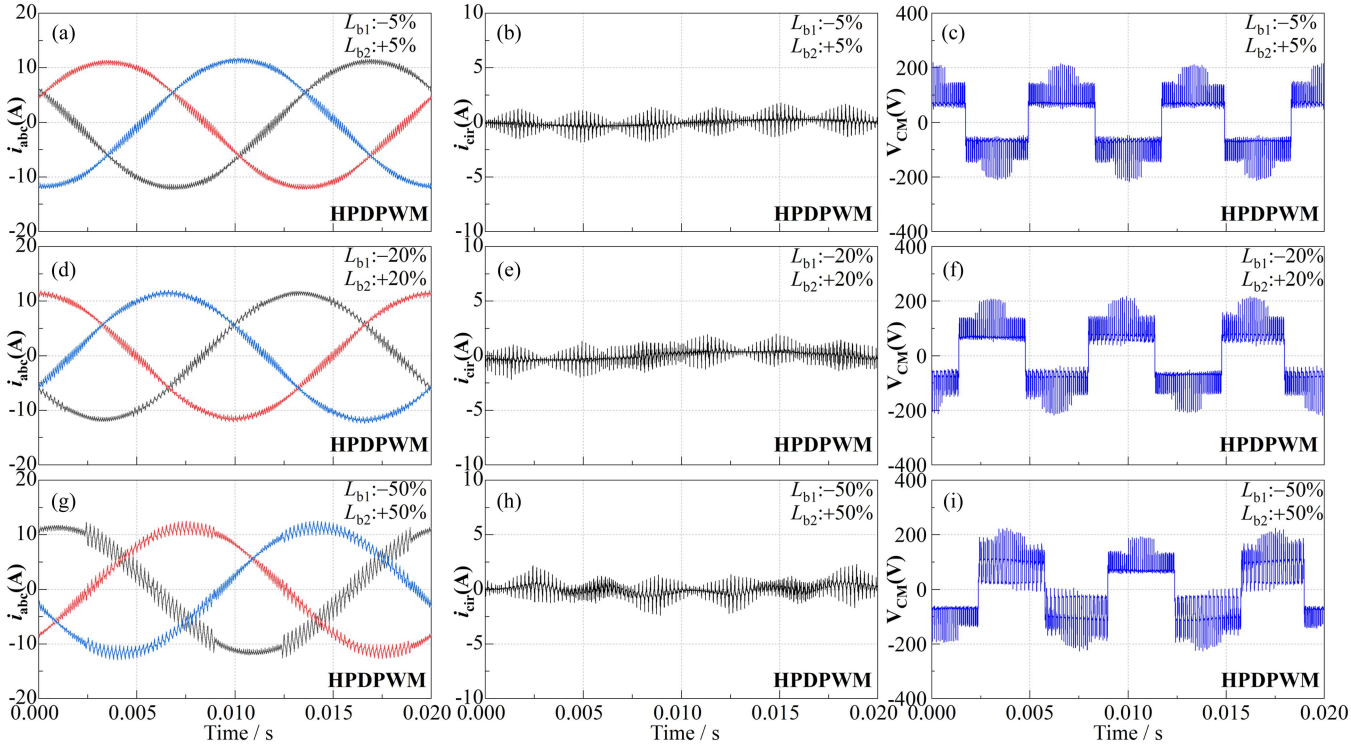

Fig. 11. Experimental output currents, zero-sequence circulating current and common mode voltage of the existing **HPDPWM** at $M = 0.6$ and $f = 5$ kHz. (a)–(c) $L_{b1} = -5\%/L_{b2} = 5\%$. (d)–(f) $L_{b1} = -20\%/L_{b2} = 20\%$. (g)–(i) $L_{b1} = -50\%/L_{b2} = 50\%$.

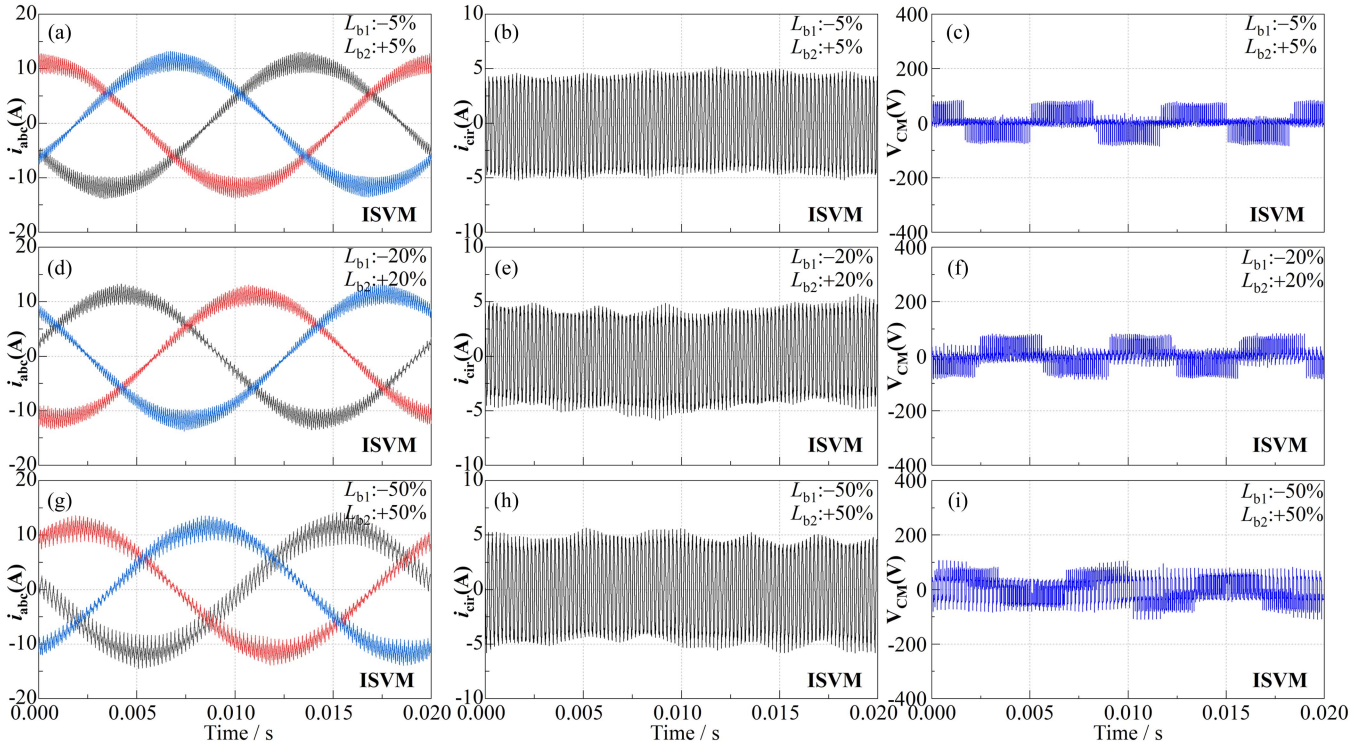

Fig. 12. Experimental output currents, zero-sequence circulating current and common mode voltage of the existing **ISVM** at $M = 0.6$ and $f = 5$ kHz. (a)–(c) $L_{b1} = -5\%/L_{b2} = 5\%$. (d)–(f) $L_{b1} = -20\%/L_{b2} = 20\%$. (g)–(i) $L_{b1} = -50\%/L_{b2} = 50\%$.

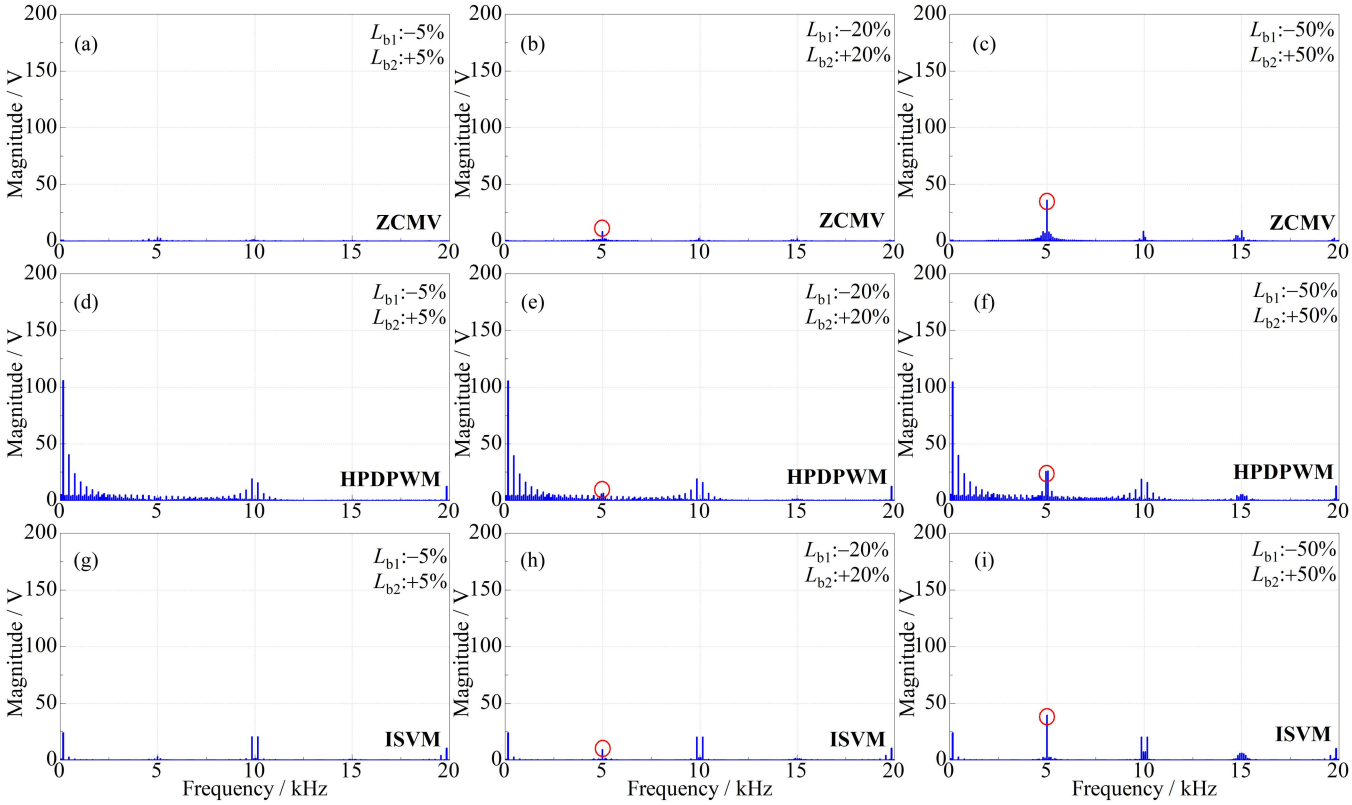

Fig. 13. Spectrums of the experimental common mode voltage of three representative PWM schemes. (a)–(c) ZCMV, (d)–(f) HPDPWM, and (g)–(i) ISVM under three typical imbalanced ratios: $L_{b1} = -5\%/L_{b2} = 5\%$, $L_{b1} = -20\%/L_{b2} = 20\%$, and $L_{b1} = -50\%/L_{b2} = 50\%$.

oscillations resulting from imbalanced inductance. Fig. 11(a), (d), and (g) demonstrates that increased imbalances result in more pronounced line current ripples, indicating a decline in line current quality. Notably, at a ±50% imbalance, a hypothetical extreme, line currents exhibit severe ripples. Importantly, the minor current ripple difference between Fig. 11(a) and (d) confirm that despite some impacts, the nearest-three-vector scheme remains largely consistent on the equivalent vector plane within the typical manufacturer tolerance (20%). Additionally, at this 20% tolerance, the common mode voltage remains consistent with that observed at 5% imbalance, without any significant increase in additional common mode voltage. Furthermore, as Fig. 11(b), (e), and (h) shows that zero-sequence circulating current only marginally increases across all levels of imbalance, aligning with our analysis.

Our analysis highlights that inductance imbalance affects the switching-related indicators for both centralized and decentralized systems. Fig. 12 displays the line current, zero-sequence circulating current, and common mode voltages within a decentralized system employing an independent modulation scheme (ISVM) with different inductor imbalances (±5%, ±20%, and ±50%). Notably, the decentralized system responds to inductance imbalance similarly to coordinated PWM schemes. Fig. 12 indicates that the line current quality of the ISVM worsens as the inductance imbalance increases. This is particularly evident at a 50% imbalance [Fig. 12(g)], in stark contrast to the less severe imbalances shown in Fig. 12(a) and (d).

Moreover, imbalanced inductance leads to an increase in common mode voltage beyond its original $\pm \boldsymbol{V}_{\mathbf{dc}}/6$. At a 50% imbalance, the amplitude of the common mode voltage rises nearly 30% compared to a 5% imbalance, introducing additional voltage stress and potential safety hazards. Fig. 12(i) shows that at 50% imbalance, the common mode voltage waveform becomes bipolar, indicating a significantly larger dv/dt. In contrast, the common mode voltage appears unipolar with lower imbalances. Additionally, Fig. 12(b), (e), and (h) demonstrates that zero-sequence circulating currents are minimally affected across all levels of imbalance, consistent with our analysis of their resilience to high-frequency disturbances.

Previous research concluded that decentralized systems could withstand inductance imbalances from 50% to 70%, based on their suppression of low-frequency zero-sequence circulating currents. However, Fig. 12 confirms that a 50% imbalance leads to increased common mode voltage and intensified rate of change (dv/dt) and EMI issues. These findings question prior understanding about the tolerance of decentralized systems to high inductance imbalances, underscoring the importance of monitoring switching-related indicators like line current ripples, common mode voltage, and dv/dt in the ISVM.

To further facilitate understanding of the impact of inductance imbalance on the common mode voltage, Fig. 13(a)–(i) illustrates the spectra of the common mode voltages for ZCMV, HPDPWM, and ISVM under three typical imbalance ratios. It can be observed that the switching-frequency-related component

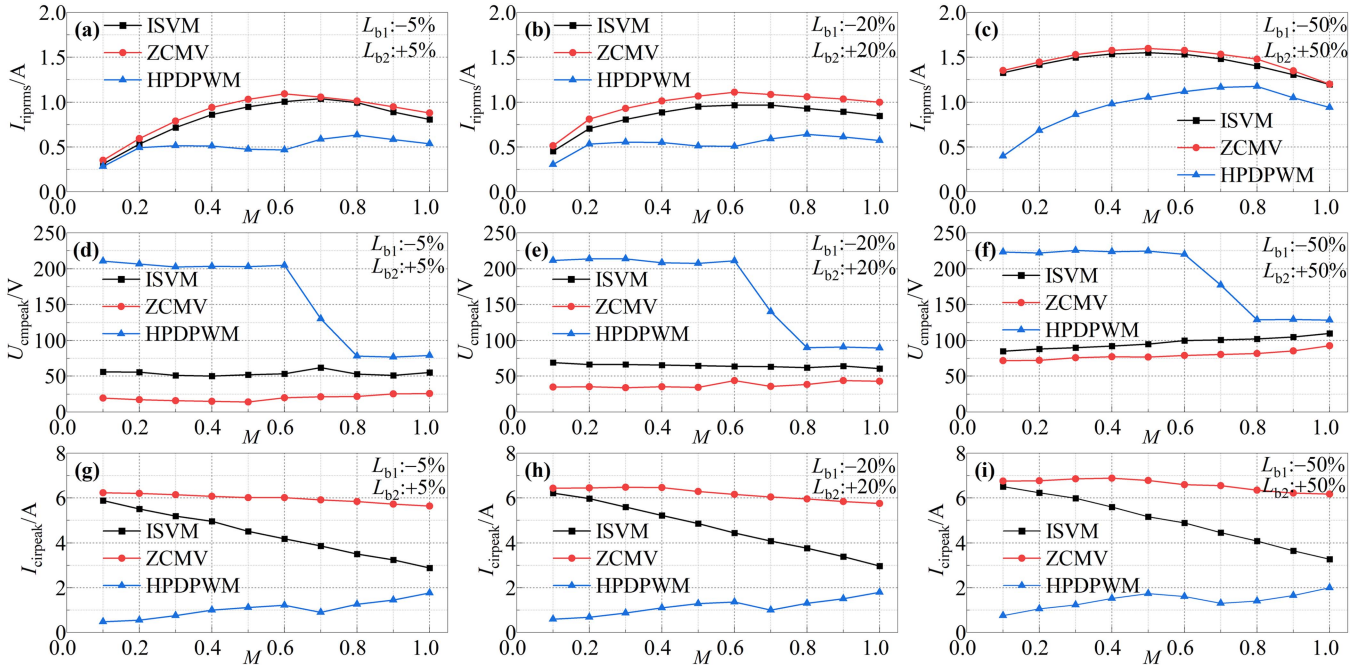

Fig. 14. Experimental output currents, zero-sequence circulating current, and common mode voltage of the three modulation methods under three different imbalance percentages. (a)–(c) Line current quality. (d)–(f) Common mode voltage peaks. (g)–(i) Zero-sequence circulating current peaks.

(5 kHz) increases with an increasing imbalance ratio. This observation is consistent with the common mode voltage waveforms presented in Fig. 10–12, where a high dv/dt is observed with increasing imbalance ratios.

To comprehensively evaluate the impact of the unbalanced inductance on the switching-related performance indicators, a series of tests were conducted with three methods under various modulation indices and three different imbalance percentages. Fig. 14 presents a detailed examination of the experimental results across three modulation methods. Fig. 14(a)–(c) compares the line current quality of three modulation methods under three different imbalance percentages. Our analysis reveals that the nearest three-vector was anticipated to be maintained if the imbalance was up to around 20%. Fig. 14(a)–(c) substantiates this analysis and confirm consistent line current quality between an imbalance of ±5% and ±20%. However, at ±50% imbalance, there is a marked deterioration for all methods, which indicates that independent PWM schemes are less tolerant to high inductance imbalance than previously believed. It is also crucial to note that, in terms of line current ripples, HPDPWM, which originally targeted minimizing line current ripples, stands out across all imbalance percentages compared to the independent PWM scheme and the ZCMV method.

Fig. 14(d)–(f) visualizes the common mode voltage peaks across the three methods. Specifically, we can observe how the ZCMV method responds to increasing imbalance, which is designed to achieve zero common mode voltage. The ZCMV method nears its optimization target at an imbalance of up to 20%, and it can effectively work within the typical manufacturer tolerance. However, with the 50% imbalance inductance that is typical in decentralized systems, the ISVM suffers from large common mode voltages, leading to additional voltage stress and EMI concerns.

Fig. 14(g)–(i) illustrates the zero-sequence circulating current peaks for each modulation method under three different imbalances. The prior analysis hinted at the minimal influence of unbalanced inductance on high-frequency zero-sequence circulating currents, especially when compared to its impact on CMV and line current ripples. Those figures further solidify this observation, illustrating a marginal increase in zero-sequence circulating current peaks with increased imbalance.

Together, these results offer a profound understanding of how an unbalanced inductance affects the switching-related performance indicators in both centralized and decentralized systems.

VII. Conclusion

This article aims to comprehensively analyze the impact of an unbalanced inductance on the switching-related indicators. The main findings reveal that inductance imbalance introduces additional common mode voltage proportional to the imbalance degree, affecting the performance of switching-related indicators in both centralized and decentralized systems. Specifically, imbalances below 20% cause minor additional common mode voltages, allowing coordinated PWM schemes to function effectively within the typical 20% manufacturing tolerance of centralized systems. However, imbalances of 50% and above lead to significant additional common mode voltage, challenging the previously assumed tolerance of decentralized systems to higher imbalances (50%-70%). Furthermore, inductance imbalance has less impact on high-frequency zero-sequence circulating currents, which slightly increase with higher imbalances.

Despite inductance imbalance challenges, coordinated PWM schemes are shown to outperform independent PWM schemes in managing switching-related performance indicators.

Moreover, while this article concentrates on exploring the impact of imbalanced inductance on switching-related performance indicators, it lays the groundwork for future development of more resilient PWM schemes. By introducing a model that predicts the additional common mode voltages caused by imbalanced inductance, we pave the way for innovative PWM designs that can effectively counteract these voltages. Future PWM schemes could leverage complex modulation signals, moving beyond the simplicity of current methods. Additionally, implementing these advanced schemes will necessitate the use of more powerful microcontrollers, enabling precise compensation for additional common mode voltages and mitigating the effects of inductance imbalance.

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