# A Full-Iteration Optimal Design Methodology of *CLLC* Converter With Minimized RMS Current

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***Abstract*—With the wide application of the *CLLC* converters in bidirectional electric vehicle chargers, it becomes more important to improve their performance through proper parameter design. Compared with the frequency domain model, the time-domain model can significantly improve the accuracy of converter design. However, the currently generalized operation mode analysis method requires complicated operating mode judgment and solving systems of transcendental equations, which limits its practicality. To address this issue, a discrete event-driven piecewise analytic model (DEPAM) of *CLLC* converter is proposed in this article. DEPAM obtains the transient and steady-state waveforms without the need for operating mode judgment and solving transcendental equations. Relying on DEPAM, a design methodology of the *CLLC* converter is introduced in this article, which applies the lookup table method to the normalized parameters and achieves a complete traversal of all possible parameter combinations of the *CLLC* converter. This traversal considers gain range, soft-switching, capacitor voltage stress, and rms current simultaneously. Finally, the design methodology is demonstrated through a 1 kW prototype with 98.8% peak efficiency.**

***Index Terms*—*CLLC* resonant converter, circuit simulation, optimal design, time-domain model, zero-voltage switching (ZVS).**

## NOMENCLATURE

| | |
|---|---|
| $C_1$ | Primary bus capacitance. |
| $C_2$ | Secondary bus capacitance. |
| $C_{\text{base}}$ | Base capacitance in normalization. |
| $C_{\text{oss}}$ | Output capacitor of switches. |
| $C_{r1}$ | Primary resonant capacitance. |
| $C_{r1N}$ | Normalized primary resonant capacitance. |
| $C_{r2}$ | Secondary resonant capacitance. |
| $C_{r2N}$ | Normalized secondary resonant capacitance. |
| $C_s$ | Simplified secondary capacitance. |
| $f_{\text{base}}$ | Base frequency in normalization. |
| $f_r$ | Resonant frequency. |
| $f_s$ | Switching frequency. |
| $f_n$ | Normalized switching frequency. |
| $i_{Lm}$ | Magnetizing current. |
| $i_{Lm\_k}$ | Magnetizing current in the $k$th stage. |
| $i_{Lr1}$ | Primary resonant inductor current. |
| $i_{Lr1\_k}$ | Primary resonant inductor current in the $k$th stage. |
| $i_{Lr2}$ | Secondary resonant inductor current. |
| $i_{Lr2\_k}$ | Secondary resonant inductor current in the $k$th stage. |
| $I_2$ | Output current of secondary side. |
| $I_{\text{base}}$ | Base current in normalization. |
| $I_s$ | Simplified secondary current source. |
| $j_{Lr1}$ | Normalized primary resonant inductor current. |
| $j_{Lr1\_\text{off}}$ | Normalized turn-OFF current of primary switches. |
| $j_{Lr2}$ | Normalized secondary resonant inductor current. |
| $j_{Lm}$ | Normalized magnetizing current. |
| $J_2$ | Normalized output current. |
| $k_1$ | Ratio of primary inductance. |
| $k_2$ | Ratio of secondary inductance. |
| $L_{\text{base}}$ | Base inductance in normalization. |
| $L_m$ | Magnetizing inductance. |
| $L_{mN}$ | Normalized magnetizing inductance. |
| $L_{r1}$ | Primary resonant inductance. |
| $L_{r1N}$ | Normalized primary resonant inductance. |
| $L_{r2}$ | Secondary resonant inductance. |
| $L_{r2N}$ | Normalized secondary resonant inductance. |
| $L_s$ | Converted secondary resonant inductance. |
| $m$ | Normalized voltage gain. |
| $m_{Cr1}$ | Normalized primary resonant capacitor voltage. |
| $m_{Cr2}$ | Normalized secondary resonant capacitor voltage. |
| $m_f$ | Normalized voltage gain in forward mode. |
| $m_r$ | Normalized voltage gain in reverse mode. |
| $M_1$ | Normalized input voltage. |
| $n$ | Turn ratio of transformer. |
| $p$ | Transmitting power. |
| $p_{k\_1}$–$p_{k\_4}$ | The constants in the solution of circuit equations of the $k$th stage. |
| $p_n$ | Normalized transmitting power. |
| $P_{\text{base}}$ | Base power in normalization. |
| $t_{\text{dead}}$ | Dead time. |
| $t_k$ | Start moment of the $k$th stage since zero state. |
| $t_{k\_p}$ | Triggering moment of passive event in the $k$th stage. |
| $t_{k\_a}$ | Triggering moment of active event in the $k$th stage. |

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| | |
|---|---|
| $v_{cd}$ | H-bridge voltage of secondary side. |
| $v_{C2}$ | Secondary bus capacitor voltage. |
| $v_{C2\_k}$ | Secondary bus capacitor voltage in the $k$th stage. |
| $v_{Cr1}$ | Primary resonant capacitor voltage. |
| $v_{Cr1\_k}$ | Primary resonant capacitor voltage in the $k$th stage. |
| $v_{Cr2}$ | Secondary resonant capacitor voltage. |
| $v_{Cr2\_k}$ | Secondary resonant capacitor voltage in the $k$th stage. |
| $V_1$ | DC voltage of primary side. |
| $V_2$ | DC voltage of secondary side($\bar{v}_{C2}$). |
| $V_{ab}$ | H-bridge voltage of primary side. |
| $V_{\text{base}}$ | Base voltage in normalization. |
| $\mathbf{x}$ | Vector of state variables. |
| $\mathbf{x_k}$ | Vector of state variables in the $k$th stage. |
| $Z_{\text{base}}$ | Base impedance in normalization. |
| $\delta$ | Tolerance in circuit parameter. |
| $\omega_r$ | Resonant angle frequency. |

## I. Introduction

With the promotion of new energy vehicles and the continuous development of renewable energy sources, isolated bidirectional dc–dc converters (IBDCs) are being widely applied, and there is a growing demand for their performance in the industry [1], [2], [3], [4]. Due to its symmetric structure, as shown in Fig. 1, the *CLLC* converter exhibits similar operational characteristics to the *LLC* converter in both forward and reverse modes. Consequently, the converter can achieve soft switching and high efficiency over a wide range of voltage and load conditions. Therefore, the *CLLC* converter is considered a structurally ideal topology for IBDCs, particularly in the context of bidirectional electric vehicle (EV) chargers, where it holds great potential to replace the *LLC* converter [5], [6]. To improve efficiency, the pulse frequency modulation is commonly employed for output voltage regulation, especially at high-power levels [7], [8].

Depending on whether the resonant frequencies of the primary and secondary sides are the same, the *CLLC* converter can be classified into two types: the D-type ($L_{r1}C_{r1} \neq L_{r2}C_{r2}$) and S-type ($L_{r1}C_{r1} = L_{r2}C_{r2}$), symmetric *CLLC* ($L_{r1} = n^2L_{r2}, C_{r2} = n^2C_{r1}$) is a special case of S-type and has been commonly employed to ensure uniform operation characteristics of the converter in both forward and reverse modes [9], [10]. However, even with symmetric resonant tank parameters, achieving completely consistent operational characteristics at the same power level in both forward and reverse modes is only possible if the voltage ranges of the primary and secondary sides, after considering the turn ratio of the transformer, are entirely identical. When the side with a wider voltage range serves as the power input side, the converter has a smaller gain range within the same switching frequency range. In the case of the dc–dc converter in EV charger, the battery side typically has a much wider voltage range compared to the bus side. Fig. 2 shows the gain curves of a symmetric *CLLC* converter in an EV charger from [11] at rated power of 1 kW with a fixed bus-side voltage of 400 V and a battery-side voltage of 250–450 V. It can be seen that the gain range in forward mode is significantly larger than

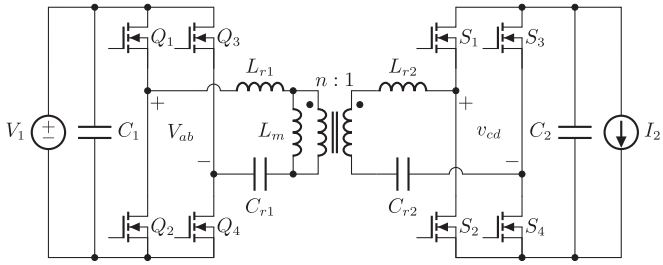



Fig. 1. Diagram of *CLLC* converter.

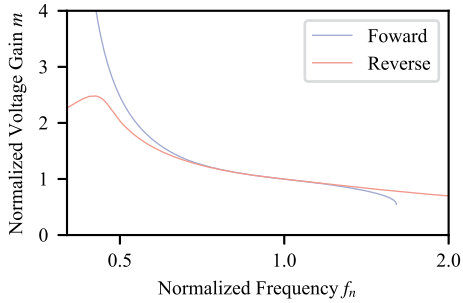



Fig. 2. Normalized voltage gains versus frequency of symmetric *CLLC* converter.

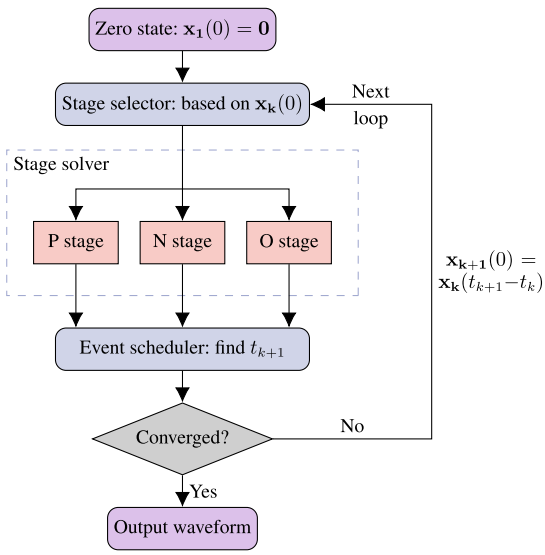



Fig. 3. Basic iteration flow of DEPAM.

that in reverse mode. The extra gain range in forward mode is wasted, which limits the freedom of design.

In order to achieve full design freedom, *CLLC* converters with arbitrary parameters should be used as design targets. Based on the parameter equivalent principle introduced in [12], any set of parameters for a D-type *CLLC* can be equivalently represented as an S-type *CLLC*, which means any *CLLC* with arbitrary parameters can be converted into an S-type *CLLC* with the same operation characteristics, and their voltage and current waveforms are entirely the same. Thus, aiming for an S-type *CLLC* design allows for the realization of full design freedom.

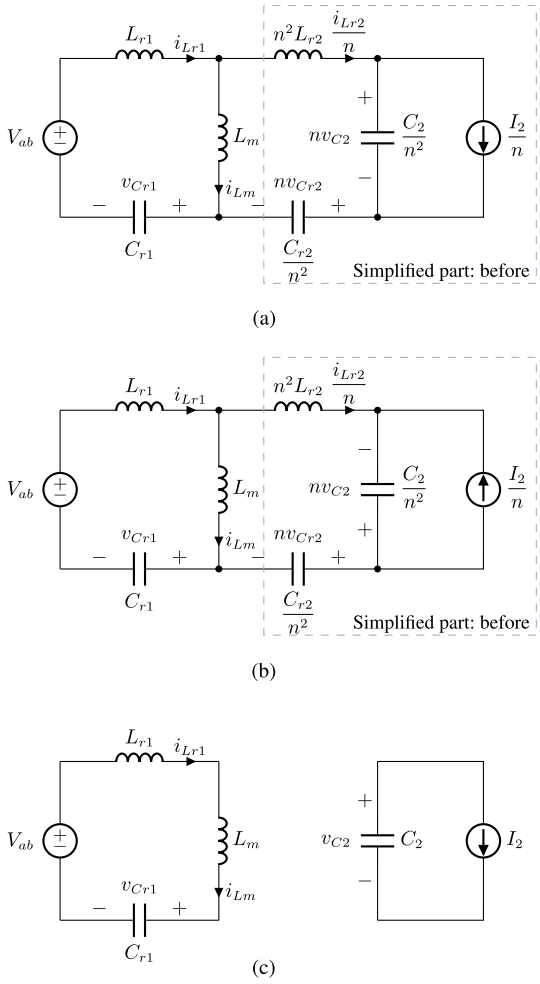



Fig. 4. Equivalent circuit of the *CLLC* resonant tank in different operating stages. (a) P stage. (b) N stage. (c) O stage.

Modeling is the foundation and core of converter design. Currently, modeling methods for *CLLC* converters can be divided into two categories: frequency domain model and time-domain model. The frequency domain modeling methods mainly include fundamental harmonic approximation (FHA) [10], [13], [14], [15] and extended describing function method [16], which is commonly used for small signal modeling. Compared to the time-domain model, the operation characteristics can be easily obtained by FHA since the analytical solution has been derived. However, the dc gain characteristic is inaccurate when the operation frequency is away from resonant frequency as it neglects higher harmonics. Time-domain model can accurately obtain the voltage and current waveforms of a *CLLC* converter, enabling an accurate prediction of the voltage gain. Another benefit is that time-domain model allows for the determination of the current at the switch turn-OFF moments, thus facilitating the assessment of the zero-voltage switching (ZVS) conditions of the converter. Therefore, for EV charger applications with wide range of voltage gain, time-domain model is more suitable.

Operation mode analysis (OMA) [9], [11], [12], as the most commonly implemented time-domain model, creates separate sets of transcendental equations for different converter operating modes to obtain all state variables in steady state. A detailed analysis adopting OMA for symmetric *CLLC* converter is introduced in [11]. The research in [12] proposed OMA for S-type *CLLC*, and with the parameters equivalent principle introduced, *CLLC* converters with arbitrary parameters can also be solved. The main task of OMA is to solve the transcendental equation set corresponding to the operation mode, which brings two challenges that reduce the practicality of OMA.

1) The operation modes of the *CLLC* converter under different operating conditions cannot be predetermined, it is necessary to perform a hypothetical operation mode and test it against the calculated results. Besides, *CLLC* has at least ten possible operation modes (OPO, PO, PN, etc.) [12], which makes mode determination time consuming and complex.
2) There are four independent state variables ($i_{Lr1}$, $i_{Lr2}$, $v_{Cr1}$, $v_{Cr2}$) in the *CLLC* resonant tank, which exist as unknowns in the solution process, plus the output voltage or the switching frequency, the number of equations in OMA is at least five. Moreover, most of the operation modes of the *CLLC* converter have multiple stages under half-switching cycle, in this case, the moment of stage switching is also unknown, so the number of equations in these operation modes is 6 or 7. It poses a higher requirement for the initial values of the iteration in numerical methods for solving those equations, and improper initial values will lead to solution failure.

In order to solve the abovementioned problems, a discrete event-driven piecewise analytic model (DEPAM) of the *CLLC* converter is proposed in this article. It iterates circuit stages from zero state, so the initial value can be set directly to zero, and the conventional requirement to determine the converter's operation mode is also eliminated. Both transient and steady-state waveforms of *CLLC* with arbitrary parameters can be obtained by DEPAM.

Based on the steady-state results of DEPAM, a full-iteration design method for S-type *CLLC* is introduced in this article, which takes the minimum average rms current under different operating conditions as the design objective and can quickly traverse the entire design space to obtain the optimal design result. Different from conventional approaches, the proposed method ensures the required bidirectional voltage gain, maximum resonant voltage limit and achievement of ZVS in the given frequency range without the analysis of parameter effects on performance.

The rest of this article is organized as follows. Section II provides the derivation of the proposed DEPAM. In Section III, the full-iteration optimal design methodology is introduced. Experimental results are provided in Section IV. Finally, Section V concludes this article and the generalization of the proposed method and the effect of parameter tolerances are discussed in Section VI.

## II. DEPAM OF *CLLC* CONVERTER

This section discusses the previously mentioned *CLLC* time-domain model, referred as DEPAM. The implementation of DEPAM is based on stage iteration, and its basic flow is shown in

TABLE I
CONDITIONS FOR STAGE SELECTION

| Secondary current | Conditions | Next stage |
|---|---|---|
| $i_{Lr2\_k}(0) \neq 0$ | $i_{Lr2\_k}(0) > 0$ | P |
| $i_{Lr2\_k}(0) \neq 0$ | $i_{Lr2\_k}(0) < 0$ | N |
| $i_{Lr2\_k}(0) = 0$ | $v_{cd\_k}(0) > v_{C2}(0)$ | P |
| $i_{Lr2\_k}(0) = 0$ | $\lvert v_{cd\_k}(0)\rvert < v_{C2}(0)$ | O |
| $i_{Lr2\_k}(0) = 0$ | $v_{cd\_k}(0) < -v_{C2}(0)$ | N |

Fig. 3. Based on the conduction states of secondary body diodes, as shown in Fig. 4, the equivalent circuit of *CLLC* referred to primary side can be divided into three operation stages, namely P stage (the body diodes of $S_1$ and $S_4$ turn-ON), N stage (the body diodes of $S_2$ and $S_3$ turn-ON), and O stage (all body diodes turn-OFF). During the $k$th stage, no switching events occur, and the input-side H-bridge voltage $V_{ab\_k}$ remains unchanged. Let $\mathbf{x}$ denote the vector of all independent state variables as

$$\mathbf{x} = [i_{Lr1}, i_{Lr2}, v_{Cr1}, v_{Cr2}, v_{C2}] \tag{1}$$

and for the $k$th stage, there is

$$\mathbf{x_k}(t - t_k) = \mathbf{x}(t), \quad t_k \leq t \leq t_{k+1} \tag{2}$$

where $t_k$ is the start moment of $k$th stage. Based on the continuity of $\mathbf{x}$, we will have

$$\mathbf{x_{k-1}}(t_k - t_{k-1}) = \mathbf{x}(t_k) = \mathbf{x_k}(0). \tag{3}$$

The stage selector use $\mathbf{x_k}(0)$ to determine which the $k$th stage is, the detailed process will be presented later. Since the iteration starts from zero state, there are $\mathbf{x_1}(0) = \mathbf{0}$ for the first stage. After stage selection, stage solver will give the analytical solution of $\mathbf{x_1}$ based on its initial value $\mathbf{x_1}(0)$. Event scheduler will then calculate the end moment of the first stage $t_2$ from the analytical solution of $\mathbf{x_1}$, which is also the start moment of the second stage. Initial values of the second stage $\mathbf{x_2}(0)$ can also be obtained by the analytical solution of $\mathbf{x_1}$ since it equals to $\mathbf{x_1}(t_2 - t_1)$.

After several iteration cycles, when the difference between values of state variables at the beginning of two consecutive switching cycles $\mathbf{x}(t_{k+1}) - \mathbf{x}(t_{k+1} - 1/f_s)$ is less than the given error limit, the iteration process is considered to have converged and the piecewise analytical waveform will be output.

### A. Stage Selector

Stage selector selects subsequent stage from P, O, and N stages, Table I presents the conditions to select the $k$th stage. The selection is based on the conduction state of the output-side body diodes at the moment of switching determined by $\mathbf{x_k}(0)$. If $i_{Lr2\_k}(0) \neq 0$, the body diodes conduction status depends on whether $i_{Lr2\_k}(0)$ is positive or negative, and if $i_{Lr2\_k}(0) = 0$, the output-side H-bridge voltage is required to determine whether the body diodes will start conduction or not, where

$$v_{cd\_k}(0) = \frac{L_m\left[V_{ab\_k} - v_{Cr1\_k}(0)\right]}{n(L_m + L_{r1})} - v_{Cr2\_k}(0). \tag{4}$$

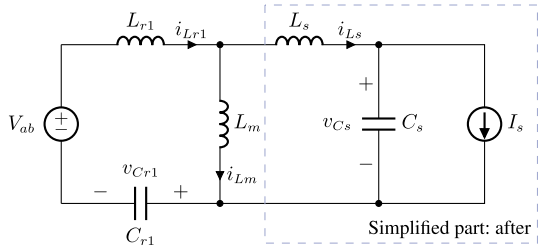



Fig. 5. Simplified equivalent circuit for P stage and N stage.

### B. Stage Solver

The purpose of the stage solver is to obtain analytical solutions for the state variables based on the initial value of state variables $\mathbf{x_k}(0)$ and circuit parameters. The derivation process of the analytic solution is different for each stage and will be described, respectively, as follows.

*1) P Stage:* As shown in Fig. 4(a), equivalent circuit of P stage consists of two independent inductors and three capacitors. In order to obtain the analytical solution, a further simplification is required. It is obvious in Fig. 4(a) that

$$i_{Lr2} = C_{r2}\frac{\mathrm{d}v_{Cr2}}{\mathrm{d}t} = C_2\frac{\mathrm{d}v_{C2}}{\mathrm{d}t} + I_2 \tag{5}$$

which can be further derived as

$$i_{Lr2} = \frac{C_{r2}C_2}{C_{r2} + C_2}\frac{\mathrm{d}(v_{Cr2} + v_{C2})}{\mathrm{d}t} + \frac{C_{r2}}{C_{r2} + C_2}I_2 \tag{6}$$

where $(v_{C2} + v_{Cr2})$ and $i_{Lr2}$ are the port voltage and port current of the simplified part in Fig. 4(a) consisting of $L_{r2}$, $C_2$, $C_{r2}$, and $I_2$, respectively. According to the form of (6), the two-port network can be externally equivalent to a parallel connection of a capacitor $C_s$ and a current source $I_s$ in the simplified equivalent circuit shown in Fig. 5. Assume the $k$th stage is P stage, the circuit parameters and state variables in Fig. 5 can be obtained as

$$\begin{cases} L_s = n^2 L_{r2} \\ C_s = \dfrac{C_{r2}C_2}{n^2(C_{r2} + C_2)} \\ I_s = \dfrac{C_{r2}}{n(C_{r2} + C_2)}I_2 \\ i_{Ls\_k} = \dfrac{i_{Lr2\_k}}{n} \\ v_{Cs\_k} = n(v_{Cr2\_k} + v_{C2\_k}). \end{cases} \tag{7}$$

According to Kirchhoff's circuit laws, state equations of the simplified circuit shown in Fig. 5 can be derived as

$$\begin{cases} \dfrac{\mathrm{d}i_{Lr1\_k}}{\mathrm{d}t} = \dfrac{(L_m + L_s)(V_{ab\_k} - v_{Cr1\_k}) - L_m v_{Cs\_k}}{L_{r1}L_s + L_{r1}L_m + L_sL_m} \\ \dfrac{\mathrm{d}i_{Ls\_k}}{\mathrm{d}t} = \dfrac{L_m(V_{ab\_k} - v_{Cr1\_k}) - (L_{r1} + L_m)v_{Cs\_k}}{L_{r1}L_s + L_{r1}L_m + L_sL_m} \\ \dfrac{\mathrm{d}v_{Cr1\_k}}{\mathrm{d}t} = \dfrac{i_{Lr1\_k}}{C_{r1}} \\ \dfrac{\mathrm{d}v_{Cs\_k}}{\mathrm{d}t} = \dfrac{i_{Ls\_k} - I_s}{C_s}. \end{cases} \tag{8}$$

Since (8) is a set of first-order differential equations with four state variables, a fourth-order differential equation can be

derived from (8) as

$$a v_{Cs\_k}^{(4)} + b v_{Cs\_k}'' + v_{Cs\_k} = 0 \tag{9}$$

where

$$\begin{aligned} a &= (L_{r1}L_s + L_{r1}L_m + L_sL_m)C_{r1}C_s \\ b &= (L_{r1} + L_m)C_{r1} + (L_s + L_m)C_s. \end{aligned} \tag{10}$$

The roots of the characteristic equation can be obtained from the root formula as

$$\begin{cases} \lambda_1^2 = \lambda_2^2 = \dfrac{-b + \sqrt{b^2 - 4a}}{2a} \\ \lambda_3^2 = \lambda_4^2 = \dfrac{-b - \sqrt{b^2 - 4a}}{2a} \end{cases} \tag{11}$$

where

$$\begin{aligned} b^2 - 4a = [(L_{r1} + L_m)C_{r1} - (L_s + L_m)C_s]^2 \\ + 4L_m^2 C_{r1}C_s > 0. \end{aligned} \tag{12}$$

It is obvious that $\sqrt{b^2 - 4a} < b$, so the four eigenvalues are pure imaginary and can be expressed as $\lambda_{1,2} = \pm\omega_1 i$ and $\lambda_{3,4} = \pm\omega_2 i$ where

$$\begin{cases} \omega_1 = \sqrt{\dfrac{b - \sqrt{b^2 - 4a}}{2a}} \\ \omega_2 = \sqrt{\dfrac{b + \sqrt{b^2 - 4a}}{2a}}. \end{cases} \tag{13}$$

The general solution of $v_{Cs\_k}$ can be obtained from the eigenvalues, and then according to (8), the analytic solutions of the state variables in the simplified equivalent circuit can be expressed as (14) shown at the bottom of this page, where $p_{k\_1} - p_{k\_4}$ are arbitrary constants. And $p_{k\_1} - p_{k\_4}$ can be solved by substituting $\mathbf{x_k}(0)$ into (14). So far we have obtained the analytical solutions of state variables in the simplified equivalent circuit. In order to map the state variables back to obtain the solutions of $v_{Cr2\_k}$ and $v_{C2\_k}$, the charge conservation principle of the capacitor needs to be used. Since $\mathbf{x_k}(0)$ are mapped to the simplified equivalent circuit when $t = 0$, there are

$$\begin{aligned} C_s\left[v_{Cs\_k}(t) - v_{Cs\_k}(0)\right] &= \int_0^t i_{Ls\_k}(t)\,dt \\ &= \int_0^t \frac{i_{Lr2\_k}(t)}{n}\,dt = \frac{C_{r2}}{n}\left[v_{Cr2\_k}(t) - v_{Cr2\_k}(0)\right] \end{aligned} \tag{15}$$

then the solutions of $v_{Cr2}$ and $v_{C2}$ can be obtained in

$$\begin{cases} v_{Cr2\_k}(t) = \dfrac{nC_s}{C_{r2}}\left[v_{Cs\_k}(t) - v_{Cs\_k}(0)\right] + v_{Cr2\_k}(0) \\ v_{C2\_k}(t) = \dfrac{v_{Cs\_k}(t)}{n} - v_{Cr2\_k}(t) \end{cases} \tag{16}$$

while the remaining state variables can be obtained by (14).

*2) N Stage:* As shown in Fig. 4(a), equivalent circuit of N stage is very similar to that of P stage, so it can also be simplified to the circuit also shown in Fig. 5. When using this equivalent circuit for N stage solution, due to the flip of rectifier polarity in N stage, it is necessary to replace expressions containing $I_2$ and $v_{C2\_k}$ in (7) and (16) with

$$\begin{cases} I_s = -\dfrac{C_{r2}}{n(C_{r2} + C_2)} I_2 \\ v_{Cs\_k} = n(v_{Cr2\_k} - v_{C2\_k}) \end{cases} \tag{17}$$

and

$$v_{C2\_k}(t) = -\frac{v_{Cs\_k}(t)}{n} + v_{Cr2\_k}(t) \tag{18}$$

respectively, and rest of the solution process is the same.

*3) O Stage:* As shown in Fig. 4(c), the equivalent circuit of O stage is much simpler than that of P stage and N stage. The solution here is directly given by

$$\begin{cases} i_{Lr1\_k}(t) = i_{Lr1\_k}(0)\cos(\omega t) + [V_{ab\_k} - v_{Cr\_k}(0)] \\ \qquad \sin(\omega t)/\left[(L_{r1} + L_m)\omega\right] \\ i_{Lr2\_k}(t) = 0 \\ i_{Lm\_k}(t) = i_{Lr1\_k}(t) \\ v_{Cr1\_k}(t) = (L_{r1\_k} + L_m)i_{Lr1\_k}(t)\omega\sin(\omega t) \\ \qquad -[V_{ab\_k} - v_{Cr\_k}(0)]\cos(\omega t) + V_{ab\_k} \\ v_{Cr2\_k}(t) = v_{Cr2\_k}(0) \\ v_{C2\_k}(t) = v_{C2\_k}(0) - I_2 t/C_2 \end{cases} \tag{19}$$

where $\omega = 1/\sqrt{(L_{r1} + L_m)C_{r1}}$.

### C. Event Scheduler

In DEPAM, the end of a stage is treated as an event, and the moment of event triggered is the end moment of the stage. For $k$th stage, the purpose of event scheduler is to obtain its end moment $t_{k+1}$, which is also the start moment of $(k+1)$th stage and triggering time of the event. Events in DEPAM can be classified as active and passive events. Active events are the switching actions of the input side H-bridge, their triggering moments $t_{k\_a}$ are determined by the control method. Passive events are changes in circuit structure due to the conduction state changes of the output side body diodes.

$$\begin{cases} v_{Cs\_k}(t) = p_{k\_1}\sin(\omega_1 t) + p_{k\_2}\cos(\omega_1 t) + p_{k\_3}\sin(\omega_2 t) + p_{k\_4}\cos(\omega_2 t) \\ i_{Ls\_k}(t) = C_s\left[p_{k\_1}\omega_1\cos(\omega_1 t) - p_{k\_2}\omega_1\sin(\omega_1 t) + p_{k\_3}\omega_2\cos(\omega_2 t) - p_{k\_4}\omega_2\sin(\omega_2 t)\right] + I_s \\ v_{Cr1\_k}(t) = V_{ab\_k} - C_s\left[L_m - (L_{r1} + L_m)(L_s + L_m)/L_m\right]\left[p_{k\_1}\omega_1^2\sin(\omega_1 t) + p_{k\_2}\omega_1^2\cos(\omega_1 t) + p_{k\_3}\omega_2^2\sin(\omega_2 t)\right. \\ \qquad \left. + p_{k\_4}\omega_2^2\cos(\omega_2 t)\right] - \left[p_{k\_1}\sin(\omega_1 t) + p_{k\_2}\cos(\omega_1 t) + p_{k\_3}\sin(\omega_2 t) + p_{k\_4}\cos(\omega_2 t)\right](L_s + L_m)/L_m \\ i_{Lr1\_k}(t) = C_{r1}\left\{C_s\left[L_m - (L_{r1} + L_m)(L_s + L_m)/L_m\right]\left[p_{k\_1}\omega_1^3\cos(\omega_1 t) - p_{k\_2}\omega_1^3\sin(\omega_1 t) + p_{k\_3}\omega_2^3\cos(\omega_2 t)\right.\right. \\ \qquad \left.\left. - p_{k\_4}\omega_2^3\sin(\omega_2 t)\right] - \left[p_{k\_1}\omega_1\cos(\omega_1 t) - p_{k\_2}\omega_1\sin(\omega_1 t) + p_{k\_3}\omega_2\cos(\omega_2 t) - p_{k\_4}\omega_2\sin(\omega_2 t)\right](L_s + L_m)/L_m\right\}. \end{cases} \tag{14}$$

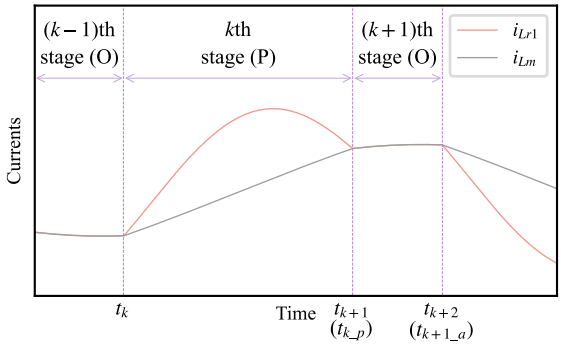



Fig. 6. First triggered event selection.

For P stage and N stage, $i_{Lr2\_k}$ is the current flowing through the body diodes, so the conduction state changes when $i_{Lr2\_k}$ crosses zero. And the triggering moment $t_{k\_p}$ can be obtained by solving

$$i_{Lr2\_k}(t_{k\_p} - t_k) = 0, (t_{k\_p} > t_k) \tag{20}$$

and for O stage, the body diodes are in the off state, their conduction state changes when they start conduction, which means the triggering moment $t_{k\_p}$ in O stage can be obtained by solving

$$|v_{cd\_k}(t_{k\_p} - t_k)| = v_{C2\_k}(t_{k\_p} - t_k), (t_{k\_p} > t_k). \tag{21}$$

Unfortunately, numerical methods need to be employed since they are transcendental equations. Specifically, we need to search for the minimum solution of $t_{k\_p}$, first using the dichotomous method to determine the interval of $t_{k\_p}$, and then using the Newton's method to obtain the exact value.

For each stage, only the event with an earlier trigger moment will be triggered while the other will become nothing. The trigger moment will be the stage's end moment, which means the start moment of $(k+1)$th stage can be obtained as

$$t_{k+1} = \min(t_{k\_a}, t_{k\_p}). \tag{22}$$

As shown in Fig. 6, the passive event of $k$th stage is earlier so it is triggered and $t_{k\_p}$ turn into the end moment of $k$th stage $t_{k+1}$.

### *D. Output Waveform*

In order for DEPAM to output waveform after convergence, the constants in analytic solutions $p_{k\_1} - p_{k\_4}$ and $V_{ab\_k}$ of each stage need to be saved during the iteration. Since the analytic solution $\mathbf{x_k}$ of each stage is known, $\mathbf{x}(t)$ at any moment can then be obtained by (2), thus, DEPAM can output waveforms with arbitrary time step.

There is a *CLLC* converter with parameters presented in Table II. Its open-loop start-up transient waveforms can be obtained, as shown in Fig. 7. Steady-state waveforms can be obtained after the iterative process converged. It can be seen that there is almost no difference between DEPAM and commercial simulation tool. Meanwhile, a comparison of the gain curves at 1 kW power is shown in Fig. 8, which indicates that the gain curves derived from DEPAM have a higher accuracy compared to FHA.

Since the analytical solution for each stage has been obtained, it only needs to be calculated once for each stage in DEPAM, which can significantly speed up the waveform solution. The comparison of computation time is shown in Table III, tests were performed using a desktop computer equipped with AMD Ryzen 7 3700X 3.6-GHz processor and 16-GB RAM. It can be seen that the solution time of DEPAM is much less than that of commercial simulation software.

TABLE II
*CLLC* PARAMETERS OF THE OUTPUT WAVEFORM

| Symbol | Parameter description | Value |
|---|---|---|
| $U_1$ | Input voltage | 400 V |
| $f_s$ | Switching frequency | 100 kHz |
| $n$ | Turn ratio | 1.15 |
| $L_{r1}$ | Primary resonant inductor | 83.2 μH |
| $L_{r2}$ | Secondary resonant inductor | 86.4 μH |
| $L_m$ | Magnetizing inductor | 490 μH |
| $C_{r1}$ | Primary resonant capacitor | 41.5 nF |
| $C_{r2}$ | Secondary resonant capacitor | 39.9 nF |
| $C_2$ | Output capacitor | 5 μF |
| $I_2$ | Load current | 4 A |

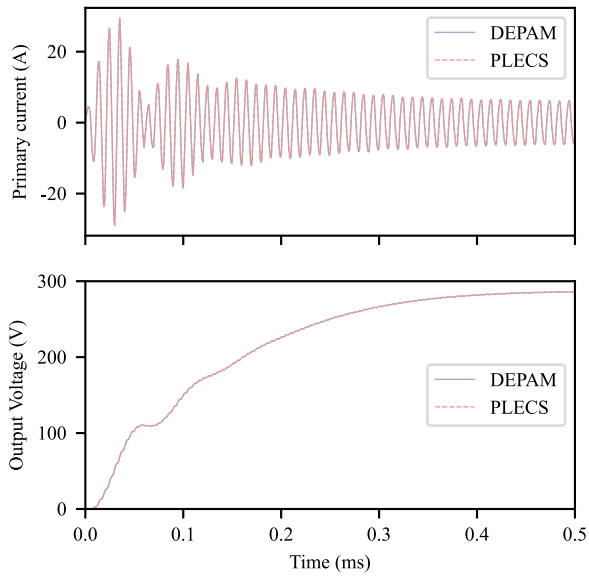



Fig. 7. Waveform comparison between DEPAM and PLECS simulation software.

TABLE III
TIME CONSUMPTION COMPARISON BETWEEN DEPAM AND COMMERCIAL SIMULATION TOOLS

| Method | Simulation time | Relative tolerance | Time |
|---|---|---|---|
| MATLAB/Simulink | 10 ms | 1e−6 | 6657 ms |
| PLECS | 10 ms | 1e−6 | 2750 ms |
| DEPAM | 10 ms | 1e−6 | 90 ms |

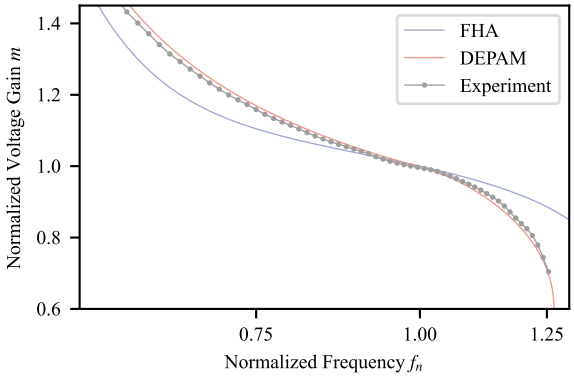



Fig. 8. Voltage gain comparison between FHA, DEPAM, and experiment.

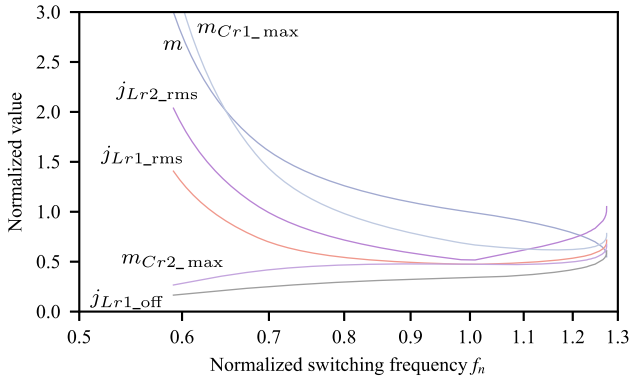



Fig. 9. Normalized attribute curves for $k_1 = 3$, $k_2 = 3$, and $p_n = 0.3$ in forward mode.

## III. Design Methodology

In this section, a parameter design method for S-type *CLLC* based on DEPAM will be proposed. With the concept of normalization and piecewise linearity, this design method has a very fast traversal speed and can complete the traversal of all possible parameter combinations of S-type *CLLC* in a short time, and then obtain the optimal design of *CLLC* parameters.

### A. Normalization

In order to make the design method generic, normalized parameters are used in the process. First, there are three main bases for normalization in forward mode as

$$\begin{cases} V_{\text{base}} = V_1 \\ L_{\text{base}} = L_{r1} \\ C_{\text{base}} = C_{r1} \end{cases} \tag{23}$$

while the other bases can be obtained as

$$\begin{cases} Z_{\text{base}} = \sqrt{L_{\text{base}}/C_{\text{base}}} \\ I_{\text{base}} = V_{\text{base}}/Z_{\text{base}} \\ P_{\text{base}} = V_{\text{base}} I_{\text{base}} \\ f_{\text{base}} = 1/\left(2\pi\sqrt{L_{\text{base}} C_{\text{base}}}\right) = f_r. \end{cases} \tag{24}$$

Denote the normalized transfer power as

$$p_n = p/P_{\text{base}}. \tag{25}$$

Then, we have the normalized parameters of S-type *CLLC* in

$$\begin{cases} L_{r1N} = 1 \\ C_{r1N} = 1 \\ L_{mN} = L_m/L_{r1} = k_1 \\ L_{r2N} = n^2 L_{r2}/L_{r1} = n^2 L_{r2} k_1/L_m = k_1/k_2 \\ C_{r2N} = 1/L_{r2N} = k_2/k_1 \\ M_1 = V_1/V_{\text{base}} = 1 \\ J_2 = I_2/(nI_{\text{base}}) = p/(mV_{\text{base}} I_{\text{base}}) = p_n/m \\ f_n = f_s/f_r \end{cases} \tag{26}$$

where $m = nV_2/V_1$ refers to the normalized voltage gain, and state variables are normalized as

$$\begin{cases} j_{Lr1} = i_{Lr1}/I_{\text{base}} \\ j_{Lr2} = i_{Lr2}/(nI_{\text{base}}) \\ j_{Lm} = j_{Lr1} - j_{Lr2} \\ m_{Cr1} = m_{Cr1}/V_{\text{base}} \\ m_{Cr2} = nm_{Cr2}/V_{\text{base}}. \end{cases} \tag{27}$$

Since the above are all the input circuit parameters required by DEPAM to obtain the steady waveform, it is clear that the normalized steady state waveform is determined by $k_1$, $k_2$, $p_n$, and $m$. It should be noted that $f_n$ is not an independent variable since it is directly related to $m$.

### B. Piecewise Linear Curves

For S-type *CLLC* converter, there are five free design parameters, namely $n$, $L_{r1}$, $L_{r2}$, $L_m$, $C_{r1}$. It is hard to iterate those all five variables directly, even single design result must be calculated many times under different operation conditions. It has been proved that the normalized gain curve can be obtained by sweeping $m$ under the given $k_1$, $k_2$, and $p_n$. In order to reuse calculation results, which can save much time, a normalized gain curves library will be introduced here. Through it the operating characteristics of the given converter parameters can be quickly obtained.

For every combination of $k_1$, $k_2$, $p_n$, as shown in Fig. 9, gain curve is determined and need to be obtained, respectively. In order for the design results to meet the design specifications, there are totally seven attributes should be conducted from the waveform, namely $m$, $f_n$, $j_{Lr1\_rms}$, $j_{Lr2\_rms}$, $m_{Cr1\_max}$, $m_{Cr2\_max}$, and $j_{Lr1\_off}$, where $m$ and $f_n$ is to ensure the frequency range can be met, $j_{Lr1\_rms}$ and $j_{Lr2\_rms}$ is to achieve the minimum rms current, $m_{Cr1\_max}$ and $m_{Cr2\_max}$ is to ensure the maximum capacitor voltage, $j_{Lr1N\_off}$ is to guarantee ZVS.

The combination of $k_1$, $k_2$, $p_n$ is the label of curves, and to ensure accuracy and general availability, sufficiently large database consists of curves from different labels should be established. Range of parameters shown in Table IV would cover most situations, that ends up with 264 191 combinations.

TABLE IV
RANGE OF PARAMETERS FOR DATABASE

| Parameter | Minimal value | Step | Maximum value |
|---|---|---|---|
| $k_1$ | 2 | 0.1 | 8 |
| $k_2$ | 2 | 0.1 | 8 |
| $p_n$ | 0.1 | 0.01 | 0.8 |

TABLE V
DESIGN SPECIFICATIONS FOR *CLLC* RESONANT CONVERTER

| Parameter | Symbol | Value |
|---|---|---|
| Primary dc voltage | $V_1$ | 400 V |
| Secondary dc voltage | $V_{2\_\min}$–$V_{2\_\max}$ | 250–450 V |
| Maximum capacitor voltage | $V_{Cr1\_\max}$,$V_{Cr2\_\max}$ | 800 V |
| Power | $p_{\min}$–$p_{\max}$ | 500–1000 W |
| Switching frequency | $f_{s\_\min}$–$f_{s\_\max}$ | 50–150 kHz |
| Dead-time | $t_{\text{dead}}$ | 200 ns |
| Switch's output capacitance | $C_{\text{oss}}$ | 80 pF |

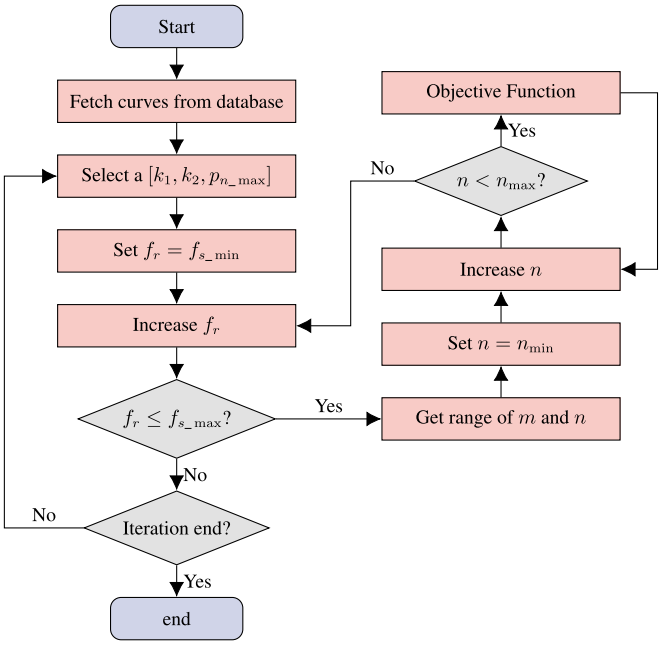



Fig. 10. Full-iteration design flow chart.

### C. Full-Iteration Method

To facilitate analysis, the five free design variables of S-type *CLLC* will be transformed into $k_1$, $k_2$, $p_{n\_\max}$, $f_r$, and $n$, where

$$p_{n\_\max} = p_{\max}/P_{\text{base}}. \tag{28}$$

A *CLLC* converter with a rated power of 1 kW has been taken as an example and the input parameters are listed in Table V, $p_{\min}$ is introduced here to represent the minimum power that can meet the voltage gain range through variable-frequency control only.

The flow chart of the design process is illustrated as Fig. 10. It can be divided into three levels of traversal loops, the top-level loops traversing all labels ($k_1$, $k_2$, $p_n$) in the curves library, the middle level loops traversing $f_r$, and the bottom level loops traversing $n$. The three loops are combined to perform a complete traversal of all five free design variables.

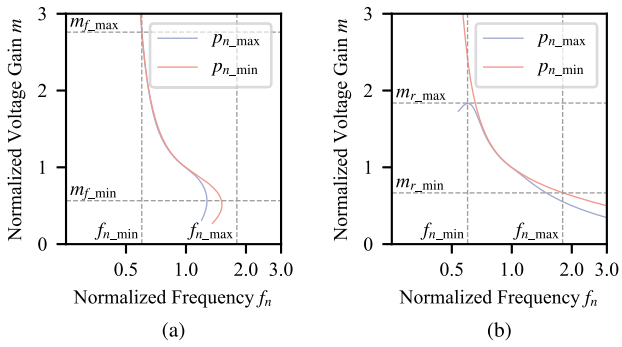



Fig. 11. Normalized voltage gain range from curves. (a) Forward mode. (b) Reverse mode.

In the top-level loops, we fetch all curves of different labels from database. To ensure that the voltage gain can be met in the power range, it is necessary to take the intersection of voltage gain ranges corresponding to $p_{n\_\min}$ and $p_{n\_\max}$, where the minimal normalized power is denoted as

$$p_{n\_\min} = p_{\min}/P_{\text{base}}. \tag{29}$$

Considering both forward and reverse modes, there are four gain curves of $p_{n\_\max}$ and $p_{n\_\min}$ for each top loop. In middle level loops, the range of $f_r$ is iterated from $f_{s\_\min}$ to $f_{s\_\max}$. Then, the range of $m$ can be obtained by apply the range of $f_n$ to those gain curves, namely $m_{f\_\min}$, $m_{f\_\max}$, $m_{r\_\min}$, and $m_{r\_\max}$ as Fig. 11 shows, where

$$\begin{cases} f_{n\_\min} = f_{s\_\min}/f_r \\ f_{n\_\max} = f_{s\_\max}/f_r \end{cases} \tag{30}$$

they represent the maximum and minimum gains in forward and reverse directions, respectively. It should be noted that in Fig. 11(a), smaller gain range than $m_{f\_\min}$ exists, but the controller cannot operate stably in the range under constant power load, and therefore, it is not taken into account. It can be seen from Fig. 8 that due to the parasitic parameters as well as tolerances in the circuit, there is still some error between the actual and time-domain modeled gain curves. Therefore, to ensure that the designed converter is able to meet the voltage gain requirements over the given frequency range, the gain margin needs to be set during the design process. The margins are set at 4% and 8% for the boost and step-down conditions, respectively, with a larger margin for the step-down condition due to the greater influence of parasitic parameters at high frequencies.

Since the gain range are required in both forward and reverse mode, the inequality can be obtained as

$$\begin{cases} V_1 m_{f\_\min} \le n V_{2\_\min} \\ V_1 m_{f\_\max} \ge n V_{2\_\max} \\ n V_{2\_\min} m_{r\_\max} \ge V_1 \\ n V_{2\_\max} m_{r\_\min} \le V_1 \end{cases} \tag{31}$$

TABLE VI
COMPARISON WITH PREVIOUS PARAMETER DESIGN METHODS

| References | Model | Operation mode | Accuracy | Iteration | Optimization goal | Design Variables | Complexity |
|---|---|---|---|---|---|---|---|
| [13] | FHA | P mode | ⋆⋆⋆ | No | Maximize $L_m/L_{r1}(k_1)$ | 3 | ⋆ |
| [17] | FHA | N/A | ⋆⋆ | Yes | Reduce frequency range | 4 | ⋆⋆ |
| [15] | FHA | N/A | ⋆ | No | N/A | 3 | ⋆ |
| [12] | OMA | N/A | ⋆⋆⋆⋆ | Yes | Maximize $L_m$ | 4 | ⋆⋆⋆⋆ |
| [18] | SOM | P/PO/NP modes | ⋆⋆⋆ | No | Maximize $L_m/L_r$ | 2 | ⋆ |
| This article | DEPAM | N/A | ⋆⋆⋆⋆ | Yes | Minimize rms current | 5 | ⋆⋆⋆ |

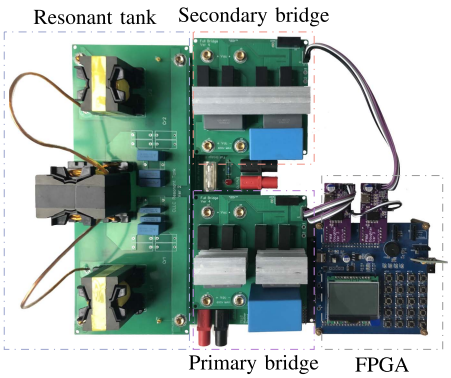



Fig. 12. *CLLC* prototype.

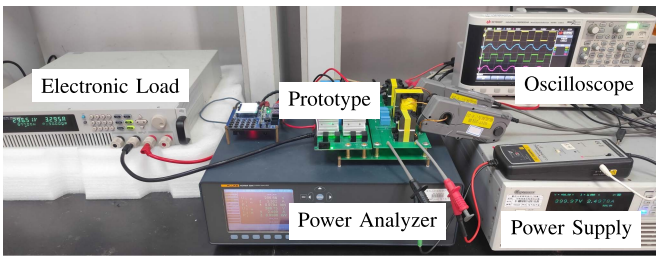



Fig. 13. Experimental test platform.

and the range of turn ratio $n$ will be

$$\begin{cases} n_{\min} = \max\left(\dfrac{m_{f\_\min}V_1}{V_{2\_\min}}, \dfrac{V_1}{m_{r\_\max}V_{2\_\min}}\right) \\ n_{\max} = \min\left(\dfrac{m_{f\_\max}V_1}{V_{2\_\max}}, \dfrac{V_1}{m_{r\_\min}V_{2\_\max}}\right). \end{cases} \tag{32}$$

Then, we can iterate $n$ from $n_{\min}$ to $n_{\max}$ in the bottom level loops, if $n_{\min} < n_{\max}$, the design variables in the loop exist and can meet the voltage gain requirements.

In order to achieve optimal design, 20 operation conditions of different $m$, $p$ and directions have been selected for the objective function while guaranteeing maximum capacitor voltage limit, ZVS and minimal rms current. Based on normalized values of capacitor voltages and switch-OFF current, the constraints for maximum capacitor voltages are

$$\begin{cases} m_{Cr1\_\max}V_{\text{base}} < V_{Cr1\_\max} \\ m_{Cr2\_\max}V_{\text{base}} < V_{Cr2\_\max} \end{cases} \tag{33}$$

TABLE VII
CIRCUIT PARAMETERS FOR COMPARATIVE EXPERIMENT

| Parameter | FHA-based | OMA-based | Proposed |
|---|---|---|---|
| $n$ | 1.1 | 1.5 | 1.15 |
| $L_m$ | 161.7 $\mu$H | 651 $\mu$H | 490 $\mu$H |
| $L_{r1}$ | 29.41 $\mu$H | 158.78 $\mu$H | 83.18 $\mu$H |
| $L_{r2}$ | 26.67 $\mu$H | 103.33 $\mu$H | 86.43 $\mu$H |
| $C_{r1}$ | 138.6 nF | 21.27 nF | 41.45 nF |
| $C_{r2}$ | 151.2 nF | 32.68 nF | 39.89 nF |

TABLE VIII
PROTOTYPE PARAMETERS FOR COMPARATIVE EXPERIMENT

| Parameter | FHA-based | OMA-based | Proposed |
|---|---|---|---|
| MOSFETs | SCT3060 | SCT3060 | SCT3060 |
| Transformer core material | PC95 | PC95 | PC95 |
| Transformer bobbin | PQ5050 | PQ5050 | PQ5050 |
| Winding wire diameter | 0.1mm | 0.1mm | 0.1mm |
| Transformer primary turns | 33 | 54 | 46 |
| Transformer primary parallel | 150 | 100 | 100 |
| Transformer secondary turns | 30 | 36 | 40 |
| Transformer secondary parallel | 150 | 100 | 100 |
| Inductor core material | PC90 | PC90 | PC90 |
| Inductor bobbin | PQ4040 | PQ4040 | PQ4040 |
| Primary inductor turns | 18 | 44 | 36 |
| Primary inductor parallel | 200 | 100 | 100 |
| Secondary inductor turns | 20 | 40 | 36 |
| Secondary inductor parallel | 200 | 100 | 100 |
| Loss angle of $C_{r1}$@100kHz | 58e−4 | 7e−4 | 8e−4 |
| Loss angle of $C_{r2}$@100kHz | 53e−4 | 9e−4 | 12e−4 |

and the constraint for forward mode to achieve ZVS can be described as

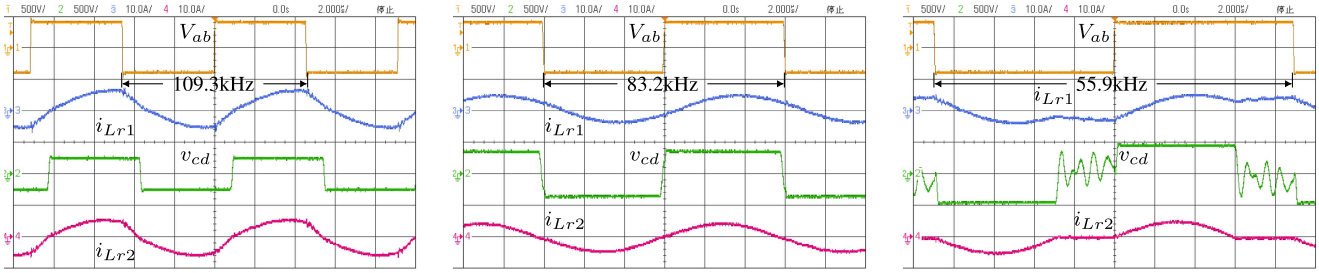
$$j_{Lr1\_\text{off}}I_{\text{base}}t_{\text{dead}} > 2V_1C_{\text{oss}} \tag{34}$$

where $I_{\text{base}} = P_{\max}/(p_nV_1)$, and for reverse mode the ZVS constraint will be

$$nj_{\text{Lr1\_off}}I_{\text{base}}t_{\text{dead}} > 2V_1C_{\text{oss}}. \tag{35}$$

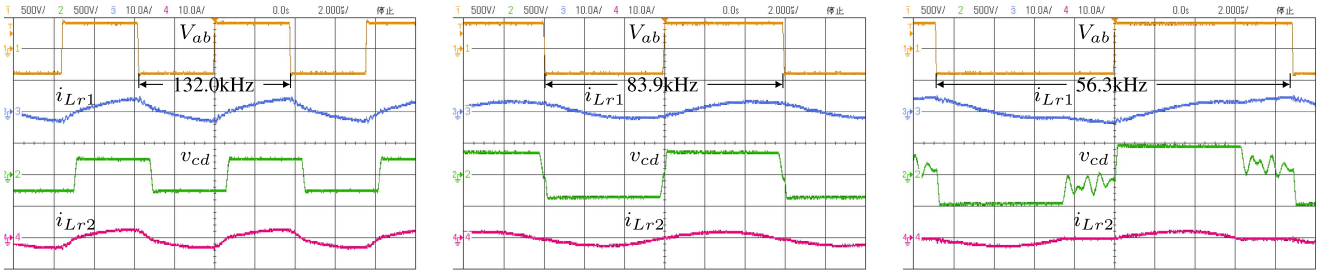
Since the circuit has been normalized to the primary side when calculating the curves. According to the expression of conduction losses, the sum of squared rms current of the both sides is selected as the objective

$$\min\ I_{\text{rms}}^2 = \sum_{k=1}^{20}(j_{\text{Lr1\_rms\_k}}^2 + j_{\text{Lr2\_rms\_k}}^2)I_{\text{base}}^2. \tag{36}$$



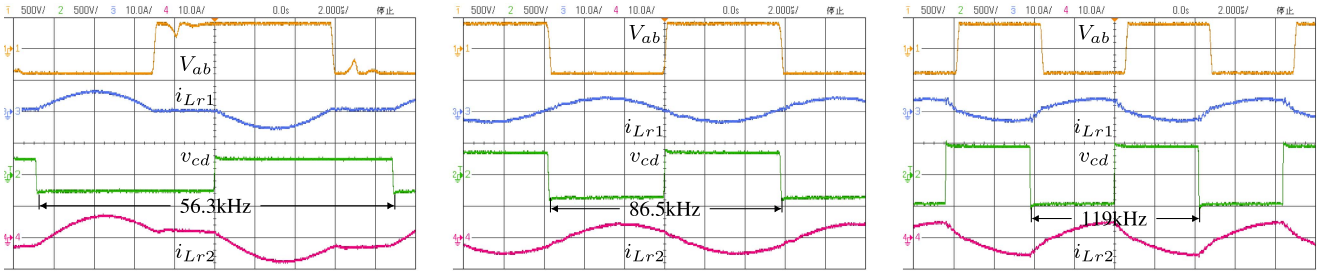

(a) (b) (c)

Fig. 14. Key waveforms of the *CLLC* prototype under 1 kW load condition in forward mode. (a) $V_1 = 400\,\mathrm{V}$, $V_2 = 250\,\mathrm{V}$, $m = 0.719$. (b) $V_1 = 400\,\mathrm{V}$, $V_2 = 350\,\mathrm{V}$, $m = 1.006$. (c) $V_1 = 400\,\mathrm{V}$, $V_2 = 450\,\mathrm{V}$, $m = 1.294$.



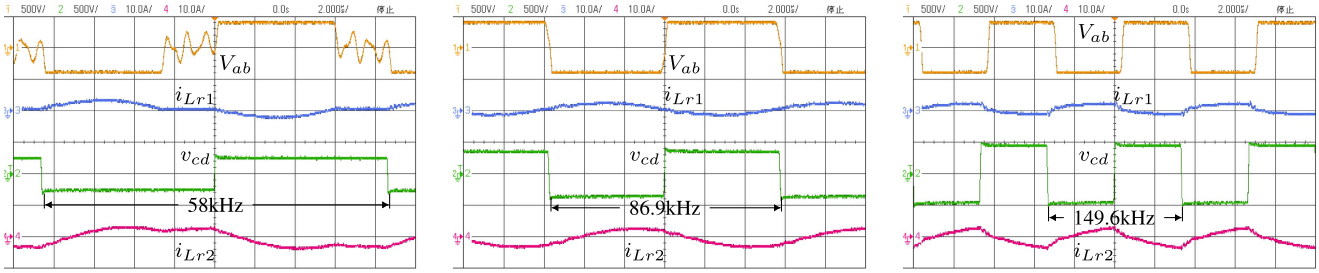

(a) (b) (c)

Fig. 15. Key waveforms of the *CLLC* prototype under 500 W load condition in forward mode. (a) $V_1 = 400\,\mathrm{V}$, $V_2 = 250\,\mathrm{V}$, $m = 0.719$. (b) $V_1 = 400\,\mathrm{V}$, $V_2 = 350\,\mathrm{V}$, $m = 1.006$. (c) $V_1 = 400\,\mathrm{V}$, $V_2 = 450\,\mathrm{V}$, $m = 1.294$.




(a) (b) (c)

Fig. 16. Key waveforms of the *CLLC* prototype under 1 kW load condition in reverse mode. (a) $V_2 = 250\,\mathrm{V}$, $V_1 = 400\,\mathrm{V}$, $m = 1.391$. (b) $V_2 = 350\,\mathrm{V}$, $V_1 = 400\,\mathrm{V}$, $m = 0.994$. (c) $V_2 = 450\,\mathrm{V}$, $V_1 = 400\,\mathrm{V}$, $m = 0.773$.




(a) (b) (c)

Fig. 17. Key waveforms of the *CLLC* prototype under 500 W load condition in reverse mode. (a) $V_2 = 250\,\mathrm{V}$, $V_1 = 400\,\mathrm{V}$, $m = 1.391$. (b) $V_2 = 350\,\mathrm{V}$, $V_1 = 400\,\mathrm{V}$, $m = 0.994$. (c) $V_2 = 450\,\mathrm{V}$, $V_1 = 400\,\mathrm{V}$, $m = 0.773$.

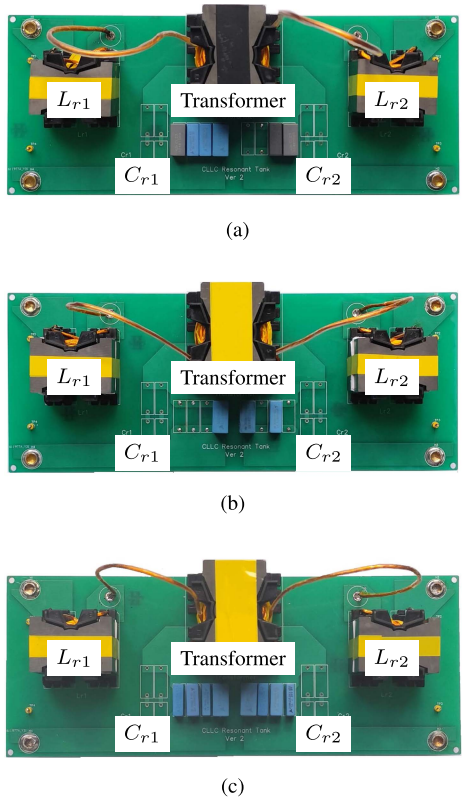



Fig. 18. Experimental resonant tanks. (a) Parameters from FHA-based method. (b) Parameters from OMA-based method. (c) Parameters from this article.

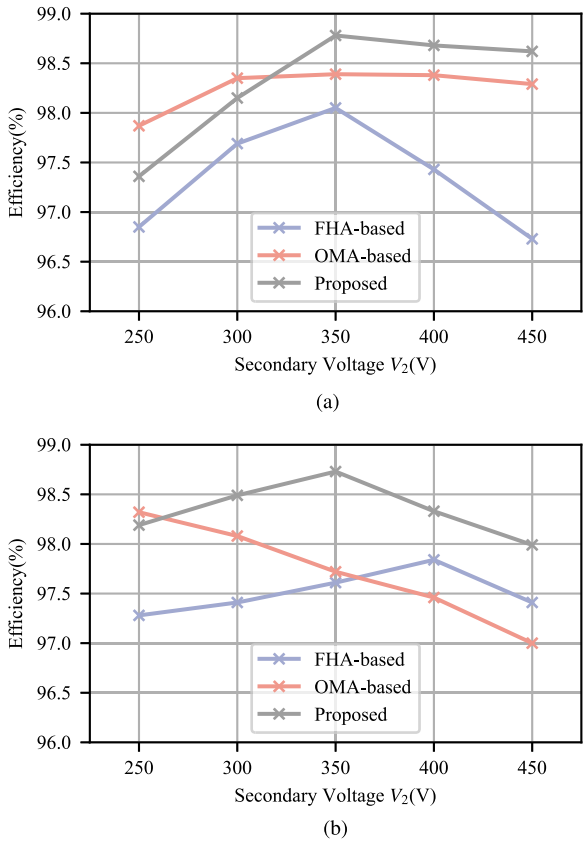



Fig. 19. Experimental efficiency curves at rated power. (a) Forward mode. (b) Reverse mode.

Candidates that exceed the capacitor voltage limitation or cannot fully achieve ZVS will be discarded outright, traverse the iterative results, the optimal design result of input parameters listed in Table V can be obtained as

$$\begin{cases} k_1 = 5.9 \\ k_2 = 4.4 \\ p_{n\_\max} = 0.28 \\ f_r = 85.7\,\text{kHz} \\ n = 1.15 \end{cases} \Rightarrow \begin{cases} V_{\text{base}} = V_1 = 400\,\text{V} \\ P_{\text{base}} = p_{\max}/p_{n\_\max} = 3571\,\text{W} \\ I_{\text{base}} = P_{\text{base}}/V_{\text{base}} = 8.93\,\text{A} \\ Z_{\text{base}} = V_{\text{base}}/I_{\text{base}} = 44.8\,\Omega \end{cases}$$

$$\Rightarrow \begin{cases} L_{r1} = Z_{\text{base}}/(2\pi f_r) = 83.2\,\mu\text{H} \\ C_{r1} = L_{r1}/Z_{\text{base}}^2 = 41.5\,\text{nF} \\ L_m = k_1 L_{r1} = 490\,\mu\text{H} \\ L_{r2} = L_m/(n^2 k_2) = 86.4\,\mu\text{H} \\ C_{r2} = L_{r1}C_{r1}/L_{r2} = 39.9\,\text{nF}. \end{cases} \tag{37}$$

## IV. Experiments

### A. Experiment Setup

To verify the proposed design methodology, as shown in Fig. 12, a S-type *CLLC* resonant converter with parameters in (37) was established based on specifications given in Table V. Metalized polypropylene film capacitors are utilized as the resonant capacitors and a self-made board based on the Cyclone IV EP4CE10 FPGA is used to control the *CLLC* converter.

The corresponding experimental test platform is shown in Fig. 13, where the four channels of the oscilloscope measure the bridge arm voltages and resonant currents, respectively. The power analyzer is used to measure the efficiency of the prototype, with its voltage measurement ports are directly connected to the input and output ports on the prototype.

### B. Waveform Results

In forward mode, the dc power supply connected to $V_1$ is fixed at 400 V, and the electronic load connected to $V_2$ is set to constant power mode. The output voltage can be adjusted from 250 to 450 V by changing the switching frequency. Figs. 14 and 15 illustrate the voltage and current waveforms at several typical voltage gains with 1 kW and 500 W load conditions, respectively. It can be seen that $V_2$ increases as switching frequency decreases, and the frequency range in forward mode is in the range of 55.6–132 kHz.

In reverse mode, the dc power supply connected to $V_2$ is varied from 250 to 450 V while the electronic load connected to $V_1$ is set to constant resistance mode, and the controller is programmed to adjust the frequency as $V_2$ changes to fix $V_1$ at 400 V. Similar to the forward mode, Figs. 16 and 17 illustrate the waveforms at 1 kW and 500 W, respectively. The switching frequency increases with $V_2$ and reaches a maximum of 149.6 kHz when $V_2$ equals to 450 V at 500 W.

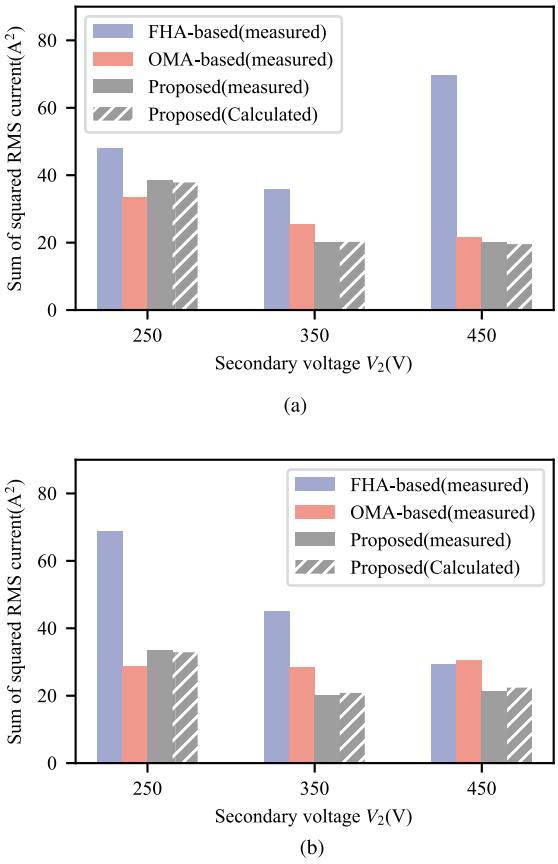



Fig. 20. Comparison of sum of squared rms current values at rated power. (a) Forward mode. (b) Reverse mode.

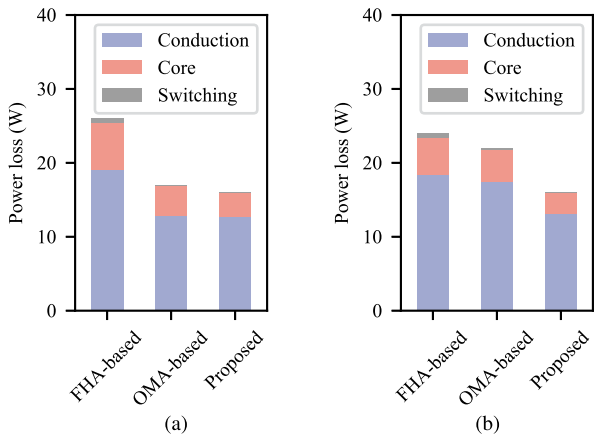



Fig. 21. Calculated average losses at rated power. (a) Forward mode. (b) Reverse mode.

For both modes, there is no switching oscillation in the inverter side voltage waveform since ZVS has been achieved. And due to the low-switching frequency and large resonant current, the secondary resonant capacitor voltage reaches a maximum of 449 V when operating in reverse mode at rated power and $V_2 = 250$ V.

TABLE IX
LOSS BREAKDOWN

| Component | Loss profile | (W) |
|---|---|---|
| Transformer | Primary copper | 1.134 |
| | Secondary copper | 1.085 |
| | Core | 1.667 |
| Resonant inductors | Primary copper | 0.646 |
| | Primary core | 0.335 |
| | Secondary copper | 0.696 |
| | Secondary core | 0.424 |
| Capacitors | Primary resonant capacitor | 0.308 |
| | Secondary resonant capacitor | 0.418 |
| | Input capacitor | 0.116 |
| | Output capacitor | 0.125 |
| MOSFETs | Primary conduction | 1.515 |
| | Secondary conduction | 1.633 |
| | Primary switching | 0.041 |
| Others | PCB | 1.009 |
| Sum (calculated) | | 11.15 |
| Efficiency (measured) | | 98.8% |

TABLE X
NORMALIZED VOLTAGE GAIN BOUNDARY VERSUS PARAMETER TOLERANCE

| $m$ | $L_{r1}$ | $C_{r1}$ | $L_{r2}$ | $C_{r2}$ | $L_m$ |
|---|---|---|---|---|---|
| $m_{f\_\max}$ | $\downarrow$ | $\downarrow\downarrow\downarrow$ | $-$ | $-$ | $\downarrow\downarrow$ |
| $m_{f\_\min}$ | $\downarrow\downarrow$ | $\downarrow$ | $\downarrow\downarrow$ | $\downarrow$ | $\uparrow\uparrow$ |
| $m_{r\_\max}$ | $\uparrow$ | $\uparrow\uparrow$ | $\downarrow$ | $\uparrow$ | $\downarrow\downarrow$ |
| $m_{r\_\min}$ | $\downarrow$ | $\downarrow$ | $\downarrow\downarrow$ | $\downarrow$ | $\uparrow\uparrow$ |

TABLE XI
COMPENSATED WORST VOLTAGE GAIN BOUNDARY

| Parameters | $m_{f\_\max}$ | $m_{f\_\min}$ | $m_{r\_\max}$ | $m_{r\_\min}$ |
|---|---|---|---|---|
| Unmodified | 1.483 | 0.565 | 1.442 | 0.708 |
| Worst $m_{f\_\max}$ | 1.572 | 0.553 | 1.487 | 0.678 |
| Worst $m_{f\_\min}$ | 1.782 | 0.565 | 1.442 | 0.708 |
| Worst $m_{r\_\max}$ | 1.767 | 0.564 | 1.442 | 0.677 |
| Worst $m_{r\_\min}$ | 1.782 | 0.565 | 1.442 | 0.708 |

### C. Comparison With Previous Parameter Design Methods

The comparison with previous parameter design methods is listed in Table VI, time-domain models such as OMA and DEPAM have higher accuracy than FHA, and their waveform calculation results can be consistent with PLECS simulation. Compared with OMA, DEPAM can solve waveforms without the need for operation mode judgement, and the initial values of iterative calculations for the first stage $\mathbf{x_1}(0)$ can be given arbitrarily or set directly to 0, therefore, it is simpler and more versatile.

Different from the previous design approaches, minimizing the rms current is taken as the optimization goal of this article, and in addition, the *CLLC* converter design method proposed in this article has the highest design freedom and is capable of complete traversal of possible parameters in several minutes. Due to similar application backgrounds and voltage ranges,

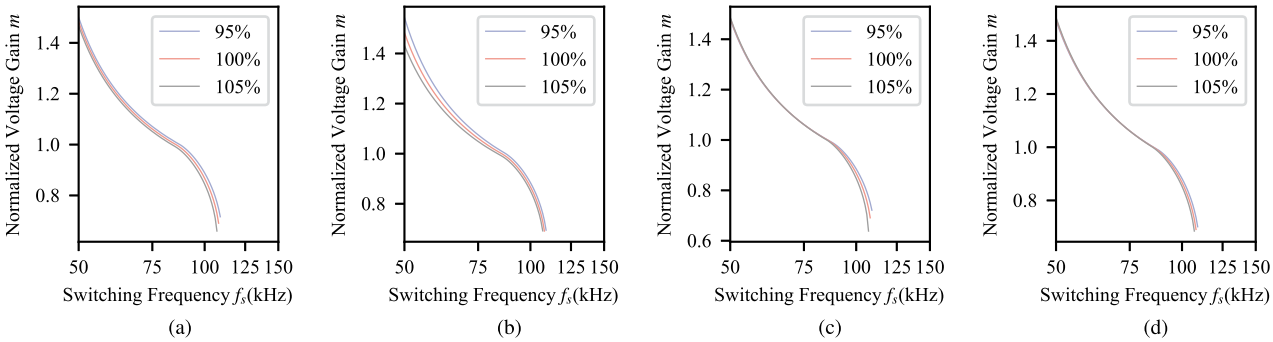



Fig. 22. Voltage gain curves affected by circuit parameter tolerances in forward mode. (a) $L_{r1}$. (b) $C_{r1}$. (c) $L_{r2}$. (d) $C_{r2}$.

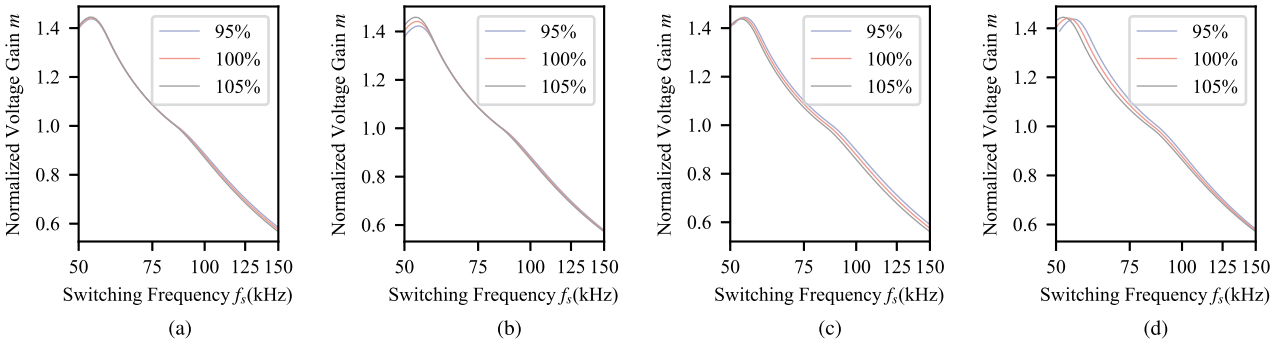



Fig. 23. Voltage gain curves affected by circuit parameter tolerances in reverse mode. (a) $L_{r1}$. (b) $C_{r1}$. (c) $L_{r2}$. (d) $C_{r2}$.

the work in [12] and [17] were selected from Table VI for comparative experiments as OMA-based and FHA-based design method, respectively. According to their design methodologies, the same design specifications as those in this article were input to obtain the parameter design results shown in Table VII, while the corresponding prototype parameters and experimental resonant tanks are shown in Table VIII and Fig. 18, respectively.

The efficiency test results of the three different design results at full load are shown in Fig. 19, by apply the proposed design method, the average efficiency increased by 0.33% and 1.04% compared to OMA-based and FHA-based method, respectively. Comparison of measured rms current values is shown in Fig. 20, the method proposed in this article reduces the sum of rms current by 3.65% and the sum of squared rms current by 9.72% compared to OMA-based method, and reduces the sum of rms current by 25.1% and the sum of squared rms current by 49% compared to FHA-based method. And the calculated values of squared rms current used for the optimal design are approximately equal to the measured values with a average error of 0.83%.

The calculated average losses based on loss models [19] are shown in Fig. 21. The OMA-based design result works in step-down mode during reverse operation, which leads to higher switching frequency and, hence, higher conduction losses due to skin effect. The proposed design result has the highest full-load efficiency of 98.8% when $V_2 = 350$ V in forward mode, and the corresponding losses are calculated as shown in Table IX, which are approximately consistent with the measured values.

## V. Conclusion

In this article, a stage iteration-based time-domain model namely DEPAM of *CLLC* converter is illustrated. Compared with OMA, the proposed DEPAM is more practical since it does not require operating mode judgment and solving system of transcendental equations, meanwhile, time-domain waveforms for arbitrary modulation method and circuit parameters can be obtained. Moreover, this article introduced a time domain-based asymmetric *CLLC* converter parameter optimization design method, which takes into account the voltage gain range, soft-switching, capacitor voltage stresses, and current rms values simultaneously. Finally, a 1 kW prototype *CLLC* converter has been built based on the design result, the effectiveness of the proposed method as a way to design high efficiency *CLLC* converters is verified by the experimental results.

## VI. Discussion

### A. Generalization of Modeling and Design Methodology

This article contains two parts, the modeling (DEPAM) and the design methodology, both of which can be applied to other converters, as discussed in the following.

*1) Modeling:* For other converters with different circuit stages, the corresponding stage solver as shown in Fig. 3 needs to be rebuilt. Since the solver requires all analytic expressions for the state variables of all stages, the number of operating stages

of the converter to be modeled should not be too many, and the order of the stage circuit should not be too high, if it is more than 4, the analytical solution of the characteristic equations cannot be obtained directly by formula, which will lead to the difficulty of modeling.

DEPAM can be applied to most single-stage converters, such as active clamp flyback converter and phase-shifted full-bridge converter. Also, since *CLLC* is already a relatively complex converter topology, it is possible to apply the DEPAM of the *CLLC* converter to other topologies by modifying the circuit parameters. For example, by setting $L_{r2}$ to 0 and $C_{r2}$ to infinite, the DEPAM of the *CLLC* converter can be applied to the *LLC* converter, and even further by setting $C_{r1}$ to infinity, it can be applied to the DAB converter.

*2) Design Methodology:* The proposed design methodology can be applied in other types of resonant converters such as the *LLC* converter and the series resonant converter. The labels of normalized curves in this article contain three dimensions, $k_1$, $k_2$, and $p_n$, while *LLC* will be relatively simpler with only two dimensions, $k$ and $p_n$, and thus, the curves database will be much smaller.

The drawback of the proposed design method is that it cannot be applied to converters where the parasitic parameters have a large influence on the operating characteristics of the circuit, thought the design method is based on parameter normalization, while the parasitic parameters usually do not have a linear relationship with the main parameters of the circuit and cannot be normalized.

### B. Effect of Circuit Parameter Tolerances

In practical applications, circuit parameters such as capacitance and inductance often exhibit tolerances. In the case of the *CLLC* converter, which involves a multitude of circuit parameters, the impact of parameter errors is particularly pronounced. Since voltage gain is a crucial metric to be satisfied during the converter design process, an analysis will be conducted on the influence of circuit parameter tolerances on the voltage gain of the converter.

To conduct tolerance analysis, it is necessary to assume that small variations in circuit parameters have a monotonic and independent impact on the voltage gain. Typically, the CBB capacitors used as resonant capacitance exhibit a tolerance of 5%. Therefore, $\delta$ is taken as 0.05 in the following analysis. The influence of different circuit parameter tolerances on the gain curve is depicted in Figs. 22 and 23. Based on the gain curve, the normalized boundary gain in relation to the parameter tolerances can be derived, as summarized in Table X.

From Table X, it can be seen that reducing $L_m$ expands the voltage gain range, this is because decreasing $L_m$ means increasing $k_1$ and $k_2$. To guarantee that $k_1$ and $k_2$ are not reduced in the presence of tolerances in $L_{r1}$ and $L_{r2}$, it is necessary to ensure that the actual $L_m$ does not exceed 95% of the design value, and then taking into account the tolerance of $L_m$ itself, we need to set $L_m$ to 90% of its design result during fabrication. In addition, tolerances in the resonance parameters will also lead to the change of resonance frequency in a range of up to 5%, so allocate a 5% margin for switching frequency range in the design specifications is also necessary.

The worst-case boundary gain values after compensation are presented in Table XI, with the minimum gain calculated for a load of 50%. It is evident that the compensated circuit parameters are able to satisfy the voltage gain range within the given tolerances.

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