A Detailed Analytical Switching Transient Model for Silicon Superjunction MOSFET and SiC Schottky Diode Pair

Manish Mandal, *Member, IEEE*, Shamibrota Kishore Roy, *Member, IEEE*, and Kaushik Basu, *Senior Member, IEEE*

***Abstract*—With high reliability and good cost-performance ratio, silicon superjunction MOSFETS (Si SJMOS) and SiC SBD pair is often preferred in commercial single-phase power factor correction applications. Switching dynamics of Si SJMOS are different compared to 650 V wide bandgap devices due to differences in device characteristics. This article presents an improved analytical model to study the switching dynamics of Si SJMOS and SiC SBD pair. Unlike the existing literature on high-voltage Si MOSFETS, this article considers the nonlinearities in channel current and internal capacitances of Si SJMOS, the nonlinear reverse-biased capacitance of SiC SBD, along with parasitic gate-drain capacitance arising due to PCB layout. As a result, the proposed analytical model presents a significant improvement over the existing models of high-voltage Si MOSFET in predicting switching loss, time, (dv/dt), (di/dt), etc. Experimental and simulation results for three 650 V Si SJMOS and SiC SBD pairs with different current ratings provide validation of the proposed analytical model.**

***Index Terms*—Analytical model, double pulse test (DPT), loss, MOSFET, Schottky diode, SiC, silicon superjunction, switching transient.**

NOMENCLATURE

V_{dc}	Ideal DC bus voltage.
I_0	Ideal DC current sink.
v_G	Gate-drive voltage with levels V_{GG} and 0.
R_{g1}, R_{g2}	Internal and external gate resistances (includes driver resistance).
R_g	Total gate resistance ($=R_{g1}+R_{g2}$).
L_s	Common source inductance.
L_d, L_g	Power loop and gate loop inductances (excluding L_s).
C_{gs}, C_{gd}, C_{ds}	Gate-source, gate-drain and drain-source capacitance of SJMOS.
C_d	SiC SBD reverse-biased depletion capacitance.
C_{x1}, C_{x2}	Layout-dependent parasitic capacitances.
V_{T1}	Transition voltage of C_{gd} and C_{ds} model.
C_{gd0}, C_{ds0}	Zero-bias gate-drain and drain-source capacitance of SJMOS.
k_1, k_4	Built-in potential of gate-drain and drain-source junction of SJMOS.
k_2, k_5	Slope of C_{gd} and C_{ds} curve in the high-voltage region.
k_3, k_6	High-voltage gate-drain and drain-source capacitance.
C_{d0}	Capacitance of the Schottky diode at zero-bias condition.
V_{T2}	Transition voltage of C_d model.
k_7	Built-in potential of the Schottky junction.
k_8	Slope of the C_d curve at the high voltage region.
k_9	Value of C_d at $v_d = V_{T2}$.
β	Transconductance parameter of SJMOS.
V_{th}	Threshold voltage of SJMOS.
θ	Transverse-field induced mobility degradation parameter.
k_p	Drain-source saturation voltage parameter.

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The authors are with the Department of Electrical Engineering, Indian Institute of Science, Bangalore 560012, India (e-mail: manishmandal@iisc.ac.in; shamibrotar@iisc.ac.in; kbasu@iisc.ac.in).

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I. INTRODUCTION

SILICON superjunction MOSFETS (Si SJMOS) have found their widespread adoption in commercial-scale power electronic converters. These devices are commercially available in the voltage range of 500–950 V (typically 600–650 V) and were found to be superior to conventional Si MOSFETS due to their better switching and conduction loss performances [1], [2].

A. Relevance of Si SJMOS

Due to their superior properties, wide bandgap (WBG) devices like SiC MOSFETS and GaN HEMTs have recently challenged Si SJMOS in the 600–650 V voltage range. However, their widespread adoption has been hindered [3] due to challenges related to reliability (e.g., threshold voltage instability, dynamic ON-state resistance) [4], [5], [6], susceptibility to issues like false turn-ON [7], sustained oscillation, EMI, etc. and higher cost. In contrast, Si SJMOS, when paired with SiC SBD, offers adequate dynamic performance comparable to these WBG devices [1], [8], [9]. Moreover, superior reliability due to years

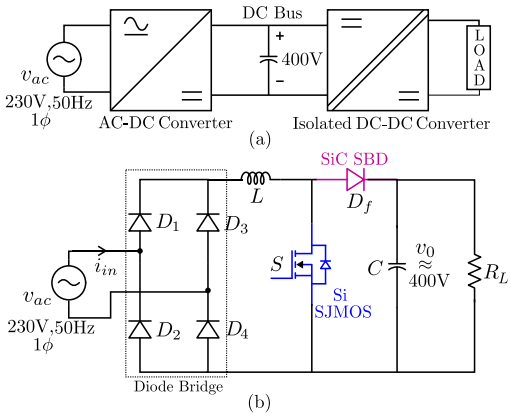


Fig. 1. (a) Two-stage architecture. (b) Conventional-boost PFC.

of field operation and lower cost make Si SJMOS a device of choice in this voltage segment [3].

B. Application of Si SJMOS and SiC SBD Pair

In applications like electric vehicle (EV) onboard chargers, telecom, and data center power supply, power flow is unidirectional, and the majority of the power electronic converters are based on a two-stage architecture, an ac–dc stage followed by an isolated dc–dc stage [see Fig. 1(a)]. A power factor correction (PFC) topology is used in the rectifier stage to rectify a single-phase ac to a 400 V dc bus. In the popular PFC topologies such as the conventional and the dual-boost PFC [10], a 600–650 V Si SJMOS is used with SiC Schottky diode due to its zero reverse recovery charge [11] [see Fig. 1(b)]. On the other hand, Si SJMOS incurs significantly higher turn-ON switching loss and current stress when used in bridgeless totem-pole PFC (BTPPFC) due to its body diode's poor reverse recovery performance [12]. Hence, the use of Si SJMOS in BTPPFC is usually avoided.

C. Estimation of Switching Loss

Understanding switching dynamics followed by estimation of switching loss is important for optimal converter design and selection of switching frequency. It also helps in selecting a suitable device for a given application. This understanding can be used further for optimizing power and gate circuit layout and better gate driver and thermal design [13], [14].

D. Analytical Approach

The approaches to studying switching dynamics can be broadly classified into experimental, simulation, and analytical. The experimental approach can be based on a double pulse test (DPT) [14] or calorimetric measurement [15]. However, it requires expensive measurement equipment and a special experimental setup.

Simulation-based approaches can be of two types: physics-based simulation or behavioral simulation. In the first approach, detailed physical models of MOSFETS and diodes are simulated along with a lumped parameter model of the external circuit [16]. However, it requires internal device parameters (not available in the datasheet), a long simulation time, and expensive simulation software, such as TCAD, Medici, etc. In contrast, behavioral models are circuit-based simulation approaches where the terminal characteristics of the devices are modeled using circuit elements, and a lumped parameter model of the external circuit is used [13], [14]. However, simulating behavioral models in circuit-based simulators (like MATLAB/Simulink) is challenging due to device nonlinearities. The device manufacturers also provide behavioral models that can be simulated in SPICE-based circuit simulators. However, it is not possible to obtain internal device variables (e.g., channel current). Moreover, these behavioral models often experience convergence issues [17]. Although relatively simple and fast, this approach does not offer insight into the switching process. Also, as the simulation must run at each operating point, this approach is more time-consuming.

Analytical models are based on simplified approximate solutions of the set of coupled nonlinear differential equations obtained from the behavioral model. This approach is suitable for gaining insight into the switching process and overcomes most of the limitations of the previously stated approaches. It provides results accurate enough for the early stages of power electronic converter design. In this article, an analytical modeling approach is proposed to study the switching dynamics of Si SJMOS and SiC SBD in a buck-chopper configuration, which uses values obtained from the device and gate driver datasheet and the values of external circuit parasitics.

E. Existing Literature

Switching dynamics of low-voltage Si MOSFETS is well studied in the literature [13], [18], [19]. During the turn-ON transition, the drain-source voltage of these devices collapses to zero as the device current rises. The same is true for low voltage GaN HEMTs [20]. Hence, the switching dynamics of low-voltage devices are significantly different from their high-voltage counterparts.

Analytical models for high voltage GaN HEMTs and SiC MOSFETS are presented in [7] and [14], respectively. Although the equivalent circuit-based model used in [7] and [14] for the WBG devices appears similar, the analytical model derived through approximations for Si SJMOS is different. This is due to differences in characteristics of Si SJMOS, like channel current, etc, and their functional dependencies on terminal voltages compared to WBG devices. The differences in characteristics are briefly described as follows.

1) Transconductance of both SiC MOSFETS and high-voltage GaN HEMTs reduces with the increase in gate-source voltage in the saturation region. On the contrary, it increases for Si SJMOS [21], [22]. While similar for GaN and Si SJMOS, the transconductance of SiC MOSFETS is considerably smaller.
2) While the transition from ohmic to saturation region occurs in a gradual manner for SiC MOSFETS [23], a sharp transition is observed for Si SJMOS [21].
3) Compared to WBG devices, the gate-drain and drain-source capacitances of Si SJMOS are highly nonlinear.

a) These capacitances change by more than two orders of magnitude in low drain-source voltage region [21], [24] [see Fig. 4(a)].
b) Unlike GaN HEMTs [22] and SiC MOSFETS [14], the gate-drain capacitance of Si SJMOS increases with voltage in the high drain-source voltage region [21].

Analytical models for high voltage Si MOSFETS are presented in [24] and [25]. In both [24] and [25], channel current is not modeled in the ohmic region, and in the saturation region, it is assumed to be a linear function of gate-source voltage. The highly nonlinear gate-drain and drain-source capacitances were modeled using two-step constant capacitance approximation in both [24], [25]. [24] considered the freewheeling diode to be ideal, whereas a constant capacitance is used in reverse biased condition in [25]. Due to these assumptions, significant errors are observed in estimating switching losses, times, (di/dt), (dv/dt), etc. A detailed discussion is presented in Section VII.

F. Contribution

As evident, there are not enough research publications that analyze the switching behavior of Si SJMOS and SiC SBD pair. To address this gap, this article makes the following contributions.

1) This article presents an improved model for analyzing the switching transients of Si SJMOS and SiC SBD pair. It makes a substantial improvement over the existing models for high-voltage Si MOSFETS in estimating switching loss, (dv/dt), (di/dt), etc, as delineated by quantitative comparison in Section VII.
2) It considers a detailed nonlinear channel current model based on Nth power law MOSFET model [26] and accurately represents the channel current of Si SJMOS in both ohmic and saturation regions.
3) Piecewise nonlinear models of the gate-drain and drain-source capacitances of the Si SJMOS are proposed.
4) A piecewise nonlinear capacitance model of SiC SBD is used in reverse-biased condition.
5) The effect of external parasitic gate-drain capacitance is also considered as it significantly impacts voltage-rise and voltage-fall periods [25]. Both [24] and [25] ignore the effect of external gate-drain capacitance in analysis.
6) Guidelines for selecting external gate resistance using the proposed analytical model are presented.

Experimental and simulation results for three Si SJMOS and SiC pair of different current ratings validates the accuracy of the proposed analytical model.

The rest of the article is organized as follows. Section II discusses the limitations of existing literature and the improvements made by the proposed model. Section III describes the behavioral model for studying hard turn-ON and turn-OFF switching dynamics of Si SJMOS and SiC SBD pair. Through approximations, the proposed analytical model is derived and described in Section IV. Section V describes the experimental setup and behavioral simulation. The proposed model is validated in Section VI using experimental and simulation results for a wide range of operating conditions. Section VII compares and presents improvements made by the proposed model compared to prior arts. Section VIII presents a brief discussion on the impact of important parasitics on the proposed model. In Section IX, the proposed model is compared with DPT, SPICE, and gate charge method. Finally, Section X concludes this article.

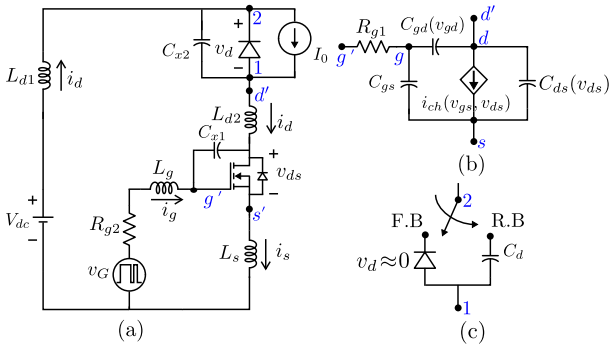


Fig. 2. (a) Buck chopper circuit with relevant parasitics for hard-switching dynamics study. (b) Equivalent circuit model of Si SJMOS. (c) Equivalent circuit model for SiC SBD: F.B - Forward Biased, R.B - Reverse Biased: L_{d1} - PCB trace inductance in the power loop, L_{d2} - drain lead inductance of Si SJMOS, $L_d = L_{d1} + L_{d2}$.

II. Comparison With Prior Arts

A detailed discussion of the existing analytical switching loss models for high-voltage Si MOSFETS is presented in this section. Turn-ON switching dynamics is divided into four modes: delay (mode I), current-rise (mode II), voltage-fall, (mode III), and ringing (mode IV). Similarly, the turn-OFF switching process is divided into four distinct modes: delay (mode V), voltage-rise (mode VI), current-fall (mode VII), and ringing (mode VIII). Tables I and II list the key assumptions used in the existing analytical models and their shortcomings in the turn-ON and turn-OFF transients, respectively. This provides motivation for this article. The tables also qualitatively discuss the improvements made in the proposed analytical model.

III. Behavioral Model to Analyze Hard-Switching Dynamics of Si SJMOS

To analyze the hard switching dynamics of Si SJMOS, a buck-chopper configuration is considered, as shown in Fig. 2(a). SiC SBD is used as the freewheeling diode due to its zero reverse recovery [11]. The input of the buck-chopper is connected to a constant dc voltage $V_{\rm dc}$, and the output is connected to a constant current sink I_0. The definition of the parameters used in this study is listed in Nomenclature. A detailed discussion of the behavioral model is presented in this section.

A. Equivalent Circuit Model of Si SJMOS

Fig. 2(b) shows the equivalent circuit model of Si SJMOS. It comprises a dependent current source to model the channel current $i_{ch}(v_{gs}, v_{ds})$. To accurately model i_{ch} in both ohmic and saturation regions, a detailed nonlinear model based on Nth power law [26] is used. While a formulation of i_{ch} similar to Nth

TABLE I
QUALITATIVE DISCUSSION ON TURN-ON SWITCHING TRANSIENT

Mode	References	Assumptions and Limitations	Improvements in the Proposed Analytical Model
II Current rise Period	[25]	• In the saturation region, channel current is modeled as a linear function of the gate-source voltage.	• A detailed nonlinear dependence of the channel current on the gate-source voltage in the saturation region is considered. • The drain-source voltage is approximately taken to be constant. This results in simple polynomial expressions of the circuit variables, switching loss, and time for this mode.
	[24]	• Similar analysis of [25] is used. However, some parameters of the analytical model are adjusted to obtain a better match with experimentally obtained (di/dt).	
III Voltage fall period	[25]	• Gate-source voltage is assumed to be constant, and the gate current flowing through the miller capacitance leads to fall in the drain-source voltage. • Channel and drain currents are considered to be the same and clamped to the load current. • Drain-source capacitance is neglected, two-step approximation of the gate-drain capacitance is considered, and reverse-biased capacitance of the diode is assumed to be constant.	• Both channel and drain current increase well beyond the load current, and a significant difference exists between them. This difference predominantly leads to the drain-source voltage fall. The gate current is usually small compared to both currents. • Coupled dynamics of gate and power loop is considered. • Nonlinear models of the capacitance of Si SJMOS and diode are considered, which leads to a better estimation of the switching dynamics. • The external gate-drain layout-dependent capacitance is also considered as it has a significant impact on the switching.
	[24]	• Analysis similar to [25] is carried out. However, reverse-biased capacitance of the diode is neglected.	

TABLE II
QUALITATIVE DISCUSSION ON TURN-OFF SWITCHING TRANSIENT

Mode	References	Assumptions and Limitations	Improvements in the Proposed Analytical Model
V Delay Period	[25], [24]	• Drain-source voltage is considered to be constant, and both the drain and channel currents are clamped to the load current. • Constant value of gate-drain capacitance corresponding to the low drain-gate voltage is considered. • Drain-source capacitance is ignored. • Decoupled gate-loop dynamics is considered with exponential decay of the gate-source voltage	• The channel current is modeled accurately in the ohmic region. Also, coupled dynamics of gate and power loop is considered. • A comprehensive model of the gate-drain capacitance is considered to estimate the delay time accurately.
VI Voltage rise period	[25]	• Its analysis is similar to mode III (see Table I)	• Nonlinear models of channel current, gate-drain, and drain-source capacitance and diode capacitance are considered • The external gate-drain capacitance plays a significant role. on the switching dynamics and it is considered in analysis. • Coupled dynamics of gate and power loop is considered.
	[24]	• During the first part of this mode, channel current is assumed to a plateau level whose value is obtained empirically. • Both the channel and the drain currents are assumed to fall to zero in this mode for Si SJMOS.	
VII Current fall period	[25]	• Similar to mode II, this mode's dynamics is governed by a second-order linear differential equation.	• Similar to mode II, the proposed method presents simple polynomial expressions of losses and time. • This mode exists for sufficiently large values of load currents.
	[24]	• This mode does not exist as drain current was zero.	

TABLE III
CHANNEL CURRENT MODEL COMPARISON

Condition	Channel Current Models of Si SJMOS: Detailed i_{ch} Model		Schokley Equation Model (Model B)	
$v_{gs} < V_{th}$	$i_{ch} = 0$	(1a)	$i_{ch} = 0$	(2a)
$v_{gs} \geq V_{th}, v_{ds} \geq v_{ds(sat)}$	$i_{ch} = \dfrac{\beta (v_{gs} - V_{th})^2}{2(1 + \theta(v_{gs} - V_{th}))}$	(1b)	$i_{ch} = \dfrac{\beta}{2}(v_{gs} - V_{th})^2$	(2b)
$v_{gs} \geq V_{th}, v_{ds} \leq v_{ds(sat)}$	$i_{ch} = \dfrac{\beta (v_{gs} - V_{th})^2}{2(1 + \theta(v_{gs} - V_{th}))}\left(2 - \dfrac{v_{ds}}{v_{ds(sat)}}\right)\left(\dfrac{v_{ds}}{v_{ds(sat)}}\right)$	(1c)	$i_{ch} = \beta v_{ds}\left(v_{gs} - V_{th} - \dfrac{v_{ds}}{2}\right)$	(2c)
	$v_{ds(sat)} = k_p (v_{gs} - V_{th})^m$	(1d)	$v_{ds(sat)} = (v_{gs} - V_{th})$	(2d)

power law model is used in the ohmic region [see (1c), (1d)], i_{ch} expression used in the saturation region is slightly modified [see (1b)]. This was done to avoid computations involving noninteger exponents, as it is not very suitable for analytical modeling.

To underscore the accuracy of the detailed i_{ch} model [see (1a)–(1d)], it is compared with the widely known Shockley-Equation model (Model B) [see (2a)–(2c)] [27] in Fig. 3. As evident, the predicted output characteristics of Model B differ from those of the datasheet, although it captures the transfer characteristics with reasonable accuracy. In contrast, the detailed i_{ch} model achieves sufficient accuracy in capturing both the transfer and the output characteristics. It is worthwhile to note that the Shockley-Equation model is linearized in the existing literature on high-voltage Si MOSFETS [24], [25].

$$C_{gd}(v_{dg}) = \begin{cases} C_{ox}, & v_{dg} < 0 \quad (3a) \\ \dfrac{C_{gd0}}{\left(1 + \frac{v_{dg}}{k_1}\right)^3}, & 0 \leq v_{dg} \leq V_{T1} \quad (3b) \\ k_2 (v_{dg} - V_{T1}) + k_3, & v_{dg} \geq V_{T1} \quad (3c) \end{cases}$$

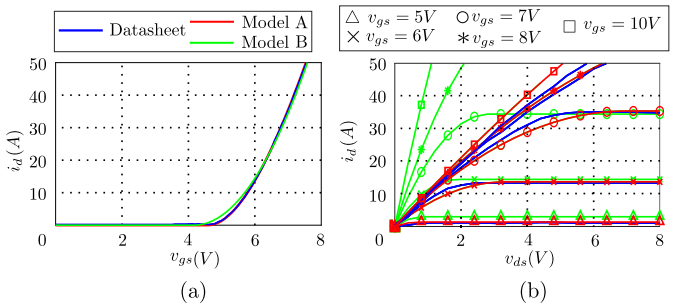


Fig. 3. (a) Transfer characteristics and (b) output characteristics of IPW65R110CFDA.

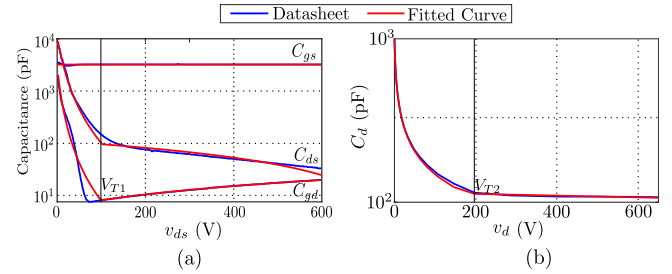


Fig. 4. $C-V$ Characteristics of (a) Si SJMOS - IPW65R110CFDA and (b) SiC SBD depletion capacitance.

$$C_{ds}(v_{ds}) = \begin{cases} \dfrac{C_{ds0}}{\left(1+\frac{v_{ds}}{k_4}\right)^3}, & 0 \le v_{ds} \le V_{T1} \quad (4a) \\ k_5\left(v_{ds} - V_{T1}\right) + k_6, & v_{ds} \ge V_{T1}. \quad (4b) \end{cases}$$

The internal capacitances of Si SJMOS are C_{gs}, C_{gd}, and C_{ds} (see Nomenclature). Whereas C_{gs} remains fairly constant, C_{gd} and C_{ds} are highly nonlinear functions of their respective terminal voltages. It is noteworthy that both C_{gd} and C_{ds} experience more than two orders of decline in magnitude when the device's drain-source voltage rises from zero to about 10% of the rated voltage [21], [24] [see Fig. 4(a)]. These capacitances can be obtained from capacitance ($C_{iss}, C_{oss}, C_{rss}$) plot provided in the datasheet as a function of drain-source voltage v_{ds} by using the following relations: $C_{gd} = C_{rss}$, $C_{gs} = C_{iss} - C_{rss}$ and $C_{ds} = C_{oss} - C_{rss}$. To model C_{gd} and C_{ds}, nonlinear models (3) and (4) and used, respectively. $C_{gs} \approx C_{iss}(V_{\text{dc}})$ as $C_{gd} \ll C_{gs}$ at high v_{ds} value. Also, $v_{dg} = v_{ds}$ as capacitance measurement is conducted at $v_{gs} = 0\text{˜}V$. Therefore, $C_{gd}(v_{ds})$ obtained from the datasheet can be directly converted to $C_{gd}(v_{dg})$ and is valid for $v_{dg} \ge 0$. For the region, where $v_{dg} < 0$, $C_{gd}(v_{dg}) \approx C_{ox}$ (oxide capacitance).

B. Equivalent Circuit Model of SiC SBD

The equivalent circuit model of SiC SBD is shown in Fig. 2(c). It is modeled as an ideal diode ($v_d \approx 0$) in the forward-biased condition. In the reverse-biased condition, a voltage-dependent capacitance model $C_d(v_d)$ is used. This capacitance plays an active role during the drain-source voltage rise and fall transitions; hence, it should be correctly modeled. In this work, a piecewise nonlinear model of the diode capacitance is proposed, which can accurately capture the capacitance over the entire operating range [see Fig. 4(b)]. A brief comparison presented in Appendix B underscores the accuracy of the proposed model compared to the existing models.

$$C_d(v_d) = \begin{cases} \dfrac{C_{d0}}{\left(1+\frac{v_d}{k_7}\right)^{0.5}}, & v_d \le V_{T2} \quad (5a) \\ k_8\left(v_{ds} - V_{T2}\right) + k_9, & v_d \ge V_{T2}. \quad (5b) \end{cases}$$

The channel current and capacitances are obtained from the datasheet using *WebPlotDigitizer* [28] and curve-fitted using (1), (3)–(5) to extract the associated parameters. Note that all the parameters are extracted for 25 °C. As the temperature deviates, the static (transfer and output) characteristics of Si SJMOS can change significantly, resulting in varied switching dynamics. On the other hand, dynamics characteristics (e.g., output capacitance) have a weak temperature dependence and can be neglected for simplicity [29].

C. Modeling Circuit Parasitics

External circuit parasitics (L_g, L_s, L_d, C_{x1}, and C_{x2}) are considered in this work, as they can significantly influence switching transients [see Nomenclature and Fig. 2(a)]. L_s primarily stems from the source lead inductance of the Si SJMOS, impacting switching transitions and losses. L_d combines dc bus inductance, device lead inductances, and interconnection inductance. C_{x1} and C_{x2} are the constant capacitances (order of pF) due to PCB layout. It depends on the geometry of the PCB traces and the dielectric material (FR4). Note: C_{x2} also includes the parasitic capacitance of the inductive load. For low current Si SJMOS, these capacitances significantly affect switching dynamics as they become comparable with the internal device capacitance at high v_{ds}. Therefore, estimating and considering their values in the switching dynamics study is essential. In this work, a measurement-based approach is adopted to determine the values of these parasitics [30]. *It is worthwhile to note that no Si* MOSFET *switching loss models consider* C_{x1} *in the analytical formulation.*

The drain-source voltage $v_{ds}(t)$ and channel current $i_{ch}(t)$ are important waveforms for switching transient study. However, due to the presence of these external circuit parasitics, it is not possible to measure these waveforms, which are associated with the actual loss incurred in the device [see (6)]. On the other hand, $v_{d's'}(t)$, and $i_d(t)$ can only be measured from the experiments, which product can be integrated over the switching transition time to obtain the apparent loss (7). The actual loss E and the apparent loss E' are significantly different [31].

$$E = \int_0^t v_{ds}(\tau) i_{ch}(\tau) d\tau \quad (6)$$

$$E' = \int_0^t v_{d's'}(\tau) i_d(\tau) d\tau. \quad (7)$$

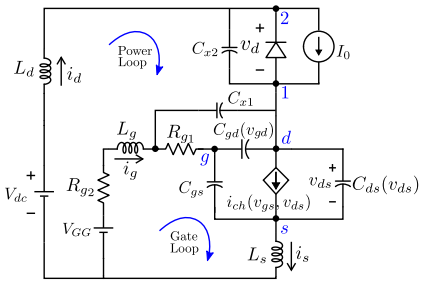


Fig. 5. Circuit for turn-ON analysis.

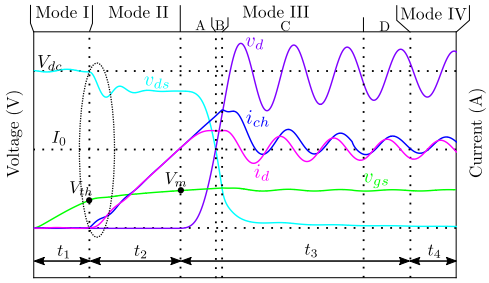


Fig. 6. Turn-ON simulation waveform.

IV. Analytical Switching Loss Model

This section presents a detailed analysis of the turn-ON and turn-OFF switching dynamics of Si SJMOS and SiC SBD pair. Based on the simulation of the behavioral models (discussed in Section III), the switching transition is divided into multiple modes. In each mode, suitable approximations are applied to obtain closed-form solutions or a set of reduced-order nonlinear differential equations, which forms our analytical model. The set of reduced-order differential equations is solved using the forward Euler-based finite difference method (FDM). Selection of proper time-step is essential for the forward Euler FDM to obtain both stability and accuracy of the results. In this work, a time-step of 10^{-12} s is used for achieving convergence in these modes. Guidelines for selecting time-step is delineated in Appendix C.

A. Turn-ON Switching Transient Analysis

The waveforms obtained from the simulation of the turn-ON behavioral model (see Fig. 5) in MATLAB/Simulink are shown in Fig. 6. Based on this figure, the turn-ON analysis is divided into four modes, and each of these modes is analyzed in detail as follows. The initial condition of each mode is obtained at the end of the previous mode.

1) Mode I: Delay Period: Initially, SiC SBD is forward biased ($v_d \approx 0$), and the current I_0 freewheels through it. Si SJMOS is in the OFF-state and blocks the total dc bus voltage $V_{\rm dc}$. In this mode, the drain current $i_d \approx 0$ and drain-source voltage $v_{ds} \approx V_{\rm dc}$ (see Fig. 6). Moreover, current through the C_{x1} and C_{gd} can be ignored as, $C_{gs} \gg C_{x1}, C_{gd}(V_{dc})$. Applying the above approximations, an equivalent circuit for this mode is obtained as shown in Fig. 7(a).

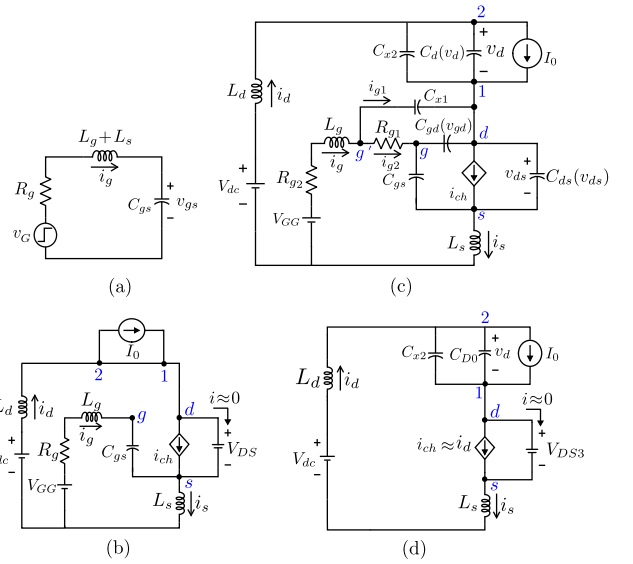


Fig. 7. Equivalent circuits for (a) Mode I, (b) Mode II, (c) Mode III, and (d) Mode IV.

$$V_{GG} = v_{gs} + R_g C_{gs} \frac{dv_{gs}}{dt} + (L_g + L_s) C_{gs} \frac{d^2 v_{gs}}{dt^2} \tag{8}$$

$$t_1 = R_g C_{gs} \ln \frac{V_{GG}}{V_{GG} - V_{th}}. \tag{9}$$

A positive voltage V_{GG} is applied to the gate terminal, and gate-source voltage v_{gs} increases from zero. Applying KVL in Fig. 7(a), a second-order differential equation in v_{gs} [see (8)] is obtained which governs the dynamics of the delay period. For a second-order system with a high damping ratio, it can be shown that the poles are well-separated and are approximately given by: $P_1 \approx -\frac{1}{R_g C_{gs}}$ and $P_2 \approx -\frac{R_g}{L_g + L_s}$ where $|P_2| \gg |P_1|$. Such a system can be approximately modeled by the slower pole, P_1. This mode ends when $v_{gs} = V_{th}$ at time t_1 given by (9) (see Fig. 6). As $v_{gs} < V_{th}$, $i_{ch} = 0$ resulting in zero switching energy loss i.e, $E_1 = 0$ [see (6)].

2) Mode II: Current-Rise Period: This mode begins when v_{gs} crosses V_{th}. SiC SBD is still forward biased $v_d \approx 0$. Si SJMOS operates in the saturation region. As v_{gs} rises beyond V_{th}, i_{ch} given by (1b) also increases. However, i_d does not change instantaneously due to the presence of L_d and L_s in the power loop. The increase in i_{ch} is supported by the discharge of the output capacitance (highlighted in Fig. 6). i_d eventually catches up with i_{ch} and hereafter, $v_{ds} \approx V_{DS}$ remains constant. The time duration for this initial transition is usually small as compared to the total time for this mode (t_2), and for the purpose of analysis can be ignored. Furthermore, $i_g \ll i_d$ except at the beginning of the mode and current through C_{gd} and C_{x1} are ignored as $C_{gs} \gg C_{x1}, C_{gd}(V_{DS})$. Using the aforementioned approximations in Fig. 5, an equivalent circuit for mode II is obtained as shown in Fig. 7(b).

$$V_{GG} = v_{gs} + R_g C_{gs} \frac{dv_{gs}}{dt} + L_g C_{gs} \frac{d^2 v_{gs}}{dt^2} + m_r L_s \tag{10}$$

$$v_{gs} \approx V_{th} + \frac{\theta m_r t}{\beta} + \sqrt{\frac{\theta m_r t}{\beta} + \frac{2 m_r t}{\beta}} \tag{11}$$

$$m_r \approx \frac{V_{GG} - V_{th} - \frac{I_0\theta}{\beta} - \sqrt{\left(\frac{I_0\theta}{\beta}\right)^2 + \frac{2I_0}{\beta}}}{\frac{R_g C_{gs}}{\beta}\left(\theta + \frac{\theta^2 I_0 + \beta}{\sqrt{(I_0\theta)^2 + 2I_0\beta}}\right) + L_s} \tag{12}$$

$$E_2 = \int_0^{t_2} m_r t V_{DS} = \frac{1}{2} m_r V_{DS} t_2^2. \tag{13}$$

As $v_{ds} \approx V_{DS}$ approximately remains constant in this mode, $i_d \approx i_{ch}$ increases with a constant slope m_r, yet to be determined. Application of KVL in the gate loop of Fig. 7(b) and above approximation, a second-order differential equation in v_{gs} is obtained [see (10)]. By substituting $i_{ch} \approx mt$ in (1b) and solving for v_{gs}, (11) is obtained. This must also be an approximate solution of (10). Mode II ends when $i_d \approx i_{ch}$ becomes equal to I_0 at time $t = t_2 = \frac{I_0}{m_r}$. By substituting (11) in (10) and replacing $t = t_2$, a quadratic equation in m_r is obtained. For a highly overdamped gate circuit, as stated in Mode I, two roots of the above quadratic equation will be well separated. m_r is selected such that $V_{DS} \approx V_{dc} - m_r(L_d + L_s) \geq 0$ and close to V_{dc} (see Fig. 6). The approximate value of m_r is given by (12). The actual switching energy loss in Mode II is given by (13).

$$(L_d + L_s)\frac{di_d}{dt} \approx V_{dc} - v_d - v_{ds} \tag{14}$$

$$(L_g + L_s)\frac{di_g}{dt} \approx V_{GG} - v_{g'd} - v_{ds} - i_g R_{g2} - \frac{L_s}{L_d + L_s}(V_{dc} - v_d - v_{ds}) \tag{15}$$

$$C_{x1}\frac{dv_{g'd}}{dt} = i_g - \frac{v_{g'd} - v_{gd}}{R_{g1}} \tag{16}$$

$$(C_d + C_{x2})\frac{dv_d}{dt} = i_d - I_0 \tag{17}$$

$$\left(C_{ds} + \frac{C_{gd}C_{gs}}{C_{gd} + C_{gs}}\right)\frac{dv_{ds}}{dt} = -\frac{C_{gs}}{C_{gd} + C_{gs}}\left(\frac{v_{g'd} - v_{gd}}{R_{g1}}\right) + (i_d - i_{ch} + i_g) \tag{18}$$

$$\left(C_{gs} + \frac{C_{gd}C_{ds}}{C_{gd} + C_{ds}}\right)\frac{dv_{gs}}{dt} = \frac{C_{ds}}{C_{gd} + C_{ds}}\left(\frac{v_{g'd} - v_{gd}}{R_{g1}}\right) + \frac{C_{gd}}{C_{gd} + C_{ds}}(i_d - i_{ch} + i_g). \tag{19}$$

3) Mode III: Voltage-Fall Period: The voltage-fall period starts when $i_d = I_0$. SiC SBD becomes reverse-biased, and it is modeled as a voltage-dependent capacitance $C_d(v_d)$ [see (5)]. SJMOS still operates in the saturation region, and i_{ch} is given by (1b). Fig. 7(c) shows the equivalent circuit in this mode. $i_g \ll i_d$ and voltage drop due to i_g in the power loop is neglected. Applying KVL in the power loop and using the aforementioned approximations, we obtain (14). By using (14) and applying KVL in the gate loop, (15) is obtained. Application of KCL at the nodes g' and 2, (16) and (17) are obtained, respectively. (18) and (19) are obtained by solving the KCL equations at the nodes g and d. (14)–(19) and (1b) govern the dynamics of this mode. They form a set of coupled nonlinear first-order differential equations, and FDM are used to obtain the solution. The analysis of this mode is further divided into multiple submodes; each of these modes is presented in detail as follows.

3) Submode III-A: In the beginning of this submode, SiC SBD is reverse-biased and starts blocking voltage across it. The difference $i_d - I_0$ charges the diode depletion capacitance C_d and v_d rises. Consequently, i_d starts to drop, and the difference between i_{ch} and i_d discharges the output capacitance ($C_{gd} + C_{ds}$) of the SJMOS. In this submode, $C_{gs} \gg C_{gd}, C_{ds}$ as $v_{ds} \geq V_{T1}$ [see (3), (4) and Fig. 4(a)]. The variation in C_{gd} and C_{ds} are small, and hence, they are replaced by equivalent charge-related capacitance given by (20) and (21), respectively. Applying the above approximations on (18) and (19), we obtain (22) and (23), respectively. Equations (14)–(17) along-with (22), (23), and (1b) determine this submode's dynamics. Submode III-A ends when $v_d = V_{T2}$ [see (5)].

$$C_{GDQ} = \frac{1}{V_{\text{dc}} - V_{T1}}\int_{V_{T1}}^{V_{dc}} \left(k_2\left(v_{ds} - V_{T1}\right) + k_3\right) v_{ds} \tag{20}$$

$$C_{DSQ} = \frac{1}{V_{\text{dc}} - V_{T1}}\int_{V_{T1}}^{V_{dc}} \left(k_4\left(v_{ds} - V_{T1}\right) + k_5\right) dv_{ds} \tag{21}$$

$$\frac{dv_{ds}}{dt} \approx \frac{i_d - i_{ch} + i_g - \frac{v_{g'd} - v_{gd}}{R_{g1}}}{C_{DSQ} + C_{GDQ}} \tag{22}$$

$$C_{gs}\frac{dv_{gs}}{dt} \approx \frac{\frac{C_{GDQ}}{C_{DSQ}}(i_d - i_{ch} + i_g) + \left(\frac{v_{g'd} - v_{gd}}{R_{g1}}\right)}{1 + \frac{C_{GDQ}}{C_{DSQ}}}. \tag{23}$$

3) Submode III-B: This submode begins when $v_d = V_{T2}$ and $C_d(v_d)$ is represented by (5b). The output capacitance continues to discharge due to $(i_{ch} - i_d)$. In this submode, variation in C_d is small, and hence, C_d is replaced by equivalent charge-related capacitance given by (24). The governing equations of this submode are similar to that of the submode III-A. This submode ends when $v_{ds} = V_{T1}$.

$$C_{DQ} = \frac{1}{V_{dc} - V_{T2}}\int_{V_{T2}}^{V_{dc}} \left(k_8\left(v_d - V_{T2}\right) + k_9\right) d\, v_d. \tag{24}$$

3) Submode III-C: Submode III-C begins when $v_{ds} = V_{T1}$. C_{gd} and C_{ds} can no longer be replaced by constant values as the previous submodes and (3b) and (4b) are used for them, respectively. As v_{ds} continues to fall, both C_{gd} and C_{ds} increase sharply [see Fig. 4(a)]. Consequently, the rate of fall of v_{ds} reduces significantly, and a second slope is observed for the v_{ds} waveform (see Fig. 6). The variation of C_d is small in this submode, and equivalent charge-related capacitance C_{DQ} is used for it. Equations (14)–(19) and (1b) governs the dynamics of this submode. Based on the relative values of C_{gd} and C_{ds},

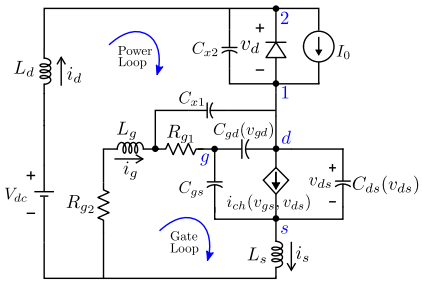


Fig. 8. Circuit for turn-OFF analysis.

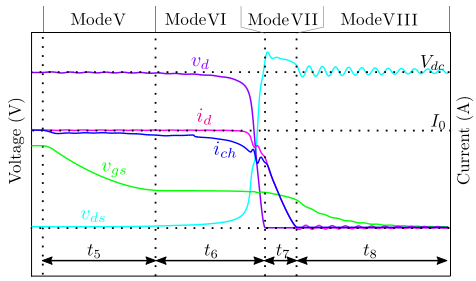


Fig. 9. Turn-OFF simulation waveform.

the coupling between gate and power loop could be significant. In such a case, drain-gate voltage v_{dg} becomes equal to zero before the SJMOS enters into the ohmic region and submode III-C ends. However, if the coupling is not significant, SJMOS enters the linear region before $v_{dg} = 0$, and submode III-D does not exist in this case.

3) Submode III-D: This submode begins when $v_{dg} = 0$. C_{gd} in this submode is a constant oxide capacitance given by (3a). The governing equations are same as that of submode III-C. This submode ends when $v_{ds} = v_{ds(sat)}$.

Voltage fall period ends when Si SJMOS enters the ohmic region. t_3 denotes the total time period for Mode III. Due to the complex coupled nature of the equations, FDM is used to numerically compute the actual energy loss incurred in Mode III. It is noteworthy that suitable approximations used in each submode make the numerical procedure simpler.

4) Mode IV: Ringing Period: When $v_{ds} = v_{ds(sat)}$, ringing period begins. i_{ch} depends on both v_{gs} and v_{ds} [see (1c)]. $v_{ds} \ll v_d, V_{dc}$ and hence neglected for simplicity. C_d, L_d and L_s form an undamped tank circuit which can be solved with the initial conditions: $v_d = V_{d3}$ and $i_d = I_{d3}$ obtained at the end of Mode III. In practice, there exists high frequency ac resistance and nonlinear channel resistance in the power loop, which provides damping in the circuit and leads to energy loss. The actual energy loss during Mode IV is obtained from (25). It is found that E_4 is negligible compared to total turn-ON switching loss (see Section VI).

$$E_4 = \frac{1}{2} C_{D0} \left(V_{d(max)}^2 - V_{dc}^2 \right) \tag{25}$$

$$V_{d(\max)} = V_{\rm dc} + \sqrt{\frac{I_{d3} - I_0}{\omega C_{D0}} + (V_{d3} - V_{dc})^2}$$

$$\text{where, } \omega = \sqrt{\frac{1}{C_{D0}\,(L_d + L_s)}}. \tag{26}$$

The total actual switching energy loss during the turn-on switching transition $E_{\rm on} \approx E_2 + E_3$ and turn-ON time, $t_{\rm on} = t_1 + t_2 + t_3$.

B. Turn-OFF Analysis

The turn-OFF switching transition begins when Si SJMOS is gated OFF. The turn-OFF behavioral model (see Fig. 8) is also simulated in MATLAB/Simulink, and the important waveforms

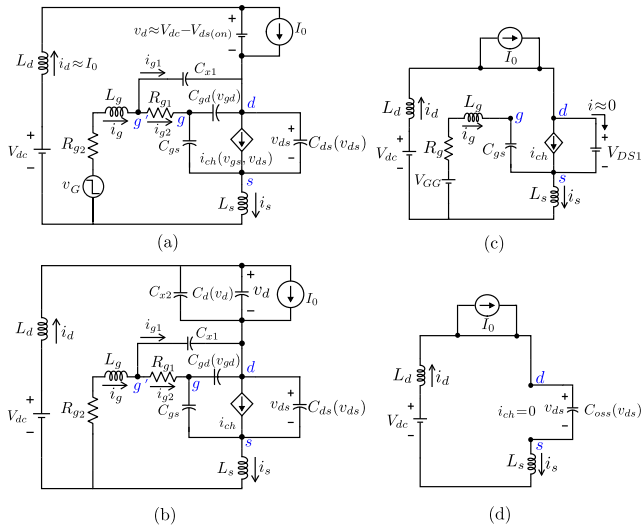


Fig. 10. Equivalent circuits for (a) Mode V, (b) Mode VI, (c) Mode VII, and (d) Mode VIII.

are shown in Fig. 9. Similar to the turn-ON analysis, turn-OFF analysis is also divided into four modes as follows.

1) Mode V: Delay Period: In the beginning of Mode V, Si SJMOS is in the ON-state with a drop of $V_{ds(\rm on)}$[1] [see (27)] and I_0 flows through it. i_{ch} depends on both v_{gs} and v_{ds} in this mode [see (1c)]. SiC SBD is reverse biased and blocks voltage ($V_{\rm dc} - V_{ds(\rm on)}$). $C_{gd} = C_{ox}$ as $v_{dg} < 0$ [see (3a)]. For the entire duration of Mode V, $v_{ds} \ll v_d, V_{\rm dc}$ and hence, power loop remains unaffected i.e., $v_d \approx V_{\rm dc} - V_{ds(\rm on)}$ and $i_d \approx I_0$. Fig. 10(a) shows the equivalent circuit of this mode.

$$V_{ds(\rm on)} = \left(1 - \sqrt{\frac{I_0}{I_{CH}(V_{GG})}}\right) V_{ds(sat)}(V_{GG}) \tag{27}$$

Mode V starts when SJMOS is gated OFF by applying $v_G = 0$V to the gate terminal. v_{gs} of the SJMOS starts dropping which in consequence also reduces i_{ch}. The difference $(i_d - i_{ch})$ charges the output capacitance (C_{oss}) and v_{ds} rises from $V_{ds(\rm on)}$. As discussed in Submode III-C, the condition $v_{dg} = 0$ is reached earlier/later than $v_{ds} = v_{ds(sat)}$ depends on the relative values

[1] $V_{ds(sat)}(V_{GG}) = kpV_{GG}(V_{GG} - V_{th})$

$I_{CH}(V_{GG}) = \dfrac{\beta(V_{GG} - V_{th})^2}{1 + \theta(V_{GG} - V_{th})}$

of C_{gd} and C_{ds}. Equations (15)–(16), (18)–(19), and (1b) determines the dynamics of this mode with $V_{GG} = 0$. These equations form reduced-order coupled nonlinear differential equations and are solved using FDM. The actual switching energy (E_5) is obtained by numerically integrating the product of v_{ds} and i_{ch}. This mode ends when Si SJMOS enters into the saturation region, i.e., $v_{ds} = v_{ds(sat)}$.

2) Mode VI: Voltage-Rise Period: As the SJMOS enters into the saturation region, Mode VI begins. Fig. 10(b) shows the equivalent circuit. Initially, $v_{ds} = v_{ds(sat)}$ and i_{ch} exclusively depends on v_{gs} see (1b). The difference $i_d - i_{ch}$ charges the output capacitor, and v_{ds} rises. Analysis of this mode is similar to the voltage-fall period analysis but in the reverse direction, i.e., Mode III-D to Mode III-A (see Mode III). This mode ends when SiC SBD becomes forward-biased.

Special Case: For low values of I_0 and/or R_{g2}, channel current becomes zero before the voltage-rise period gets over. In this case, Mode VII does not exist.

3) Mode VII: Current-Fall Period: When the diode gets forward-biased, Mode VII starts. Except for the above-mentioned special case, there exists a small difference between i_d and i_{ch} which increases v_{ds} beyond V_{dc} (see Fig. 9). Similar to Mode II, a linear fall in channel current is assumed, i.e., $i_d \approx i_{ch} \approx I - m_f t$. $I = \frac{1}{2}(I_{D6} + I_{CH6})$ where I_{D6} and I_{CH6} are the values of i_d and i_{ch} at the end of Mode VI. Consequently, $v_{ds} \approx V_{DS1}$ is approximately taken to be constant. Fig. 10(c) depicts the equivalent circuit of this mode.

A procedure similar to Mode II, along with the condition that at time $t = t_7$, $i_{ch} = 0$ or $m_f = \frac{I}{t_7}$ is applied to obtain a quadratic equation in m_f. The roots of the above equation will be well separated for an over-damped gate circuit. An approximate value of m_f is obtained such that resultant $V_{DS1} = V_{dc} + (L_d + L_s)m_f$ is close to V_{dc} [see (28)]. The actual energy loss in this mode is given by (29). This mode ends when $i_{ch} = 0$.

$$m_f = \frac{V_{th} + \frac{I\theta}{2\beta} + \sqrt{\left(\frac{I\theta}{2\beta}\right)^2 + \frac{I}{\beta}}}{\frac{R_g C_{gs}}{\beta}\left(\theta + \frac{0.5\theta^2 I + \beta}{\sqrt{(0.5I\theta)^2 + I\beta}}\right) + L_s} \tag{28}$$

$$E_7 = \int_0^{t_t} (I - m_f t) V_{DS1} = V_{DS1} t_7 \left(I - \frac{1}{2} m_f t_7\right). \tag{29}$$

4) Mode VIII: Ringing Period: When v_{gs} falls below V_{th}, $i_{ch} = 0$ and the ringing period starts. As v_{ds} is comparable to V_{dc}, both C_{gd} and C_{ds} does not vary much and (20) and (21) can be used for them. These capacitances form an undamped tank circuit with the parasitic inductances L_d and L_s. In practice, there exists high frequency ac resistance in the circuit that leads to energy loss. The actual switching energy loss in this mode is given as follows:

$$E_8 = \frac{1}{2}(C_{GDQ} + C_{DSQ})(V_{DS1}^2 - V_{dc}^2) \tag{30}$$

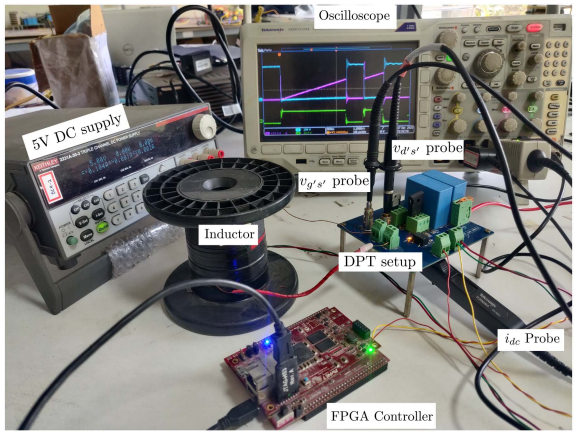


Fig. 11. DPT Setup.

TABLE IV
DEVICE PAIRS USED IN THIS STUDY

	Si SJMOS	Rating (A)	SiC SBD	Rating (A)
Pair 1	IPW65R110CFDA	31.2	CVFD20065A	26
Pair 2	IPP60R280P7	12	IDH04G65C6	12
Pair 3	STW37N60DM2AG	28	CVFD20065A	26

TABLE V
OPERATING CONDITIONS

	V_{dc} (V)	I_0 (A)	R_{g2} (Ω)
Pair 1	400	5,10,15,20,25	5,10
Pair 2	400	2.5,5,7.5,10	5,10
Pair 3	400	5,10,15,20,25	5,10

V. DETAILS OF EXPERIMENT AND SIMULATION

In this section, a detailed description of the simulation and the experiment is provided, and clear distinctions are made.

A. Details of the Experimental Setup

A DPT setup is designed to experimentally characterize the switching transients of Si SJMOS and SiC SBD pair (see Fig. 11). It can operate at $V_{\text{dc}} = 400\,\text{V}$ and load currents till $I_0 = 30\,\text{A}$. Two $8\,\mu\text{F}$ film capacitors and three $0.1\,\mu\text{F}$ ceramic capacitors are used as the dc bus. A $150\,\mu\text{H}$ air-core inductor is used as the load.

The DPT is conducted for three pairs of devices (see Table IV) and a wide range of operating conditions (see Table V). An isolated gate driver, Si8271, and a $+15/0\,\text{V}$ supply are used for driving Si SJMOS. $v_{d's'}(t)$, $v_{g's'}(t)$, and $i_d(t)$ are the important waveforms for switching dynamics characterization. These waveforms are captured in an oscilloscope using the equipment listed in Table VI and processed in MATLAB to obtain switching losses, times, (di/dt) and (dv/dt). Propagation delay matching was done before the experiment using the deskew fixture.

B. Description of Behavioral Simulation

The behavioral model, as delineated in section III, is implemented and simulated in MATLAB/Simulink using a fixed-step

TABLE VI
EQUIPMENT USED IN DPT

Equipment	Part No.	Key Features	waveforms measured
Oscilloscope	MDO3104	1GHz	–
Deskew Fixture	067-1686-00	8V max	–
Differential Voltage Probe	THDP0200	200MHz, 1.5kV	$v_{d's'}(t)$
AC/DC Current Probe	TCP0030A	120MHz, 50A	$i_d(t)$

TABLE VII
PARAMETERS—OBTAINED FROM MEASUREMENT

	L_{d1} (nH)	L_{d2} (nH)	L_s (nH)	L_g (nH)	C_{x1} (pF)	C_{x2} (pF)
Pair 1	57.59	54.617	9.5	10	4	15
Pair 2	58.1	47.85	14	10	4	15
Pair 3	57.85	53.74	9.2	9.5	4	15

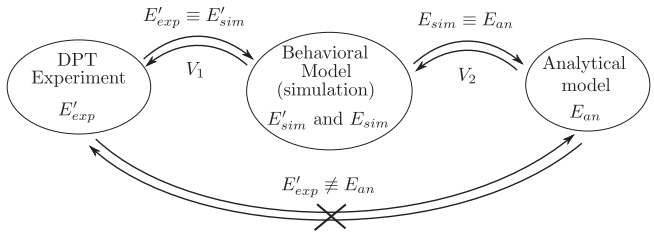
TABLE VIII
STATIC DEVICE PARAMETERS—EXTRACTED FROM DATASHEET

	V_{th} (V)	β (A/V^2)	θ (1/V)	k_p (1/V)
Pair 1	4.5833	16.588	0.1521	0.378
Pair 2	4.317	11.53	0.0761	0.9
Pair 3	4.827	30.87	0.1047	2.5

discrete-time solver and a step size of 1 ps. This is referred to as simulation in this article. The device characteristics are obtained from their respective datasheets. By curve-fitting these characteristics using (1), (3)–(5), the associated parameters are extracted and listed in Tables VIII and IX. Note: C_{ox} [see (3)] is obtained from the gate charge characteristics [32]. The external circuit parasitics are obtained through an experimental procedure as illustrated in [30]. For the power loop inductance measurement, the test voltage was set to 3.5 V. A current shunt and a 120 MHz ac/dc current probe were used to measure the device current. The same current shunt is used for measuring device current in both DPT and parasitic inductance measurement setups. Therefore, the inductance of the current shunt is a part of the power loop inductance L_d. Hence, it does not require to be compensated. Under elevated temperature conditions, $V_{\rm dc}$ should be properly selected by considering the change in the output characteristics. However, the parasitic inductance remains invariant to temperature changes.

VI. EXPERIMENTAL AND SIMULATION RESULTS

This section validates the proposed analytical model (see Section IV) through simulation and experimental results. Due to the presence of circuit parasitics, loss [$E'_{\rm exp}$ given by (7)] measured from DPT can be significantly different from the actual loss ($E_{\rm an}$) predicted by the proposed model. Hence, DPT cannot be directly used for validating the proposed model. An indirect approach is adopted in this article where the behavioral model is validated first by comparing its $E'_{\rm sim}$ with $E'_{\rm exp}$ obtained from DPT. The validated behavioral model is then used for verifying the proposed analytical model. Fig. 12 depicts the procedure for the proposed model validation.



V_1: Validation of the Behavioral model and extracted parameters from datasheet and measurement
V_2: Validation of the Proposed Analytical method using behavioral model

Fig. 12. Procedure undertaken for the proposed analytical model validation.

A. Validation of the Behavioral Model

To validate the behavioral model, key switching transient waveforms $[v_{d's'}(t), i_d(t)]$ obtained from the MATLAB simulation of the behavioral model are compared with that obtained from the DPT. Figs. 13–15 compares these key waveforms during the turn-ON and turn-OFF switching transients for device pair 1 to pair 3, respectively. As evident, the waveforms $[v_{d's'}(t), i_d(t)]$ predicted by the behavioral model match closely with the DPT experimental waveforms. The same observation also holds true for the remaining operating conditions. To further validate the behavioral model, the apparent losses obtained from the simulation (E'_{sim}) and DPT (E'_{exp}) are compared in Table X. A close match can be observed between E'_{sim} and E'_{exp} can be observed. Hence, it can be concluded that the behavioral model is sufficiently accurate in replicating the experimental waveforms over a wide range of operating conditions. It further asserts the accuracy of the extracted parameters from the datasheet and measured circuit parasitics.

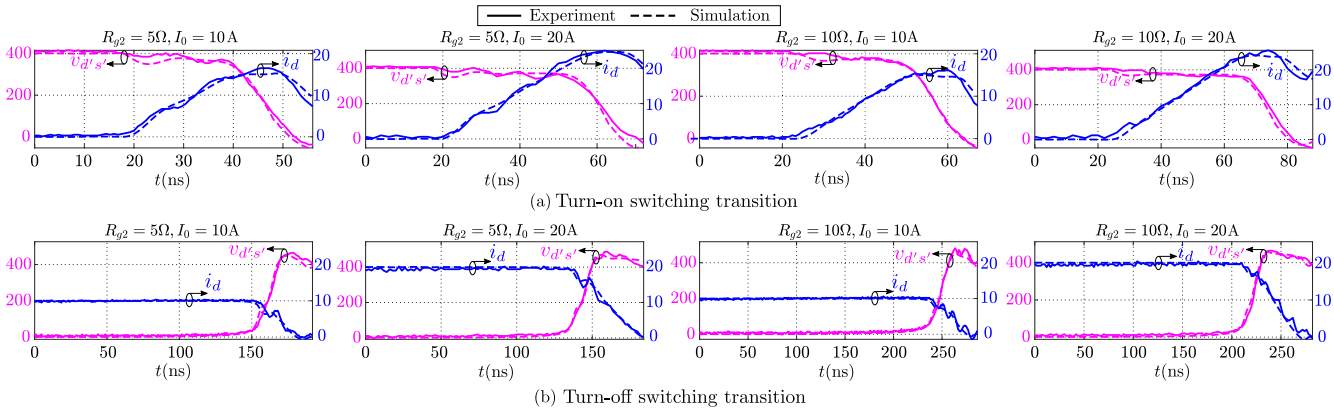
B. Validation of the Proposed Analytical Model Through Simulation and Experiment

In this section, the proposed analytical model is validated through simulation and experimental results. The validated behavioral model from the previous subsection is taken as a benchmark for validating the proposed analytical model. First, the switching transient waveforms obtained from the proposed model are compared with the behavioral model mode-by-mode. Then, using behavioral as the reference, additional comparison results like actual loss (E), (di/dt), and (dv/dt) are presented.

1) Modewise Validation of the Proposed Analytical Model: To validate the proposed analytical model, key waveforms (v_{ds}, v_{gs}, i_d, and i_{ch}) predicted by the analytical model are compared with the behavioral model in Fig. 16 for pair 1. Whereas Fig. 16(a) compares the turn-ON transition waveforms, the comparison of the waveforms during the turn-OFFswitching transition is shown in Fig. 16(b). A close match can be observed between the waveforms predicted by the two models. Due to approximations used in the proposed model, the waveforms show a slight deviation. However, it can be concluded that the proposed analytical model is sufficiently accurate in predicting the switching dynamics.

TABLE IX
DYNAMIC DEVICE PARAMETERS—EXTRACTED FROM DATASHEET

	C_{gs}	C_{gd}					C_{ds}				V_0	C_d				
		C_{ox}	C_{gd0}	k_1	k_2	k_3	C_{ds0}	k_4	k_5	k_6		C_{d0}	k_7	k_8	k_9	V_{d0}
	(pF)	(pF)	(pF)	(1/V)	(pF/V)	(pF)	(pF)	(1/V)	(pF/V)	(pF)	(V)	(pF)	(1/V)	(pF/V)	(pF)	(V)
Pair 1	3240	6650	3972	15	0.02334	8.8143	12960	25	-0.1666	103.68	100	1133	1.797	-0.01411	106.9169	200
Pair 2	761	1500	299.1	9	0.0057	1.3611	17830	5.5	-0.0374	22.615	45.31	336.6	0.4	-0.084	15.0382	200
Pair 3	1950	5950	1414	10.23	0.006	1.103	12420	19.11	-0.0016	50.15	100.9	1133	1.797	-0.01411	106.9169	200



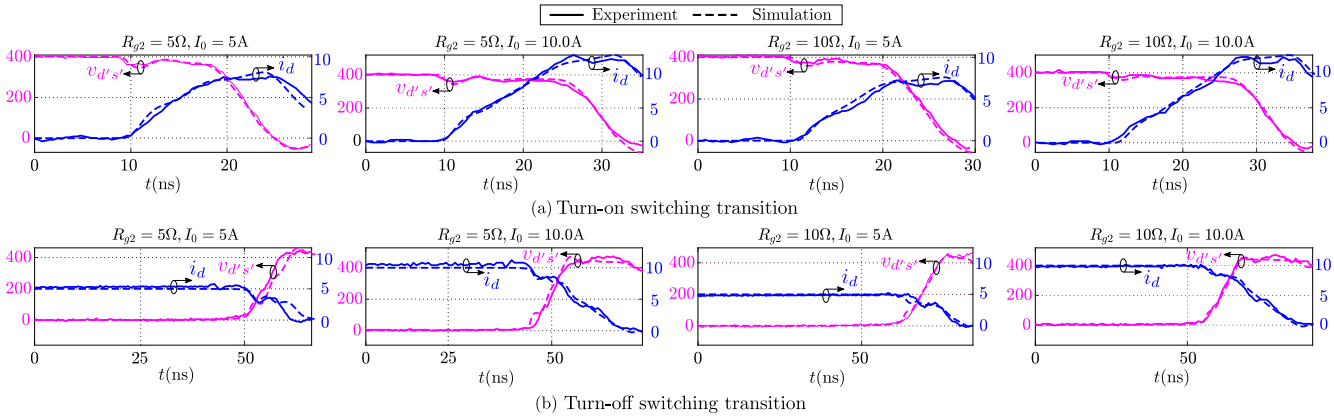
(a) Turn-on switching transition

(b) Turn-off switching transition

Fig. 13. Pair 1—Comparison of simulation and experimental waveforms: superimposed [$V_{dc} = 400$V].

TABLE X
COMPARISON OF APPARENT LOSS ($E' = \int_0^T I_d V_{d's'} dt$) OBTAINED FROM SIMULATION AND EXPERIMENT (I_0 IN A AND E' IN μJ)

	Pair 1					Pair 2					Pair 3	
	[400 V, 5 Ω]		[400 V, 10 Ω]			[400 V, 5 Ω]		[400 V, 10 Ω]			[400 V, 10 Ω]	
I_0	E'_{sim}	E'_{exp}	E'_{sim}	E'_{exp}	I_0 (A)	E'_{sim}	E'_{exp}	E'_{sim}	E'_{exp}	I_0	E'_{sim}	E'_{exp}
5	45.746	44.632	51.045	46.359	2.5	10.894	10.947	11.820	11.566	5	45.557	44.962
10	92.792	86.146	101.158	100.908	5	22.267	22.042	23.420	22.972	10	90.125	87.173
15	148.154	141.030	166.844	152.378	7.5	36.584	37.583	38.422	34.567	15	139.746	132.908
20	218.953	208.977	239.220	230.840	10	54.612	54.664	57.076	50.853	20	225.240	215.244
25	323.347	312.253	334.080	325.900						25	317.688	305.805



(a) Turn-on switching transition

(b) Turn-off switching transition

Fig. 14. Pair 2—Comparison of simulation and experimental waveforms: superimposed [$V_{\rm dc} = 400$V].

2) Comparison of Actual Loss, (di/dt) and (dv/dt): Fig. 17(a) presents a comparison of actual turn-ON switching loss obtained from the proposed analytical model with the behavioral model. Similarly, Fig. 17(b) compares the actual turn-OFF switching loss. A close agreement can be observed between the actual switching loss predicted by the analytical model and the behavioral model. A comparison of (di/dt) and (dv/dt) predicted by the analytical model with the simulation and the experiment is shown in Figs. 18 and 19, respectively. It can be observed that the analytical model can estimate (di/dt) and (dv/dt) with sufficient accuracy.

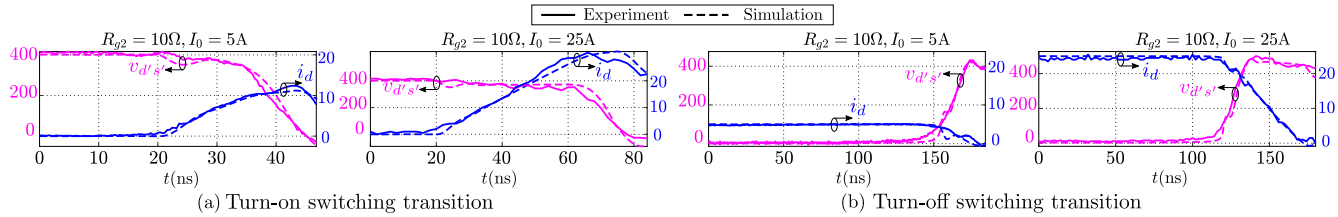


Fig. 15. Pair 3—Comparison of simulation and experimental waveforms: superimposed [$V_{\rm dc} = 400$V].

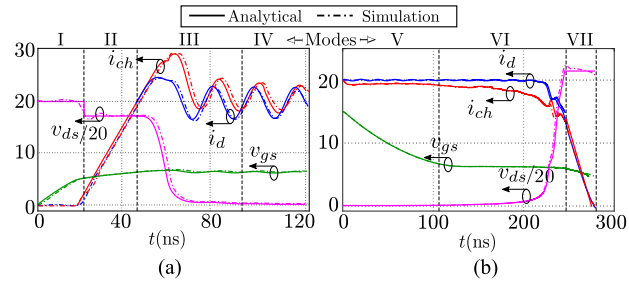


Fig. 16. Pair 1—Comparison of modewise simulation and analytical waveforms: [400 V, 20 A, 10Ω] (a) Turn-ON switching transition (b) Turn-OFF switching transition.

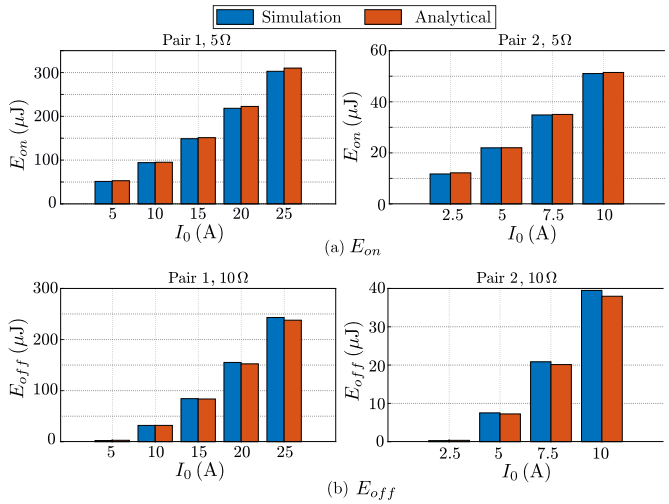


Fig. 17. Validation of analytical model [400 V]: (a) actual turn-ON switching loss $E_{\rm on}$ and (b) actual turn-OFF switching loss $E_{\rm off}$.

VII. Comparison With the Prior Arts

In this section, the proposed model is compared with the existing analytical model for high-voltage Si MOSFETS. It is worth noting that only two such references exist [24], [25]. By using the behavioral model as the reference, important switching transient-related quantities such as switching losses, times, (dv/dt), and (di/dt) obtained from the proposed model are compared with the prior arts. This reveals the merit of the proposed analytical model as compared to the existing literature. A comparison of the turn-ON and the turn-OFF switching dynamics is discussed in the following sections.

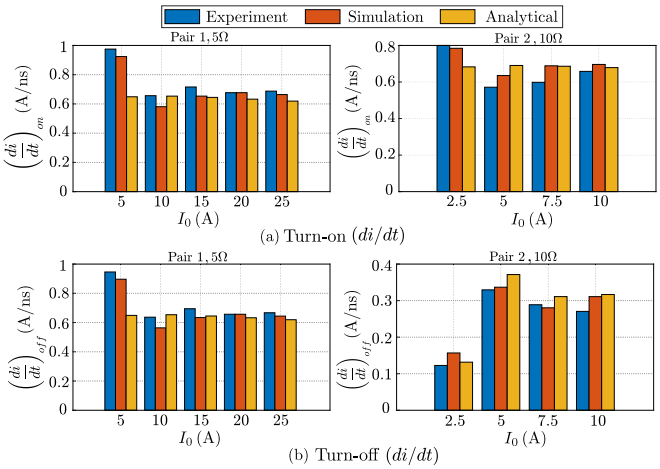


Fig. 18. Validation of analytical model: (di/dt) Comparison (a) Turn-ON (b) Turn-OFF.

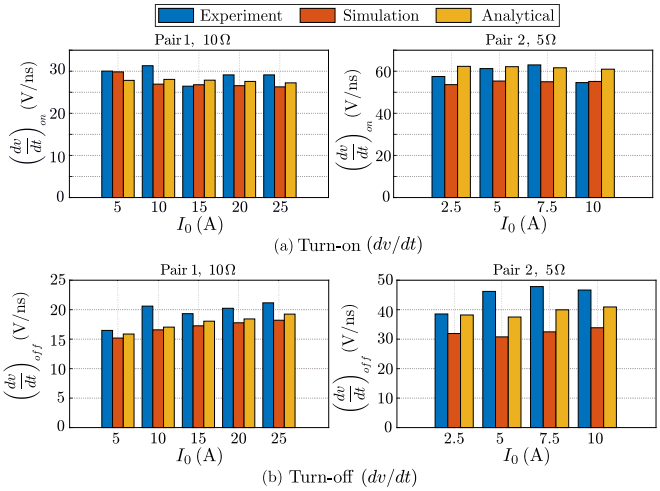


Fig. 19. Validation of analytical model: (dv/dt) comparison (a) turn-ON (b) turn-OFF.

A. Turn-ON Switching Dynamics

From Table I, it can be observed that both the prior art have a similar model for analyzing the turn-ON dynamics. Equation [25] is taken as the prior art for the comparison as it also considers the reverse-biased capacitance of the diode. From Fig. 20, the following observations are obtained.

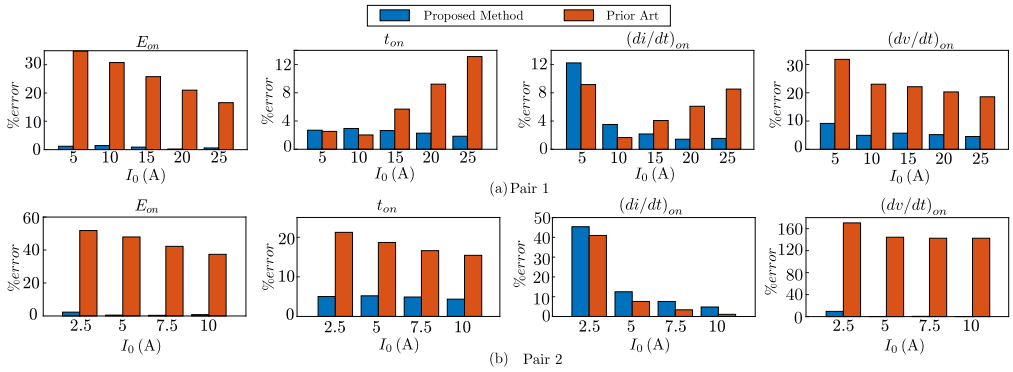


Fig. 20. Quantitative comparison of the proposed method with prior arts—E_{on}, t_{on}, $(di/dt)_{\text{on}}$ and $(dv/dt)_{\text{on}}$ at [$V_{\text{dc}} = 400\,\text{V}, R_{g2} = 10\,\Omega$].

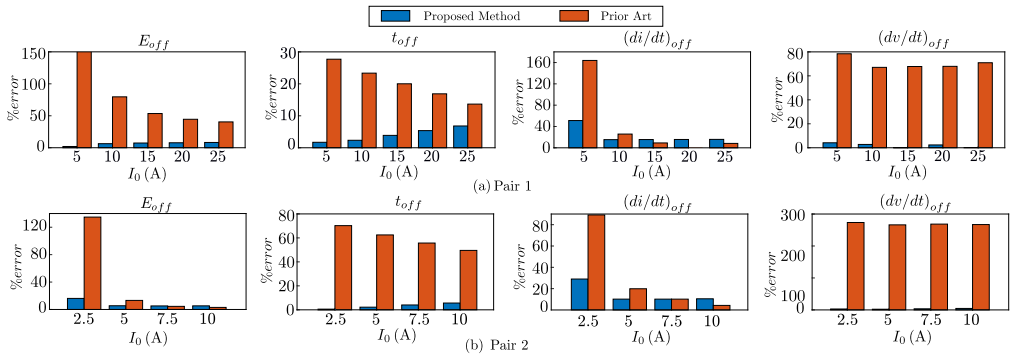


Fig. 21. Quantitative comparison of the proposed method with prior arts—E_{off}, t_{off}, $(di/dt)_{\text{off}}$ and $(dv/dt)_{\text{off}}$ at [$V_{\text{dc}} = 400\,\text{V}, R_{g2} = 10\,\Omega$].

1) Prior arts underestimates the turn-ON switching loss (E_{on}) significantly. While this error is close to 41% at the operating condition [5 Ω, 5 A], it reduces to about 16.7% at [10 Ω, 25 A] for pair 1. The error is more pronounced for pair 2 with the minimum error of 37%. The error is observed to reduce with both I_0 and R_{g2}. On the contrary, the proposed method estimates E_{on} with less than 6.75% error for all device pairs and operating conditions.
2) Prior arts also shows considerable error in estimating the turn-ON switching time t_{on}. Whereas the error increases to about 14% at higher currents for pair 1, an opposite trend is observed for pair 2. In contrast, the proposed model has an error of less than 5% for all operating conditions.
3) Both the proposed method and the prior arts perform equally well in predicting $(di/dt)_{\text{on}}$ during the turn-ON switching transients.
4) Prior arts is observed to overestimate the $(dv/dt)_{\text{on}}$ considerably. The error can be as high as 40% at low gate resistance. It reduces with both I_0 and R_{g2} for pair 1. This overestimation is even more pronounced for pair 2, with a minimum error of about 142% at all operating conditions. In contrast, the proposed method has an error of less than 16% and 9.58% for pair 1 and pair 2.

a) Turn-OFF switching dynamics: From Table II, it can be observed that prior arts have different performances in the modes V–VII. For a given mode, the prior art with the best performance is chosen for that mode. Whereas [24] is chosen for modes V and VI, [25] is used for mode VII. This constitutes the prior art for the comparison with the proposed model. The following important observations are obtained from Fig. 21.

1) Prior arts is observed to overestimate turn-OFFswitching losses E_{off} by >50% for pair 1. However, the prior arts have similar performance in estimating E_{off} for pair 2. Due to a significantly higher (dv/dt) rate, switching loss is small in mode VI, compensating for the prior arts' overestimation in mode VII. On the contrary, the proposed model has an accuracy of >92% for all device pairs and operating conditions.
2) It is observed that prior arts significantly underestimate the turn-OFF switching time t_{off}. The error of more than 10% and 40% are observed for pair 1 and pair 2, respectively. Underestimating turn-OFF times may lead to shorter dead times, causing shoot-through events. The proposed method, in contrast, has an error <7% for all conditions.
3) Both the proposed method and the prior arts predict the turn-OFF $(di/dt)_{\text{off}}$ with similar accuracy.
4) It is also observed that $(dv/dt)_{\text{off}}$ is significantly overestimated by the prior arts. While error is estimating $(dv/dt)_{\text{off}}$ is more than 80% at $R_{g2} = 5\,\Omega$, it reduces to about 62% at $R_{g2} = 10\,\Omega$ for pair 1. Overestimation is even more pronounced for pair 2 with a minimum error of about 250% at all operating conditions.

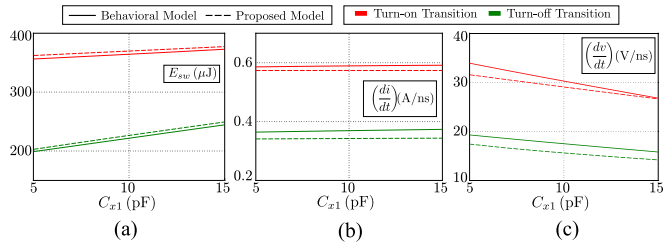


Fig. 22. Impact of C_{x1} variation [$V_{\text{dc}} = 400\,\text{V}$, $R_{g2} = 10\,\Omega$, $I_0 = 10$ A]: (a) switching loss E_{sw}, (b) (di/dt), and (c) (dv/dt).

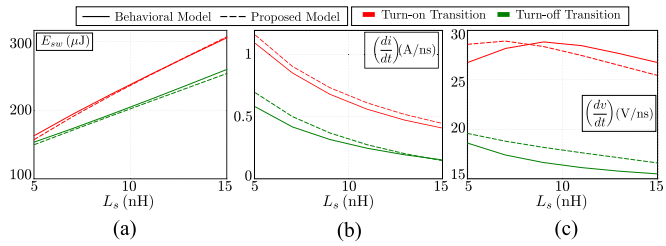


Fig. 23. Impact of L_s variation [$V_{\text{dc}} = 400\,\text{V}$, $R_{g2} = 10\,\Omega$, $I_0 = 10$ A]: (a) switching loss E_{sw}, (b) (di/dt), and (c) (dv/dt).

VIII. Impact of Important Parasitics on the Proposed Model

This section briefly discusses the impact of the external circuit parasitics on the outcome of the proposed model, such as loss, time (di/dt), and (dv/dt). Among the considered parasitics in this article, the impact on C_{x1} and L_s is presented as they significantly impact the model's outcomes.

For a practical converter C_{x1} can vary in the range $(5, 15)pF$. The impact of C_{x1} variation on the turn-ON and turn-OFFswitching losses is shown in Fig. 22(a). Similarly, its impact on (di/dt) and (dv/dt) are shown in Fig. 22(b) and (c), respectively. It can be observed that whereas switching loss and (dv/dt) is impacted significantly due to variation in C_{x1}, (di/dt) is least affected. On the other hand, L_s significantly impacts the switching losses and (di/dt). Whereas, (dv/dt) is weakly dependent on L_s. It can also be observed from Figs. 22 and 23 that the proposed model can incorporate the parasitic parameter variation for estimating its outcomes with sufficient accuracy.

IX. Comparison With the Gate Charge, SPICE, and DPT Methods

This section compares the switching loss estimated by the proposed analytical model with the conventional gate charge method [33] and the apparent loss estimated by the SPICE simulation and the experimental (DPT) method. The behavioral model (simulation) is taken as a benchmark for comparison as it is sufficiently accurate in predicting the switching dynamics. The losses estimated by the gate-charge method are significantly different from actual loss [34].

As mentioned in Section III, due to the inaccessibility of the internal nodes, it is not possible to obtain actual drain-source voltage and channel current from the SPICE simulation and DPT experiment. Hence, only apparent loss E' [see (7)] can be obtained from these two methods, and it can be significantly different from the actual loss E [see (6)]. To show this, the actual switching loss obtained from the proposed analytical model is compared with the apparent loss obtained from SPICE and DPT in Fig. 24. The percentage error in these plots is computed with the actual switching loss obtained from the behavioral model as a reference. It can be observed that both SPICE and DPT have similar performance in predicting the switching losses. Whereas they underestimate the turn-ON loss, turn-OFF losses are significantly overestimated. *Hence, it can be concluded that losses obtained from SPICE and DPT can differ from actual losses considerably.*

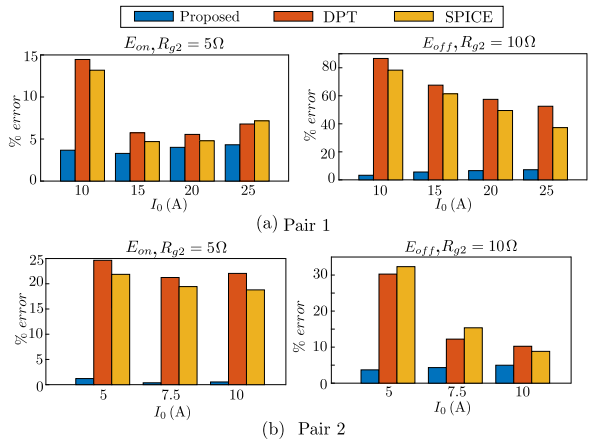


Fig. 24. Comparison of % error in switching energy loss.

X. Conclusion

In this article, an improved analytical model is presented for studying the hard switching dynamics of Si SJMOS and SiC SBD pair. Unlike the existing literature for high-voltage Si MOSFETS, this article considers nonlinearities in channel current and capacitance of Si SJMOS and reverse-biased capacitance of SiC SBD. In addition, it also takes parasitic capacitance due to PCB layout into account. The proposed analytical model is derived by dividing switching transients into multiple modes and applying suitable approximations in each mode. This results in either closed-form expressions or reduced-order nonlinear equations, which is solved using FDM. Experimental and simulation results for three pairs of 650 V Si SJMOS and SiC SBD with different current ratings validate the proposed model. The presented model is also valid for the entire spectrum of Si SJMOS and 650 V SiC SBDs. It is noteworthy that the existing models of low-voltage Si MOSFETS, GaN HEMTs, and SiC MOSFETS are not directly applicable to Si SJMOS due to differences in characteristics.

The proposed analytical model achieves a precise estimation of switching loss (with less than 5% error for E_{on} and less than 8% error for E_{off}) across the majority of operating conditions. Moreover, it demonstrates high accuracy in predicting time, (di/dt), and (dv/dt), with accuracies exceeding 97.5%, 92%,

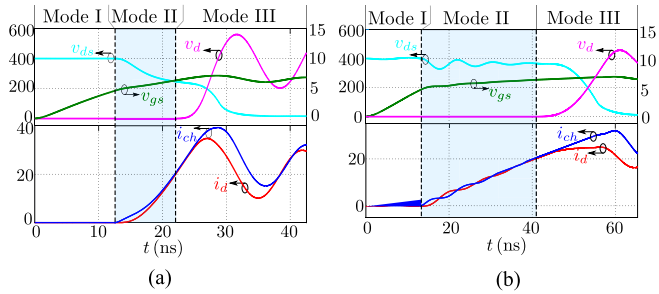


Fig. 25. Turn-ON switching transient waveforms: (a) Kelvin-source configured Si SJMOS and (b) common-source configured Si SJMOS.

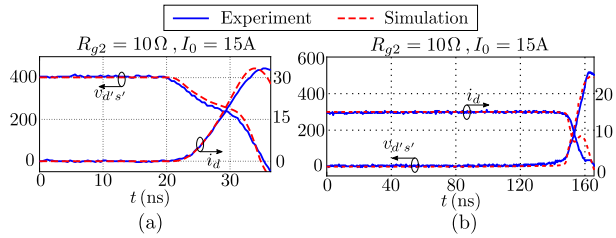


Fig. 26. Validation of behavioral model for the Kelvin-source configured Si SJMOS [$V_{\rm dc} = 400$ V]: (a) turn-ON switching transient and (b) turn-OFF switching transient.

and 94%, respectively. In addition, the proposed model can accurately estimate the turn-OFF delay time due to the accurate modeling of the gate-drain capacitance adopted in this article, which is essential for the proper selection of dead time. As a result, this article presents significant improvements over the existing literature on high-voltage Si MOSFETS and also establishes the importance of modeling the nonlinearities. Among the popular switching loss estimation techniques, gate charge results in a significant error. DPT and SPICE-based simulation perform moderately well for most operating conditions. However, the loss obtained from DPT and SPICE can be considerably different from the actual loss.

APPENDIX

A. Analytical Model for Si SJMOS in Kelvin-Source Configuration

To analyze the switching dynamics of Kelvin-source configured (TO-247-4 packaged) Si SJMOS, the equivalent circuit shown in Fig. 2 can be used. However, the value of common-source inductance L_s is very small ($\approx 0.2 - 1nH$) due to the Kelvin-source connection.

Turn-ON simulation waveforms obtained for both TO-247-4 packaged and TO-247-3 packaged Si SJMOS are shown in Fig. 25. As evident, v_{ds} of TO-247-4 packaged Si SJMOS experiences a significant fall during mode II. As a result, the gate and the power loop get fully coupled through C_{gd} and C_{x1}. Note: v_{ds} can fall by more than 50% of its initial value ($V_{\rm dc}$). Consequently, approximations stated in Section IV-A are not applicable. Note: L_{gT} is ignored as it does not significantly impact the switching transients. (31)–(33) govern the dynamics of mode II and can be solved using FDM. Analysis for the other modes (Mode I and III) remains the same

$$V_{GG} \approx \tau_1 \frac{dv_{gs}}{dt} + v_{gs} + L_s \frac{di_d}{dt} - \tau_2 \frac{dv_{ds}}{dt} \tag{31}$$

$$v_{ds} = V_{dc} - (L_{dc} + L_s) \frac{di_d}{dt} \tag{32}$$

$$(i_d - i_{ch}) \approx \underbrace{(C_{ds}(v_{ds}) + C_{gd}(v_{dg}) + C_{x1})}_{C_{oss(eq)}(v_{dg}, v_{ds})} \frac{dv_{ds}}{dt}. \tag{33}$$

The analysis of modes V and VI also remains the same as they are negligibly impacted due to small L_s. However, it impacts Mode VII. v_{ds} experiences significant variation in this mode, resulting in coupled dynamics similar to mode II, which can be solved numerically. On the other hand, v_{ds} was approximated to be constant and $i_d \approx i_{ch}$ for common-sourced Si SJMOS in this mode.

TABLE XI
VALIDATION OF THE ANALYTICAL MODEL

R_{g2} (Ω)	I_0 (A)		Turn-on switching Transient		Turn-off switching Transient	
			t_{on} (ns)	E_{on} (μJ)	t_{off} (ns)	E_{off} (μJ)
10	5	A	45.958	31.277	163.752	0.671
		S	49.375	32.047	175.86	0.656
	25	A	43.876	77.764	153.04	87.415
		S	56.24	80.34	154.095	84.515

A - Analytical Model S - Behavioral Simulation

The validation of the analytical model developed for the Kelvin-source configured Si SJMOS is done along similar steps. Fig. 26 compares the experimentally obtained $v_{g's'}$, $v_{d's'}$, and i_d waveforms with the behavioral model for the operating condition $V_{\rm dc} = 400\,{\rm V}$, $R_{g2} = 10\,\Omega$, $I_0 = 15$ A. It can be observed that the model can predict the switching transients with good accuracy. However, a slight deviation is observed in the estimation of $v_{g's'}$ and $v_{d's'}$ overshoot. The behavioral model is then taken as a reference for validating the analytical model for TO-247-4 packaged Si SJMOS. Table XI shows switching transient times and losses obtained from the analytical model match closely with the behavioral model. This validates the analytical model for the Kelvin-source configured Si SJMOS. From these results, it can be concluded that, by suitably modifying the analytical model presented in Section IV for the common-source configuration during the modes II and VII, an analytical model for Kelvin-source configured Si SJMOS can be obtained, which is sufficiently accurate in estimating the switching losses.

B. Comparison of Proposed SiC SBD Capacitance Model With Existing Nonlinear Models

A comparison of the proposed reverse-biased capacitance model of the SiC SBD with the existing models in the literature [14], [35], [36] is presented in this section. These models are listed in Table XII. The performance of these models in representing the capacitance characteristics obtained from the diode's datasheets is also shown in Fig. 27 for three 650 V rated Schottky diodes (CVFD20065 A - 57 A, C6D10065 A - 37 A and IDH04G65C6 - 12 A).

TABLE XII
SIC SBD REVERSE-BIASED CAPACITANCE MODELS

Reference	Diode's Capacitance Model $C_d(v_d)$
[35]	$\frac{C_0}{(1+\frac{v_d}{V_J})^m}$
[36]	$\frac{C_0}{(1+\frac{v_d}{V_J})^m}+C_1$
[14]	$\frac{C_0}{1+k(v_d)^m}+C_1$
Proposed Piecewise Capacitance Model	$\begin{cases} C_{d0}\left(1+\frac{v_d}{V_J}\right)^{-0.5} & v_d \le V_{T2} \\ k_8(v_{ds}-V_{T2})+k_9 & v_d \ge V_{T2} \end{cases}$

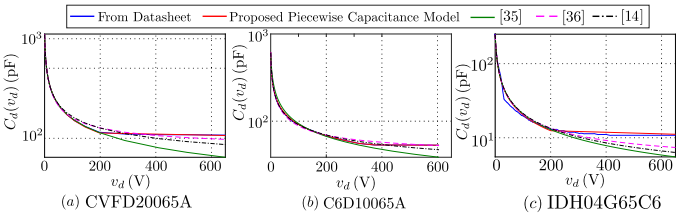


Fig. 27. Comparison of SiC SBD reverse-biased capacitance models: (a) CVFD20065 A, (b) C3D08065I, and (c) IDH04G65C6.

Among the existing models, [35] is a well-known model used to represent the SiC Schottky diode's capacitance. Although it can adequately model the low-voltage region of the capacitance curve, a significant deviation is observed in the high-voltage regions (see the dark green curve in Fig. 27). Wang et al. [36] extended the model given in [35] by adding a constant term C_1 to obtain a better fitting result in the high-voltage region. However, it still has distinct mismatch regions (see the dotted magenta curve in Fig. 27). The junction capacitance model of the low-voltage Si MOSFETS (<40 V) was used in [14] with an additional constant term C_1. It has a performance similar to [36] (see the dash-dotted black curve in Fig. 27). In contrast, the proposed piecewise model can accurately represent the reverse capacitance of SiC SBD throughout the voltage range (see the red curve in Fig. 27). It is also to be noted that this capacitance was either neglected [24] or considered to be constant [25] for the switching dynamics analysis of Si MOSFETS in the earlier work.

C. Guidelines to Select Proper Time-Step for FDM

In this work, the forward Euler-based FDM is used to solve the set of reduced-order nonlinear differential equations obtained in some modes of the analytical model. For an explicit method such as the forward Euler, it can be shown that the method will converge if the step-size (h) used satisfies ($h < 2/|\lambda_{\max}|$) where $\lambda_{\max}$ is the maximum eigenvalue of a linear system [37]. However, in a nonlinear system, obtained eigenvalues of the linearized system also keep varying, and it is difficult to determine the maximum eigenvalue. Here, we present a guideline to obtain the proper time step for solving a nonlinear switching transient circuit with nonlinearly varying device capacitances. 1) Linearize the system at operating points where devices' capacitances are minimum. This can be done at the voltages

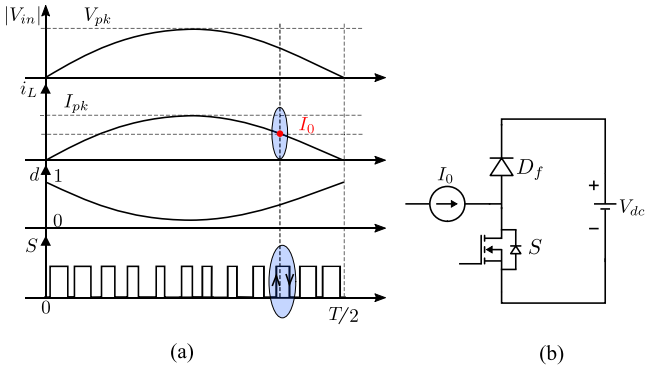


Fig. 28. (a) Representative waveforms of conventional boost PFC. (b) Equivalent model during switching.

where capacitances undergo a sharp change and attain a very small value. 2) Obtain the eigenvalues of the linearized system at all such operating points. 3) Select the maximum eigen value $|\lambda_{\max}|$ from the obtained set of eigenvalues. 4) Select a time-step such that such that $h < (0.1/\lambda)$ condition is satisfied. This will lead to both stable and accurate results, and no convergence issues will be encountered.

D. Implemenation of the Proposed Analytical Model in Conventional PFC Circuit

The conventional boost PFC topology is shown in Fig. 1, and its representative waveforms over half a line cycle are shown in Fig. 28(a). $|V_{\text{in}}|$ represents the rectified voltage after the diode-bridge and i_L denotes the inductor current in phase with $|V_{\text{in}}|$. Note: current ripple is ignored to present a simpler analysis. During each switching instant, the inductor current (i_L) and output voltage (V_{dc}) do not change significantly. Hence, the PFC can be modeled as an equivalent buck circuit, as shown in Fig. 28(b). Then, the proposed model can be used to estimate the switching loss (E_{sw}) during turn-ON and turn-OFFtransitions (see Figs. 6 and 9). As i_L varies sinusoidally, switching loss estimation is carried out at multiple operating currents I_0. In contrast, conduction loss is relatively simple to obtain and independent of frequency. For a given loss budget and maximum allowable junction temperature, the switching frequency of the PFC converter can be obtained.

To illustrate this, a 2 kW conventional boost PFC with a unity power factor is considered. It has a single phase supply of $V_{\text{in}} = 230$ V , 50 Hz as input. The current through the boost inductor i_L is sinusoidal with a peak of $I_{pk} = \sqrt{2}(2000)/V_{\text{in}} = 12.3$ A. The proposed analytical model is used to estimate switching loss at multiple load currents, which is then curve-fitted to obtain total switching loss as a function of load current, as shown in Fig. 29(a). By integrating over the line cycle, the average switching loss can be obtained as

$$P_{sw} = f_{sw}\left(\frac{1}{T}\int_0^T E_{sw}(i_L)dt\right) \tag{34}$$

$$= \frac{f_{sw}}{2\pi}\left(a_2 I_{pk}^2\pi + 4a_1 I_{pk} + 2a_0\pi\right) \tag{35}$$

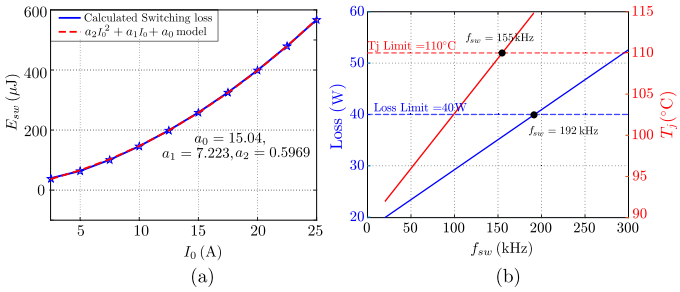


Fig. 29. (a) Switching loss as a function of current I_0. (b) Switching frequency estimation.

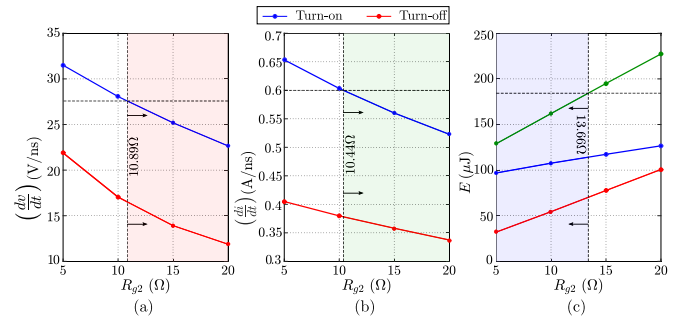


Fig. 30. Impact of R_{g2} on (a) (dv/dt) (b) (di/dt) and (c) Loss.

$$P_{cond} = \frac{1}{\pi}\left(\int_0^{T/2} (i_L^2 R_{on} d)dt \tag{36}$$

$$+ \int_0^{T/2} (i_L^2 R_d + i_L V_d)(1-d)dt\Bigg) \tag{37}$$

$$P_{total} = 116.7516 f_{sw} + 17.5773\, W. \tag{38}$$

Conduction loss can be obtained as (37). The first and second terms denote conduction loss in the MOSFET and diode, respectively. With $R_{\text{on}} = 0.099\,\Omega$, $V_d = 0.9681\,\text{V}$ and $R_d = 0.01885\,\Omega$ are obtained from the datasheets of Si SJMOS and SiC SBD, $P_{\text{cond}} = 17.5773\,W$. The total loss as a function of frequency is shown in (38). Now, for a maximum loss of 2% in the power device, i.e., $P_{\text{total}} = 0.02 * 2000\,\text{W}$ and maximum junction temperature of 110 °C with case temperature (T_c) fixed at 80 °C, the switching frequency can be selected as shown in Fig. 29(b). It can be observed that $f_{\text{sw}} = 155\,\text{kHz}$ can be selected as junction temperature exceeds the maximum T_j allowable value of 110 °C much before it hits the loss limit.

E. Guidelines for Selecting Gate Resistance

The gate driver circuit can significantly influence losses, (dv/dt) and (di/dt) through external gate resistance R_{g2}. Fig. 30 shows the effect of R_{g2} on these important quantities for device pair 1 (IPW65R110CFDA and CVFD20065 A), for $V_{\text{dc}} = 400\,\text{V}$ and $I_0 = 20\,\text{A}$. As evident, (dv/dt) and (di/dt) reduce with the increase in R_{g2}, whereas switching loss increases substantially. Therefore, the selection of R_{g2} is a tradeoff between the total switching loss and (dv/dt), (di/dt). Note: gate voltages are usually fixed (+15V/0 for Si SJMOS).

The selection of R_{g2} is illustrated by considering an example. Say, from the efficiency perspective, the total switching loss is to be kept less than 180 μJ. At the same time, (dv/dt) and (dv/dt) should be less than 27.5 V/ns and 0.6 A/ns, respectively. From Fig. 30, R_{g2} should be greater than 10.89Ω and 10.44Ω for satisfying the (di/dt) and (dv/dt) requirements, whereas R_{g2} should be less than 13.66Ω for meeting the loss limit. Therefore, $R_{g2} \in (10.89, 13.66)\,\Omega$ is a feasible solution. However, for more stringent requirements, it may not be possible to meet loss and slew rate requirements simultaneously.

F. Generality of the Model

The circuit-based model, as depicted in Fig. 2(b), (1), (3), (4), is verified across a spectrum of Si SJMOS sourced from various manufacturers and featuring diverse voltage and current specifications. This encompasses Si SJMOS rated at 500 V (IPA50R380CE), 600-650 V (FCH040N65S3, IPA65R065C7, IPA60R080P7, IPW60R017C7, R6012JNJ, R6030JNZ4, STP18N60DM2, STWA45N65M5, STY112N65M5) and 950 V (IPW95R130PFD7). Similarly, the model [shown in Fig. 2(c), (5)] is verified for multiple 650 V SiC SBD from different manufacturers and current ratings (GE10MPS06 A, IDDD20G65C6, LSIC25D065D20 A, PSC1065 A, SCS210AM, SCS220AGC17, STPSC10H065, STPSC20065-Y, C3D10065 A).

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Manish Mandal (Member, IEEE) received the B.Tech. degree in electrical and electronics engineering from the National Institute of Technology, Warangal, India, in 2017. He is currently working toward the Ph.D. degree in power electronics with the Electrical Engineering Department, Indian Institute of Science, Bangalore, India.

In 2018, he joined the Electrical Engineering Department, Indian Institute of Science. His research interests include the characterization and modeling of various aspects of switching dynamics of power semiconductor devices and active gate driving.

Shamibrota Kishore Roy (Member, IEEE) received the B.E. degree from Jadavpur University, Kolkata, India, in 2014, and the M.E. degree from the Indian Institute of Science, Bangalore, India, in 2016, both in electrical engineering. He is currently working toward the Ph.D. degree in power electronics with the Electrical Engineering Department, Indian Institute of Science, Bangalore, India.

From 2016 to 2017, he worked as a System Engineer with Cypress Semiconductor India. His research interests include characterization and modeling of wide bandgap power devices.

Kaushik Basu (Senior Member, IEEE) received the B.E. degree from the Bengal Engineering and Science University, Shibpore, India, in 2003, the M.S. degree in electrical engineering from the Indian Institute of Science, Bangalore, India, in 2005, and the Ph.D. degree in electrical engineering from the University of Minnesota, Minneapolis, in 2012.

He was a Design Engineer with Cold Watt India in 2006 and an Electronics and Control Engineer with Dynapower Corporation USA from 2013–2015. He is currently an Associate Professor with the Department of Electrical Engineering, Indian Institute of Science. He has been an author and co-author of several technical papers published in peer-reviewed journals and conferences. His research interests include various aspects of the general area of Power Electronics.

Dr. Basu is the founding chair of both IEEE PELS and IES Bangalore Chapter.