A DC/AC Modular Converter With Mid-Point Transformer for Integrating MVDC With MVAC for Railway Traction Power Supply

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***Abstract*—This work presents a half bridge (HB) submodules (SMs) based modular multilevel converter (MMC) topology intended to integrate MVdc grid with a single phase MVac grid for railway traction power supply. The topology uses reduced arms/chain-links (two arms) of conventional HB-MMC and a mid-point transformer at the ac side to employ galvanic isolation needed for this application. Further, by utilizing the appropriate modulation technique and mid-point transformer, the cancellation of dc flux within the transformer is achieved. The inductance of the arm inductor can be combined with the leakage inductance of the mid-point transformer, thus eliminating the requirement for extra inductors. A unique precharging methodology for SM capacitors in the proposed topology is discussed, which differs from conventional approaches. The converter's performance during various fault scenarios is analyzed, showcasing its inherent fault-blocking capability. The operational principles are explained mathematically and validated through simulations and a scaled-down experimental prototype under both normal and fault conditions.**

***Index Terms*—DC flux balancing, faults, modular multilevel converter (MMC), MVac traction system, MVdc, precharging.**

I. Introduction

MVDC supply is getting popular alongside MVac supply due to the high penetration of renewable energy sources and batteries, easy grid integrations, reduced transmission losses, etc. [1], [2], [3]. With the MVdc grid, different applications like EVs, rail traction, data centers, renewable integrations, etc. are also booming [4], [5]. Furthermore, MVdc can also solve some serious problems related to MVac rail traction power supply like railway power quality issues and problems caused by neutral sections [6], [7], [8].

Electric railway traction systems are vital for a country's economic growth. Currently, a single-phase MVac traction power supply is predominant, where power is converted from three-phase MVac/ HVac grids to a single-phase MVac supply of 25 kV, 50 Hz. This gives rise to power quality challenges like imbalanced ac side voltage, the need for reactive power, and the presence of negative sequence components [9], [10], [11], [12]. These challenges present a notable risk to the stability and dependability of the power grid system, especially with the growing implementation of capacity-sharing features in electric railways [12].

To address these issues, the virtual cophase traction power supply system (i.e., railway power conditioner and railway unified power quality controller) are used. Despite their use, the existing challenges cannot be completely eradicated [12]. Moreover, in the literature, the application of the MMC-multiterminal dc (MMdc) technique [12], [13] provides promising remedies for creating traction power supply because of its modular design, independent regulation of active and reactive power, scalability, and absence of unnecessary reactive power demands [12].

The adoption of a dc system (such as MVdc [14] or MMC-MTdc [12]) in lieu of a three-phase MVac/HVac grid for rail traction power supply holds promise in tackling two noteworthy challenges. First, it can lead to the complete elimination of neutral sections, and second, it can effectively resolve power quality concerns [6]. Hence, with the increasing popularity of MVdc, it has become an alternate option for conversion of power from MVdc to single-phase MVac traction power supply. A comparative analysis of different rail traction power supply systems is explained in [12] showing their advantages and limitations. Recent literature studies [4], [5], [6], [12], [13], [14], [15] suggest that the single-phase MVac rail traction power supply can be derived from MVdc grids. Furthermore, MVdc can serve as a gateway for easily tapping into various distributed energy sources like wind, solar energy, battery energy storage system, etc. [4], [5], [6], [30].

To convert MVdc to MVac rail traction power supply, VSC-based multilevel converter topologies can be employed, thanks to their advantages such as modularity, scalability, and efficient fault management [4]. In 2003, a groundbreaking development occurred when Mraquardt et al. introduced the concept of a modular multilevel converter (MMC). The MMC swiftly emerged as the primary focus of research and application in the field of multilevel converters. Recently, researchers have started investigating the integration of MMC into railway traction power supply [4], [6], [11], [15].

For this application, a conventional single-phase half-bridge submodules (SMs) based MMC (HB-MMC) [11] can be used which requires four arms (four chain link). Each arm consists of a series connection of HB SMs along with an arm inductor to handle the MVdc voltage. However, conventional HB-MMC has

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four arms, which increases the device count and is vulnerable to both dc and ac faults.

In recent years, researchers have been investigating various configurations of MMCs with the aim of reducing switch count, minimizing energy storage needs, and improving the converter's ability to withstand various faults. Numerous research papers have been published, focusing on resolving the mentioned challenges. These configurations can be categorized into groups such as HB-MMC topologies with reduced arm, HB-FB based MMC topologies, and hybrid MMC topologies that incorporate director switches (DSs) [16], [17], [18], [19], [20].

HB-MMC topologies with a reduced arm (reduced device count) were presented by the researcher in [16] (two arms) and [19] (one arm). However, in [16], a bipolar MVdc grid or split capacitor at the dc side is necessitated for its operation. Furthermore, both ac and dc components flow through the primary side of the transformer in [16], requiring precise control over the transformer's saturation. In [19], multiple series-connected full-bridge SMs (FB-SMs) and passive filters on the ac side of the converter are utilized to prevent any dc component from entering the ac grid-side transformer. This leads to an escalation in the device and passive requirements within the topology.

Hybrid HB-MMC topologies with DSs can also be used for this MVdc to MVac grid integration are described in [17] and [18] where each phase contains a chain of HB-SMs and two [18] or four [17] DSs to generate required ac voltage. However, both [17] and [18] are susceptible to dc faults with HB-SMs. To make these topologies dc fault-tolerant, a modification is presented in [20] where a chain of FB-SMs is added in series with ac sides to protect the converter from dc faults. However, it increases the device count and overall losses in the converter during normal operation.

Some researchers have proposed MMC-based push-pull arrangements intended for battery storage applications [21] where the phases are connected in parallel to handle high current and low voltage. Another similar configuration [22] is made using FB-SMs instead of HB-SMs to make the converter fault-tolerant. Alternatively, for HVdc-HVac applications where high voltage and low current are involved, Kaya et al. [23] introduce a series-connected MMC setup featuring three three-winding transformers for three-phase HVac integration. This arrangement involves connecting the phases in a series configuration to effectively manage the entire dc voltage.

While the above-mentioned research has focused on reducing the number of devices in HB-MMC-based topologies, the fault-handling capability of these configurations remains a significant concern. Conventional HB-SMs-based MMCs are susceptible to both dc short-circuit faults and ac faults. During faults, the MMC may act as a rectifier, causing excessive stress on the devices due to the high magnitude of fault current which may damage the devices. Hence to improve the reliability and robustness of MMC-based systems DCCBs [24] or SMs with fault blocking capabilities [25] or fault current limiter [26] have been used in literature to block the fault current. In contrast, the proposed topology uses HB-SMs and a tuned filter (parallel LC filter) at the MVdc side resulting in a converter configuration that inherently possesses fault-blocking capability.

This article describes an HB-MMC topology that incorporates a mid-point transformer for integrating MVdc with single-phase MVAC for railway traction applications. The proposed topology requires a reduced number of switches and has fault-blocking capability.

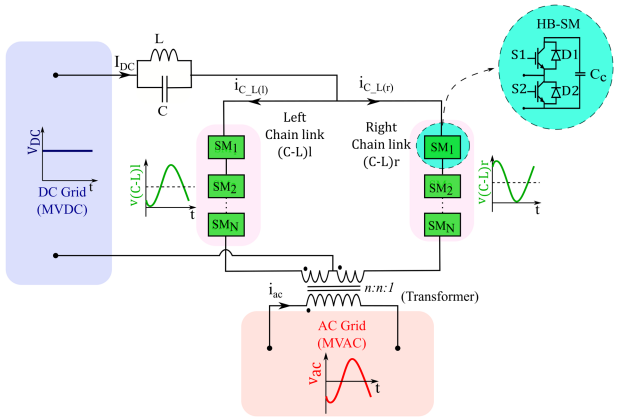

Fig. 1. Proposed topology for integrating MVdc with single-phase MVac for traction application.

The main contributions of this work are as follows.

1) Proposes a modular circuit topology for this MVdc-MVac (single phase) with key features as
   a) Reduced arms or C-Ls.
   b) Galvanically isolated using a mid-point transformer which has dc flux cancellation within the transformer with appropriate modulation technique.
   c) The inductance of the arm inductor can be combined with the leakage inductance of the mid-point transformer, thus eliminating the requirement for extra inductors.
   d) Fault-tolerant operation of the converter is possible.
2) A comprehensive theoretical model describing the operational principles of the proposed converter.
3) Precharging scheme for charging SM capacitor.
4) Evaluation of the converter's performance in various fault scenarios.

II. Topology for the MVDC to Single Phase MVAC Grid Integration

A. Circuit Configuration

Fig. 1 shows the proposed topology, an MVdc voltage (V_{DC}) is interfaced to an MVac single-phase network (V_{ac}) through one-stage conversion and a mid-point transformer of line frequency. The mid-point transformer has two primary windings as shown in Fig. 1 and one secondary winding. The primary windings consist of an identical number of turns and are coiled in a uniform direction around the transformer core. The primary windings are connected to the MVdc grid through two chain links (C-Ls) and a tuned Filter (parallel LC filter) (see Fig. 1). The arm inductance is integrated with the leakage inductance of the mid-point transformer, eliminating the need for extra inductors. Each C-L contains multiple HB-SMs in a cascaded connection. Each HB-SMs contain two IGBTs with antiparallel diodes and a SM capacitor as shown in Fig. 1. This cascaded connection of HB-SMs is responsible for the wave shaping in each C-L thereby

generating the required voltage waveform. A sorting algorithm is employed to regulate and equalize the voltages of all the SM capacitors.

The mid-point of the primary sides of the transformer is connected to the negative terminal of the MVdc while the positive terminal of the MVdc is connected to the C-Ls via the tuned filter. The tuned filter is connected between the MVdc grid and between the C-Ls, so that no fundamental ac components can flow into the MVdc grid.

The converter's attributes that render it suitable for integrating MVdc with single-phase MVac for railway traction systems include modularity, scalability, the inherent fault-blocking capability of the converter, dc flux cancellation, and the complete utilization of the mid-point transformer. The operational concept of the converter is elaborated extensively in Section II-B.

B. Principle of Operation

To achieve the necessary voltage handling capability and facilitate multilevel operation, the converter's C-L is comprised of N series-connected HB-SMs, with each SM's voltage denoted as $V_{\rm cap}$. The C-L acts as a controllable voltage source containing both dc and ac components. The total C-L voltage is the sum of all the SM capacitor voltages within that C-L unit.

To simplify the analysis, the following assumptions are made.

1) The analysis is done in the steady state.
2) The converter is a loss-less system.
3) The switching harmonics are ignored in the C-L due to the multilevel nature of the C-L voltage.

The ac grid voltage and current can be defined as

$$\left.\begin{aligned} v_{\rm ac} &= V_{\rm ac}\sin(\omega t) \\ i_{\rm ac} &= I_{\rm ac}\sin(\omega t+\phi) \end{aligned}\right\}. \tag{1}$$

The ac grid is connected with the converter via a mid-point transformer with a turns ratio as *n:n:1* (n_{py1}:n_{py2}:n_{sy}) where the ac grid is connected with the secondary of the transformer and this mid-point transformer has two primary windings, which are connected with the C-Ls of the converter.

Applying KVL in each converter's C-L, the C-L voltage can be expressed as

$$\left.\begin{aligned} v_{C-L(r)} &= V_{\rm DC} - nV_{\rm ac}\sin(\omega t) \\ v_{C-L(l)} &= V_{\rm DC} + nV_{\rm ac}\sin(\omega t) \end{aligned}\right\}. \tag{2}$$

The C-Ls of the converter act as a controllable voltage source and it is modulated in such a way that the C-Ls have the same magnitude but are out of phase with each other. These C-Ls modulated signals are represented as

$$\left.\begin{aligned} v_{C-L(r)} &= V_{\rm DC}(1-m\sin(\omega t)) \\ v_{C-L(l)} &= V_{\rm DC}(1+m\sin(\omega t)) \end{aligned}\right\} \tag{3}$$

where *m* is the modulation index of the converter, which varies from 0 to 1. Putting (3) into (2), the relation between MVdc voltage and MVac voltage can be found as

$$V_{\rm ac} = \frac{mV_{\rm DC}}{n}. \tag{4}$$

Putting $m = 1$

$$V_{\rm ac} = \frac{V_{\rm DC}}{n}. \tag{5}$$

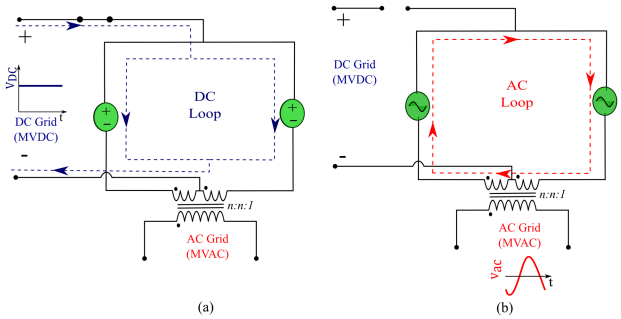

Fig. 2. (a) DC and (b) AC equivalent circuit shown in Fig. 1.

Substituting (5) in (2), it can be said that the C-L voltage varies from 0 to $2V_{\rm DC}$. Further, it can be said that the C-L voltages are unipolar in nature. Hence, HB-SMs can be employed only.

From the dc equivalent circuit shown in Fig. 2(a), it is observed that the dc component of current flows through the converter via parallel LC filter and the C-Ls and returns via the mid-point of the primary winding of the transformer. The dc current splits in the C-Ls equally. These currents enter at the primary winding of the transformers with opposite sides as shown in Fig. 2(a). Hence no dc flux is induced in the core of the transformer. The dc flux cancellation is explained in Section II-D.

Fig. 2(b) shows the ac equivalent circuit of the converter. The parallel LC filter is tuned at fundamental frequency; hence opposes any ac components flowing into the MVdc grid. The relation between the ac components of C-L currents and the MVac grid side currents is expressed as

$$i_{\rm ac} = n\big(i_{C-L(r)} - i_{C-L(l)}\big)_{\rm AC\_component}. \tag{6}$$

As seen from the dc equivalent circuit, the dc current divides equally in the C-Ls, and from the ac equivalent circuit, the ac current flows within the C-Ls. The C-L currents can be expressed as

$$\left.\begin{aligned} i_{C-L(r)} &= \tfrac{I_{\rm DC}}{2} + \tfrac{i_{\rm ac}}{n} \\ i_{C-L(l)} &= \tfrac{I_{\rm DC}}{2} - \tfrac{i_{\rm ac}}{n} \end{aligned}\right\}. \tag{7}$$

Therefore, each C-L must be rated for the full peak magnitude of ac current plus half the dc current which is expressed as

$$I_{C-L(\rm rating)} = \frac{I_{\rm DC}}{2} + \frac{I_{\rm ac}}{n}. \tag{8}$$

If the C-L currents are not equal in magnitude, then some ac component may flow into the MVdc side, which is limited due to the presence of the tune parallel LC filter. Generally, the transformer is over-designed to prevent any saturation due to the dc current if complete dc flux cancellation does not take place completely. This dc flux cancellation in the mid-point transformer of the proposed converter is explained in Section II-D.

C. C-L Energy Balancing

In a steady state, the power contributed by each C-L must be zero. The instantaneous C-L power can be represented as P_{C-L}

$$P_{C-L} = V_{\rm DC}(1-m\sin(\omega t)) \times \left(\frac{I_{\rm DC}}{2} + \frac{i_{\rm ac}}{n}\right). \tag{9}$$

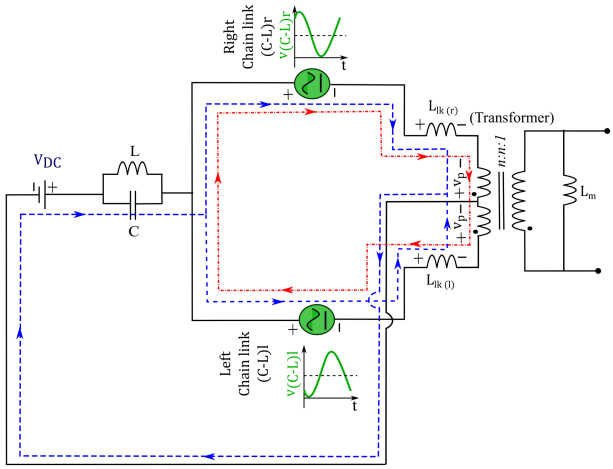

Fig. 3. Equivalent circuit diagram to explain the DC flux cancellation in the primary side of the transformer.

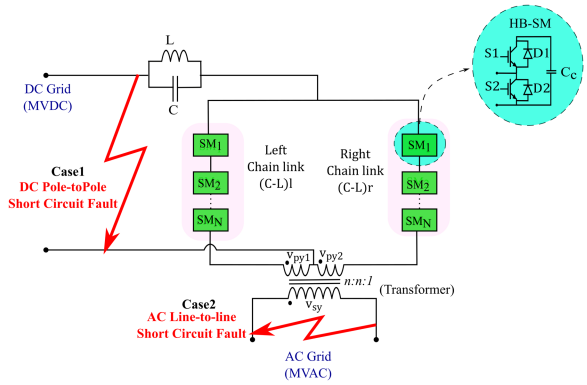

Fig. 4. DC pole-to-pole short circuit fault and AC line-to-line short circuit fault cases in proposed topology.

Simplifying and separating both dc and ac components of C-L power

$$P_{(C-L)\mathrm{DC}} = V_{\mathrm{DC}}\,\frac{I_{\mathrm{DC}}}{2} - mV_{\mathrm{DC}}\frac{I_{\mathrm{ac}}}{2n}\cos(\phi) \tag{10}$$

$$P_{(C-L)\mathrm{ac}} = -V_{\mathrm{DC}}\,\frac{I_{\mathrm{DC}}}{2}m\sin(\omega t) + V_{\mathrm{DC}}\frac{I_{\mathrm{ac}}}{n}\sin(\omega t+\phi) + mV_{\mathrm{DC}}\frac{I_{\mathrm{ac}}}{2n}\cos(2\omega t+\phi). \tag{11}$$

For steady state power balance, the $P_{(C-L)\mathrm{DC}}$ must be equated to zero and the I_{DC} can be determined in terms of the I_{ac} as

$$I_{\mathrm{DC}} = \frac{mI_{\mathrm{ac}}}{n}\cos(\phi). \tag{12}$$

A similar expression can be obtained by equating the input and output power of the converter

$$V_{\mathrm{DC}}\,I_{\mathrm{DC}} = V_{\mathrm{ac}}\,I_{\mathrm{ac}}\cos(\phi) = \frac{mV_{\mathrm{DC}}}{n}I_{\mathrm{ac}}\cos(\phi) \tag{13}$$

$$I_{\mathrm{DC}} = \frac{mI_{\mathrm{ac}}}{n}\cos(\phi).$$

The ac component of the C-L is used to transfer the power from the converter to the single-phase MVac traction power supply, meanwhile dc component in the C-L helps establish the energy balance and recover energy from the MVdc.

D. DC Flux Cancellation

In this section, the dc flux cancellation concept is explained with an equivalent circuit model. From the equivalent model, the voltage across each primary winding is found using KVL. Assumption: drop across the filter, and transformer are neglected.

Applying KVL (see Fig. 3)

$$v_{py(l)} = v_{Lk(l)} + v_p \tag{14}$$

$$v_{py(r)} = v_{Lk(r)} - v_p \tag{15}$$

$$v_{py(l)} = v_{\mathrm{DC}} - v_{cl(l)} \tag{16}$$

$$v_{py(r)} = v_{\mathrm{DC}} - v_{cl(r)}. \tag{17}$$

Addition of (14) and (15) gives

$$v_{py(l)} + v_{py(r)} = v_{Lk(l)} + v_{LK(r)}. \tag{18}$$

Therefore, it is only the common mode voltage of $v_{py(l)}$ and $v_{py(r)}$ that appears across the leakage inductance

$$v_{Lk(l)} + v_{LK(r)} = 2V_{\mathrm{DC}} - v_{cl(l)} - v_{cl(r)}.$$

In an ideal transformer

$$v_{Lk(l)} = v_{LK(r)} = \frac{1}{2}\left(2V_{\mathrm{DC}} - v_{cl(l)} - v_{cl(r)}\right). \tag{19}$$

Similarly, an expression for the voltage across the magnetizing branch of the transformer referred to the primary side is obtained by subtracting (14) and (15)

$$v_{py(l)} - v_{py(r)} = v_p + v_p$$

$$v_p = \frac{1}{2}(V_{\mathrm{DC}} - v_{cl(l)} + v_{cl(r)} - V_{\mathrm{DC}}) = mV_{\mathrm{DC}}\sin(\omega t). \tag{20}$$

It is only the differential mode voltage of $v_{py(l)}$ and $v_{py(r)}$ appearing across the transformer's magnetizing branch. Since the two primary windings are wound in the same direction around the transformer core and the proposed topology's C-L are connected opposite to the dot polarity (see Fig. 3) of the transformer winding, the common mode current does not induce any dc flux in the transformer core.

E. DC and AC Short-Circuit Fault Analysis

Conventional HB-MMCs are vulnerable to short-circuit faults such as dc pole-to-pole and ac line-to-line faults. In the event of a short circuit fault, the HB-MMC behaves as an uncontrolled rectifier, leading to high fault currents flowing through the MMC arm [24], [25], [26], potentially causing damage to the devices within it. To safeguard the converter from such faults, measures such as DCCBs [24], fault-tolerant SMs such as FB-SMs, diode clamp SMs, and fault current limiting devices [25], [26] are employed. However, these devices result in additional conduction losses during normal operation and escalate the overall system cost.

The topology proposed in this article has inherent fault-blocking capability using HB-SMs due to its topological structure. Different short-circuit faults are applied in the proposed

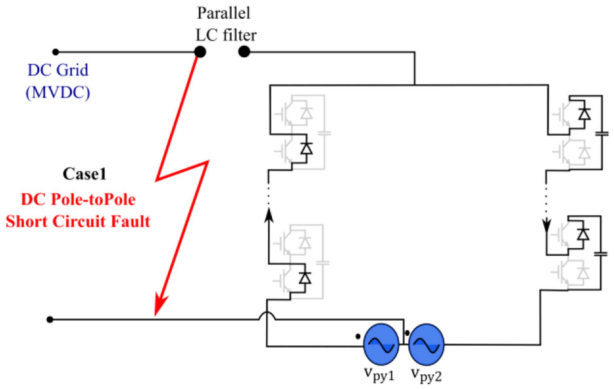

Fig. 5. Equivalent circuit diagram of the proposed converter during DC pole-to-pole fault.

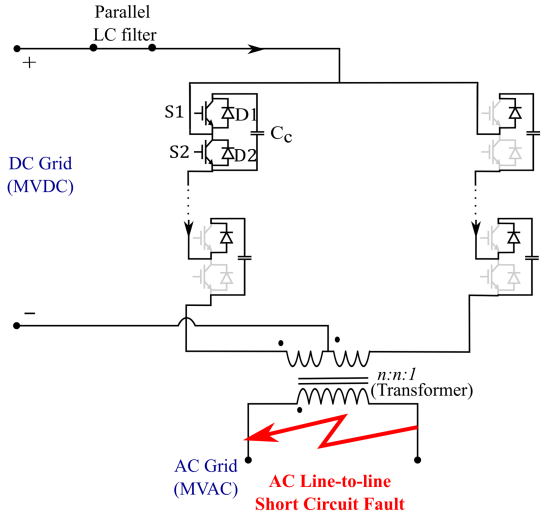

Fig. 6. Equivalent circuit diagram of the proposed converter during AC line-to-line fault.

converter (shown in Fig. 4) to verify and explain its fault-blocking capability. The sequence of events during these short-circuit faults is also listed as follows.

1) DC pole-to-pole fault at the MVdc side: In the event of a dc pole-to-pole fault at the MVdc side, all the IGBTs are blocked. The equivalent circuit during this dc fault is shown in Fig. 5. The parallel LC filter blocks the ac current flowing into the fault location. For simplicity, we can assume the primary windings of the transformer to be two ac sources as shown in Fig. 5. After blocking of the IGBTs, the possible current path is from the lower antiparallel diode (D2) of the left chain link's SMs and upper antiparallel diode (D1) and SM capacitor (Cc) of right chain link's SMs.

At this instant, the equivalent SMs capacitor voltage is twice V_{DC}, which is higher than the primary winding voltage [according to (2) and (5)]. Hence the diode D2 of right C-L and diode D1 of left C-L become reversed biased. So, no current will flow within the C-L's of the converter and hence the converter is protected. This also explains the inherent dc fault-blocking capability feature of the converter.

2) AC line-to-line fault at the MVac side: Similarly, in the event of ac line-to-line fault, the converter is blocked by removing the gating pulses of IGBTs. The parallel LC filter acts as a short circuit for dc components. The equivalent circuit during this ac line-to-line fault is shown in Fig. 6. The possible current path is from MVdc side to the fault location through the upper antiparallel diode D1 and Cc of both the C-L's SMs (see Fig. 6). However, the equivalent SM capacitor voltage of C-Ls is $2V_{\mathrm{DC}}$, higher than the V_{DC} voltage. Due to this, D1 gets reversed biased, and no current will flow through the converter's C-L. Hence the converter is protected from ac line-to-line short circuit fault.

F. Precharging of SM Capacitors in the Proposed Converter

Precharging the capacitors of MMC SMs is an essential task that must be completed before initiating the converter [27]. During the start-up process of the MMC, prior to transitioning to normal operation, it is crucial that all SM capacitors are charged equally to a specific value (nominal voltage, i.e., V_{sm}). Failure to do so may result in damage to the devices within the MMC due to the high inrush current at that moment [27]. Hence, a suitable precharging method is necessary.

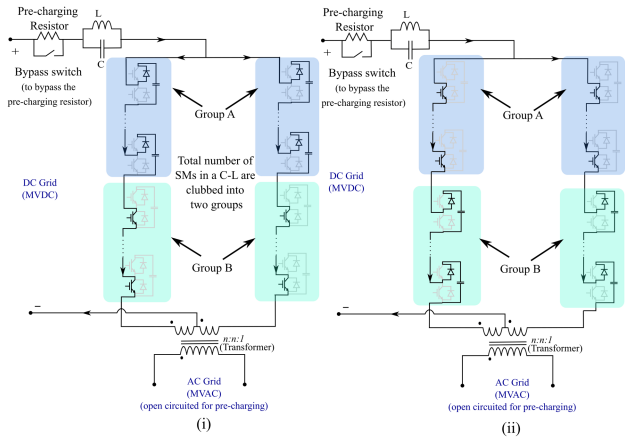

Fig. 7. Precharging of the proposed converter.

For the proposed topology, a precharging control scheme is proposed. In the proposed converter, the equivalent SM capacitor voltage of a C-L is $2V_{\mathrm{DC}}$ which is twice the MVdc voltage [according to (2) and (5)]. So, if the converter is charged from the dc side with precharging resistor using an uncontrolled method, the equivalent SM capacitor voltage of a C-L will become V_{DC}. Further, at that instant, if the converter is switched to normal operation, then a high inrush current will flow, which may threaten the safe operation of the IGBTs and capacitors. (Note that the precharging resistor is bypassed during normal operation of the converter.)

The proposed precharging methodology is a controlled precharging technique with a precharging resistor and a parallel bypass switch. This approach ensures a controlled and gradual increase in voltage across the system components during the precharging phase. In this scheme, the SM's IGBTs are turned ON and OFF to get the equivalent SM capacitor of a C-L to 2 V_{DC} and the precharging resistor is used to limit high in-rush current. Fig. 7 shows the precharging process of the proposed converter. The below steps explain the controlled precharging technique and how to charge the equivalent SMs capacitor voltage of a C-L

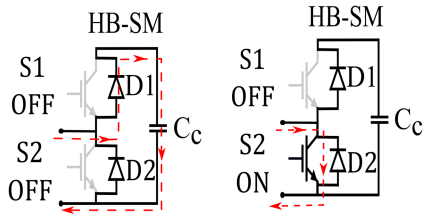

Fig. 8. Equivalent circuit of HB-SM during SM capacitor charging and SM capacitor bypass stage.

to $2V_{\mathrm{DC}}$. Sequential steps followed in the proposed precharging method.

1) The total number of SMs in a C-Ls are clubbed equally into two groups (Group A and Group B) as shown in Fig. 7. Suppose N SMs are there in a C-L, then $N/2$ SMs form group A and other $N/2$ SMs forms group B.
2) At the initial stage the ac circuit breakers are kept open. Therefore, the current can flow from MVdc side via precharging resistor and the CLs and return through the negative terminal of MVdc grid.

The charging of the SM capacitor is possible when both the IGBTs are blocked (i.e., S1 and S2 are OFF) and the dc current flowing through the C-L is positive, which is generally called the charging stage. In the bypass stage, S1 is OFF and S2 is ON, which bypasses the SM capacitor charging (see Fig. 8).

3) A high-frequency square wave PWM technique (with 50% duty) is given to SM's S2 switch of Group A and Group B in a complementary fashion (i.e., if S2 of group B is ON, then at that instant S2 of Group A is OFF) as shown in Fig. 7(i).
4) During one-half cycle of the PWM switching frequency, $N/2$ SMs with charge to V_{DC}. Similarly, during the next half cycle, other $N/2$ SMs get charged to V_{DC}.
5) Hence the equivalent SM capacitor voltage of a C-L is $2V_{\mathrm{DC}}$. At this instant precharging of the SMs gets completed and the converter can be switched to normal operation by bypassing the precharging resistor using a circuit breaker at the MVdc side.

G. Control Logic Diagram

The complete controller structure is shown in Fig. 9. The schematic includes the power loop (to send controlled power), phase locked loop (PLL) synchronization, modulation technique (LS-PWM), algorithm for capacitor balancing [28], circulating current control [29] and short-circuit fault protection logic. A sorting algorithm [28] is employed to equalize the voltages of SM capacitors. Based on the sensed capacitor voltages and C-L current direction, the sorting logic determines whichever SM must be turned ON or OFF and who should receive the gate signals. The generated reference ac voltage signal at the output of the current control loop is added (or subtracted for other C-L) with dc voltage to generate the required reference signals for the two C-Ls, which are passed through the LS-PWM technique and sorting algorithm, which finally is used for the gating pulses of the two C-L's SMs. The output of the fault logic block is passed through the enable block along with the gating signals (see Fig. 9) and is used to protect the converter from a short-circuit fault. The enable block in Fig. 9 represents a protection logic block (AND Gate) that blocks or allows the gating pulses during normal or fault operation according to the $\mathrm{Fault}_{\mathrm{out}}$ value. If $\mathrm{Fault}_{\mathrm{out}}$ is 0 (which means fault case in the converter), then gating pulses to the IGBTs are blocked. Otherwise, if $\mathrm{Fault}_{\mathrm{out}}$ is 1, then gating pulses are allowed. The circulating component of the 2nd harmonics in the C-L loop is controlled by using a circulating current controller (see Fig. 9), which is shown below. The generated circulating current loop (i_z) is forced to follow the command of the circulating current reference ($i_{\mathrm{dq2\,(ref)}}$), producing the voltage command, which is added to the modulating voltage waveform.

III. Comparison With Other Topologies

In this section, the proposed topology is compared with different solutions to show the advantages and limitations of the proposed topology. This comparison is presented in Table I. For this comparison, the MVdc side voltage (V_{dc}), and each SM voltage rating (V_{dc}/n) are assumed constants for all the topologies. Furthermore, the MVac voltage (V_{ac}) is assumed to be constant and the peak magnitude of the MVac voltage is the same as V_{dc}.

A detailed explanation of the proposed topology is highlighted in terms of switch count, efficiency, and other parameters.

1) *C-L voltage:* The proposed topology has twice the arm voltage magnitude compared to conventional MMC. Hence twice the number of SM required per arm/C-L compared to conventional. Due to this, the ac output voltage is at a higher level than conventional HB-MMC. As only two arm/C-L arm present in the proposed converter, therefore the total number of SMs and switch counts are $4n$ and $8n$ respectively. Thus, the level formed at the ac side of the converter is $4n+1$, which represents the voltage impressed at the transformer's primary is highly sinusoidal, whereas the levels formed at the transformer's primary side by conventional HB-MMC is $2n+1$.
2) *Elimination of arm inductor:* The required C-L/ arm inductance is combined with the leakage inductance of the mid-point transformer, thus eliminating the requirement of extra inductors, which is not possible in conventional MMC.
3) *Fault-tolerant feature:* The proposed topology can protect its devices from ac and dc short-circuit faults, which are not possible in conventional HB-MMC.
4) *C-L current:* In the proposed topology, the C-L current is $I_{\mathrm{dc}}/2 + I_{\mathrm{ac}}$, which is the same as the conventional MMC is the peak magnitude of ac voltage is V_{dc}. Hence, the turn ratio of the mid-point transformer is 0.5:0.5:1 whereas the turns ratio of conventional MMC is 1:2. However, in two C-L based MMCs, there is a chance of saturation of the transformer because both ac and dc current flows through the transformer [30].

Hence from the above-mentioned comparison, it can be said that the proposed converter has many advantages like reduced C-Ls, no requirements for extra C-L inductors and inherent fault-tolerant capability. It can also the observed that the ac output voltage produced by the proposed converter has higher voltage magnitude and higher levels; twice that of conventional

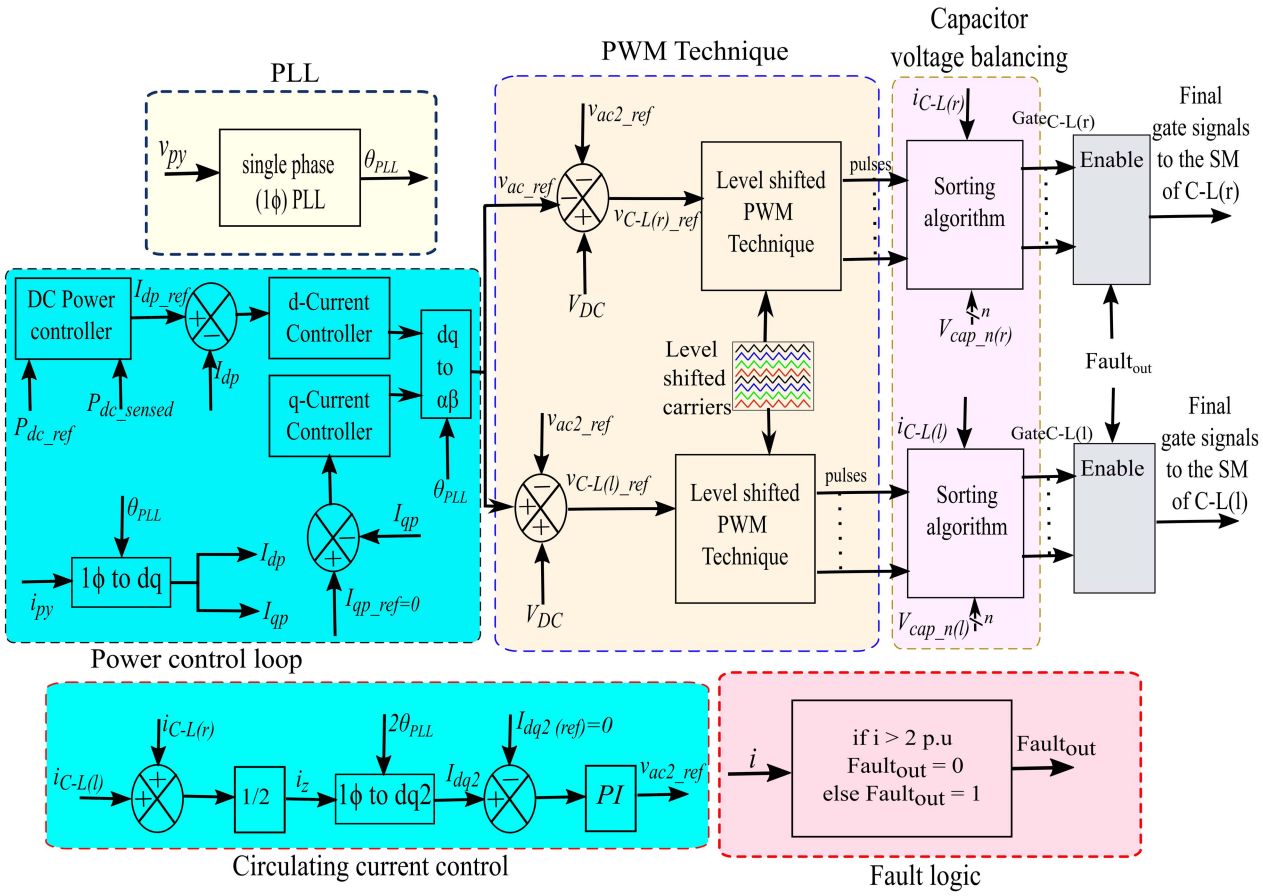

Fig. 9. Overall controller structure.

TABLE I
COMPARISON OF PROPOSED TOPOLOGY WITH STATE-OF-THE-ART METHODOLOGIES

Sl. No.	Parameters	Conventional HB-MMC [11],[31],[32]	Two arm HB-MMC [16],[33]	Proposed Topology
1.	MVDC side voltage	V_{dc}	V_{dc}	V_{dc}
2.	SM voltage rating	V_{dc}/n	V_{dc}/n	V_{dc}/n
3.	Total number of SM in the converter	$4n$	$2n$	$4n$
4.	Total number of IGBTs	$8n$	$4n$	$8n$
5.	Number of transformer	1	1	1 (mid-point transformer)
6.	Number of arm inductor	4	2	-
7.	Additional Filter	-	2	1
8.	Number of levels across primary winding of transformer	$2n+1$	$2n+1$	$4n+1$
9.	AC output of the converter	$V_{dc}/2$	$V_{dc}/2$	V_{dc}
10.	AC and DC fault tolerant	No	No	Yes
11.	Turns ratio (np:ns)	1:2	1:2	0.5:0.5:1
12.	SM current rating	$I_{dc}/2 + I_{ac}$	$I_{dc} + I_{ac}$	$I_{dc}/2 + I_{ac}$

n is the number of SM per arm in conventional MMC.

HB-MMC. However, the proposed topology requires a special kind of transformer with mid-point tapping.

IV. RESULTS

The validity of the converter is confirmed through both MATLAB Simulink simulations and testing with a scaled-down experimental prototype. The detailed parameters of the proposed converter are given in Table II.

The SM of the proposed experimental prototype (see Fig. 17) is designed using intelligent power module (as SM switch), electrolytic capacitors (as SM capacitor), and their corresponding control circuitry. The proposed topology is controlled by employing a combination of TI-DSP development board alongside Altera FPGA board. The simulation results are shown in Figs. 10–16 and the experimental results are shown in Figs. 18–21.

TABLE II
CONVERTER PARAMETERS

Parameter	Simulation	Experimental
Rated Power	30 MW	1.5 kW
MVDC voltage	$35kV$	300 V
Fundamental AC frequency	50 Hz	50Hz
Mid-point transformer turns ratio	1:1:1.2	1:1:2
SMs per C-L	20	4
SM capacitor	20 mF	7.5 mF
Parallel filter inductor	20 mH	10 mH
Parallel filter capacitor	0.5 mF	1 mF
Modulation index	0.95	0.85

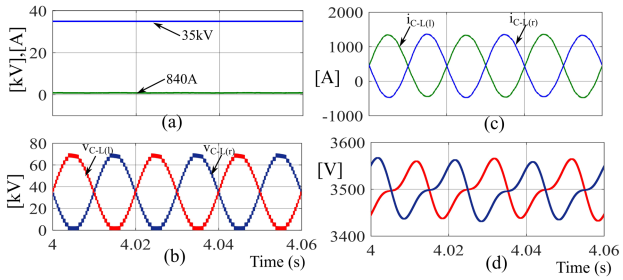

Fig. 10. Simulation result of converter during steady state. (a) MVdc voltage and currents. (b) Voltage across the C-Ls. (c) Current flowing through the C-Ls. (d) SM capacitor voltages of the C-Ls.

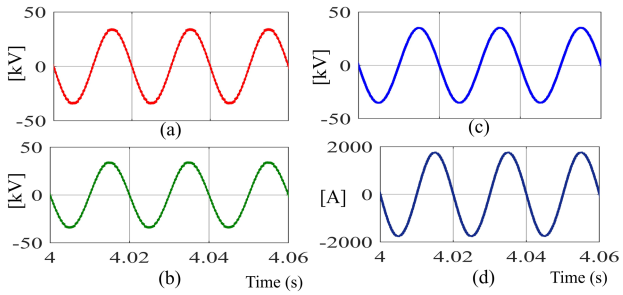

Fig. 11. Simulation result of the converter during steady state. (a) Voltage across primary winding 1. (b) Voltage across primary winding 2. (c) Voltage across secondary winding. (d) Current flowing at the secondary side of the transformer.

The proposed converter converting MVdc to single-phase MVac for rail traction power supply is connected to an MVdc grid of 35kV and has a power of around 30 MW [see Fig. 10(a)]. The voltages across the C-L and current flowing through it are shown in Fig. 10(b) and (c), respectively. The C-L voltages and currents contain both dc and ac in it and one of the C-L's voltage and current are 180° out of phase [according to (3)] w.r.t other C-L's voltage and current. The C-L voltages contain 21 levels as 20 SMs are used in each C-L. The voltage across SM capacitors is balanced at 3.5 kV using a sorting algorithm [see Fig. 10(d)].

From Fig. 11(a) and (b), it is observed that the voltages across the transformer's primary windings are perfectly sinusoidal in nature and have a peak magnitude of nearly 35 kV according to (16). The secondary side voltages and currents are shown in Fig. 11(c) and (d) respectively. The converter converts MVdc to 25 kV single-phase ac for railway traction application according to (4).

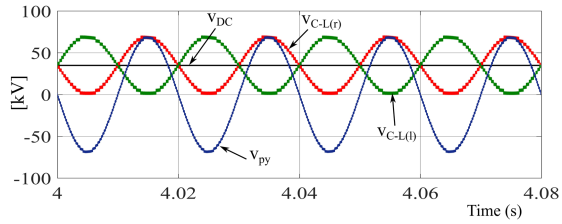

Fig. 12. DC flux cancellation in the primary side of the transformer ($v_{py} = v_{py1} + v_{py2}$).

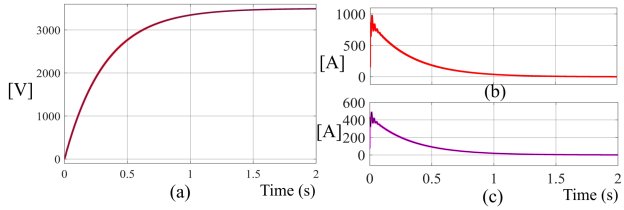

Fig. 13. Precharging in the proposed converter. (a) SM capacitor voltages. (b) MVdc side charging current. (c) Precharging currents flowing through the C-Ls.

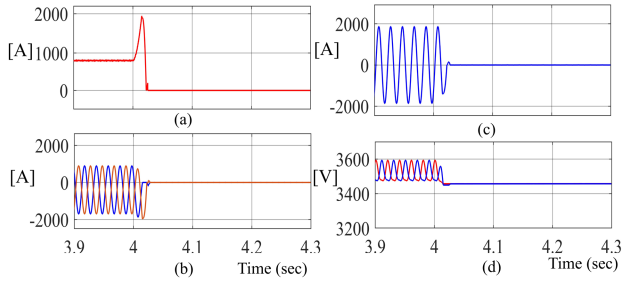

Fig. 14. Performance of the converter during pole-to-pole short circuit fault at the MVdc side. (a) MVdc side current. (b) Left C-L current and right C-L current. (c) Secondary side current. (d) SM capacitor voltages.

From Fig. 12, it is observed that even though the C-L voltages contain both dc and ac in it but the voltage across the primary winding (v_{py}) is perfectly sinusoidal in nature [according to (16)]. Further, due to the topological configuration, the modulation technique of the C-Ls, the primary side voltage is perfectly ac, and the arm currents do not induce any dc flux in the transformer core.

Fig. 13 shows the precharging of the SMs in the converter. It is observed that the SM capacitor of the converter is charged to the required SM capacitor voltage [according to (18)] with the proposed precharging scheme. The precharging currents flowing through the C-Ls are within the switch current rating.

In the event of pole-to-pole MVdc side fault, the SMs are blocked by removing the gating pulses after the fault is detected. The parallel LC filter blocks the ac current flowing into the fault location from the ac side (as it provides high impedance at tuned frequency). Further, it is observed that all current quickly become zero [see Fig. 14(a)–(c)] as the antiparallel diodes get reversed biased as the equivalent SM voltage of each C-L is twice the peak MVAC voltage (as described in Section II-E). After the blocking of the SMs, the capacitor voltages become constant as shown in Fig. 14(d).

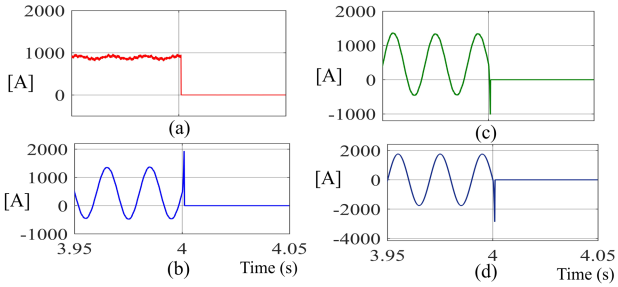

Fig. 15. Performance of the converter during MVAC line-to-line fault. (a) MVdc side current. (b) Left C-L current. (c) Right C-L current. (d) Secondary side current.

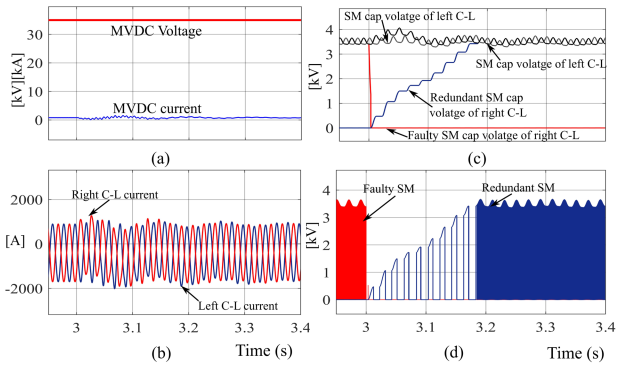

Fig. 16. Transient condition (SM fault in one of the C-L). (a) MVdc voltage and MVdc current. (b) Right and left C-L current. (c) Capacitor voltages of the C-Ls. (d) Voltage across faulty and redundant SM.

Suppose a line-to-line fault happens at the MVac side (secondary side of the transformer). After detection of the fault, all the SM's IGBTs are blocked. All the currents become zero (see Fig. 15) as the equivalent SM capacitor voltage of the C-L is twice the MVdc side voltage; hence all the upper antiparallel diodes of the SM get reversed biased as explained in Section II-E.

DC flux cancellation also happens during transient conditions. This is explained through a momentary transient condition i.e., SM fault in one of the C-L. Suppose the SM fault happens at $t = 3$ s. The faulty SM is bypassed using bypass switch and a redundant SM is substituted for the faulty one. As the faulty SM is bypassed, the power contributed by that SM becomes zero, which causes power unbalance between both the C-Ls that can be observed in Fig. 16(b).

It is observed that the C-L currents are not equal. A redundant SM is inserted during a point to make both the C-L power equal. However, at that instant, the redundant SM voltage charges from 0 V to V_{SM} voltage (3.5 kV) as shown in Fig. 4(c). The SM capacitor voltage of all the SM of both the C-L and the redundant SM are shown in Fig. 16(c). Fig. 16(d) shows the output voltage of faulty SM and redundant SM before and after the fault. As one of the SM capacitor voltages in the right C-L becomes zero, other capacitor voltages of that C-L increase, trying to keep the currents in both C-L same. During this complete time interval, there will be unequal C-L currents till the redundant SM capacitor voltage becomes 3.5 kV. After that the power in both the C-L becomes equal and the stable operation of the converter continues. It seems that the converter can operate in one of the worst transient states without its transformer getting saturated.

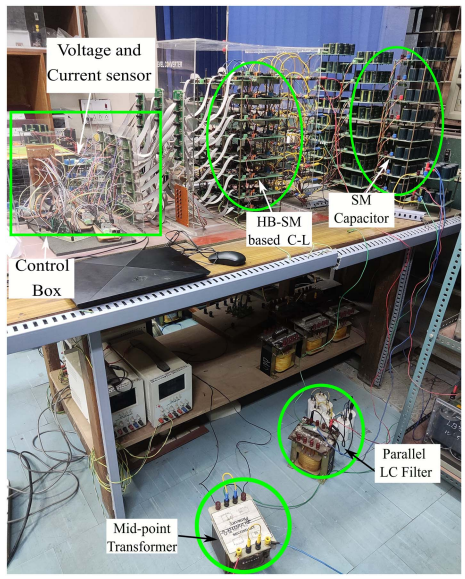

Fig. 17. Scaled-down laboratory prototype.

The experimental results of the scaled-down laboratory prototype (see Fig. 17) are shown in Figs. 18–20. The dc side voltage and C-L voltages are shown in Fig. 18(i). It is observed that the C-L voltages have five levels as four SMs are used in each C-L. Further, both dc and ac components are present in C-L voltage and have a peak magnitude of nearly 600 V according to (3). Fig. 18(ii) shows the voltage across each of the primary windings of the transformer and total voltage across the primary winding. The voltage across the primary winding is perfectly ac with nine levels in it [according to (20)] and each primary winding voltage has a peak magnitude of nearly 300 V. The dc side current, C-L currents, and transformer's secondary side current is shown in Fig. 18(iii). It has been noticed that the current in the C-L circuit comprises both dc and ac components [according to (7)]. The secondary side current is perfectly sinusoidal in nature according to (1) and has a peak magnitude of 4 A [according to (13)]. All the SM capacitor voltages are perfectly balanced in both the C-Ls at 150 V [see Fig. 18(iv) and (v)], which signifies that the sorting algorithm is working properly. The precharging of the SM capacitor is done from the dc side using the proposed precharging scheme as explained in Section II-F [see Fig. 18(vi)].

The dc flux cancellation in the transformer's primary winding in the proposed converter is also verified in a scaled-down laboratory prototype through experimental results shown in Fig. 19. In Fig. 19(i), it is observed that even though the chain link voltages contain both dc and ac in it but the total voltage across the primary winding of the transformer is perfectly sinusoidal in nature according to (20). Also, from Fig. 19(ii) i.e., the B-H curve of the transformer, it is observed that the transformer is operating in linear region, and it does not saturate.

The experimental results during ac and dc fault conditions in the converter are shown in Fig. 20(i) and (ii), respectively. In the event of fault, the gating pulses to the SMs are blocked. All the currents become zero [see Fig. 20(i)] as the equivalent SM capacitor voltage of the C-L is twice the dc side voltage; hence all the upper antiparallel diode of the SM get reversed

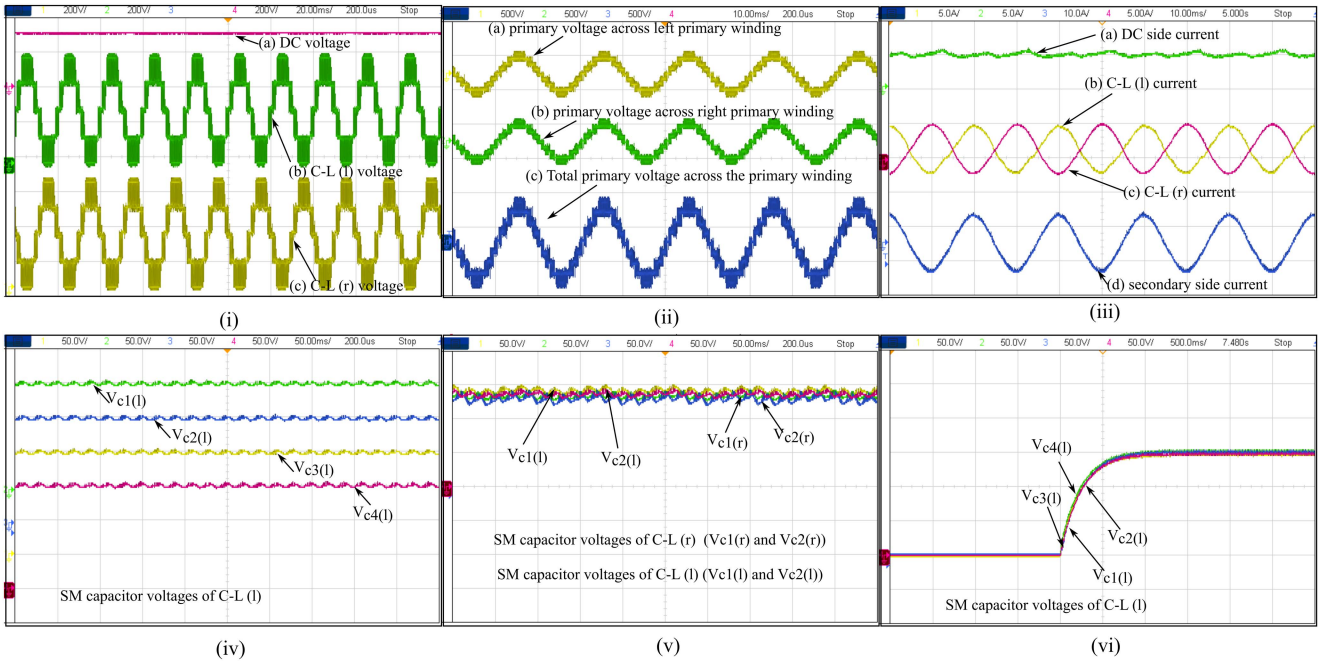

Fig. 18. Experimental results of the proposed converter. (i) (a) DC voltage. (b) Voltage across C-L(l). (c) Voltage across C-L(r). (ii) (a) voltage across left primary winding. (b) Voltage across right primary winding. (c) Total voltage across the primary winding of the transformer. (iii) (a) DC side current. (b) Current flowing through the C-L(l). (c) Current flowing through the C-L (r). (d) Secondary side current of the transformer. (iv) All the SM capacitor voltages of C-L(l). (v) Vc1(l) and Vc2(l) Upper two SM capacitor voltage of C-L(l), and Vc1(r) and Vc2(r) Upper two SM capacitor voltage of C-L(r). (vi) Precharging of SM capacitor voltages.

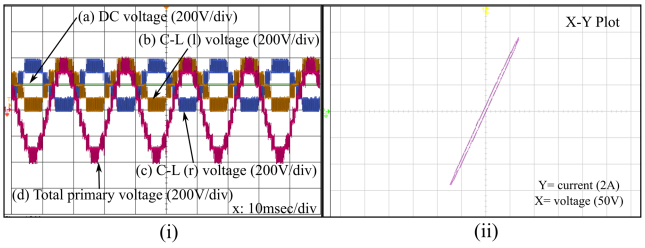

Fig. 19. Experimental results of the proposed converter showing dc flux cancellation. (i) (a) DC voltage. (b) C-L (l) voltage. (c) C-L(r) voltage. (d) Total voltage across the primary winding of the transformer. (ii) B-H curve of the transformer.

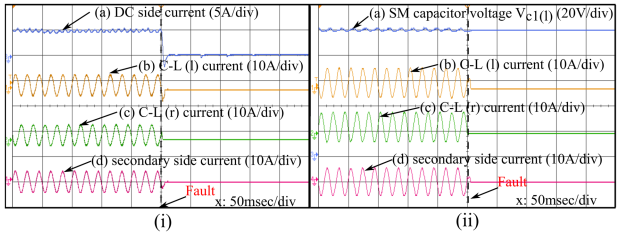

Fig. 20. Experimental results during fault conditions. (i) AC side fault. (a) DC side current. (b) C-L (l) current. (c) C-L(r) current. (d) Secondary side current. (ii) DC side fault. (a) SM capacitor voltage of C-L(l). (b) C-L (l) current. (c) C-L(r) current. (d) Secondary side current.

biased as explained in Section II-E. Similarly, in case of dc fault, the parallel LC filter blocks any ac current flowing into the fault location and the equivalent SMs capacitor voltage of the C-L is twice V_{DC}, which is higher than each of the primary winding voltage of the transformer [see Fig. 20(ii)]. Hence, the diode D2 of right C-L and diode D1 of left C-L become

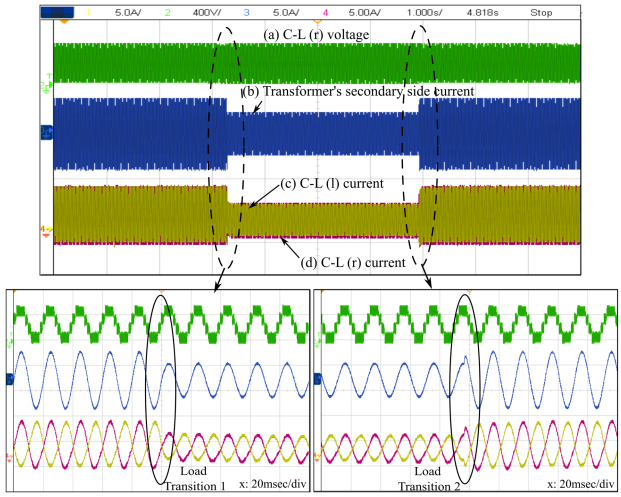

Fig. 21. Experimental results during load transition. (a) C-L(r) voltage. (b) secondary side current. (c) C-L (l) current. (d) C-L(r) current.

reversed biased. So, no current will flow within the C-Ls of the converter and hence the converter is protected. After the SM is blocked, the SM capacitor voltages become constant [see Fig. 20(ii)(a)].

In Fig. 21, the dynamic performance of the converter is shown wherein the first transition, a load change is applied from 1 to 0.6 p.u. It is observed that the C-L voltage remains constant even after the load transition whereas the transformer's secondary side current and both the C-L's current decrease by 40% (see Fig. 21). In the second transition, a load change is applied from 0.6 to 1 p.u. and it is observed that the C-L voltage remains constant throughout the load transition whereas the

transformer's secondary side current and both the C-L's current changes accordingly (see Fig. 21).

V. Conclusion

In this article, a single-phase HB-MMC topology with reduced arms/chain-links (equivalent to 2 arms of conventional HB-MMC) and a mid-point transformer is introduced. This configuration presents a promising solution for integrating MVdc grid with single-phase MVac grid for railway traction applications. A comprehensive analysis of the converter's operation during steady-state, precharging, and fault conditions has been elaborated. The arm inductance present in the conventional HB-MMC can be integrated with the leakage inductance of the mid-point transformer of the proposed converter, eliminating the requirement for extra inductors. The proposed converter preserves the advantages of conventional HB-MMC modularity and scalability, while also incorporating additional features such as inherent fault-blocking capability. Moreover, in the proposed converter, dc flux cancellation is accomplished within the transformer's primary side through a suitable modulation scheme and topological configuration. This article also includes precharging of the proposed converter, which is different from conventional HB-MMC. The validity and effectiveness of the proposed converter have been confirmed through the MATLAB-Simulink platform and scaled-down laboratory prototype results.

References

[1] S. Coffey, V. Timmers, R. Li, G. Wu, and A. Egea-Àlvarez, "Review of MVDC applications, technologies, and future prospects," *Energies*, vol. 14, no. 24, 2021, Art. no. 8294.

[2] P. Simiyu and I. E. Davidson, "MVDC railway traction power systems; state-of-the art, opportunities, and challenges," *Energies*, vol. 14, no. 14, 2021, Art. no. 4156.

[3] J. K. Steinke, P. Maibach, G. Ortiz, F. Canales, and P. Steimer, "MVDC Applications and Technology," in *Proc. PCIM Europe 2019; Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, 2019, pp. 1–8.

[4] L. Camurca, M. Langwasser, R. Zhu, and M. Liserre, "Future MVDC applications using modular multilevel converter," in *Proc. 6th IEEE Int. Energy Conf.*, 2020, pp. 1024–1029.

[5] CIGRE, "Medium voltage direct current grid feasibility study," in WG C6.31 Technical Brochure 793, France 2020.

[6] X. He, J. Peng, P. Han, Z. Liu, S. Gao, and P. Wang, "A novel advanced traction power supply system based on modular multilevel converter," *IEEE Access*, vol. 7, pp. 165018–165028, 2019.

[7] X. Li, C. Zhu, and Y. Liu, "Traction power supply system of China high-speed railway under low-carbon target: Form evolution and operation control," *Electric Power Syst. Res.*, vol. 223, 2023, Art. no. 109682.

[8] A. Verdicchio, P. Ladoux, H. Caron, and C. Courtois, "New medium-voltage DC railway electrification system," *IEEE Trans. Transp. Electrific.*, vol. 4, no. 2, pp. 591–604, Jun. 2018.

[9] L. Liu, N. Dai, K. W. Lao, and W. Hua, "A Co-phase traction power supply system based on asymmetric three-leg hybrid power quality conditioner," *IEEE Trans. Veh. Technol.*, vol. 69, no. 12, pp. 14645–14656, Dec. 2020.

[10] S. M. Mousavi Gazafrudi, A. Tabakhpour Langerudy, E. F. Fuchs, and K. Al-Haddad, "Power quality issues in railway electrification: A comprehensive perspective," *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 3081–3090, May 2015.

[11] P. Li et al., "Impedance modeling and mechanism analysis of low-frequency oscillations in single-phase MMC-RPC integrated vehicle-grid coupling system," *IEEE Trans. Power Electron.*, vol. 38, no. 4, pp. 4820–4839, Apr. 2023.

[12] P. Guo, Z. Tian, Z. Yuan, X.-Y. Zhang, and D. Sharifi, "Research on symmetric bipolar MMC-M2Tdc-based flexible railway traction power supply system," *IEEE Trans. Transp. Electrific.*, vol. 10, no. 1, pp. 1043–1055, Mar. 2024, doi: 10.1109/TTE.2023.3290591.

[13] L. Bessegato, K. Ilves, L. Harnefors, S. Norrga, and S. Östlund, "Control and admittance modeling of an AC/AC modular multilevel converter for railway supplies," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2411–2423, Mar. 2020.

[14] Cigre, "The first MVDC station project in Korea," ELECTRA-326, 2024.

[15] J. Yuan, L. Peng, H. Zhou, D. Gan, and K. Qu, "Recent research progress and application of energy storage system in electrified railway," *Electric Power Syst. Res.*, vol. 226, 2024, Art. no. 109893.

[16] Y. Chen, S. Zhao, Z. Li, X. Wei, and Y. Kang, "Modeling and control of the isolated DC–DC modular multilevel converter for electric ship medium voltage direct current power system," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 124–139, Mar. 2017.

[17] S. K. Patro and A. Shukla, "Modular Directed series multilevel converter for HVDC applications," *IEEE Trans. Ind. Appl.*, vol. 56, no. 2, pp. 1618–1630, Mar./Apr. 2020.

[18] M. B. Ghat et al., "The hybrid-legs bridge converter: A flexible and compact VSC-HVDC topology," *IEEE Trans. Power Electron.*, vol. 33, no. 8, pp. 6537–6554, Aug. 2018.

[19] F. Tardelli, A. Costabeber, D. Trainer, and J. Clare, "Series chain-link modular multilevel AC–DC converter (SCC) for HVDC applications," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 5714–5728, Jun. 2020.

[20] S. K. Patro, A. Shukla, and M. B. Ghat, "Hybrid series converter: A DC fault-tolerant HVDC converter with wide operating range," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 1, pp. 765–779, Feb. 2021.

[21] M. Hagiwara and H. Akagi, "Experiment and simulation of a modular push–Pull PWM converter for a battery energy storage system," *IEEE Trans. Ind. Appl.*, vol. 50, no. 2, pp. 1131–1140, Mar./Apr. 2014.

[22] H. Kilicoglu, H. Arya, M. Das, and P. Tricoli, "A new high-power charging points for battery electric vehicles with modular push-pull converters," in *Proc. Int. Symp. Power Electron., Elect. Drives, Autom. Motion*, 2022, pp. 581–586.

[23] M. Kaya, A. Costabeber, A. J. Watson, F. Tardelli, and J. C. Clare, "A push–Pull series connected modular multilevel converter for HVdc applications," *IEEE Trans. Power Electron.*, vol. 37, no. 3, pp. 3111–3129, Mar. 2022.

[24] H. Iman-Eini and M. Liserre, "DC fault current blocking with the coordination of half-bridge MMC and the hybrid DC breaker," *IEEE Trans Ind. Electron.*, vol. 67, no. 7, pp. 5503–5514, Jul. 2020.

[25] J. Qin, M. Saeedifard, A. Rockhill, and R. Zhou, "Hybrid design of modular multilevel converters for HVDC systems based on various submodule circuits," *IEEE Trans. Power Del.*, vol. 30, no. 1, pp. 385–394, Feb. 2015.

[26] M. Yang, X. Wang, W. Sima, T. Yuan, P. Sun, and H. Liu, "Air-core-transformer-based solid-State fault-current limiter for bidirectional HVdc systems," *IEEE Trans. Ind. Electron.*, vol. 69, no. 5, pp. 4914–4925, May 2022.

[27] W. A. M. Ghoneim and A. A. Aziz, "Sequential capacitors charging methods during single phase modular multilevel converter uncontrolled start-up pre-charging phase," *IEEE Access*, vol. 8, pp. 209043–209054, 2020.

[28] S. Shao, M. Jiang, J. Zhang, and X. Wu, "A capacitor voltage balancing method for a modular multilevel DC transformer for DC distribution system," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 3002–3011, Apr. 2018.

[29] D. Jovcic, *High Voltage Direct Current Transmission: Converters, Systems and DC Grids*, 2nd ed. Hoboken, NJ, USA: Wiley, 2015.

[30] L. Zheng, R. P. Kandula, and D. Divan, "Current-source solid-State DC transformer integrating LVDC microgrid, energy storage, and renewable energy into MVDC grid," *IEEE Trans. Power Electron.*, vol. 37, no. 1, pp. 1044–1058, Jan. 2022.

[31] S. Bazyar, J.-H. Jung, H. Beiranvand, J. V. M. Farias, and M. Liserre, "Quasi two-level modulation for the MMC-based isolated DC/DC converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2023, pp. 2424–2430.

[32] R. Mo, H. Li, and Y. Shi, "A phase-shifted square wave modulation (PS-SWM) for modular multilevel converter (MMC) and DC transformer for medium voltage applications," *IEEE Trans. Power Electrons.*, vol. 34, no. 7, pp. 6004–6008, Jul. 2019.

[33] N. Parida and A. Das, "Modular multilevel DC–DC power converter topology with intermediate medium frequency AC stage for HVDC tapping," *IEEE Trans. Power Electrons.*, vol. 36, no. 3, pp. 2783–2792, Mar. 2021.