A Current-Fed Dual-Active-Bridge Integrated *LC*-Resonant Converter With Dynamic Power Allocating for Wide Input and Output Voltage Range Operation

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***Abstract*—Current-fed isolated bidirectional dc–dc converters (CFIBDCs) are suitable solutions for feeding batteries. However, maintaining high efficiency over wide input and output voltage (IOV) range remains a challenge for them. This article proposes a hybrid CFIBDC intended for wide IOV range operation, which is constructed by integrating a current-fed dual-active-bridge and an *LC*-resonant converter (LCRC). It has two power channels, i.e., a DAB-based channel and an LCRC-based channel. The DAB-based channel can achieve zero-voltage-switching (ZVS) regardless of the IOV condition. And the LCRC-based channel, which features zero-current-switching (ZCS), can share the power for the DAB-based channel, thus reducing conduction losses. By properly allocating the power between two channels, low conduction losses, full-voltage-range ZVS or ZCS, as well as low turn-OFF losses can be simultaneously attained over wide IOV range, thus maintaining high efficiency for the proposed converter. Meanwhile, the total device capacity is not increased compared to the state of the art. Moreover, since LCRC provides a unity voltage gain, the proposed converter is naturally voltage-matched, leading to a simplified control scheme. The effectiveness of the converter is verified by a 1.5 kW experimental setup.**

***Index Terms*—Bidirectional dc–dc convert, current-fed converter, dual active bridge, resonant converter, wide voltage range.**

I. Introduction

ENERGY storage systems (ESSs) develop rapidly due to the high penetration of electrical vehicles (EVs) and renewable energy systems. Numerous ESSs contain battery packs with different voltage levels, which need to be bridged via power converters. For instance, traction batteries and low-voltage batteries in EVs are practically linked by auxiliary power modules. Such a scenario imposes requirements on power converters, e.g., high efficiency over wide input and output voltage (IOV) range, high security, high current quality, and bidirectional operation capability [1].

Current-fed isolated bidirectional dc–dc converters (CFIBDCs) are intrinsically adapted to these requirements owing to their inherent short-circuit protection, low current ripple on the low-voltage port, and direct current control capability [2]. CFIBDCs can be categorized into single-stage and two-stage types. The single-stage CFIBDCs are superior in terms of efficiency and cost, whereas the two-stage CFIBDCs offer higher reliability and control flexibility. Among various single-stage CFIBDCs [3], [4], [5], [6], [7], [8], current-fed dual-active-bridge (CFDAB) [5] is the best candidate to feed batteries due to its high reliability and outstanding overall performance [2]. As for the two-stage CFIBDCs [9], [10], [11], [12], the boost cascaded *LLC* (Boost+LLC) structure in [9] is the most popular choice owing to its low turn-OFF losses. Although CFDAB and Boost+LLC are the most attractive CFIBDCs for battery bridging, they still struggle to maintain high efficiency over wide IOV range.

CFDAB is constructed by sharing the switches of an interleaved boost converter and a DAB converter. By adjusting the duty cycles of the shared switches, CFDAB can maintain voltage matching on its DAB stage despite port voltage variations. Matched voltages give CFDAB low backflow power and excellent ZVS performance over wide IOV range [13], [14], [15], [16]. However, since voltage matching is realized via the shared switches, wide IOV range inevitably causes low duty cycles on them. This leads to a narrow high-frequency-ac (HFAC) power transfer window of the DAB stage, and ultimately a high transformer current. To suppress this current at a narrow power transfer window, dual-transformer-CFDAB (DT-CFDAB) in [17] enhances the modulation flexibility via an auxiliary transformer. Flexible modulation reduces the peak transformer current but has limited influence on the rms value. To fundamentally avoid a narrow power transfer window,

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H5-CFDAB [18] provides topological decoupling between boost and DAB stages through an H5-bridge. The DAB stage, which operates independently, eliminates high transformer current in principle. Nevertheless, decoupling operation limits the IOV range, and its ZVS restrictions as well as single boost inductor render it preferable for dc transformer rather than wide IOV high current application. CFDAB in paper [19] is able to avoid narrow power transfer window while guaranteeing wide IOV range via reconfigurable topology. But the unsmooth transition limits its practical application. The discussion above reveals that, for wide IOV range operation, the high transformer current caused by the narrow power transfer window is still not properly addressed for CFDAB. High transformer current induces high conduction and turn-OFF losses, which reduces efficiency.

Two-stage CFIBDCs are immune from the drawback of CFDAB due to the absence of shared switches. A detailed comparison between them was performed in paper [20], which indicated that Boost+LLC has more potential to realize high efficiency compared to single-stage CFIBDCs for wide IOV applications. Furthermore, in this scenario, Boost+LLC features lower total switch capacity despite employing more switches. However, Boost+LLC suffers from the inherent boost stage ZVS problem. If the boost stage operates with continuous conduction mode [20], ZVS cannot be achieved. And, if bidirectional conduction mode is adopted [21], high circulating currents and peak currents will occur on the boost inductors. Zhu et al. [22] employ variable-frequency modulation on the boost stage to maintain critical conduction mode, which is able to ensure ZVS while eliminating the circulating currents. But the widely varying frequency leads to severe hardware design issues, especially in wide IOV operations. In summary, the efficiency of Boost+LLC is degraded by the boost stage ZVS problem.

Additionally, single-stage and two-stage CFIBDCs also share some common issues, i.e., excessive number of voltage sensors and complex control loops. For a CFDAB performing voltage matching control, at least three voltage sensors are required to sample port voltages and low-voltage-side (LVS) dc-bus voltage. Two control loops are also necessary for voltage matching and power flow control. Similarly, two-stage CFIBDCs usually require attention to the intermediate dc-bus voltage in addition to the port voltages, which also introduces numerous voltage sensors and control loops.

This article constructs a dual-power-channel CFIBDC by integrating a CFDAB and an *LC*-resonant converter (LCRC). The principal part of the proposal is based on a CFDAB, thus providing a DAB-based power channel. While the integrated LCRC offers an additional paralleled power channel. These two channels feature different power transfer characteristics. Hence, the advantages of CFDAB and Boost+LLC can be combined, and their three above-mentioned defects can be overcome.

1) The DAB channel enables single-stage power transfer, but its transformer current is sensitive to the IOV ratio. Whereas, the LCRC channel is independent of IOV. Hence, the power of these two channels can be dynamically allocated according to IOV, and the impact of IOV on DAB transformer current can be mitigated by the LCRC channel.
2) Since the proposal integrates a CFDAB, the boost circuit shares switches with the DAB circuit, and the boost ZVS can be facilitated by the DAB transformer current. All switches enable full-voltage-range soft-switching. Besides, since the LCRC channel shares current for the DAB channel with zero-current-switching (ZCS), the DAB turn-OFF currents as well as turn-OFF losses can be suppressed.
3) Benefiting from the unity voltage gain of the LCRC at the resonant frequency, the converter is naturally voltage-matched without closed-loop control. A voltage sensor and control loop can be economized.

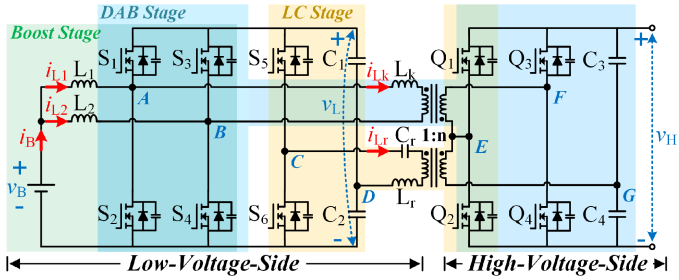

Fig. 1. Proposed current-fed DAB and LC-resonant hybrid converter.

In addition, under the wide IOV condition, the proposal features a lower total device capacity compared to CFDAB, despite adding a half-bridge and auxiliary transformer. This is because the current stresses on the devices are reduced.

The rest of the article is organized as follows. First, the proposed topology and its operation principle are analyzed in Section II. This is followed by a description of the power allocation strategy in Section III. Thereafter, the performances of the proposal, including conduction losses, soft-switching analysis, total device capacity, and power efficiency, are gauged and compared in Section IV. The experimental results are given in Section V. Section VI concludes this article.

II. Topology and Operation Principle

A. Circuit Configuration

Fig. 1 illustrates the schematic diagram of the proposed CFIBDC. The LVS switches S_1–S_4 together with boost inductors L_1, L_2 form a bidirectional interleaved boost topology. The inductive terminal of this boost stage interfaces with the low-voltage battery, while the other terminal feeds the LVS dc-bus which is supported by C_1 and C_2. The boost stage offers wide-range voltage regulation and current-fed feature for the converter.

Then, the boost stage switches S_1–S_4 are shared to form a DAB topology with high-voltage-side (HVS) switches Q_1–Q_4. The LVS and HVS of this DAB topology are linked by a transformer and leakage inductor L_k, which provide an isolated power channel to the proposed converter. This power channel is

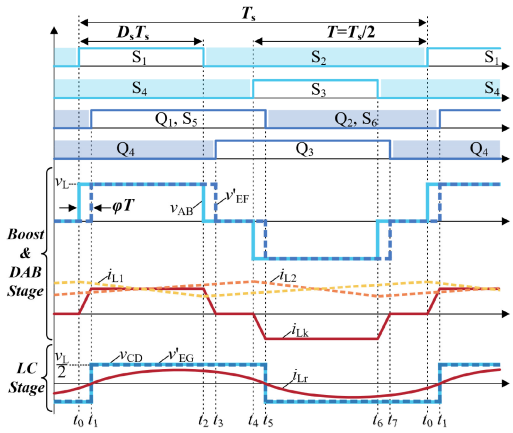

Fig. 2. Operational waveforms of power flow from LVS to HVS.

set as the major power channel, because its single-stage power transfer feature guarantees efficiency in most cases.

Thereafter, DAB stage switches Q_1, Q_2 are shared to form a bidirectional LCRC with LVS switches S_5, S_6. Its LVS and HVS are linked by an auxiliary transformer and a resonant tank composed of L_r and C_r. The resonant frequency of this tank is designed to coincide with the switching frequency, which ensures ZCS and unity gain of the *LC* stage. Since the *LC* stage is independent of the boost stage, it can be used as an auxiliary power channel to mitigate the impact of the boost stage on the DAB stage power transfer.

B. Operation Principle

The proposed CFIBDC can be regarded as a combination of interleaved boost, DAB, and LCRC. Therefore, the corresponding operation principles can be illustrated separately. The following illustration is based on a power flow from LVS to HVS. Fig. 2 shows the operational waveforms. Note that the symbol (') in Fig. 2 specifies the value reflected to the LVS.

1) Boost Stage:: In this topology, the boost stage is mainly employed to regulate the output voltage (or current). Its operation principle is consistent with that of a typical interleaved boost converter, i.e., S_1 and S_3 share a common duty cycle D_s, which determines the boost stage voltage gain. Thus, the boost stage voltage characteristic is described as follows:

$$v_L = \frac{v_B}{D_s} \tag{1}$$

where v_L is the LVS dc-bus voltage, and v_B is the LVS battery voltage. It is noted that D_s is preferred to be less than 0.5 to ensure full-voltage-range ZVS, like conventional CFDAB.

The current characteristic of the boost stage also needs to be modeled to prepare for the ZVS analysis in the following section. As can be seen from Fig. 2, for i_{L1}, we have $i_{L1}(t) = I_{L1,\text{avr}} + \Delta i_{L1}(t)$, where $I_{L1,\text{avr}}$ is the dc-bias current on L_1, and $\Delta i_{L1}(t)$ is the ripple current on L_1. $I_{L1,\text{avr}}$ can be calculated from the load power P_{tot}, as $I_{L1,\text{avr}} = P_{\text{tot}}/2v_B$. And $\Delta i_{L1}(t)$ can be derived from the differential equation of the inductor

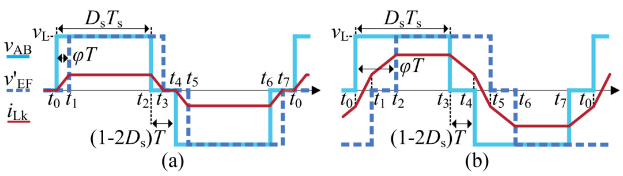

Fig. 3. DAB stage detailed waveforms under (a) mode I and (b) mode II.

current [23]. Finally, the expression of i_{L1} is obtained as follows:

$$i_{\text{L1}} = \begin{cases} \frac{P_{\text{tot}}}{2v_{\text{B}}} + \frac{v_{\text{B}}(1-D_{\text{s}})(D_{\text{s}}T+t_0-t)}{D_{\text{s}}\text{L}_1}, t \in [t_0, t_0+D_{\text{s}}T_{\text{s}}] \\ \frac{P_{\text{tot}}}{2v_{\text{B}}} + \frac{v_{\text{B}}(t-t_0-(1+D_{\text{s}})T)}{\text{L}_1}, t \in [t_0+D_{\text{s}}T_{\text{s}}, t_0+T_{\text{s}}] \end{cases} \tag{2}$$

where t_0 denotes the turn-ON moment of S_1 (see Fig. 2), and T signifies half a switching cycle $T_s/2$. The expression of i_{L2} is similar to i_{L1}, except that it lags i_{L1} by T.

2) DAB Stage: The DAB stage of the proposed topology is used for single-stage power transfer between LVS and HVS. Its operation principle is analogous to that of a typical DAB converter, that is, the HFAC voltages on the LVS and HVS of the transformer dictate the transformer current i_{Lk}, and thus determine the transferred power.

Following this principle, the generation of two HFAC voltages is analyzed first. For the LVS HFAC voltage v_{AB}, it is entirely dependent on the boost stage due to the shared LVS switches. As can be observed from Fig. 2, the pulsewidth of v_{AB} equals D_sT_s, while the amplitude of v_{AB} equals v_L. For the HVS HFAC voltage v_{EF}, its amplitude equals v_H. And its pulsewidth depends on both the phase-shift time between Q_1 and Q_3 as well as the duty cycles of Q_1 and Q_3. Since the duty cycles of Q_1 and Q_3 are fixed at 50% for proper operation of the *LC* stage, the pulsewidth of v_{EF} is only governed by the phase-shift time between Q_1 and Q_3 (see Fig. 2). This phase-shift time is designed to be D_sT_s to keep the pulsewidth of v_{EF} consistent with that of v_{AB}, which leads to an optimized operation pattern [24]. After reflecting v_{EF} to LVS, v'_{EF} and v_{AB} have the same pulsewidth and amplitude.

Thereafter, these two HFAC voltages (i.e., v_{AB} and v'_{EF}) generate current i_{Lk} on the inductor L_k. Given that v_{AB} and v'_{EF} share the same pulsewidth and amplitude, i_{Lk} is generated only if there is a phase-shift between them. This phase-shift time is determined by the time that Q_1 lags behind S_1, denoted as φT (see Fig. 2). When φT is shorter ($\varphi < 1-2D_{\text{s}}$), i_{Lk} behaves as a discontinuous trapezoidal wave, as depicted in Fig. 3(a). Otherwise, i_{Lk} is a continuous pentagonal wave, as shown in Fig. 3(b). These two i_{Lk} waveforms correspond to two DAB stage operation modes, which are defined as mode I and mode II, respectively. Based on the differential equation and volt-second balance of L_k, the expression of i_{Lk} for both modes can be derived [25], as follows:

$$\text{ModeI}: i_{Lk}(D_s,\varphi,t) = \begin{cases} \frac{v_L T}{L_k}\varphi, t = t_1, t_2 \\ 0, t = t_0, t_3, t_4, t_7 \\ -\frac{v_L T}{L_k}\varphi, t = t_5, t_6 \end{cases}$$

TABLE I
DEFINITION OF THE SWITCHING MOMENTS

Mode	t_0	t_1	t_2	t_3
I	0	φT	$2D_sT$	$(2D_s+\varphi)T$
II	0	$(\varphi-1+2D_s)T$	φT	$2D_sT$

Mode	t_4	t_5	t_6	t_7
I	T	$(1+\varphi)T$	$(1+2D_s)T$	$(1+2D_s+\varphi)T$
II	T	$(\varphi+2D_s)T$	$(1+\varphi)T$	$(1+2D_s)T$

$$\text{ModeII}: i_{Lk}(D_s,\varphi,t)=\begin{cases}-\frac{v_LT}{L_k}(\varphi+1-2D_s), t=t_0,t_5\\ \frac{v_LT}{L_k}(\varphi+1-2D_s), t=t_1,t_4\\ \frac{v_LT}{L_k}\varphi, t=t_2,t_3\\ -\frac{v_LT}{L_k}\varphi, t=t_6,t_7\end{cases} \tag{3}$$

i_{Lk} between two adjacent t_x varies linearly with t, and t_x can be identified by defining t_0 as the zero moment, as shown in Table I. Then, according to (3) and Table I, the rms value of i_{Lk} is deduced as follows:

$$i_{Lk,\mathrm{rms}}(D_s,\varphi)=\begin{cases}\frac{v_LT}{L_k}\varphi\sqrt{2D_s-\frac{\varphi}{3}}, 0<\varphi<1-2D_s\\ \frac{v_LT}{L_k}\sqrt{-\frac{2}{3}\varphi^3+\varphi^2-\varphi(1-2D_s)^2+\frac{(1-2D_s)^3}{3}}, \varphi>1-2D_s\end{cases}. \tag{4}$$

Finally, by performing the average time integral over $v_{AB}\cdot i_{Lk}$, the power characteristic of DAB stage can be identified, as follows:

$$P_{\mathrm{DAB}}(D_s,\varphi)=\begin{cases}\frac{v_L^2T}{L_k}\left(2\varphi D_s-\frac{\varphi^2}{2}\right), 0<\varphi<1-2D_s(\text{modeI})\\ \frac{v_L^2T}{L_k}\left(\varphi-\varphi^2-\frac{(1-2D_s)^2}{2}\right), \varphi>1-2D_s(\text{modeII})\end{cases}. \tag{5}$$

As can be seen from (5), the DAB stage power P_{DAB} is related to D_s and φ. But D_s is utilized to regulate voltage, which is dictated by the boost stage. As a result, the DAB stage power is only regulated by φ.

3) LC Stage: In the proposed converter, the *LC* stage is used to share the power for the DAB stage, as well as to achieve voltage matching between LVS and HVS dc-buses.

The *LC* stage HVS switches Q_1, Q_2 are switched with a 50% duty cycle (see Fig. 2), as mentioned above. The LVS switches S_5, S_6 share the gate pulses of Q_1, Q_2, respectively. Hence, the *LC* stage can be equated to two in-phase square-wave voltage sources linked via an *LC* resonant tank, as exhibited in Fig. 4(a). Here,R_p represents the parasitic resistance in the circuit. The square-wave sources in Fig. 4(a) can be further simplified as sine-wave sources in Fig. 4(b). This is because the bandpass filtering characteristic of the resonant tank renders the power transfer dominated by the fundamental component of the voltage sources. Furthermore, since the resonant tank has no impedance at its resonant frequency, v_{CD} and v'_{EG} are equivalent to being directly paralleled via R_p [see Fig. 4(c)]. This gives the *LC* stage a natural voltage matching feature. Meanwhile, the self-matching voltages drive the *LC* stage to automatically share the total power for the DAB stage. The voltage characteristic of the *LC* stage can be described as follows:

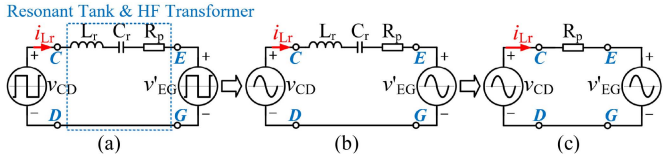

Fig. 4. Equivalent circuits of the *LC* stage.

$$v_H=nv_L \tag{6}$$

where n denotes the turns ratio of the DAB and *LC* stage transformers. According to (1) and (6), the overall voltage characteristic of the proposed CFIBDC is obtained as follows:

$$v_H=\frac{n}{D_s}v_B. \tag{7}$$

The current of the *LC* stage can also be characterized through the equivalent circuit in Fig. 4(c). Since the equivalent circuit is resistive, the current on it is purely sinusoidal and in phase with v_{CD} and v'_{EG}. This guarantees the ZCS feature of the *LC* stage. The amplitude of this current (i.e., i_{Lr}) can be calculated from the fundamental component of v_{CD} [26], as $i_{Lr,\mathrm{peak}}=\pi P_{LC}/v_L$. Then, the expression of i_{Lr} can be derived from $i_{Lr,\mathrm{peak}}$ and the moment definitions in Table I, as follows:

$$i_{Lr}(t)=\frac{\pi P_{LC}}{v_L}\sin\left(\frac{2\pi}{T_s}t-\pi\varphi\right). \tag{8}$$

4) Overall Operation: The overall operation principle of the converter can be summarized based on the description above. When power flows from LVS to HVS, the boost stage is responsible for the output voltage (or current) regulation via D_s; the DAB stage is responsible for the power transfer via φ; and the *LC* stage is responsible for the voltage matching and the power sharing with the DAB stage. When the power flow is reversed, the basic operation principle remains unchanged, except that the boost stage operates in buck mode.

As can be seen, the proposed converter has only two control variables, i.e., D_s and φ, which makes it control-friendly. D_s is directly dependent on the target output voltage (or current), whereas φ depends on the target DAB stage power. In the next section, we will find this target DAB stage power that enables high-efficiency operation of the converter over wide IOV range, and finally derive the control law for φ.

III. POWER ALLOCATION STRATEGY

The proposed CFIBDC has two power channels, i.e., the DAB-based major power channel, and the LCRC-based auxiliary power channel. The DAB-based power channel is affected by the boost stage duty ratio D_s, whereas the LCRC-based power channel is able to operate independently of the boost stage. To

prevent too low D_s from causing excessively high DAB stage current, the DAB stage power P_{DAB} and the *LC* stage power P_{LC} need to be allocated properly according to D_s.

In Section III-A, a power allocation strategy aimed at current balancing between two stages is provided, which mitigates the effect of D_s on the DAB stage via the *LC* stage. Moreover, since the boost stage cannot achieve ZVS individually, the power allocation strategy is also required to ensure that the DAB stage current i_{Lk} is sufficient to facilitate the boost ZVS. The ZVS constraint for the power allocation strategy is discussed in Section III-B. Finally, by combining the current balancing and ZVS constraint, the comprehensive power allocation strategy is provided in Section III-C. It is worth noting that this power allocation strategy does not necessarily guarantee the most efficient operation of the proposed converter. More optimized power allocation strategies may exist based on the proposed topology.

A. Power Allocation Strategy Aimed at Current Balancing

This strategy aims to compute a P_{DAB} that keeps $i_{Lk,\text{rms}}$ as close as possible to $i_{Lr,\text{rms}}$. As D_s decreases, the DAB stage power transfer window shrinks, and $i_{Lk,\text{rms}}$ tends to increase at constant power. In contrast, the *LC* stage power transfer window is unaffected, and $i_{Lr,\text{rms}}$ tends to remain constant. To maintain $i_{Lk,\text{rms}}$ close to $i_{Lr,\text{rms}}$, this strategy will automatically reduce P_{DAB}. And the *LC* stage will automatically share more power. Although $i_{Lk,\text{rms}}$ and $i_{Lr,\text{rms}}$ still rise after D_s decreases, the increments of both currents are not excessive. In this way, the effect of D_s on the DAB stage is mitigated by the *LC* stage. The evenly distributed currents will significantly reduce the conduction and switching losses on the switches.

Assume that the relationship between the DAB stage power and current is $i_{Lk,\text{rms}} = K_{\text{DAB}} \cdot P_{\text{DAB}}$, and the relationship for the *LC* stage is $i_{Lr,\text{rms}} = K_{LC} \cdot P_{LC}$. The total load power is shared by the DAB and LC stages, i.e., $P_{\text{tot}} = P_{\text{DAB}} + P_{LC}$. Based on these three relationships, the target DAB stage power for current balancing can be obtained, as follows:

$$P_{\text{DAB},cb} = \frac{K_{LC}}{K_{\text{DAB}} + K_{LC}} P_{\text{tot}}. \tag{9}$$

Then, the challenge is to find the analytical solution of $P_{\text{DAB},cb}$. In (9), K_{LC} can be easily deduced from (8) and is equal to $\pi/\sqrt{2}v_L$, whereas K_{DAB} is difficult to obtain directly. K_{DAB} represents the relationship between $i_{Lk,\text{rms}}$ and P_{DAB}. According to (4) and (5), $i_{Lk,\text{rms}}$ and P_{DAB} are all related to D_s and φ. Therefore, we can first compute $i_{Lk,\text{rms}}$ and P_{DAB} at different D_s and φ, then plot $i_{Lk,\text{rms}}$ versus P_{DAB} curves to induce the regularity of K_{DAB}. The $i_{Lk,\text{rms}}$ versus P_{DAB} curves at different D_s and φ are shown in Fig. 5.

As can be seen, when φ is relatively small, $i_{Lk,\text{rms}}$ and P_{DAB} are approximately linear, and the slope (i.e., K_{DAB}) depends almost exclusively on D_s. As φ increases beyond a certain value, the increment of $i_{Lk,\text{rms}}$ grows rapidly. For a conventional CFDAB with a single power channel, at low D_s, φ will inevitably be excessive in order to transfer sufficient power, resulting in excessively high i_{Lk}. In contrast, for the proposed topology, the DAB power channel will not carry high power at low D_s due

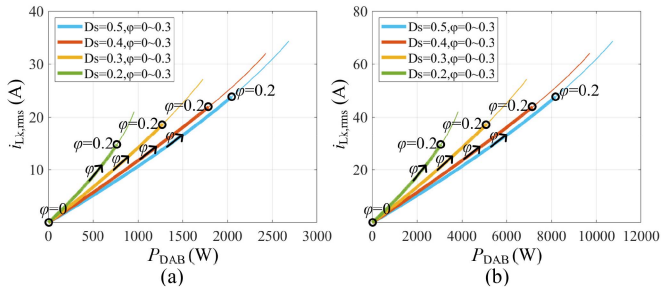

Fig. 5. Relationship between $i_{Lk,\text{rms}}$ and P_{DAB} at (a) $v_H = 200$ V, (b) $v_H = 400$ V. (hardware parameters: $L_k = 8\ \mu$H, $f_s = 48.9$ kHz, $n = 2$).

to the existence of the LC stage, which avoids excessive φ. As a result, it can be assumed that there is a linear relationship between $i_{Lk,\text{rms}}$ and P_{DAB} of the proposed topology, and K_{DAB} depends only on D_s but not on φ. Hence, we can select φ as a specific value, and then divide the corresponding $i_{Lk,\text{rms}}$ and P_{DAB} to fit K_{DAB}. Here, φ is selected to be 0.2. This is because, under the hardware and power conditions of this article, φ will not exceed 0.2, which will be verified in Section C. Following this, K_{DAB} is fitted as follows:

$$\begin{aligned} K_{\text{DAB}}(D_s) &\approx \frac{i_{Lk,\text{rms}}(\varphi = 0.2, D_s)}{P_{\text{DAB}}(\varphi = 0.2, D_s)} \\ &= \begin{cases} \frac{1}{v_L} \frac{\sqrt{2D_s - \frac{1}{15}}}{2D_s - \frac{1}{10}}, D_s \le 0.4 \\ \frac{1}{v_L} \frac{\sqrt{\frac{13}{375} - \frac{(1-2D_s)^2}{5} + \frac{(1-2D_s)^3}{3}}}{\frac{4}{25} - \frac{(1-2D_s)^2}{2}}, D_s > 0.4 \end{cases}. \end{aligned} \tag{10}$$

Substituting K_{DAB} and K_{LC} into (9) yields the analytical solution of $P_{\text{DAB},cb}$. It is observed that the $1/v_L$ in K_{DAB} and K_{LC} is canceled, and only two variables, P_{tot} and D_s, are involved in $P_{\text{DAB},cb}$. This reveals that the power allocation strategy is independent of the hardware parameters and operational states.

Finally, based on $P_{\text{DAB},cb}$ in (9) and the DAB stage power expression in (5), φ can be calculated. The DAB stage is open-loop regulated by this φ to achieve current balancing. This φ is denoted as φ_{cb}.

B. ZVS Constraint

The current balancing strategy avoids high i_{Lk} of the DAB stage. However, i_{Lk} also contributes to the boost stage ZVS because the boost stage shares switches with the DAB stage. i_{Lk} yielded by the current balancing strategy may not satisfy the ZVS constraint. Therefore, the ZVS constraint on i_{Lk} should be derived to refine the power allocation strategy.

From Fig. 1, one can observe that the boost stage ZVS conditions are described as follows:

$$\begin{cases} \text{S}_1\text{: } i_{LK} - i_{L1} < 0 \text{ before } S_1 \text{ turned ON} \\ \text{S}_2\text{: } i_{LK} - i_{L1} > 0 \text{ before } S_2 \text{ turned ON} \\ \text{S}_3\text{: } i_{LK} + i_{L2} > 0 \text{ before } S_3 \text{ turned ON} \\ \text{S}_4\text{: } i_{LK} + i_{L2} < 0 \text{ before } S_4 \text{ turned ON} \end{cases}. \tag{11}$$

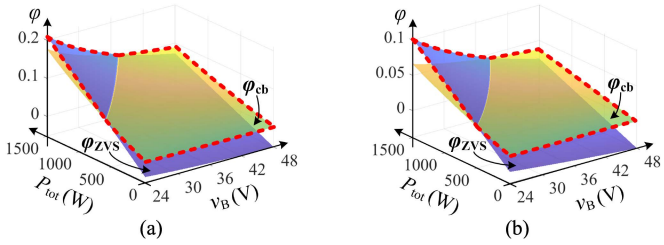

Fig. 6. φ_{cb} and φ_{ZVS} at different v_B and P_{tot} when v_H equals (a) 200 V, (b) 400 V. (hardware parameters: $L_{1,2} = 40\ \mu$H, $L_k = 8\ \mu$H, $f_s = 48.9$ kHz, $n = 2$)

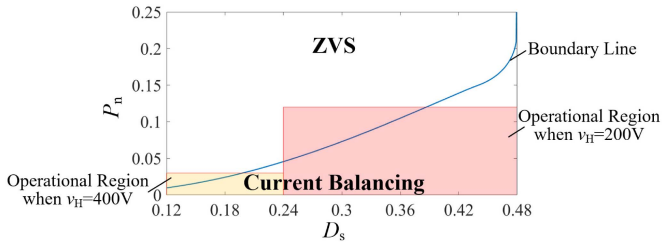

Fig. 7. Boundary between φ_{cb} and φ_{ZVS}.

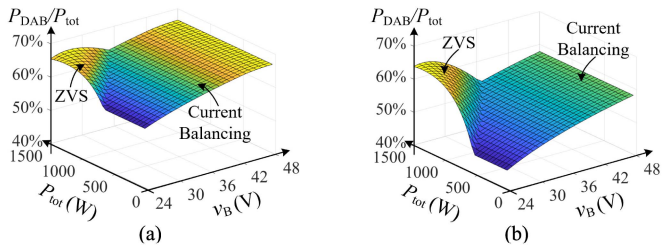

Fig. 8. DAB stage power proportion at different v_B and P_{tot} when v_H equals (a) 200 V, (b) 400 V. (hardware parameters: $L_{1,2} = 40\ \mu$H, $L_k = 8\ \mu$H, $f_s = 48.9$ kHz, $n = 2$).

Then, referring to the waveform in Fig. 2, (11) is transformed into the following:

$$\begin{cases} \mathrm{S}_1{:}i_{LK}(t_0) < i_{L1}(t_0) \\ \mathrm{S}_2{:}i_{LK}(t_2) > i_{L1}(t_2) \\ \mathrm{S}_3{:}i_{LK}(t_4) > -i_{L2}(t_4) \\ \mathrm{S}_4{:}i_{LK}(t_6) < -i_{L2}(t_6) \end{cases}. \tag{12}$$

Since i_{Lk} is close to zero at t_0 and t_4 while i_{L1} and i_{L2} reach their peak values at these two moments, the ZVS conditions for S_1 and S_3 can be easily achieved. For S_2 and S_4, since $i_{Lk}\ (t_2) = -i_{Lk}(t_6)$ and $i_{L1}\ (t_2) = i_{L2}\ (t_6)$, their ZVS conditions are identical. Then, based on (2), (3) and Table I, the ZVS condition for S_2 and S_4 can be expanded as follows:

$$\frac{v_L T}{L_k}\varphi > \frac{P_{\mathrm{tot}}}{2v_B} - \frac{v_B(1-D_s)T}{L_1}. \tag{13}$$

Equation (13) indicates that φ must be higher than a certain lower limit value to guarantee the boost stage ZVS, as follows:

$$\varphi > \frac{D_s P_{\mathrm{tot}} L_k}{v_B^2 T_s} - \frac{D_s(1-D_s)L_k}{L_1}. \tag{14}$$

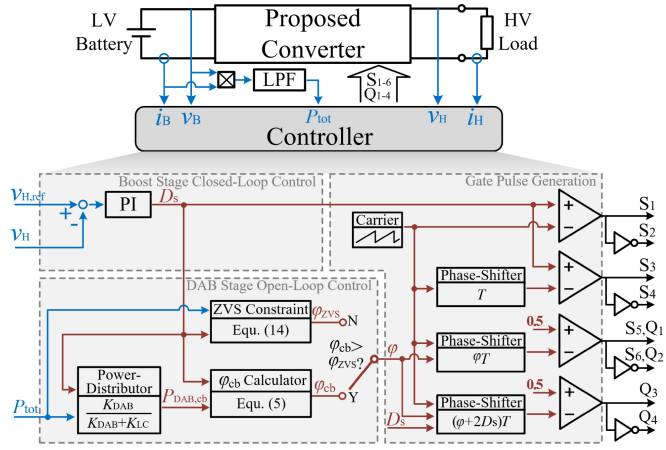

Fig. 9. Overall control framework of the proposed converter.

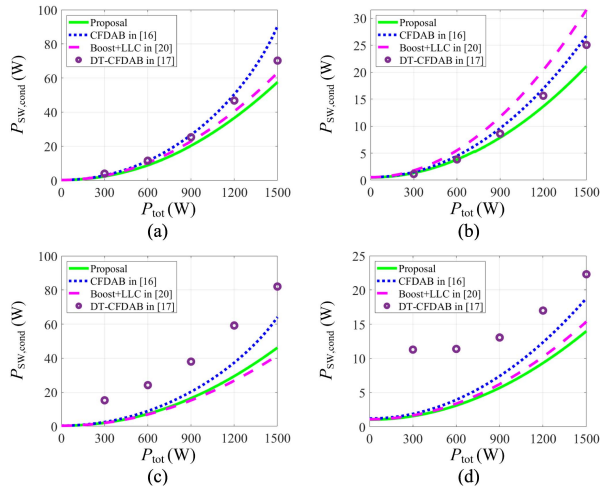

Fig. 10. Conduction loss performances of different CFIBDCs at (a) $v_H = 200$ V, $v_B = 24$ V; (b) $v_H = 200$ V, $v_B = 48$ V; (c) $v_H = 400$ V, $v_B = 24$ V; (d) $v_H = 400$ V, $v_B = 48$ V.

This lower limit value of φ to achieve ZVS is labeled as φ_{ZVS}.

Besides, if the junction capacitor on S_2 (or S_4) is required to be fully discharged, i_{Lk} needs to be slightly higher than i_{L1} by a certain value at its turn-ON moment (i.e., t_2). According to paper [13], this value is expressed as follows:

$$i_{Lk}(t_2) - i_{L1}(t_2) > \frac{v_H}{2nL_k}t_d + 2C_{\mathrm{oss},S2}\frac{v_H}{nt_d} \tag{15}$$

where t_d is the LVS deadtime, and $\mathrm{C}_{\mathrm{oss},S2}$ is the junction capacitance on S_2. Accordingly, φ_{ZVS} needs to be compensated by one term $\Delta\varphi_{\mathrm{ZVS}}$ to ensure that (15) holds, as follows:

$$\Delta\varphi_{\mathrm{ZVS}} = \frac{t_d}{T_s} + \frac{4C_{\mathrm{oss},S2}L_k}{T_s t_d}. \tag{16}$$

This compensation term $\Delta\varphi_{\mathrm{ZVS}}$ will drive $i_{Lk}(t_2)$ higher than $i_{L1}(t_2)$, thus resulting in a current sufficient to discharge the junction capacitor on S_2 (or S_4).

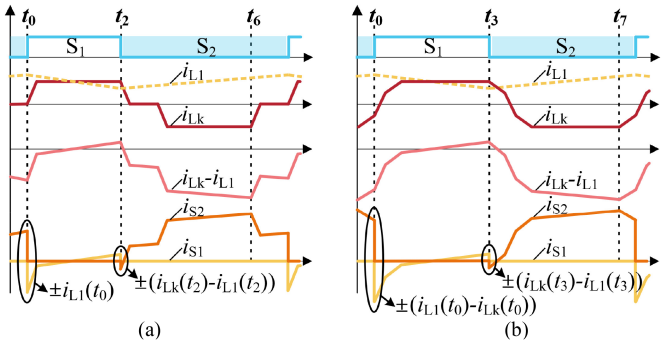

Fig. 11. Switching currents on S_1, S_2 under (a) mode I and (b) mode II.

C. Comprehensive Power Allocation Strategy

The above-mentioned analysis shows that the power allocation strategies aimed at current balancing and ZVS impose different requirements on φ, respectively. To verify the compatibility of these two strategies, we will compute and compare φ_{cb} and φ_{ZVS} under a specified operation scenario. Given that the proposal is intended for high voltage ratio and wide IOV operation, v_B and v_H are specified at 24–48 V and 200–400 V, respectively, with a maximum power of 1500 W.

Thereafter, the comparison results of φ_{cb} and φ_{ZVS} at $v_H =$ 200 V and $v_H =$ 400 V are exhibited in Fig. 6(a) and (b), respectively. As can be seen, in most cases, current balancing and ZVS can be simultaneously achieved. However, if v_B is low while P_{tot} is high, φ_{cb} cannot ensure ZVS. In this case, the designer should evaluate the priority of current balancing and ZVS, and then select a more suitable value for φ. Here, to achieve the full-voltage-range soft-switching, ZVS is prioritized. That is, if $\varphi_{cb} < \varphi_{\text{ZVS}}$, φ_{ZVS} is selected, otherwise, φ_{cb} is selected. The φ-surface yielded by this comprehensive strategy is outlined by the red dashed line in Fig. 6. In addition, Fig. 6 also indicates that neither φ_{cb} nor φ_{ZVS} exceeds 0.2 for the given scenario, which validates the pre-assumption on φ in Section III-A.

Fig. 7 exhibits the distribution of current balancing strategy and ZVS strategy over the entire operating region. P_n in Fig. 7 is the normalized total power, $P_n = P_{\text{tot}} / P_{\text{base}}$, where $P_{\text{base}} = {v_H}^2 T/(n^2 L_k)$. The boundary line equation in Fig. 7 is deduced by combining (14), (5), and (9), since at the boundary of two strategies we have $\varphi_{\text{ZVS}} = \varphi_{cb}$. The deduced boundary line equation is only determined by P_n and D_s, where P_n depends on P_{tot} and v_H, and D_s depends on v_B and v_H. Fig. 7 shows that the operating region of the converter is separated into two parts by the boundary line. When P_n is high and D_s is low, ZVS strategy is encountered, otherwise, current balancing strategy is implemented.

To visualize the power distribution among two power channels under the proposed strategy, the percentage of P_{DAB} at different operating conditions is depicted in Fig. 8. P_{DAB} in Fig. 8 is calculated based on the φ in Fig. 6 and the DAB stage power expression in (5). As can be seen, the power distribution exhibits two different characteristics depending on the operating conditions. In most cases, the converter operates under the current balancing strategy. As v_B decreases, D_s decreases, the DAB power transfer window shrinks, and $P_{\text{DAB}}/P_{\text{tot}}$ decreases to maintain current balancing. On the other hand, when P_{tot} is high and v_B is low, the large $i_{L1,2}$ will drive the converter to operate under the ZVS strategy. In this case, the DAB stage current i_{Lk} is required to facilitate the boost stage ZVS, and $P_{\text{DAB}}/P_{\text{tot}}$ will increase as P_{tot}/v_B increases.

The overall control framework is shown in Fig. 9, with v_H as the controlled variable. If the converter is feeding a voltage source load and needs to regulate the power, an outer power loop can be first built outside the "Boost Stage Closed-Loop Control" in Fig. 9. Based on the difference between the target power and sampled power, this power loop yields the reference value for i_B (i.e., $i_{B,\text{ref}}$). Then, $i_{B,\text{ref}}$ and i_B can be fed back into Fig. 9 instead of $v_{H,\text{ref}}$ and v_H, and the framework will not change. The controller consists of three parts, i.e., boost stage closed-loop control, DAB stage open-loop control, and gate pulse generation logic. For the boost stage, closed-loop control of v_{H} generates D_s. D_s is compared with the carrier to yield boost stage gate pulses. For the DAB stage, the power allocation aimed at current balancing is first performed, and $P_{\text{DAB},cb}$ is obtained. Then, φ_{cb} can be calculated. Meanwhile, φ_{ZVS} is obtained from (14). φ_{cb} and φ_{ZVS} yields DAB stage direct control variable φ. φ is utilized to phase shift the original carrier, and generates the DAB and *LC* stage gate pulses. As can be seen, the controller only needs to sample the port voltages and currents without concern for v_L. Furthermore, the DAB stage operates in open loop without complex control. And the equations used in the controller have simple analytical solutions, which are friendly to industrial applications. These advantages benefit from the combination of CFDAB and LCRC.

IV. Performance Analysis and Comparison

A. Conduction Losses Analysis

The conduction losses of the converter can be evaluated via the mean-square current on all the switches. We define the conduction losses on all the switches as $P_{\text{sw,cond}}$, then we have the following:

$$P_{\text{sw,cond}} = R_{ds,L} \sum_{x=1}^{6} i_{S_x,\text{rms}}^2 + R_{ds,H} \sum_{x=1}^{4} i_{Q_x,\text{rms}}^2 \tag{17}$$

where $R_{ds,L}$ and $R_{ds,H}$ are the ON-resistances of the LVS and HVS switches, respectively. And $i_{S_x,\text{rms}}$ $i_{Q_x,\text{rms}}$ are the rms currents on S_1–S_6 and Q_1–Q_4, respectively. Then, based on Fig. 2 and (11), $i_{S_1,\text{rms}}^2$ and $i_{S_2,\text{rms}}^2$ can be expressed as follows:

$$\begin{cases} i_{S_1,\text{rms}}^2 = \frac{1}{T_s}\int_{t_0}^{t_2} \left(i_{Lk}(t) - i_{L1}(t)\right)^2 dt \\ i_{S_2,\text{rms}}^2 = \frac{1}{T_s}\int_{t_2}^{t_0+T_s} \left(i_{Lk}(t) - i_{L1}(t)\right)^2 dt \end{cases}. \tag{18}$$

Summing up $i_{S_1,\text{rms}}^2$ and $i_{S_2,\text{rms}}^2$, we obtain the following:

$$i_{S_1,\text{rms}}^2 + i_{S_2,\text{rms}}^2 = \frac{1}{T_s}\int_{t_0}^{t_0+T_s} \left(i_{Lk}(t) - i_{L1}(t)\right)^2 dt. \tag{19}$$

As can be seen, $i_{S_1,\text{rms}}^2 + i_{S_2,\text{rms}}^2$ is equals to the mean-square value of $i_{Lk} - i_{L1}$. $i_{S_3,\text{rms}}^2 + i_{S_4,\text{rms}}^2$ has a same expression. Following a similar procedure, $i_{S_5,\text{rms}}^2 + i_{S_6,\text{rms}}^2$ is calculated as

TABLE II
HARDWARE PARAMETERS

Description	Variable	Value
HVS voltage	v_H	200~400 V
LVS battery voltage	v_B	24~48 V
Maximum load power	$P_{\text{tot,max}}$	1500 W
Switching frequency	f_s	48.9 kHz
DAB and LC stage transformer turns ratio	1:n	1:2
DAB stage leakage inductance	L_k	8 μH
LC stage resonant inductance	L_r	2.1 μH
LC stage resonant capacitance	C_r	5 μF
Boost inductances[a]	L_1, L_2	40 μH
LVS split capacitances	C_1, C_2	68 μF
HVS split capacitances	C_3, C_4	12 μF
LVS switches	S_1–S_6	IRF300P226
HVS switches	Q_1–Q_4	C3M0025065D

Note: [a]Detailed parameters of magnetic components are provided in Appendix B.

$i^2_{Lr,\text{rms}}$, $i^2_{Q_3,\text{rms}} + i^2_{Q_4,\text{rms}}$ is deduced as $i^2_{\text{Lk,rms}}/n^2$, and $i^2_{\text{Q}_1,\text{rms}} + i^2_{\text{Q}_2,\text{rms}}$ is determined by the mean-square value of $(i_{\text{Lk}} + i_{\text{Lr}})/n$. Accordingly, $P_{\text{sw,cond}}$ in (17) can be expanded as follows:

$$\begin{aligned} P_{\text{sw,cond}} = &\left(2R_{ds,L} + \frac{2R_{ds,H}}{n^2}\right) i^2_{Lk,\text{rms}} \\ &+ \left(R_{ds,L} + \frac{R_{ds,H}}{n^2}\right) i^2_{Lr,\text{rms}} \\ &+ 2R_{ds,L} i^2_{L1,\text{rms}} \\ &- 4R_{ds,L} \int_{t_0}^{t_0+T_s} i_{Lk}(t) i_{L1}(t) dt \\ &+ \frac{2R_{ds,H}}{n^2} \int_{t_0}^{t_0+T_s} i_{Lk}(t) i_{Lr}(t) dt. \end{aligned} \tag{20}$$

Equation (20) can be solved based on (2), (4), (8), and Table I. The explicit solution for (20) is omitted here for the sake of brevity. The final calculated $P_{\text{sw,cond}}$ is related to the hardware parameters, v_B, v_H, and P_{tot}.

To visualize the conduction loss performance of the proposal, Fig. 10 depicts $P_{\text{sw,cond}}$ versus P_{tot} curves at different v_B and v_H, which are marked with green solid lines. The corresponding hardware parameters are presented in Table II. The design considerations for the hardware parameters are illustrated in Appendix A. Fig. 10 also exhibits the conduction loss performances of three existing state-of-the-art CFIBDCs for comparison. Among them, the $P_{\text{sw,cond}}$ of CFDAB and Boost+LLC are obtained through mathematical calculation. Whereas the $P_{\text{sw,cond}}$ of DT-CFDAB are obtained from the simulation, since its power expression is implicit. To align the hardware conditions as closely as possible, different topologies are based on similar hardware parameters (see Table II). However, it is worth noting that CFDAB has no resonant tank, Boost+LLC has no L_k, and different topologies have different transformer turns ratios.

From Fig. 10, one can observe that different topologies feature different conduction loss performances, despite employing similar hardware. In addition, the same topology performs quite distinctly at different IOV. When both v_B and v_H are low (see Fig. 10(a)), the relatively large difference between v_B and v_H results in a low D_s, thus limiting the power transfer windows of CFDAB and DT-CFDAB. As a result, their conduction losses are high. In contrast, the two-stage Boost+LLC features lower conduction losses because its power transfer window is unaffected by D_s. Similarly, the proposal utilizes an *LC* stage, which is independent of D_s, to share the power for the DAB stage, which also offers low conduction losses. As v_B increases, the situation changes [see Fig. 10(b)]. The relatively small gap between v_B and v_H yields a D_s close to 0.5, which enables CFDAB and DT-CFDAB to transfer power over the entire switching cycle. Benefiting from single-stage power transfer, CFDAB and DT-CFDAB have lower conduction losses compared to Boost+LLC. Even so, the proposal can further reduce the conduction losses via two current-balanced power channels. Fig. 10(c) and (d) demonstrate the conduction loss performances at higher v_{H} ($v_{\text{H}} = 400$ V). Higher v_{H} leads to lower D_{s}, which in turn imposes large current stresses on CFDAB and DT-CFDAB. Moreover, high v_{H} causes high backflow power on the auxiliary transformer of DT-CFDAB, which further aggravates the conduction losses. In contrast, the two-stage topology and the proposal are more adaptable to higher v_H. It can be concluded that the proposal combines the merits of CFDAB and Boost+LLC, and therefore adapts well to the wide IOV and power variations.

B. Switching Performance Analysis

Different switches of the proposed converter have different switching performances. For S_1 and S_2, the currents on them (i.e., i_{S1} and i_{S2}) can be expressed as $\pm(i_{\text{Lk}} - i_{\text{L1}})$, where i_{Lk} has two different waveforms (see Fig. 3). Hence, i_{S1} and i_{S2} have two different modes, as depicted in Fig. 11. In mode I, at S_1 turn-ON and S_2 turn-OFF moment [t_0 in Fig. 11(a)], i_{S1} and i_{S2} are equal to $-i_{L1}(t_0)$ and $i_{L1}(t_0)$, respectively. This reveals that S_1 can easily achieve ZVS turn-ON, while the S_2 turn-OFF loss will not exceed that of a typical boost converter. On the other hand, at S_1 turn-OFF and S_2 turn-ON moment [t_2 in Fig. 11(a)], i_{S1} and i_{S2} are equal to positive and negative $i_{Lk}(t_2) - i_{L1}(t_2)$, respectively. According to the power allocation strategy, the DAB phase-shift ratio φ is able to render $i_{Lk}(t_2)$ higher than, but not excessively higher than, $i_{L1}(t_2)$. This is because, if $\varphi = \varphi_{\text{ZVS}}$, $i_{Lk}(t_2)$ will be modulated to be only slightly higher than $i_{L1}(t_2)$; whereas, if $\varphi = \varphi_{\text{cb}}$, the current balancing strategy will suppress the value of $i_{Lk}(t_2)$. As a result, S_2 can achieve ZVS turn-ON, while S_1 has low turn-OFF loss. For mode II, the situations are similar, except for a slightly increased turn-OFF loss on S_2. The switching performances of S_3, S_4 are consistent with those of S_1, S_2. It is worth noting that the soft-switching of S_1–S_4 can be realized independently of the load power as long as the boost stage inductors $L_{1,2}$ are not overly large, as demonstrated in [13].

For S_5 and S_6, which are only involved in the *LC* stage, their switching currents are close to zero. Therefore, ZCS can be realized. Besides, ZVS of $S_{5,6}$ can also be achieved via the magnetic current as long as the magnetic inductance of *LC* stage transformer is properly designed [27]. For Q_3 and Q_4, they are only involved in the DAB stage. And their switching currents are also close to zero, as shown in Fig. 2. Thus, Q_3 and Q_4 can also realize ZCS. If ZVS is required for $Q_{3,4}$, the optimized

switching patterns in [16] can be employed on DAB stage to replace the basic trapezoidal modulation in this article.

For Q_1 and Q_2, which are shared by the DAB and *LC* stages, their switching performances depend on both i_{Lk} and i_{Lr}. Furthermore, since i_{Lr} is close to zero at the switching moments, i_{Lk} dominates the switching performances. At heavy loads, ZVS can be easily achieved on $Q_{1,2}$ due to the negative peak value of i_{Lk}, as shown in Fig. 2. However, if the load is too light, the peak value of i_{Lk} will be insufficient to fully discharge the junction capacitors on $Q_{1,2}$, and $Q_{1,2}$ will operate at incomplete ZVS. The load range that enables complete ZVS of $Q_{1,2}$ is determined by the value of L_k. A larger L_k results in a higher power on L_k, thus guaranteeing the full discharge of $Q_{1,2}$ junction capacitors even if $i_{Lk,\text{peak}}$ (or load power) is relatively low. In this article, L_k is designed to guarantee the complete ZVS of $Q_{1,2}$ for a load power higher than 1/3 of the rated power in the worst case, as detailed in Appendix A. Therefore, when $P_{\text{tot}} > 500$ W, $Q_{1,2}$ can achieve complete ZVS in arbitrary conditions. Furthermore, since the proposal avoids high i_{Lk}, Q_1 and Q_2 will not suffer from high turn-OFF currents, thus avoiding high turn-off losses as well.

In summary, the proposed converter can realize ZVS or ZCS turn-ON for all the switches. Moreover, ZCS turn-OFF or low-loss turn-OFF can also be realized. In contrast, Boost+LLC is subject to the boost stage hard-switching, while CFDAB and DT-CFDAB cannot guarantee low turn-OFF losses.

C. Switching Device and Transformer Capacity Analysis

Compared to single-stage CFIBDCs, the proposed topology requires an additional half-bridge and transformer. However, the proposal is more cost-effective for wide IOV operation thanks to the lower transformer current. To prove this, we will calculate the total capacity of the switching devices and transformers at different given powers over wide IOV range. The IOV range and hardware parameters are shown in Table II.

The total switching device capacity of the proposal is expressed as follows:

$$UI_{\text{sw}} = \frac{v_{\text{H,max}}}{n}\sum_{x=1}^{6}|i_{S_x}|_{\max} + v_{\text{H,max}}\sum_{x=1}^{4}|i_{Q_x}|_{\max} \tag{21}$$

where UI_{sw} denotes the total switching device capacity, $v_{\text{H,max}}$ represents the maximum value of v_{H}, and $|i_{S_x}|_{\max}$ and $|i_{Q_x}|_{\max}$ are the absolute maximum currents on the switches over the entire IOV range.

Obviously, $|i_{S_1}|_{\max}$ and $|i_{S_2}|_{\max}$appear at the lowest v_B and v_H. Therefore, $|i_{S_1}|_{\max}$ and $|i_{S_2}|_{\max}$ are actually the peak values of i_{S_1} and i_{S_2} at $v_B = 24$ V, $v_H = 200$ V. The peak value moments can be obtained from Fig. 11. Thereafter, based on (2), (3) and Table I, $|i_{S_1}|_{\max}$ and $|i_{S_2}|_{\max}$ at different given powers can be computed. $|i_{S_3}|_{\max}$ and $|i_{S_4}|_{\max}$ have same values as $|i_{S_1}|_{\max}$ and $|i_{S_2}|_{\max}$. Following a similar principle, $|i_{Q_3}|_{\max}$ and $|i_{Q_4}|_{\max}$ are the peak value of i_{Lk} at $v_B = 24$ V, $v_H = 200$ V, which can be calculated from (3) and Table I.

The situations are different for the remaining four switches. For $|i_{S_5}|_{\max}$ and $|i_{S_6}|_{\max}$, they are determined by the maximum value of $i_{Lr,\text{peak}}$ over the entire IOV range. $i_{Lr,\text{peak}}$ is higher

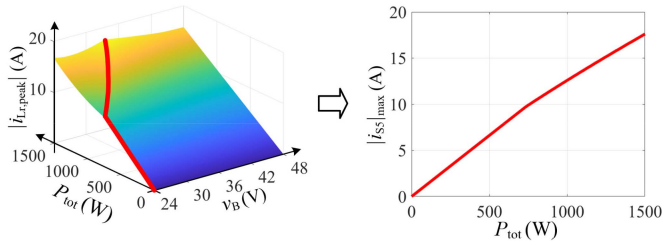

Fig. 12. Maximum current on S_5 at different given powers.

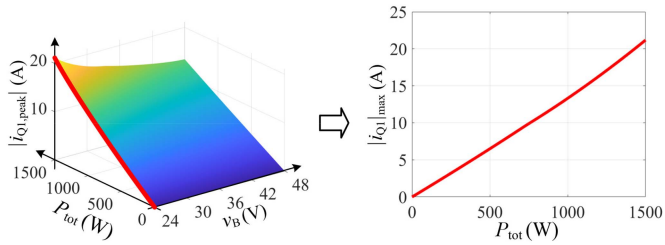

Fig. 13. Maximum current on Q_1 at different given powers.

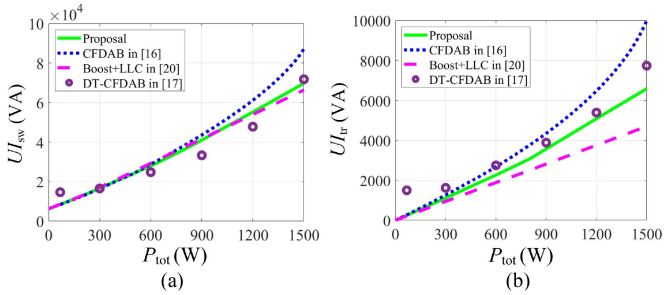

Fig. 14. Total capacity of (a) switching devices and (b) transformers.

when v_H is lower, but its relationship with v_B is not evident. Thus, we can first fix v_H at 200 V, then compute $i_{Lr,\text{peak}}$ at different v_B and load powers through (8), and finally extract the maximum value of $i_{Lr,\text{peak}}$ at different given powers by traversing the surface of $i_{Lr,\text{peak}}$, as demonstrated in Fig. 12. Following a similar procedure, $|i_{Q_1}|_{\max}$ and $|i_{Q_2}|_{\max}$ at different given powers can also be extracted (see Fig. 13).

Finally, by substituting the obtained $|i_{S_x}|_{\max}$ and $|i_{Q_x}|_{\max}$ into (21), UI_{sw} at different given powers can be calculated. UI_{sw} of three other CFIBDCs are also computed for comparison. The comparison results are shown in Fig. 14(a). As can be seen, the proposal features a lower total switching device capacity compared to the conventional single-stage CFIBDC (i.e., CFDAB), despite employing an additional half-bridge. Note that this conclusion is only for the wide IOV range scenario.

Following a similar procedure, the total transformer capacity (labeled as UI_{tr}) can be calculated. For the proposed converter, UI_{tr} is expressed as follows:

$$UI_{\text{tr}} = \frac{v_{H,\max}}{n}|i_{Lk}|_{\max} + \frac{v_{H,\max}}{2n}|i_{Lr}|_{\max}. \tag{22}$$

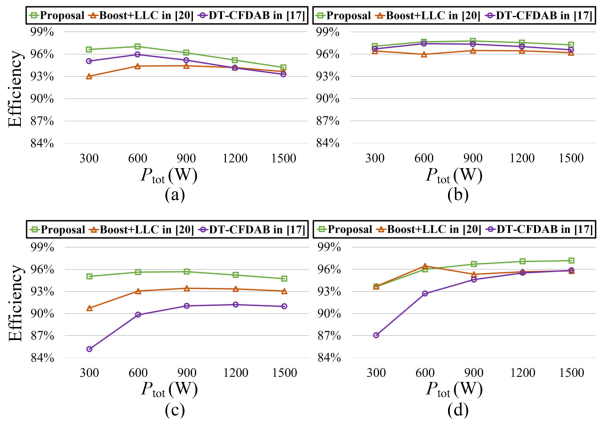

Fig. 15. Efficiency curves of different CFIBDCs at (a) $v_H = 200$ V, $v_B = 24$ V; (b) $v_H = 200$ V, $v_B = 48$ V; (c) $v_H = 400$ V, $v_B = 24$ V; (d) $v_H = 400$ V, $v_B = 48$ V.

The detailed calculations for $|i_{Lk}|_{\max}$ and $|i_{Lr}|_{\max}$ have been provided in the above-mentioned discussion, and the final obtained UI_{tr} is depicted in Fig. 14(b). As can be observed, compared to CFDAB, the proposal offers a lower total transformer capacity in spite of using an auxiliary transformer. This is because neither transformer in the proposal will carry excessive current.

However, it is worth noting that excessively large boost inductors $L_{1,2}$ will eliminate the device capacity advantage of the proposal compared to CFDAB. If $L_{1,2}$ are excessively large, the current ripples on i_{L1} and i_{L2} will be oversuppressed, which will excessively increase the valley values of i_{L1} and i_{L2}. Based on (12), the peak value of DAB stage current i_{Lk} depends on the valley values of i_{L1} and i_{L2} at ZVS strategy. Hence, overly high valley values of i_{L1} and i_{L2} will force DAB stage to carry excessive power and idle the *LC* stage, which will ultimately increase the converter device capacity. As a result, it is not recommended to use excessively large $L_{1,2}$. Even for conduction loss reduction, smaller boost inductors are adequate at the target operating conditions, as discussed in paper [14].

D. Efficiency Analysis and Comparison

Fig. 15 exhibits the efficiency comparison between the proposal and the other two state-of-the-art CFIBDCs. All the efficiency curves are obtained based on the methodology provided in [2] and the hardware parameters in Table II. As can be seen, the proposal presents the highest efficiency over wide IOV range and load range. The full-load efficiency of the proposal can reach up to 97.3% at $v_B = 48$ V, $v_H = 200$ V. Even in the worst case, the full-load efficiency can be maintained at over 94.2%. In contrast, the efficiency of DT-CFDAB is quite sensitive to the IOV ratio, since a large IOV difference yields high conduction losses on it. Whereas, the efficiency of Boost+LLC is quite sensitive to v_H, because its hard-switching losses are dependent on the dc-bus voltage.

Fig. 16 demonstrates the power loss breakdown of the proposal. It is observed that, at heavy-load condition, conduction loss and copper loss dominate the total power losses. Whereas, for light-load condition, the switching loss and core loss are the dominant losses. Moreover, the variation of v_B significantly affects the conduction loss and inductor copper loss; the variation of v_H significantly impacts the switching loss, transformer core loss and copper loss.

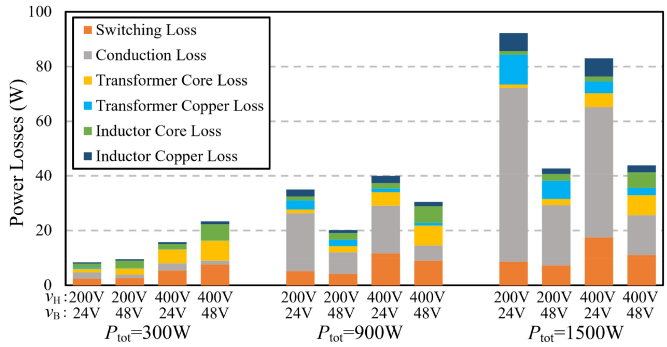

Fig. 16. Power loss breakdown for the proposed CFIBDC.

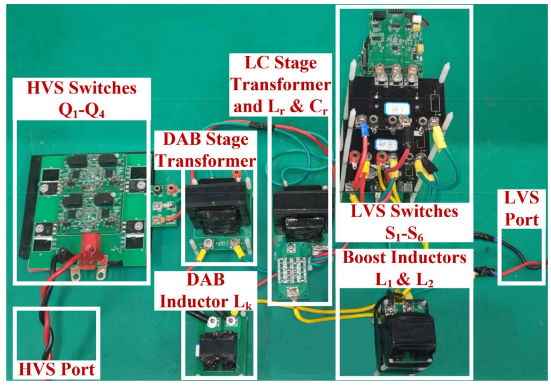

Fig. 17. Photograph of the experimental setup.

Table III compares the proposal with several recently presented CFIBDCs. It can be observed that the proposal maintains relatively high efficiency over twice the input and twice the output voltage ranges without employing a complex control scheme.

V. Experimental Results

To further verify the performance of the proposed converter with its power allocation strategy, an experimental setup rated at 1500 W is constructed (see Fig. 17). As discussed above, the operation principle of the converter remains consistent regardless of the power flow direction. Consequently, the experimental waveforms only demonstrate the power flows from LVS to HVS. The HVS port of the converter is connected to an adjustable resistive load, and the output voltage v_{H} is controlled by the converter in this scenario. Based on the target P_{tot} and v_H, the adjustable load resistance can be determined. The hardware parameters are summarized in Table II.

A. Steady-State Operation

The steady-state operating waveforms of the converter at different IOV and load conditions are shown in Figs. 18 –21. Here,

TABLE III
COMPREHENSIVE COMPARISON BETWEEN DIFFERENT CFIBDCS

Ref.	LVS Port Voltage	HVS Port Voltage	IOV Range	Rated-Load Efficiency over the Entire IOV Range		LVS Battery Current Ripple	Control Complexity	Switches	Voltage Sensors
				Highest	Lowest				
CFDAB [16]	18–28 V (1.55 times)	300 V (1 times)	Medium	97.1% @ 1000 W, v_{in}: 28 V, v_o: 300 V	95.8% @ 1000 W, v_{in}: 18 V, v_o: 300 V	Low	Medium	8	3
DT-CFDAB [17]	18–36 V (2 times)	250–400 V (1.6 times)	Wide	95.7% @ 1000 W, v_{in}: 27 V, v_o: 250 V	90.8% @ 1000 W, v_{in}: 18 V, v_o: 400 V	Low	Medium	8	3
H5-CFDAB [18]	99–121 V (1.22 times)	110 V (1 times)	Narrow	96.9% @ 1100 W, v_{in}: 121 V, v_o: 110 V	96.1% @ 1100 W, v_{in}: 99 V, v_o: 110 V	High	High	9	3
Reconfigurable CFDAB [19]	6–16 V (2.66 times)	180–900 V (5 times)	Ultra-Wide	96.1% @ 2750 W, v_{in}: 500 V, v_o: 14 V	84.1% @ 1100 W, v_{in}: 900 V, v_o: 6 V	Low	High	10	4
Boost+LLC [20]	90–170 V (1.88 times)	375 V (1 times)	Medium	95.4% @ 4800 W, v_{in}: 170 V, v_o: 375 V	93.9% @ 4800 W, v_{in}: 90 V, v_o: 375 V	Low	Low	10[a]	3
Proposal	24–48 V (2 times)	200–400 V (2 times)	Wide	97.3% @ 1500 W, v_{in}: 48 V, v_o: 200 V	94.2% @ 1500 W, v_{in}: 24 V, v_o: 200 V	Low	Low	10	2

Note: [a]Number of switches in case of bidirectional operation.

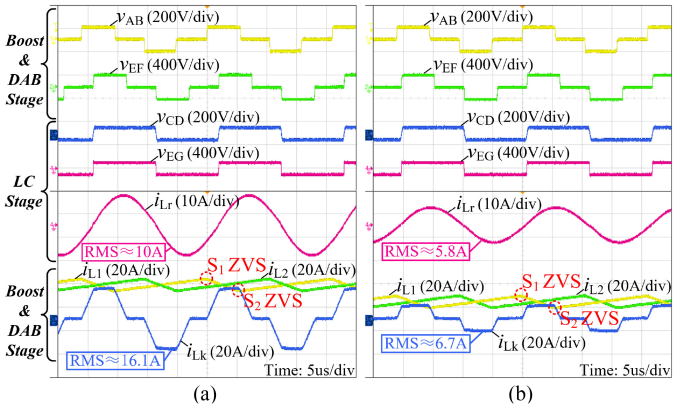

Fig. 18. Steady-state operating waveforms of the proposal at $v_B = 24$ V, $v_H = 200$ V with (a) $P_{tot} = 1500$ W; (b) $P_{tot} = 750$ W.

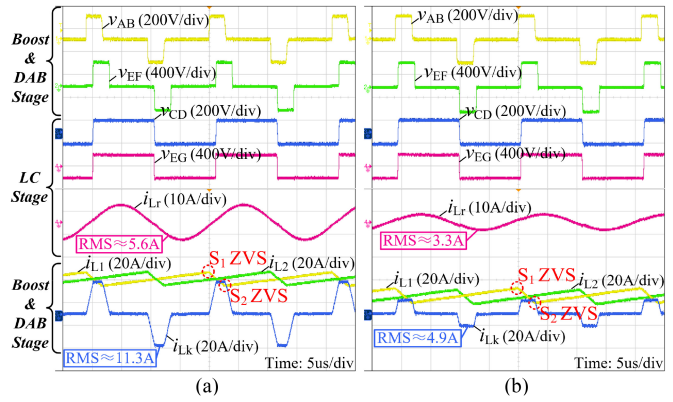

Fig. 19. Steady-state operating waveforms of the proposal at $v_B = 24$ V, $v_H = 400$ V with (a) $P_{tot} = 1500$ W; (b) $P_{tot} = 750$ W.

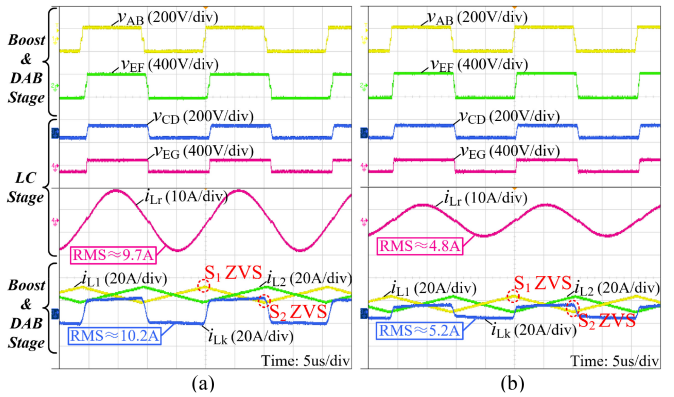

Fig. 20. Steady-state operating waveforms of the proposal at $v_B = 48$ V, $v_H = 200$ V with (a) $P_{tot} = 1500$ W; (b) $P_{tot} = 750$ W.

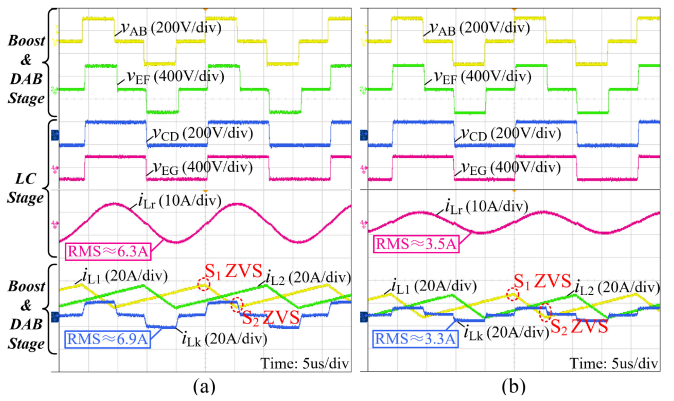

Fig. 21. Steady-state operating waveforms of the proposal at $v_B = 48$ V, $v_H = 400$ V with (a) $P_{tot} = 1500$ W; (b) $P_{tot} = 750$ W.

the voltage and current waveforms are displayed separately in the upper and lower scope windows in one figure.

In Fig. 18, the converter is operating at $v_B = 24$ V, $v_H = 200$ V. The corresponding boost stage duty ratio D_s is close to 0.24, and the DAB stage is operating under mode I. According to the power allocation strategy in Section III, ZVS is required to be prioritized. Hence, the peak value of i_{LK} in Fig. 18 is modulated slightly higher than the valley value of i_{L1} (or i_{L2}), which satisfies the ZVS constraint for S_2 in (11). Meanwhile, the ZVS of S_1 can be achieved by the positive i_{L1} in Fig. 18. The ZVS situations of S_3 and S_4 are consistent with those of S_1 and S_2. For the LC stage switches $S_{5,6}$ and $Q_{1,2}$, soft-switching can be achieved via i_{Lr} and i_{Lk}, respectively, because i_{Lr} is close to zero while i_{Lk} reaches its peak value at their switching moments. For Q_3 and Q_4, soft-switching can also be achieved

because i_{Lk} is close to zero at their switching moments. As can be seen, under the operating condition in Fig. 18, soft-switching of all the switches are guaranteed. It is worth noting that, since v_B is low in Fig. 18, i_{L1} and i_{L2} are relatively high. To facilitate the boost stage ZVS, i_{Lk} is also relatively high. In such a case, the rms value of i_{Lk} is higher than the rms value of i_{Lr}, and the current balancing aim of the power allocation strategy cannot be accommodated.

Fig. 19 shows the operating waveforms of the converter at $v_B = 24$ V, $v_H = 400$ V. The corresponding D_s is close to 0.12, the DAB stage is operating under mode I. Similar to the waveforms in Fig. 18, the peak value of i_{Lk} is modulated higher than the valley value of i_{L1}, thus ensuring boost stage ZVS. And the remaining switches can also be soft-switched, as discussed above. In addition, since v_B is low and $i_{L1,2}$ are high, i_{Lk} that satisfies the ZVS constraint has a higher rms value compared to i_{Lr}. The power allocation strategy prioritizes ZVS over current balancing.

Fig. 20 exhibits the operating waveforms at $v_B = 48$ V, $v_H = 200$ V. The corresponding D_s is close to 0.48, and the DAB stage is operating under mode II. In this case, a relatively high v_B results in relatively low $i_{L1,2}$. And the relatively low $i_{L1,2}$ render the boost stage ZVS easy to be implemented, as illustrated in (11). As a result, current balancing as well as soft-switching can be achieved simultaneously via the power allocation strategy. It can be observed from Fig. 20 that i_{Lk} and i_{Lr} have approximate rms values, which indicates that the current balancing aim is attained. Furthermore, soft-switching is implemented for all the switches.

Fig. 21 shows the operating waveforms of the converter at $v_B = 48$ V, $v_H = 400$ V. The corresponding D_s is close to 0.24, and the DAB stage is operating under mode I. Similar to the operating condition in Fig. 20, $i_{L1,2}$ is relatively low, which makes the ZVS constraint of the power allocation strategy easy to be satisfied. Therefore, current balancing and soft-switching can be ensured simultaneously.

From Figs. 18–21, one can conclude that the experimental results of the converter agree well with the theoretical waveforms (see Fig. 2), which validates the theoretical analysis in Section II. In addition, the soft-switching performance of the converter as well as the measured rms values of i_{Lk} and i_{Lr} at different operating conditions verify the effectiveness of the proposed power allocation strategy.

B. ZVS Verification At Maximum Voltage and Light Load

To validate the worst-case ZVS performance of the proposal, experiments at the maximum voltage and light loads are performed. The HVS output voltage v_H is set at its maximum value, i.e., 400 V (also resulting in the maximum v_L). The maximum v_H and v_L make it most difficult to discharge the junction capacitors on the switches. And the load power is set at 25% rated power (i.e., 375 W) in Fig. 22(a) and (b), and 10% rated power (i.e., 150 W) in Fig. 22(c) and (d). As for the LVS input voltage v_B, since it has no explicit contribution to the worst case, experiments based on different v_B (i.e., $v_B = 24$ and 48 V) are performed. As shown in Fig. 22, even if v_H is at its maximum, S_1 and S_2 can achieve ZVS independent of the load power and v_B. The same holds for S_3 and S_4. As for Q_1 (or Q_2), when $v_B = 24$ V and $P_{\text{tot}} = 375$ W, ZVS can be completely realized due to the relatively high peak value of i_{Lk} [see Fig. 22(a)]. However, when $v_B = 48$ V and $P_{\text{tot}} = 375$ W,

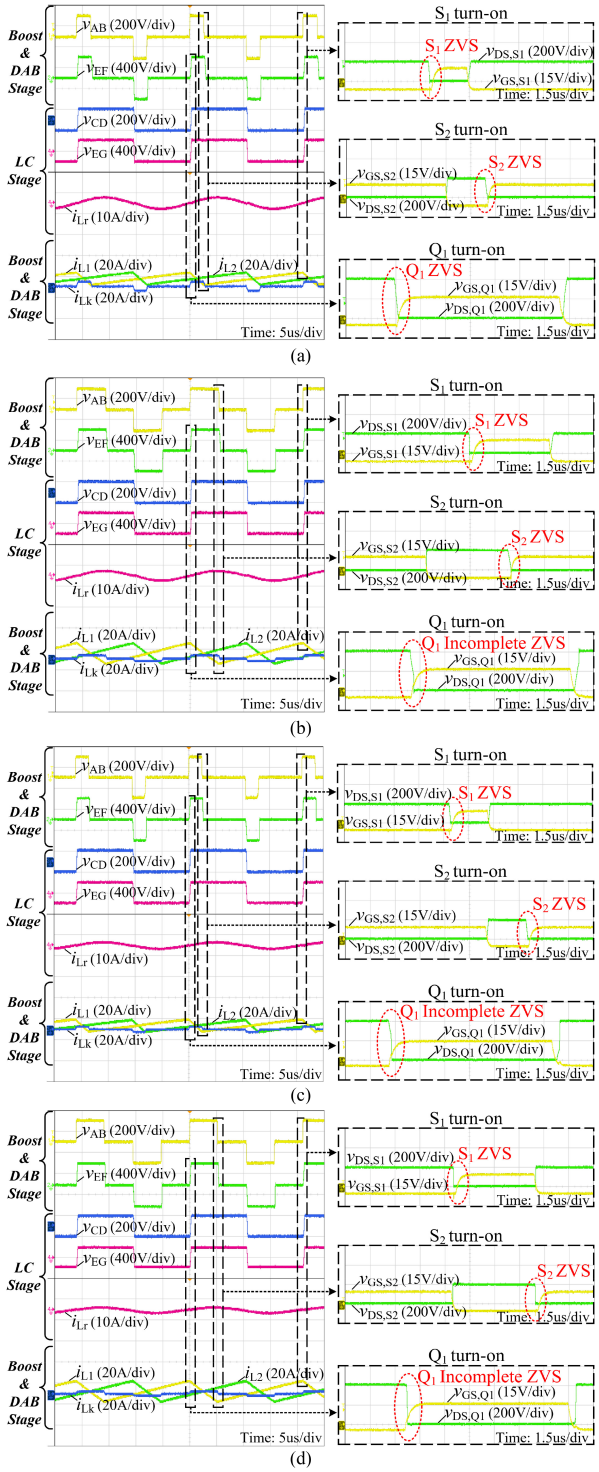

Fig. 22. Operating waveforms of the proposal at maximum v_{H} and light loads when (a) $P_{\text{tot}} = 375$ W, $v_B = 24$ V; (b) $P_{\text{tot}} = 375$ W, $v_B = 48$ V; (c) $P_{\text{tot}} = 150$ W, $v_B = 24$ V; (d) $P_{\text{tot}} = 150$ W, $v_B = 48$ V.

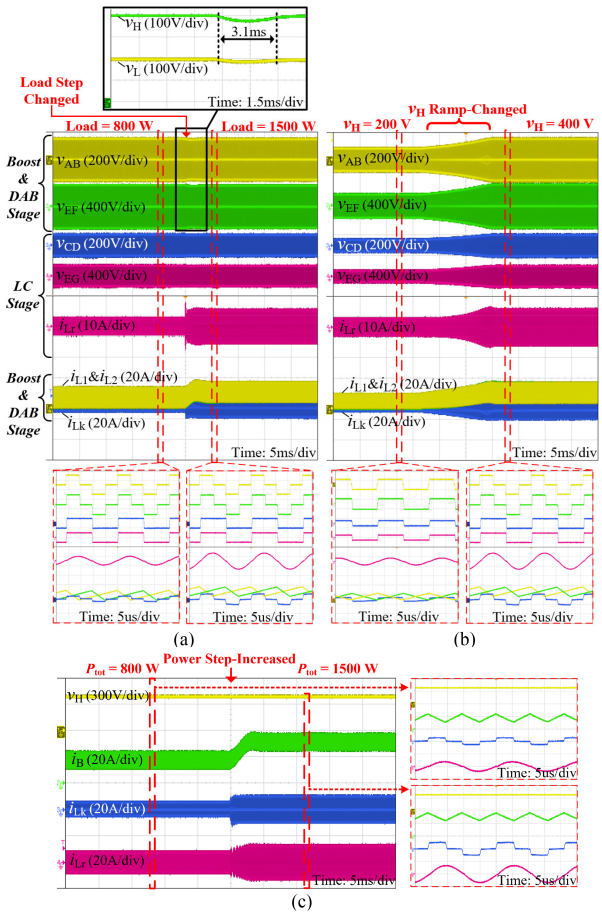

Fig. 23. Dynamical operating waveforms of the proposal. (a) Load step-changed with resistive load. (b) Output voltage ramp-changed. (c) Power regulation when connected to a 400 V voltage source load.

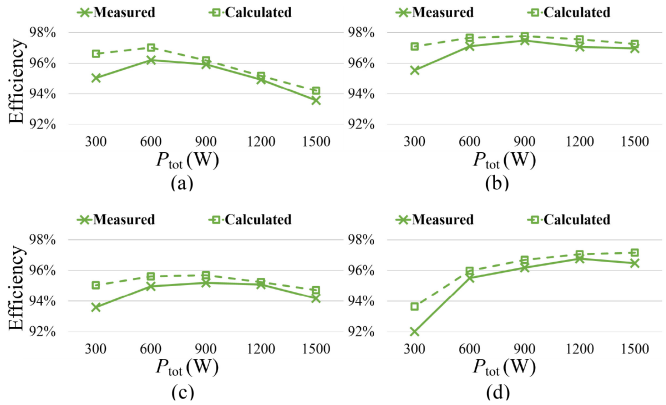

Fig. 24. Measured efficiency curves of the proposal at (a) $v_H = 200$ V, $v_B = 24$ V; (b) $v_H = 200$ V, $v_B = 48$ V; (c) $v_H = 400$ V, $v_B = 24$ V; (d) $v_H = 400$ V, $v_B = 48$ V.

the peak value of i_{Lk} is insufficient to enable complete ZVS for Q_1 [see Fig. 22(b)]. The same holds for situations with very light loads [see Fig. 22(c) and (d)]. The experimental results are consistent with the ZVS analysis in Section IV-B.

C. Dynamical Operation

Fig. 23(a) shows the dynamic waveforms of the converter operating at $v_B = 48$ V, $v_H = 400$ V with a load step from 800 to 1500 W. As can be seen, a step increase in load leads to step rises in i_{L1} and i_{L2}. Meanwhile, under the regulation of the power allocation strategy, i_{Lk} and i_{Lr} rise in appropriate proportions. From the zoomed-in waveforms, it can be observed that soft-switching as well as current balancing are maintained despite the load step-changing. Moreover, as can be observed from the zoomed-in waveforms of v_H and v_L, the load step-changing does not significantly affect the output voltage v_H due to the closed-loop control, and v_L is well-matched with v_H due to the *LC* stage. The settling time for the output voltage v_H is measured to be 3.1 ms.

Fig. 23(b) shows the dynamic waveforms of the converter operating at $v_B = 48$ V with the output voltage v_H ramping up from 200 to 400 V. During this process, the resistive load is fixed at 106 Ω. Accordingly, the load power increases from 377 to 1500 W. As can be seen, as v_H rises, the boost stage duty ratio D_s decreases from 0.48 to 0.24, and the DAB stage operation mode is switched from mode II to mode I. Although the voltage and current states vary considerably during this process, the converter is still able to maintain proper operation while ensuring soft-switching and current balancing.

Fig. 23(c) shows the power regulation process of the proposal when connected to a 400 V voltage source load. In this case, $v_B = 48$ V, $v_H = 400$ V, and P_{tot} is regulated from 800 to 1500 W. As can be seen in Fig. 23(c), v_H is sustained by the voltage source load, and thus remains constant at 400 V. The average value of i_B is step-increased from about 17 to 32 A with a step increase in reference power. And i_{Lk} and i_{Lr} increase synchronously. The proposal is able to operate properly when connected to a voltage source load.

D. Measured Efficiency

To confirm the validity of the efficiency comparison in Fig. 15, the experimental efficiencies of the proposed converter are measured and exhibited in Fig. 24. The calculated efficiencies in Fig. 15 are also depicted in Fig. 24 for comparison. It is admitted that there are some deviations between calculated and measured efficiencies, especially at light loads. This is mainly caused by the stray losses in the experimental setup, the nonideal characteristics of the components, and the estimation errors of the magnetic losses. Nevertheless, the trends of the calculated and measured efficiency curves are consistent. Besides, efficiency estimation errors could also exist in the topologies used for comparison in Fig. 15. It can be asserted that under the same experimental condition, the efficiency superiority of the proposed topology is verified.

VI. Conclusion

In this article, a high-efficiency CFIBDC for wide IOV range operation is proposed and studied. By sharing switches, the proposed topology integrates a CFDAB and an LCRC, and thus

has two power channels with different characteristics. These two channels are able to leverage their own benefits to maintain high efficiency for the converter over wide IOV range via dynamic power allocating. First, the DAB channel enables single-stage power transfer, which guarantees its efficiency when the IOV difference is relatively small. However, when IOV differ significantly, this channel suffers from large conduction losses. Fortunately, since the LCRC channel is independent of IOV, it can share more power for the DAB channel when the IOV difference is large, thus suppressing the conduction losses. Second, the DAB channel can ensure ZVS over wide IOV range, but is subject to large turn-OFF currents. The LCRC channel, on the other hand, can share the current for the DAB channel while enabling ZCS, thus reducing the DAB turn-OFF currents and turn-OFF losses. In addition to the efficiency improvement, the LCRC channel can also simplify the control loop due to its unity voltage gain. Detailed conduction losses analysis, switching performance analysis and efficiency comparisons were carried out to prove the superiority of the proposal. Total device capacity was calculated to demonstrate that the superiority of the proposal does not require excessive costs. Experimental results validate the effectiveness of the proposed converter and the power allocation strategy.

Appendix A
Design Considerations for Hardware Parameters

This Appendix illustrates the design considerations for critical hardware parameters in Table II. The critical hardware parameters include: *LC* stage resonant inductance L_r and capacitance C_r; DAB stage leakage inductance L_k; boost stage inductances L_1 and L_2. As for the dc-bus capacitances C_1–C_4, they only need to be sufficient to suppress excessive dc-bus voltage fluctuations. Since the parameter design is not the major concern of this paper, this design guideline only guarantees the proper operation of the proposal instead of optimizing the performance.

A. Design Consideration of L_r and C_r

Since the *LC* stage of the proposal simply operates at series resonant state, the resonant tank parameters L_r and C_r only need to satisfy

$$\frac{1}{2\pi\sqrt{L_rC_r}} = f_s. \tag{23}$$

In low voltage scenarios, C_r can be designed larger in order to make L_r smaller. A smaller L_r is easier to be integrated into the transformer as leakage inductance.

B. Design Consideration of L_k

In this article, L_k is designed with three considerations:

First, to guarantee that i_{Lk} is sufficient to facilitate boost stage ZVS at the worst operating conditions, L_k cannot be overly large. As shown in (13), if L_k is overly large, the left-hand-side of (13) will be overly small, and the inequality may not be realizable at the worst operating conditions. The restriction for L_k can be derived from (13), as follows:

$$L_k < \frac{v_L T\varphi}{\frac{P_{\text{tot}}}{2v_B} - \frac{v_B(1-D_s)T}{L_1}}. \tag{24}$$

As can be seen, the not-yet-designed parameter L_1 is involved in the restriction for L_k. To decouple the parameter design, we assume that L_1 is at its worst value for boost stage ZVS realization, that is, L_1 is infinity. Accordingly, the maximum value of L_k has to satisfy the following:

$$L_{k,\max} < \min\left\{\frac{v_B v_L T_s \varphi_{\text{upper}}}{P_{\text{tot}}}\right\}. \tag{25}$$

where φ_{upper} is the upper limit of φ. When $D_s > 0.25$, the upper limit of φ is 0.5, otherwise, $\varphi_{\text{upper}} = 2\,D_s = 2v_B/v_L$. Finally, to guarantee the realizability of the boost stage ZVS at the worst operating conditions, L_k has to satisfy

$$L_{k,\max} < \frac{2{v_{B,\min}}^2 T_s}{P_{\text{tot,max}}}. \tag{26}$$

Second, to guarantee the ZVS range of HVS switches at light loads, L_k cannot be overly small. According to Section IV-B, i_{Lk} determines the ZVS performances of HVS switches $Q_{1,2}$. If L_k is overly small, the energy on L_k will be too low to fully discharge the junction capacitor on Q_1 (or Q_2) at light loads. If the junction capacitor on Q_1 (or Q_2) can be fully discharged by i_{Lk}, the following constraint [28] must be satisfied:

$$\frac{1}{2}L_k{i_{Lk}(t_1)}^2 > C_{\text{oss},Q1}{v_H}^2. \tag{27}$$

where $i_{Lk}(t_1)$ is the peak value of i_{Lk} (see Fig. 2), and $\text{C}_{\text{oss,Q1}}$ is the junction capacitor on Q_1. At light loads, i_{Lk} can be approximated as a three-level square wave due to the low DAB stage phase-shift ratio φ. Then, the peak value of i_{Lk} can be approximately calculated from the power, as follows:

$$i_{Lk,\text{peak}} \approx \frac{P_{\text{DAB}}}{2D_s v_L}. \tag{28}$$

Thereafter, by combining (27), (28), and (9), the L_k restriction that enables full discharge of Q_1 junction capacitor is derived, as follows:

$$L_k > \frac{8{v_B}^2{v_H}^2 C_{\text{oss},Q1}}{K^2{P_{\text{tot}}}^2} \tag{29}$$

where K is the DAB stage power proportion under current balancing strategy, and $K = K_{LC}/(K_{\text{DAB}} + K_{LC})$. As indicated in (29), the lighter the load, the larger L_k is required to fully discharge the junction capacitor. It is impossible to ensure full discharge of junction capacitor over the entire load range. In this article, we guarantee the full ZVS of $Q_{1,2}$ under at least the load conditions of $P_{\text{tot}} > P_{\text{tot,max}}/3$ in the worst case ($v_B = 48$ V, $v_H = 400$ V).

Third, to reduce the DAB stage current i_{Lk}, a smaller L_k is preferable. For DAB-based converter, large leakage inductor leads to high circulating power. Therefore, L_k should be designed smaller within the acceptable range.

TABLE IV
CRITICAL PARAMETERS OF MAGNETIC COMPONENTS

Description	Core	Core Material	LVS Winding	HVS Winding
DAB Stage Transformer	FERROXCUBE E55/28/25	3C90	#32 AWG × 204 11 turns	#32 AWG × 102 22 turns
LC Stage Transformer	FERROXCUBE E42/21/20	3C90	#32 AWG × 142 10 turns	#32 AWG × 71 20 turns
Boost Stage Inductors	MAGNETICS 77074A7	Kool Mμ	#11 AWG × 3 27 turns	

C. Design Consideration of L_1 and L_2

Since L_1 and L_2 share the same value, only the parameter design of L_1 is illustrated here. In this paper, L_1 is designed based on general engineering experience. To avoid excessive boost stage current ripple as well as excessive inductor value, the maximum boost stage input current ripple is set to 20% at full load. Then, we have

$$\frac{v_B(1-2D_s)T_s}{2L_1} \leq \frac{P_{\text{tot,max}}}{v_B} * 20\%. \tag{30}$$

Since $D_\text{s} = nv_\text{B}/v_\text{H}$, the restriction for L_1 can be deduced as follows:

$$L_{1,\text{min}} \geq \max\left\{\frac{{v_B}^2(v_H - 2nv_B)T_s}{2v_H P_{\text{tot,max}} * 20\%}\right\}. \tag{31}$$

The right-hand-side of (31) reaches its maximum at $v_B = 48$ V, $v_H = 400$ V. And L_1 is finally designed at its lower limit shown in (31).

APPENDIX B
DESIGN OVERVIEW OF MAGNETIC COMPONENTS

This Appendix provides the critical parameters of magnetic components for power loss investigation. The parameters are designed based on the methodology presented in [29] and [30], and the power losses are estimated via the approaches provided in [2] and [30]. The design results are shown in Table IV.

REFERENCES

[1] C. Wang, P. Zheng, and J. Bauman, "A review of electric vehicle auxiliary power modules: Challenges, topologies, and future trends," *IEEE Trans. Power Electron.*, vol. 38, no. 9, pp. 11233–11244, Sep. 2023.

[2] X. Pan, H. Li, Y. Liu, T. Zhao, C. Ju, and A. K. Rathore, "An overview and comprehensive comparative evaluation of current-fed-isolated-bidirectional DC/DC converter," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2737–2763, Mar. 2020.

[3] F. Z. Peng, H. Li, G.-J. Su, and J. S. Lawler, "A new ZVS bidirectional DC-DC converter for fuel cell and battery application," *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 54–65, Jan. 2004.

[4] A. K. Rathore, A. K. S. Bhat, and R. Oruganti, "Analysis, design and experimental results of wide range ZVS active-clamped L-L type current-fed DC/DC converter for fuel cells to utility interface," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 473–485, Jan. 2012.

[5] H. Xiao and S. Xie, "A ZVS bidirectional DC–DC converter with phase-shift plus PWM control scheme," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 813–823, Mar. 2008.

[6] J. Xu, Y. Sun, G. Xu, X. Liang, and M. Su, "Current-fed LC series resonant converter with load-independent voltage-gain characteristics for wide voltage range applications," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 11509–11522, Oct. 2021.

[7] U. R. Prasanna, A. K. Rathore, and S. K. Mazumder, "Novel zero-current-switching current-fed half-bridge isolated DC/DC converter for fuel-cell-based applications," *IEEE Trans. Ind. Appl.*, vol. 49, no. 4, pp. 1658–1668, Jul./Aug. 2013.

[8] P. Xuewei and A. K. Rathore, "Novel bidirectional snubberless naturally commutated soft-switching current-fed full-bridge isolated DC/DC converter for fuel cell vehicles," *IEEE Trans. Ind. Electron.*, vol. 61, no. 5, pp. 2307–2315, May 2014.

[9] J.-Y. Lee and H.-J. Chae, "6.6-kW onboard charger design using DCM PFC converter with harmonic modulation technique and two-stage DC/DC converter," *IEEE Trans. Power Electron.*, vol. 61, no. 3, pp. 1243–1252, Mar. 2014.

[10] Q. Zhu, L. Wang, A. Q. Huang, K. Booth, and L. Zhang, "7.2-kV single-stage solid-state transformer based on the current-fed series resonant converter and 15-kV SiC mosfets," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1099–1112, Feb. 2019.

[11] M. Soleimanifard and A. Y. Varjani, "A bidirectional buck-boost converter in cascade with a dual active bridge converter to increase the maximum input and output currents and extend zero voltage switching range," in *Proc. 11th Power Electron., Drive Syst., Technol. Conf.*, 2020, pp. 1–6.

[12] B. N. Alajmi, I. Abdelsalam, M. I. Marei, and N. A. Ahmed, "Two stage single-phase EV on-board charger based on interleaved cascaded non-inverting buck-boost converter," in *Proc. IEEE Conf. Power Electron. Renewable Energy*, 2023, pp. 1–6.

[13] D. Sha, F. You, and X. Wang, "A high-efficiency current-fed semi-dual-active bridge DC–DC converter for low input voltage applications," *IEEE Trans. Ind. Electron.*, vol. 63, no. 4, pp. 2155–2164, Apr. 2016.

[14] J. Guo et al., "Design considerations for PPS controlled current-fed DAB converter to achieve full load range ZVS and low inductor current stress," *IEEE Trans. Ind. Appl.*, vol. 57, no. 6, pp. 6261–6276, Nov./Dec. 2021.

[15] Z. Guo, K. Sun, T.-F. Wu, and C. Li, "An improved modulation scheme of current-fed bidirectional DC–DC converters for loss reduction," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 4441–4457, May 2018.

[16] D. Sha, X. Wang, and D. Chen, "High-efficiency current-fed dual active bridge DC–DC converter with ZVS achievement throughout full range of load using optimized switching patterns," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1347–1357, Feb. 2018.

[17] D. Sha, J. Zhang, and K. Liu, "Leakage inductor current peak optimization for dual-transformer current-fed dual active bridge DC–DC converter with wide input and output voltage range," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 6012–6024, Jun. 2020.

[18] T. Chaudhury and D. Kastha, "H5-CFDAB: A current-fed dual-active-bridge converter for application in modular DC solid-state transformer," *IEEE Trans. Power Electron.*, vol. 38, no. 6, pp. 7271–7284, Jun. 2023.

[19] L. Zhu, H. Bai, and A. Brown, "Model and control of a current-fed dual active bridge based ultrawide-voltage-range auxiliary power module for 400 V/800 V electric vehicles," *IEEE Trans. Power Electron.*, vol. 39, no. 3, pp. 3263–3276, Mar. 2024.

[20] V. K. Goyal and A. Shukla, "Two-stage hybrid isolated DC–DC boost converter for high power and wide input voltage range applications," *IEEE Trans. Ind. Electron.*, vol. 69, no. 7, pp. 6751–6763, Jul. 2022.

[21] J. Wen et al., "An iterative-based dead-time compensation method for integrated interleaved boost-LLC converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2023, pp. 3341–3348.

[22] L. Zhu, H. Bai, A. Brown, and M. McAmmond, "Design a 400 V–12 V 6 kW bidirectional auxiliary power module for electric or autonomous vehicles with fast precharge dynamics and zero dc-bias current," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 5323–5335, May 2021.

[23] G. Xu, Y. Lin, L. Yuan, W. Xiong, and Y. Sun, "Dead-time optimization and magnetizing current design for a current-fed dual active bridge DC–DC converter to secure full load range ZVS in wide voltage range," *IEEE Trans. Transp. Electrific.*, vol. 9, no. 2, pp. 2164–2176, Jun. 2023.

[24] Y. Shi, R. Li, Y. Xue, and H. Li, "Optimized operation of current-fed dual active bridge DC–DC converter for PV applications," *IEEE Trans. Ind. Electron.*, vol. 62, no. 11, pp. 6986–6995, Nov. 2015.

[25] D. Sha, J. Zhang, X. Wang, and W. Yuan, "Dynamic response improvements of parallel-connected bidirectional DC–DC converters for electrical drive powered by low-voltage battery employing optimized feedforward control," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7783–7794, Oct. 2017.

[26] S. Mukherjee, A. Kumar, and S. Chakraborty, "Comparison of DAB and LLC DC–DC converters in high-step-down fixed-conversion-ratio (DCX) applications," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 4383–4398, Apr. 2021.

[27] T. Guillod, D. Rothmund, and J. W. Kolar, "Active magnetizing current splitting ZVS modulation of a 7 kV/400 V DC transformer," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1293–1305, Feb. 2020.
[28] M. Kasper, R. M. Burkart, G. Deboy, and J. W. Kolar, "ZVS of power MOSFETs revisited," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8063–8067, Dec. 2016.
[29] J. Xue, F. Wang, D. Boroyevich, and Z. Shen, "Single-phase vs. three-phase high density power transformers," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2010, pp. 4368–4375.
[30] MAGNETICS, 2018. [Online]. Available: https://www.mag-inc.com/Media/Magnetics/File-Library/Product%20Literature/Powder%20Core%20Literature/Magnetics-Powder-Core-Catalog-2020.pdf

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