Three-Phase *LLCL* Bidirectional Resonant Converter With Wide Output Voltage Range

Qinglin Zhao, Tianrui Wang, Yi Zheng, Hao Ding, *Member, IEEE*, and Deyu Wang, *Member, IEEE*

***Abstract*—This article proposes a three-phase *LLCL* bidirectional resonant dc–dc converter with wide voltage range in both ports. Combined with the interleaving technique, the converter can effectively reduce the current ripples of input and output ports, and the size of filter capacitors can be extremely reduced. Meanwhile, with three power transmission paths and the ability of self-current sharing, the converter has a larger power capacity and higher power density compared with conventional *LLC* converters. The operation principles and the detailed design method are presented in this article. Finally, a 3.3-kW prototype, which interfaces the dc bus and battery, is built to validate the effectiveness and applicability of the proposed converter. During the whole time, the bus voltage is fixed at 400 V. In forward mode, the output voltage range is 250–420 V, and the peak efficiency of up to 97.8%. In backward mode, the inverter side voltage range is 300–420 V, and the peak efficiency of up to 98.0%.**

***Index Terms*—Bidirectional dc–dc converter (BDC), resonant tank, self-current sharing, three-phase interleaved parallel, wide gain range.**

I. Introduction

With the rapid development of distributed renewable energy generation, the design of bidirectional dc-dc converters (BDCs) with wide voltage gain, high efficiency, and high power density has become a research hotspot in the fields of electric vehicles (EVs), microgrids, energy storage systems (ESSs), uninterruptible power supplies (UPSs) [1], [2], [3], [4], [5], etc. Among them, the isolated bidirectional dc-dc converter (IBDC) can connect dc bus of different voltage levels with energy storage devices (ESD), playing a significant role in voltage variation, isolation, and two-way flow of energy [6], [7], [8].

Bidirectional isolated LLC resonant converters with high efficiency and simple topology have been widely used [9], [10]. However, it is equivalent to an *LC* resonant network in backward mode, thus the voltage gain is less than 1, which cannot meet the requirement of a wide voltage range [11]. To address the issue, researchers attempt to conduct research from two aspects: improving the modulation strategy or resonant topology of the converter. For the first idea, in [12], by combining the delay-time control and pulse frequency modulation (PFM), the series resonant converter is regulated with boost gain capability. Nevertheless, the delay time is generated by a zero-crossing detection circuit, which makes the control more complicated and increases the converter cost. Besides, the system is easily affected by high *dv/dt* or *di/dt*. In [13], the proposed converter adopts PFM control and phase delay control, which can help the backward mode obtain high voltage gain. However, the efficiency is reduced compared with the conventional *LLC* converter. In [14] and [15], fixed-frequency pulsewidth modulation (PWM) control is employed to regulate the output voltage in a series resonant converter, whose switching frequency is fixed at the resonant frequency. Thus, the design of magnetic components can be simplified. Nevertheless, auxiliary inductors are required in the series resonant converter to realize zero-voltage switching (ZVS) of all the switches in the whole load range.

Alternatively, improving the resonant topology of *LLC* converter to gain bi-directional wide voltage regulation capability is also widely studied. In [16], based on the conventional LLC converter, the *CLLC* resonant converter is studied by placing an additional resonant capacitor on the secondary side, which make the converter possess buck/boost operation capability in two directions [17]. Nevertheless, the voltage gain curve of the converter is nonmonotonic in the inductive operating region and heavy load, which restricts the operation voltage range of the converter and complicates the iterative optimization process for parameter design [18]. In [19], a set of *LC* resonant network is introduced on the secondary side of the traditional *LLC* converter, the symmetrical *CLLLC* bidirectional resonant converter is studied, which has completely consistent operating characteristics in both directions. Besides, the voltage gain characteristics and parameter design of the converter are similar to the traditional *LLC* resonant converter. Nevertheless, excessive resonant elements increase the conduction losses and make the parameter design more complicated. Moreover, the voltage gain of the *CLLLC* resonant network decreases slowly when the working frequency is greater than resonant frequency, thus it requires a wider frequency range to achieve low voltage output [20]. In [21], an *L-LLC* resonant converter is studied by paralleling an auxiliary inductor to the primary side of the

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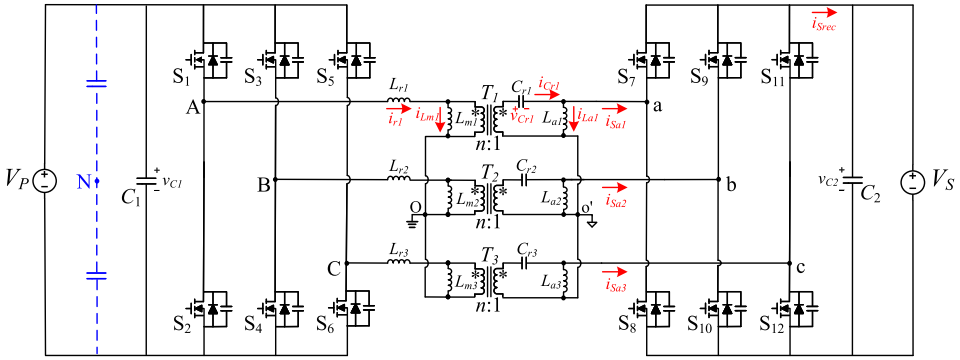

Fig. 1. Topology of the proposed three-phase *LLCL* resonant converter.

traditional *LLC* converter. However, the addition of the auxiliary inductor will increase the power losses, and reduce the efficiency of the converter.

Given the benefits and disadvantages of the above-mentioned circuit structure, the *LLCL* resonant topology is proposed in [22]. On the basis of traditional *LLC* converter, it places the resonant capacitor to the secondary side and parallels an auxiliary inductor, which makes the converter possess excellent bidirectional voltage gain adjustment ability with fewer resonant elements. Compared with *CLLC* converter, *LLCL* resonant converter only has one peak value in the both modes voltage gain curves, which extremely reduces the design difficulty. However, as a single-phase converter, it still has the problem of the large current ripple. For solving the problem of the single-phase converter, a two-phase interleaved *LLC* resonant converter is studied in [23] and [24]. Compared with single-phase converters, the power capacity of the converter increases, while the current stress and current ripple reduce. Nevertheless, the inductance or capacitance of the resonant element in the *LLC* resonant converter often has a tolerance of $\pm 5\%$ in the mass production process, which will cause a serious imbalance in the power of each phase, and reduce the efficiency and reliability of the converter.

To further increase the power capacity of the converter and make the converter possess self-current sharing ability, a three-phase interleaved parallel *LLC* resonant converter is studied in [25] and [26]. Zhou et al.[25] combined the *CLLLC* topology and three-phase structure, which have many advantages over single-phase and two-phase structures at high power levels, such as better loss distribution and easier thermal management. In [27] and [28], the voltage gain range of the three-phase resonant converter is expanded by using the phase shedding strategy. Nevertheless, in the low-gain mode, the converter is still working in a single-phase structure, and the size of the output filter should be designed in a single-phase mode [28]. Therefore, the advantages of the three-phase structure cannot be exerted completely.

In this article, a modified three-phase *LLCL* bidirectional resonant converter is proposed. It inherits the advantages of the network in [22], and the improved three-phase interleaved structure enables the circuit to achieve high-power energy transfer over a wide voltage range in both directions. Furthermore, the converter adopts simple PFM control, and the rectifier side's MOSFETs can achieve ZVS in the whole operating time, thereby ensuring the low control costs and high efficiency of the proposed converter.

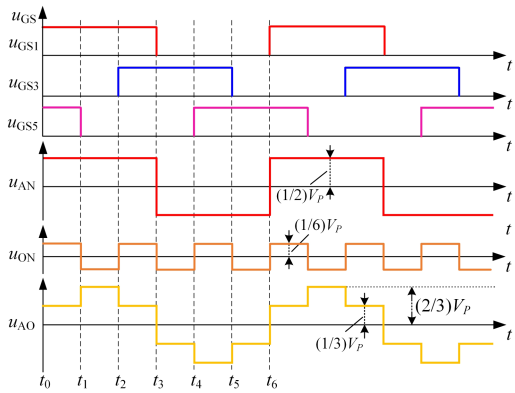

Fig. 2. Derivation process of the waveform u_{AO} in forward mode.

II. Operation Principle

The schematic of the proposed three-phase *LLCL* bidirectional resonant converter is shown in Fig. 1. The three switching legs positioned at the side of the energy input port, phase shifted by 120° and the upper and lower switches of the same leg complementary conduction with 50% duty ratio, act as an inverter, while MOSFETs at the other side, used as diodes without driving signal, act as a rectifier. In the converter, the voltages of two dc ports are defined as V_P and V_S. Assuming that V_P and V_S are connected to the dc bus and the energy storage devices, respectively. If power is transferred from V_P to V_S, the converter works in forward mode, otherwise it works in backward mode.

The converter has three resonant tanks, which have the same parameters, that is, $L_{r1} = L_{r2} = L_{r3} = L_r$, $C_{r1} = C_{r2} = C_{r3} = C_r$, $L_{m1} = L_{m2} = L_{m3} = L_m$, $L_{a1} = L_{a2} = L_{a3} = L_a$, and turns ratio $n_1 = n_2 = n_3 = n$. Therefore, the converter can be divided into three independent phases, which have a similar working process. In this section, only the working process of the phase-A is analyzed in detail.

Fig. 2 shows the derivation process of u_{AO} in forward mode, where *N* is the imaginary midpoint at two ends of the dc voltage source V_P. Fig. 3(a) shows the small current ripple principle of

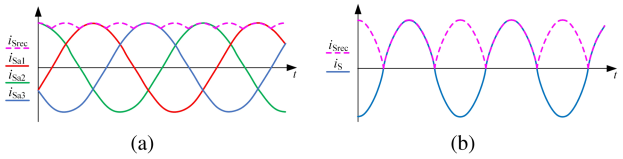

Fig. 3. Theoretical output current waveforms($f_s = f_r$). (a) The proposed three-phase *LLCL* converter. (b) The traditional single-phase *LLC* converter.

the converter. The current i_{Sa1}, i_{Sa2}, i_{Sa3} are interleaved by 120°, and after rectification, the majority of the ripple currents in each phase cancel each other out, leading to a significant reduction of overall current ripple compared with traditional *LLC* resonant converter presented in Fig. 3(b).

A. Analysis of the Key Waveforms

Fig. 4 shows that when $f_s \neq f_r$, u_{AO} and $u_{ao'}$ will experience phase shift. When $f_s < f_r$, the $u_{ao'}$ phase lags u_{AO} and the circuit network is intuitive. When $f_s > f_r$, the $u_{ao'}$ phase leads u_{AO} and the circuit network is capacitive. In addition, when $f_s \neq f_r$, the resonant current i_{r1} is not pure sinusoidal, which will show some steps. When $f_s < f_r$, the working process of the converter is the most complicated, so only this process is analyzed, which can be summarized into two aspects. On the one hand, when $f_s < f_r$, the current is discontinuous. In $[t_2, t_3]$, the energy is no longer transmitted to the secondary side, thus forming a step. On the other hand, step waves u_{AO} and $u_{ao'}$ jump seven times in half-cycle, which affects the sine of the resonant current. Whenever they jump once, the resonant current waveform will experience a certain amount of jitter. Therefore, different degrees of steps are formed in i_{r1}. The similar analysis occurs in Fig. 6, so it will not be detailed here.

B. Working Process of Forward Mode

Fig. 4 shows the key waveforms of the converter operating under three switching frequencies in forward mode. According to Fig. 4, S_1 and S_2 complement each other, and the duty cycle of S_1 and S_2 is 50%. When $f_s < f_r$, the working process of the converter is the most complicated, so only this process is analyzed, which includes six working stages. Half-cycle equivalent circuit of phase-A in forward mode when $f_s < f_r$ is shown in Fig. 5, where the positive directions of voltage and current are also marked.

State I [t_0, t_1] [see Fig. 5(a)]: Before t_0, S_2 is turned ON. The resonant current i_{r1} is negative. At t_0, S_2 is turned OFF, since the current i_{r1} cannot be mutated, i_{r1} turns to flow through the parasitic capacitors of S_1 and S_2. Thus, the parasitic capacitor of S_2 is charged, while the one of S_1 is discharged to zero. Since the drain-source voltage of S_1 drops to zero, the current i_{r1} flows through the body diodes of S_1, which creates the ZVS condition for S_1.

State II [t_1, t_2] [see Fig. 5(b)]: At t_1, S_1 is turned ON under ZVS condition, after resonant current i_{r1} gradually changes from negative to positive, and flows into the resonant network through S_1. When resonant current i_{r1} is greater than excitation current i_{Lm1}, the energy begins to transfer to the secondary side. Resonant capacitor current i_{Cr1} is greater than auxiliary inductor current i_{La1}. Thus, current i_{Sa1} is positive and flows through the body diode of S_7, the energy is transferred to the load. The auxiliary inductor L_{a1} is clamped by the resonant tank output voltage $u_{ao'}$. Therefore, during t_1 to t_2, the resonant elements only include L_{r1}, L_{m1}, and C_{r1}, whose resonant frequency is defined as the main resonant frequency. This state is the main power transmission stage of the converter in forward mode.

State III [t_2, t_3] [see Fig. 5(c)]: At t_2, i_{Cr1} is equal to i_{La1}, i_{sa} decrease to zero. Thus, the current i_{D7} decreases to zero, achieving zero-current switching (ZCS) turn OFF for the body diode of S_7. The energy input side of the converter no longer transmits energy to the secondary side, and L_{a1} is no longer clamped by the output voltage $u_{ao'}$ of the resonant tank and participates in the resonant process until S_1 is turned OFF at t_3. After t_3, the converter will enter the second half of the cycle, which works similarly to the above process, so it will not be detailed here.

C. Working Process of Backward Mode

The same as the forward mode, there are six working stages in backward mode. Fig. 6 shows the key waveforms of the converter operating under three switching frequencies in backward mode. When $f_s < f_r$, the half-cycle equivalent circuit of phase-A in backward mode is shown in Fig. 7, where the positive directions of voltage and current are also marked.

State I [t_0, t_1] [see Fig. 7(a)]: At t_0, S_7 is turned OFF. The current i_{Sa1} charges the parasitic capacitor of S_8 while discharging the one of S_7 to zero. When the voltage across C_{S7} drops to zero, the current i_{Sa1} flows through the body diode of S_7, creating the condition for ZVS switching. For a more intuitive analysis, the i_{Cr1} expansion by $1/n$ times is equivalent to i_{Cr1_H} on the primary side, which can be decomposed to i_{r1} and i_{Lm1}.

State II [t_1, t_2] [see Fig. 7(b)]: At t_1, S_7 is turned ON under ZVS condition, after equivalent current i_{Cr1_H} gradually changes from negative to positive, and flows into the resonant network through S_7. The current i_{Cr1_H} is greater than the resonant capacitor current i_{Lm1}, and the energy is transferred to the load through the body diode of S_1. The auxiliary inductor L_{a1} is clamped by the input voltage $u_{ao'}$ of the resonant tank and does not participate in resonance in the whole operation time. Therefore, from t_1 to t_2, the resonant frequency of the backward mode is the main resonant frequency, which is similar to the forward mode. This state is the main power transmission stage of the converter in backward mode.

State III [t_2, t_3] [see Fig. 7(c)]: At t_2, i_{Cr1_H} is equal to i_{Lm1}, i_{r1} decreases to zero, and the current flowing into the diode of S_1 drops to zero, realizing ZCS turn OFF for the body diode of S_1. The energy input side of the converter no longer transmits energy to the other side until S_7 is turned OFF at t_3. After t_3, the converter will enter the second half of the cycle, which works similarly to the above process, so it will not be detailed here.

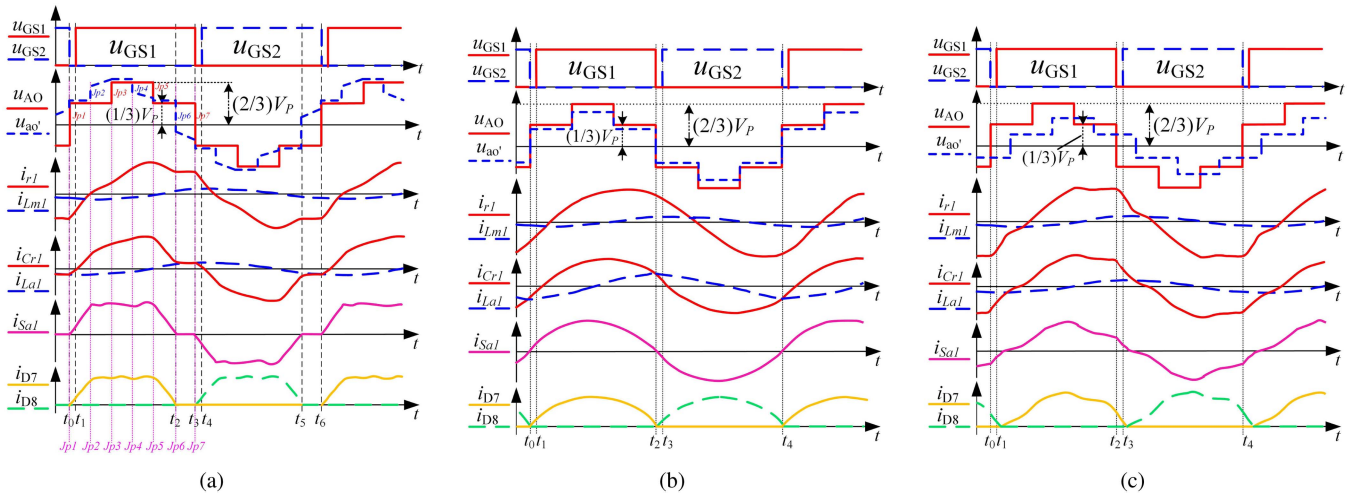

Fig. 4. Phase-A key operation waveforms of the proposed *LLCL* resonant converter in forward mode. (a) $f_s < f_r$. (b) $f_s = f_r$. (c) $f_s > f_r$.

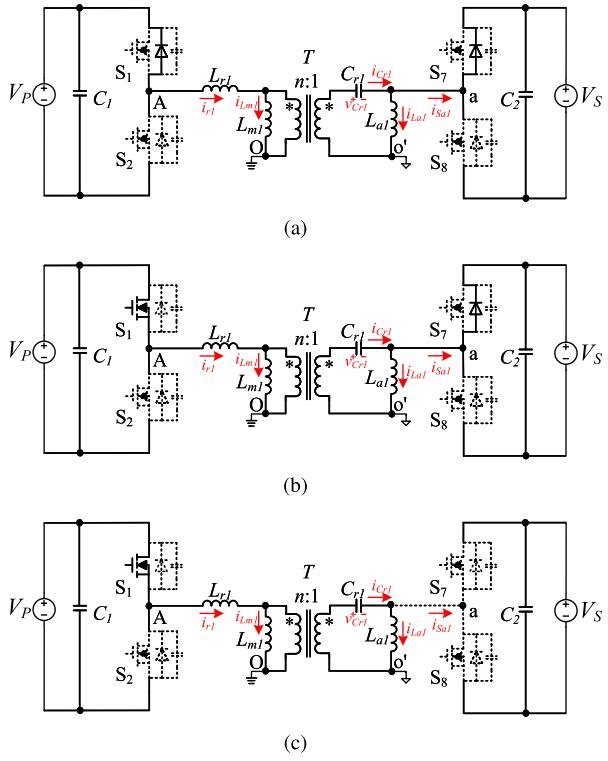

Fig. 5. Phase-A operation states for half of switching period in forward mode. (a) State I $[t_0, t_1]$. (b) State II $[t_1, t_2]$. (c) State III $[t_2, t_3]$.

III. Modeling and Gain Analysis

A. Analysis of the Equivalent Circuit Model

In the converter, the resonant parameters of the three resonant tanks are the same, so the impedance of each phase is equal. Thus, the converter's gain characteristics can be analyzed from a single-phase resonant network.

Assuming that all components of the converter are ideal and the switching frequency is equal to the resonant frequency. At this time, the resonant network has zero impedance to the fundamental component and exhibits high impedance to the harmonic component, thus the resonant current waveform is approximately sinusoidal. The single-phase circuit is analyzed by the fundamental harmonic approximation (FHA).

Based on the Fourier series analysis, the phase voltage $u_{\mathrm{AO}}(t)$ can be expressed as

$$u_{\mathrm{AO}}(t) = \frac{2U_{\mathrm{p}}}{\pi}\sin\omega t + \frac{2U_{\mathrm{p}}}{5\pi}\sin 5\omega t + \cdots \tag{1}$$

It can be seen from (1) that the amplitude of the fundamental component of $u_{\mathrm{AO}}(\mathrm{t})$ is $(2U_{\mathrm{P}})/\pi$. Similarly, the amplitude of the fundamental component of $u_{\mathrm{ao}}(\mathrm{t})$ is $(2U_{\mathrm{S}})/\pi$, whose effective value can be expressed as follows:

$$U_{\mathrm{ao1(rms)}} = \frac{(2U_{\mathrm{s}})/\pi}{\sqrt{2}} = (\sqrt{2}U_{\mathrm{s}})/\pi. \tag{2}$$

As the power transmitted by each phase is the same, each phase transfers one-third of the total power

$$\frac{U_{\mathrm{s}}^2}{3R_{\mathrm{s}}} = \frac{U_{\mathrm{ao1(rms)}}^2}{R_{\mathrm{e}}} \tag{3}$$

where R_{s} is the equivalent resistance of the secondary side load in forward mode. The equivalent ac resistance R_{e} of the secondary side can be obtained from (3).

Therefore, the equivalent ac resistance $R_{\mathrm{eq\_s}}$ can be obtained by converting R_{e} to the primary side

$$R_{\mathrm{eq\_s}} = n^2 \cdot \frac{3\,U_{\mathrm{ao1(rms)}}^2 R_{\mathrm{s}}}{{U_{\mathrm{s}}}^2} = \frac{6R_{\mathrm{s}}n^2}{\pi^2} \tag{4}$$

Similar to the process above, the equivalent ac resistance $R_{\mathrm{eq\_p}}$ in backward mode can be derived as

$$R_{\mathrm{eq\_p}} = \frac{6R_{\mathrm{p}}}{\pi^2}. \tag{5}$$

Based on the above analysis, the single-phase equivalent circuit of the proposed converter in both modes can be obtained, as shown in Fig. 8.

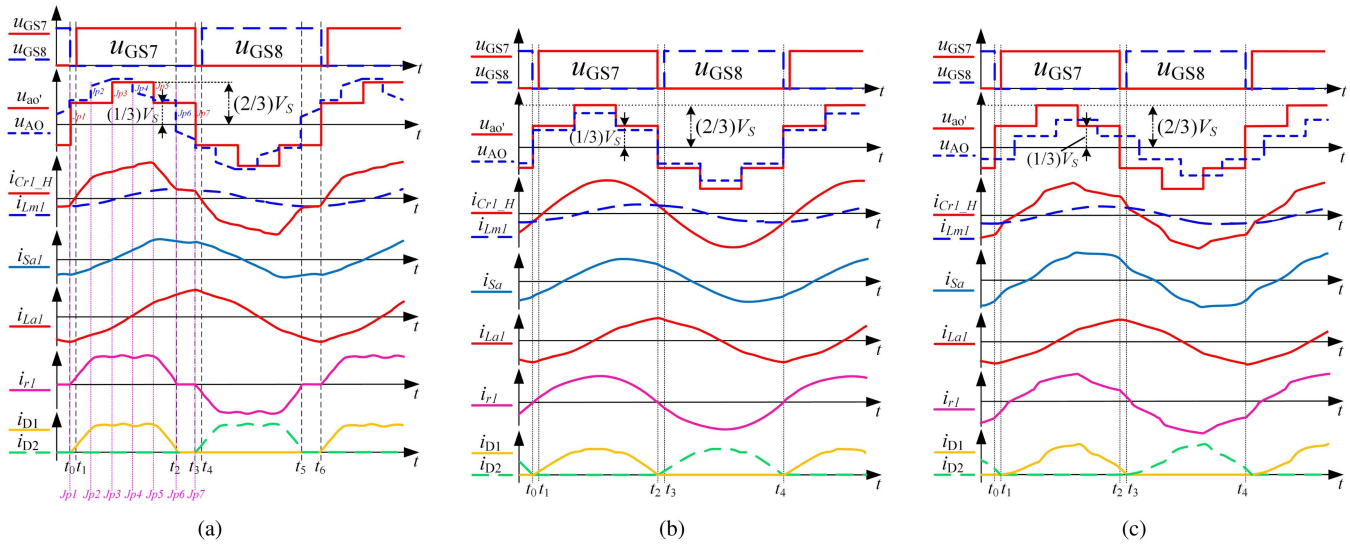

Fig. 6. Phase-A key operation waveforms of the proposed *LLCL* resonant converter in backward mode. (a) $f_s < f_r$. (b) $f_s = f_r$. (c) $f_s > f_r$.

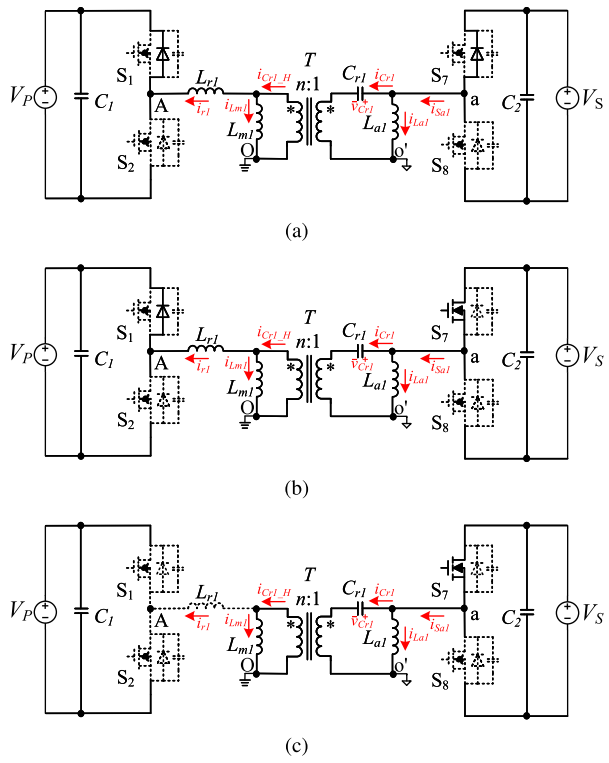

Fig. 7. Phase-A operation states for half of switching period in backward mode. (a) State I $[t_0, t_1]$. (b) State II $[t_1, t_2]$. (c) State III $[t_2, t_3]$.

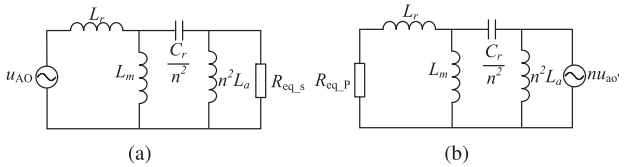

Fig. 8. A-phase FHA equivalent circuit of the proposed three-phase converter. (a) Forward mode. (b) Backward mode.

B. Analysis of the Voltage Gain

According to the analysis in the previous section, the forward and backward modes have the same resonant frequency in the main power transmission stage, which is defined as the main resonant frequency f_r

$$f_r = \frac{1}{2\pi}\sqrt{\frac{1}{L_{eq}C_{eq}}} = \frac{n}{2\pi}\sqrt{\frac{L_m + L_r}{L_m L_r C_r}}. \tag{6}$$

For simplifying the voltage gain expression of the converter, seven additional variables are defined: the normalized frequency f_n, the inductance ratios k and g, and the equivalent inductance and capacitance L_{eq} and C_{eq}, the quality factor in forward mode Q_F and backward mode Q_B. These parameters are shown as follows:

$$f_n = \frac{f_s}{f_r} \tag{7}$$

$$k = \frac{L_r}{L_m} \tag{8}$$

$$g = \frac{L_a}{L_m} \tag{9}$$

$$C_{\text{eq}} = \frac{C_r}{n^2} \tag{10}$$

$$L_{\text{eq}} = \frac{L_m L_r}{L_m + L_r} \tag{11}$$

$$Q_F = \frac{\sqrt{L_{\text{eq}}/C_{\text{eq}}}}{R_{\text{eq\_}s}} \tag{12}$$

$$Q_B = \frac{\sqrt{L_{\text{eq}}/C_{\text{eq}}}}{R_{\text{eq\_}p}}. \tag{13}$$

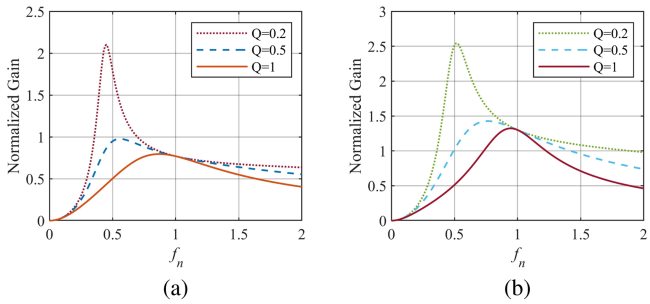

Fig. 9. Voltage gain versus normalized frequency of the proposed three-phase converter (a) Forward mode. (b) Backward mode.

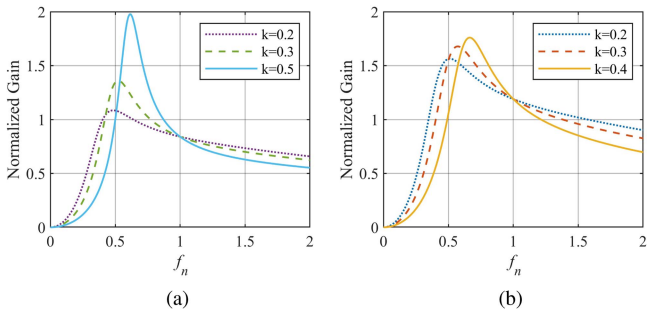

Fig. 10. Effect of k on both modes voltage gains. (a) Forward mode. (b) Backward mode.

TABLE I
CONVERTER DESIGN SPECIFICATIONS

Items	Forward Mode	Backward Mode
Voltage V_P/V	400	400
Voltage V_S/V	250–420	300–420
Output power P_o/kW	3.3	3.3
Output current I_o/A	7.8	4.7–8.2

Based on FHA, the voltage gain of both modes can be obtained

$$M_F = \frac{1}{\sqrt{\left[\frac{k}{gn}\left(1-\frac{1}{f_n^2}\right)+(1+k)n\right]^2+Q_F^2\left(f_n-\frac{1}{f_n}\right)^2(1+k)^2n^2}} \tag{14}$$

$$M_B = \frac{1}{\sqrt{\left[\frac{1}{n}-\frac{k}{f_n^2(1+k)n}\right]^2+Q_B^2\left(f_n-\frac{1}{f_n}\right)^2(1+k)^2\frac{1}{n^2}}}. \tag{15}$$

When the converter works in backward mode, the auxiliary inductor L_a is clamped and does not participate in resonance, which means that the voltage gain is only related to k and Q_B. Fig. 9 shows that both voltage gain curves operate monotonically in the inductive region and the converter can achieve boost and buck in both directions. As smaller quality factor Q, the voltage gain is higher, but the voltage gain curve shifts to the left.

IV. Design Considerations

A. Analysis of Constraint Condition

The design specifications of the proposed converter are listed in Table I. The proposed converter has the highest efficiency at the main resonant frequency, and as the frequency departs from the main resonant frequency, the efficiency decreases. To tradeoff the gain range and efficiency, the operating frequency range of the converter in both modes is finally selected to be $0.7f_r$–$1.5f_r$. Therefore, the range of normalized frequency f_n is

$$0.7 \le f_n \le 1.5. \tag{16}$$

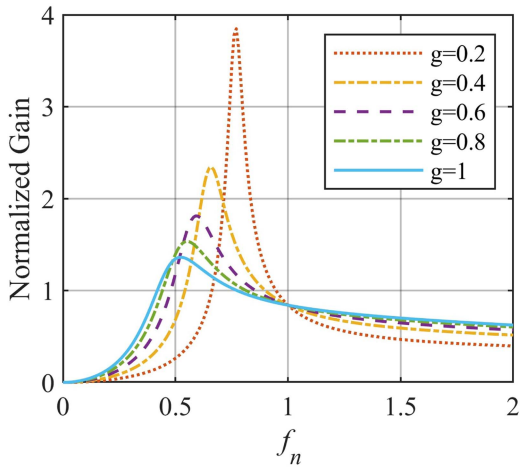

Fig. 11. Effect of g on forward voltage gains.

When the converter operates at the main resonant frequency, the voltage V_S is set to 335 V, and the bus voltage V_P is fixed at 400 V. Both voltage gains of the converter at the main resonant frequency are $1/[(1+k)n]$ and $(1+k)n$ respectively, which are mutually reciprocal. Thus, the relationship between n and k should satisfy (17)

$$(1+k)\,n = \frac{400}{335} = 1.19. \tag{17}$$

B. Analysis of the Resonant Tank

As can be seen from (12) and (13), when the load resistance of the converter is determined, as the reduction of Q, the equivalent inductance of the resonant tank will reduce, which will increase the current flowing through the resonant tank and the loss of the converter.

Meanwhile, with the reduction of Q, the voltage gain curve shifts to the left, which will cause the converter to fail to achieve the desired gain range. Therefore, the values of Q_F and Q_B cannot be too small. Fig. 10(a) and (b) presents that with an increase in k, the voltage gain ranges in both modes expand. However, an excessive k will increase the loss of magnetic components and reduce the efficiency.

According to (14) and (15), g only affects the forward voltage gain. Fig. 11 presents that as smaller g, the forward voltage gain

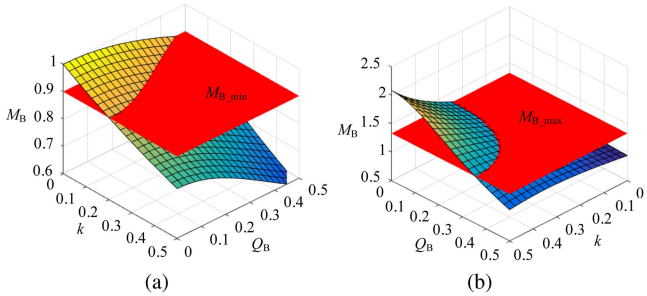

Fig. 12. Impact of circuit parameters on voltage gains in backward mode. (a) M_B versus Q_B and k when $f_n = 1.5$. (b) M_B versus Q_B and k when $f_n = 0.7$.

range is wider. From (9), we can see that with the reduction of g, the value of L_a decreases.

C. Analysis of Forward and Backward Voltage Gain Range

Substituting (17) into (14) and (15), the simplified voltage gains of the converter operates in both modes can be derived, respectively, as follows:

$$M_F = \frac{1}{\sqrt{\left[\frac{k(1+k)}{1.19\,g}\left(1-\frac{1}{f_n^2}\right)+1.19\right]^2+1.416Q_F^2\left(f_n-\frac{1}{f_n}\right)^2}} \tag{18}$$

$$M_B = \frac{1.19}{\sqrt{\left[1+k-\frac{k}{f_n^2}\right]^2+Q_B^2\left(f_n-\frac{1}{f_n}\right)^2(1+k)^4}}. \tag{19}$$

1) Analysis of Backward Voltage Gain Range: For simplifying the design process, a reasonable range of k and Q_B can be determined by analyzing the backward voltage gain M_B. In the backward mode, the minimum gain $M_{B\_\min}$ and maximum gain $M_{B\_\max}$ are, respectively,

$$M_{B\_\min} = \frac{U_P}{U_{S\_\max}} = \frac{400}{420} = 0.95 \tag{20}$$

$$M_{B\_\max} = \frac{U_P}{U_{S\_\min}} = \frac{400}{300} = 1.33. \tag{21}$$

As long as the converter can meet the minimum voltage gain at the lowest operating frequency and maximum voltage gain at the highest operating frequency respectively, the converter can meet the voltage gain requirements under the whole operating time.

According to (19) and the obtained minimum voltage gain $M_{B\_\min}$ and maximum voltage gain $M_{B\_\max}$ of backward mode, a three-dimensional surface diagram of Q_B, k and backward voltage gain M_B can be drawn, as shown in Fig. 12. Fig. 13(a) and (b) can be obtained by projecting the intersection lines of the voltage gain M_B with $M_{B\_\min}$ and $M_{B\_\max}$ in Fig. 12(a) and (b) onto the k, Q_B plane, respectively.

According to the previous analysis, the smaller the k, the greater the voltage gain range M, but the loss will also increase.

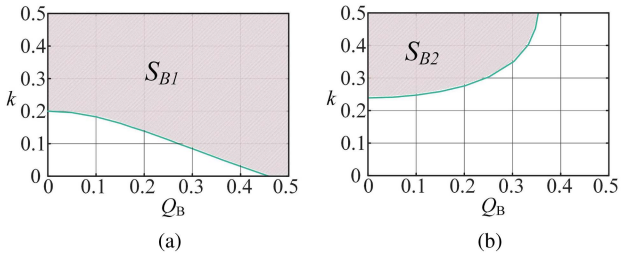

Fig. 13. Relationship between k and Q_B. (a) k versus Q_B when $f_n = 1.5$. (b) k versus Q_B when $f_n = 0.7$.

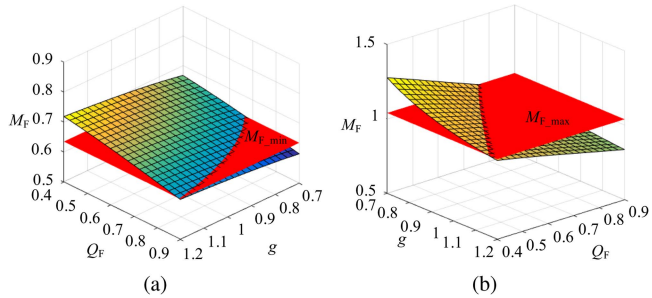

Fig. 14. Impact of circuit parameters on voltage gains in forward mode. (a) M_F versus Q_F and g when $f_n = 1.5$. (b) M_F versus Q_F and g when $f_n = 0.7$.

Thus, considering both voltage gain and efficiency, $k = 0.3$ is selected, and then $n = 0.918$ can be calculated by (17). Fig. 13(a) presents that when $k = 0.3$, the inequality $M_B(f_n = 1.5) < M_{B\_\min}$ can be satisfied regardless of the range of Q_B. However, to meet the requirement of $M_B(f_n = 0.7) > M_{B\_\max}$, Q_B should satisfy (22)

$$Q_B\,(f_n = 0.7) < 0.25. \tag{22}$$

2) Analysis of Forward Voltage Gain Range: In forward mode, the minimum gain $M_{\mathrm{F\_min}}$ and maximum gain $M_{F\_\max}$ are as follows:

$$M_{F\_\min} = \frac{U_{S\_\min}}{U_P} = \frac{250}{400} = 0.625 \tag{23}$$

$$M_{F\_\max} = \frac{U_{S\_\max}}{U_P} = \frac{420}{400} = 1.05. \tag{24}$$

Substituting $k = 0.3$ into (18), 3-D surface diagrams of Q_F, g, and forward voltage gain M_F are drawn, as shown in Fig 14. Fig. 15(a) and (b) can be obtained by projecting the intersection lines of the forward voltage gain M_F with $M_{F\_\min}$ and $M_{F\_\max}$ in Fig. 14(a) and (b) onto the g, Q_F plane, respectively.

With k is fixed at 0.3, the value of g corresponds to the value of the auxiliary inductor L_a. During most of the converter's working time in forward mode, L_a is clamped by the secondary side voltage $u_{ao'}$, and i_{La} is a triangular wave. When g is too small, the i_{La} peak increases, so the circuit loss increases; When g is excessive, the converter cannot maintain the voltage gain requirements. To meet the requirements of wide voltage gain and high efficiency, while simplifying the design process of the converter, $g = 1$ is finally selected.

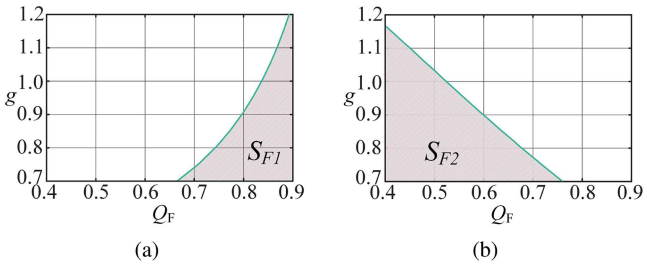

Fig. 15. Relationship between g and Q_F. (a) g versus Q_F when $f_n = 1.5$. (b) g versus Q_F when $f_n = 0.7$.

Fig. 15(a) and (b) shows that for $g = 1$, the range of Q_F should satisfy (25) and (26)

$$Q_F(f_n = 1.5) > 0.83 \tag{25}$$

$$Q_F(f_n = 0.7) < 0.52 \tag{26}$$

To simplify the calculation we can make

$$Z_{\text{eq}} = \sqrt{\frac{L_{\text{eq}}}{C_{\text{eq}}}}. \tag{27}$$

Then, according to (7) and (13), it can be obtained

$$Q_F = \frac{Z_{\text{eq}}}{R_{\text{eq\_}s}} \tag{28}$$

$$Q_B = \frac{Z_{\text{eq}}}{R_{\text{eq\_}p}}. \tag{29}$$

According to (22), (25), and (26), the range of Z_{eq} can be obtained, and finally, $Z_{\text{eq}} = 14$ is selected.

D. Design of the Circuit Parameters and ZVS Condition

In circuit hardware design, capacitive components are best to use a single capacitor. If the required capacitor is composed of multiple capacitors in series and parallel, it is best to use the same type of capacitor.

Therefore, the resonant capacitor $C_r = 66$ nF is ultimately chosen, which can be composed of two 33 nF capacitors in parallel. The parameters of k, n, g, Z_{eq}, C_r have been determined, thus the values of L_r, L_m, L_a, f_r can be calculated by the formula (10), (8), (9), (6), and (27), that are $L_r = 20$ μH, $L_m = 66.7$ μH, $L_a = 66.7$ μH and $C_r = 66$ nF and main resonant frequency $f_r = 142$ kHz.

The dead time between S_1 and S_2 driving signals is set to 200 ns, the parasitic capacitance C_{oss} of the switches is 200 pF, and the minimum cycle time T_{min} is 4.7 μs. To ensure the switches on the inverter side can realize ZVS, L_m needs to satisfy the following requirements:

$$L_m < \frac{T_{\text{min}} n U_{S\_\text{min}} t_{\text{dead}}}{16 C_{\text{oss}} U_P}. \tag{30}$$

The L_m selected by calculation can meet (30) and achieve ZVS.

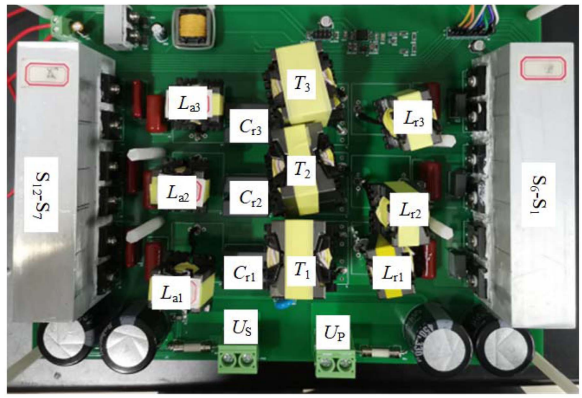

Fig. 16. Prototype of the proposed three-phase *LLCL* bidirectional resonant converter.

TABLE II
PARAMETERS OF EXPERIMENTAL PLATFORM

Items	Parameters
Main resonant frequency f_r	142 kHz
Switch frequency f_s	100 kHz–237 kHz
Resonant inductor L_r	20 μH (Ferroxcube PQ26/25)
Resonant capacitance C_r	66 nF (MMKP82333J1600V)
Auxiliary inductor L_a	66.7 μH (Ferroxcube PQ26/25)
Magnetizing inductor L_m	66.7 μH (Ferroxcube PQ35/35)
Turns ratio $n = (n_1 : n_2)$	0.917 = (22:24)
Switches S_1–S_{12}	IPW60R070CFD7

V. EXPERIMENTAL VERIFICATION

For validating the correctness of the theoretical analysis, a 3.3-kW prototype is developed and tested under different operating conditions, as shown in Fig. 16. Digital signal processor (DSP) controller TMS320F28035 from Texas Instruments (TI) is used to carry out PFM control. The specifications of the experimental platform are given in Table II.

A. Experimental Results

Fig. 17 shows the steady-state experimental waveforms in forward mode. Fig. 17(a)–(c) shows the current waveforms of L_r of each phase, which are all tested at $V_P = 400$ V, while f_S are 100, 142, and 237 kHz, respectively. The three-phase resonant current is balanced in each phase. When the switching frequency is equal to the main resonant frequency, the resonant current waveform is similar to the sine wave, as shown in Fig. 17(b).

Fig. 17(d)–(f) shows the ZVS characteristics of the MOSFETs are independent of the switching frequency. In Fig. 17(d), the driving voltage u_{gs2} begins to rise after the drain-source voltage of the switches S_2 drops to zero, which indicates that the parasitic capacitor of S_2 discharged to zero and the body diode of S_2 conducts. Thus, the ZVS condition is satisfied. The ZVS process of Fig. 17(d) and (f) is similar to Fig. 17(d).

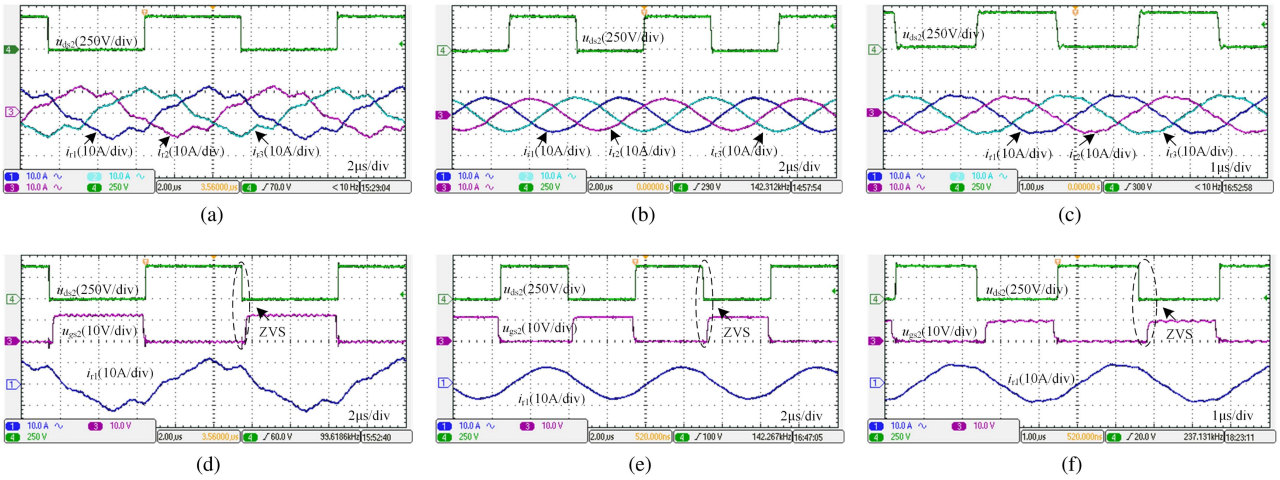

Fig. 17. Experimental waveforms of forward mode. (a) i_{r1}, i_{r2}, i_{r3}, and u_{ds2} when output 420 V/7.8 A($f_s < f_r$). (b) i_{r1}, i_{r2}, i_{r3}, and u_{ds2} when output 335 V/7.8 A($f_s = f_r$). (c) i_{r1}, i_{r2}, i_{r3}, and u_{ds2} when output 250 V/7.8 A($f_s > f_r$). (d) u_{ds2}, u_{gs2}, and i_{r1} when output 420 V/7.8 A($f_s < f_r$). (e) u_{ds2}, u_{gs2}, and i_{r1} when output 335 V/7.8 A($f_s = f_r$). (f) u_{ds2}, u_{gs2}, and i_{r1} when output 250 V/7.8 A($f_s > f_r$).

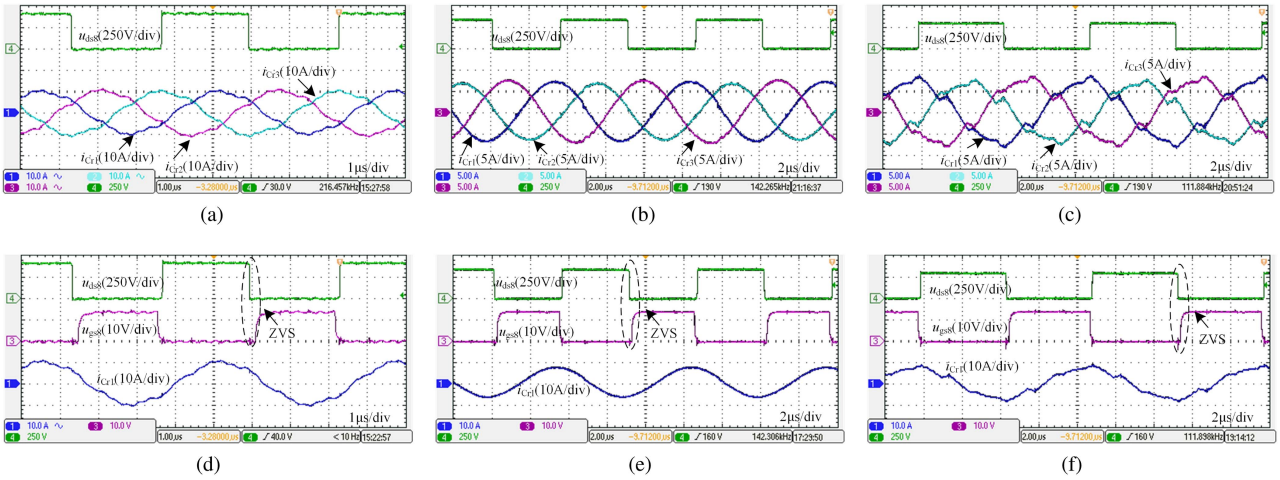

Fig. 18. Experimental waveforms of backward mode. (a) i_{Cr1}, i_{Cr2}, i_{Cr3}, and u_{ds8} when $V_S = 420$ V, $P_o = 3.3$ kW($f_s > f_r$). (b) i_{Cr1}, i_{Cr2}, i_{Cr3} and u_{ds8} when $V_S = 335$ V, $P_o = 2.3$ kW($f_s = f_r$). (c) i_{Cr1}, i_{Cr2}, i_{Cr3}, and u_{ds8} when $V_S = 300$ V, $P_o = 1.9$ kW($f_s < f_r$). (d) u_{ds8}, u_{gs8} and i_{Cr1} when $V_S = 420$ V, $P_o = 3.3$ kW($f_s > f_r$). (e) u_{ds8}, u_{gs8}, and i_{Cr1} when $V_S = 335$ V, $P_o = 2.3$ kW($f_s = f_r$). (f) u_{ds8}, u_{gs8}, and i_{Cr1} when $V_S = 300$ V, $P_o = 1.9$ kW($f_s < f_r$).

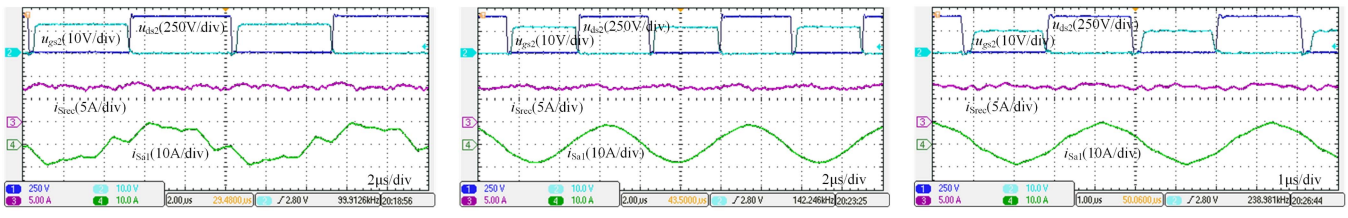

Fig. 19. Current ripple experimental waveforms in forward mode. (a) i_{Srec}, i_{Sa1}, u_{gs2}, and u_{ds2} when output 420 V/7.8 A($f_s < f_r$). (b) i_{Srec}, i_{Sa1}, u_{gs2}, and u_{ds2} when output 335 V/7.8 A($f_s = f_r$). (c) i_{Srec}, i_{Sa1}, u_{gs2}, and u_{ds2} when output 250 V/7.8 A($f_s > f_r$).

Fig. 18 shows the steady-state experimental waveforms in backward mode. The waveforms shown in Fig. 18(a)–(c) are all tested at $V_P = 400$ V, while f_S are 216, 142, and 111 kHz, respectively. The three-phase resonant current is balanced in each phase. Fig. 18(d)–(f) shows the ZVS characteristic of S_8, where it can be observed that the driving voltage u_{gs8} begins to rise after the drain-source voltage u_{ds8} of the switch drops to 0, which shows that the parasitic capacitor of the MOSFET discharged to zero and the body diode conducts. This demonstrates the implementation of ZVS.

Fig. 19 shows the waveforms of i_{Srec} is basically consistent with the theoretical waveform presented in Fig. 3(a). Due to the

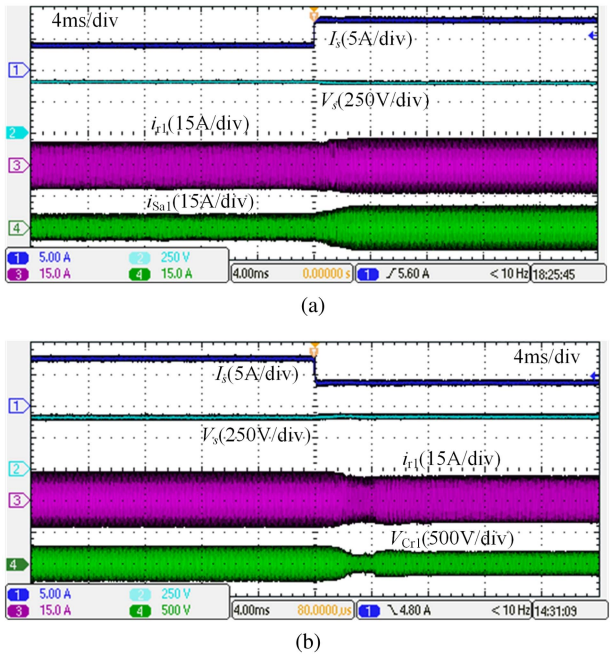

Fig. 20. Dynamic experimental waveforms in forward mode. (a) i_S, V_S, i_{r1}, and i_{Sa1} ($V_S = 420$ V, P_o jumps from half-load to full-load). (b) i_S, V_S, i_{r1}, and i_{Sa1} ($V_S = 420$ V, P_o jumps from full-load to half-load).

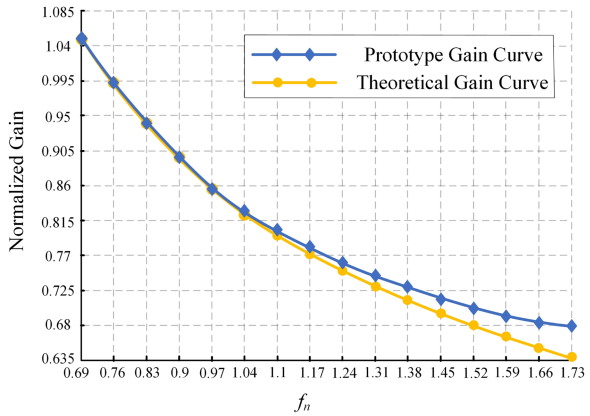

Fig. 21. Comparison curve between theoretical gain and prototype gain in forward mode ($Q_F = 0.5$).

bypass thin film capacitor of the bridge-arm, which is used to suppress the turn-OFF voltage spikes, the experimental waveform of i_{Srec} is approximately flat. Fig. 20 shows the dynamic experimental waveforms of the converter under constant voltage (CV) control. Fig. 20(a) and (b) presents the adjustment process of the converter from half-load to full-load and full-load to half-load, respectively. It can be seen that the respond speed is fast and there is less overshoot.

Fig. 21 shows a comparison between the theoretical gain and prototype gain curves, with Q_F maintaining a maximum value of 0.5. When $f_s < f_r$, the theoretical gain and prototype gain are basically consistent. When $f_s > f_r$, there is a deviation between the prototype gain and the theoretical gain, but the deviation is relatively small. The overall experimental results meet expectations.

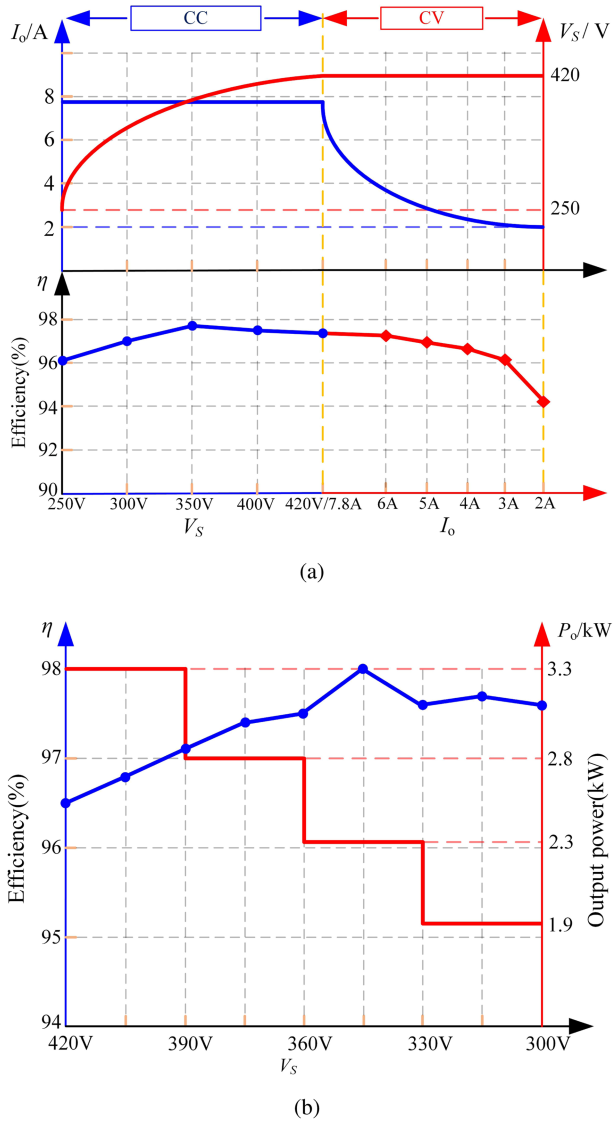

Fig. 22. Efficiency curves of the proposed converter. (a) For the forward mode. (b) For the backward mode.

B. Analysis of Working Process and Efficiency Curves

Fig. 22(a) shows the process of the constant current (CC) charging stage to the CV charging stage in forward mode. In the CC charging stage, the output current is fixed at 7.8 A, and the load is constantly increased to simulate the process. When the output voltage U_S rises from 250 to 420 V, the converter enters the CV charging stage. U_S remains at 400 V, the load still increases to simulate the CV charging stage, and the output current I_o gradually reduces from 7.8 A to the cut-off current 2 A. The whole charging process is completed.

In the whole CC charging stage and CV charging state when the output current exceeds 3 A, the efficiency of the prototype is above 96%. Besides, the efficiency exceeds 97% during most of the time, and the peak efficiency reaches 97.8%. When working in backward mode, the voltage range 300–420 V is chosen to prevent the battery from over discharging and the output power is set to reduce with the decrease of input voltage U_S for making

TABLE III
COMPARISON OF THE PROPOSED CONVERTER AND EXISTING CONVERTERS

References	Converter in [6]	Converter in [15]	Converter in [17]	Converter in [25]	Converter in [26]	Proposed
DC bus voltage Voltage	400 V	400 V	400 V	380-420 V	400 V	400 V
Topology	Single-Phase CLLLC	Single-Phase L-LLC	Single-Phase CLLC	Three-Phase CLLLCL	Three-Phase LLC	Three-phase LLCL
Direction	Bidirectional	Bidirectional	Bidirectional	Bidirectional	Unidirectional	Bidirectional
Forward output voltage V_S	250–450 V	320–480 V	250–450 V	280–420 V	200–400 V	250–420 V
Backward input voltage V_P	250–450 V	320–480 V	250–450 V	300–400 V	×	300–420 V
Output power	3.5 kW	1.6 kW	1.2 kW	3.3 kW	1.4 kW	3.3 kW
Forward peak efficiency	97.7%	97.8%	96%	97.2%	95.6%	97.8%
Backward peak efficiency	98.1%	97.8%	95%	96.9%	×	98%

full use of the power capacity of the converter, which is presented in Fig. 22(b). Such as when the input voltage U_S is reduced from 390 to 420 and from 360 to 390, the output power is decreased from 3.3 to 2.8 kW.

The efficiency is greater than 96.5% in the whole process of the proposed converter and the peak efficiency reaches 98.0%. A comparison between the proposed topology and existing converters is given in Table III. The proposed converter has outstanding performance in voltage gain range and peak efficiency.

VI. CONCLUSION

Aiming at the problems of limited gain range, inability to realize high-efficiency bidirectional energy transfer, and large ripple current of traditional LLC resonant converter, a three-phase $LLCL$ bidirectional resonant converter with PFM control is proposed in this article. Soft switching can be realized throughout the entire operation time, which is beneficial for reducing switching losses and improving converter efficiency. Besides, the proposed converter has the advantages of wide gain range, low current ripple, and large power capacity, etc. A 3.3 kW experimental prototype is built and tested under different conditions to validate the correctness of theory analysis and parameter design. The bus voltage is fixed at 400 V, in forward mode, the output voltage range is 250–420 V, and the peak efficiency is up to 97.8%. In backward mode, the inverter side voltage range is 300–420 V, and the peak efficiency is up to 98.0%. Therefore, the proposed converter has high overall efficiency over a wide output voltage range in both directions.

REFERENCES

[1] H. V. Nguyen, D.-C. Lee, and F. Blaabjerg, "A novel SiC-based multifunctional onboard battery charger for plug-in electric vehicles," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 5635–5646, May 2021.

[2] Y. Wei and A. Mantooth, "An LLC converter with fixed switching frequency operation for renewable energy applications," in *Proc. IEEE Transp. Electrific. Conf. Expo*, 2021, pp. 354–359.

[3] H. Wu, K. Sun, L. Chen, L. Zhu, and Y. Xing, "High step-up/step-down soft-switching bidirectional DC–DC converter with coupled-inductor and voltage matching control for energy storage systems," *IEEE Trans. Ind. Electron.*, vol. 63, no. 5, pp. 2892–2903, May 2016.

[4] C. Bai, B. Han, B.-H. Kwon, and M. Kim, "Highly efficient bidirectional series-resonant DC/DC converter over wide range of battery voltages," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3636–3650, Apr. 2020.

[5] A. Q. Huang, "Medium-voltage solid-state transformer: Technology for a smarter and resilient grid," *IEEE Ind. Electron. Mag.*, vol. 10, no. 3, pp. 29–42, Sep. 2016.

[6] Z. U. Zahid, Z. M. Dalala, R. Chen, B. Chen, and J. -S. Lai, "Design of bidirectional DC–DC resonant converter for vehicle-to-grid (V2G) applications," *IEEE Trans. Transp. Electrific*, vol. 1, no. 3, pp. 232–244, Oct. 2015.

[7] Y.-E. Wu and Y.-T. Ke, "A novel bidirectional isolated DC-DC converter with high voltage gain and wide input voltage," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 7973–7985, Jul. 2021.

[8] F. Wu, K. Wang, and S. Luo, "Hybrid-three-level current-fed series-resonant isolated DC-DC converter and its optimization modulation strategy," *IEEE Trans. Power Electron.*, vol. 37, no. 1, pp. 196–205, Jan. 2022.

[9] I. Demirel and B. Erkmen, "A very low-profile dual output LLC resonant converter for LCD/LED TV applications," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3514–3524, Jul. 2014.

[10] M. Li, Z. Ouyang, and M. A. Andersen, "High-frequency LLC resonant converter with magnetic shunt integrated planar transformer," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2405–2415, Mar. 2019.

[11] S. S. Shah, S. K. Rastogi, and S. Bhattacharya, "Paralleling of LLC resonant converters," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 6276–6287, Jun. 2021.

[12] G. Liu, Y. Jang, M. M. Jovanović, and J. Q. Zhang, "Implementation of a 3.3-kw DC–DC converter for EV on-board charger employing the series-resonant converter with reduced-frequency-range control," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4168–4184, Jun. 2017.

[13] H. Li et al., "A bidirectional synchronous/asynchronous rectifier control for wide battery voltage range in SiC bidirectional LLC chargers," *IEEE Trans. Power Electron.*, vol. 37, no. 5, pp. 6090–6101, May 2022.

[14] H. Wu, K. Sun, Y. Li, and Y. Xing, "Fixed-frequency PWM-controlled bidirectional current-fed soft-switching series-resonant converter for energy storage applications," *IEEE Trans. Power Electron.*, vol. 64, no. 8, pp. 6190–6201, Aug. 2017.

[15] H. Wu, S. Ding, K. Sun, L. Zhang, Y. Li, and Y. Xing, "Bidirectional soft-switching series-resonant converter with simple pwm control and load-independent voltage-gain characteristics for energy storage system in DC microgrids," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 3, pp. 995–1007, Sep. 2017.

[16] W. Chen, P. Rong, and Z. Lu, "Snubberless bidirectional DC–DC converter with new CLLC resonant tank featuring minimized switching loss," *IEEE Trans. Ind. Electron.*, vol. 57, no. 9, pp. 3075–3086, Sep. 2010.

[17] Z. Bai, J. Shao, J. Gu, H. Liu, X. Zhang, and D. Xu, "Design and modeling of CLLC converter for bidirectional on-board charger," *IEEE Trans. Ind. Applic.*, vol. 59, no. 5, pp. 6095–6102, Sep./Oct. 2023.

[18] J. Sun, L. Yuan, Q. Gu, R. Duan, Z. Lu, and Z. Zhao, "Design-oriented comprehensive time-domain model for CLLC class isolated bidirectional DC-DC converter for various operation modes," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3491–3505, Apr. 2020.

[19] S. Ditze, "Steady-state analysis of the bidirectional CLLLC resonant converter in time domain," in *Proc. IEEE Int. Telecommun. Energy Conf.*, 2014, pp. 1–9.

[20] G. F. S. Zong and X. Yang, "Double voltage rectification modulation for bidirectional DC/DC resonant converters for wide voltage range operation," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6510–6521, Jul. 2019.

[21] J. Liu, Y. Ai, S. Chen, Z. Zhang, and Y. Shi, "A hybrid pulse frequency modulation control strategy for L-LLC resonant converter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 6, pp. 6960–6972, Dec. 2022.
[22] X. Ma, P. Wang, H. Bi, and Z. Wang, "A bidirectional LLCL resonant DC-DC converter with reduced resonant tank currents and reduced voltage stress of the resonant capacitor," *IEEE Access*, vol. 8, pp. 125549–125564, Jul. 2020.
[23] O. Kirshenboim and M. M. Peretz, "Combined multilevel and two-phase interleaved LLC converter with enhanced power processing characteristics and natural current sharing," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5613–5620, Jul. 2018.
[24] H. Dong, X. Xie, S. Xu, and H. Yu, "A novel current sharing scheme for two-phase interleaved LLC converter based on virtual controllable voltage sources," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1210–1216, Feb. 2022.
[25] Y. H. Zhou, Y. Huang, and S. Zheng, "Research on bidirectional on-board charging system based on three-phase wye-wye connected CLLLC resonant converter," *IEEE Access*, vol. 11, pp. 101998–102013, Sep. 2023.
[26] G. Li, D. Yang, B. Zhou, Y. -F. Liu, and H. Zhang, "Integration of three-phase LLC resonant converter and full-bridge converter for hybrid modulated multioutput topology," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 5, pp. 5844–5856, Oct. 2022.
[27] A. Chiba, Y. Aoyagi, and K. Takagi, "Current balancing and phase shedding by split capacitor for a three-phase LLC resonant converter," in *Proc. IEEE Energy Convers. Congr. Expo,*, 2020, pp. 377–384.
[28] S. A. Arshadi, M. Ordonez, W. Eberle, M. Craciun, and C. Botting, "Three-phase LLC battery charger: Wide regulation and improved light-load operation," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1519–1531, Feb. 2021.

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