On-Chip Concurrent Device Aging Prognosis and Dielectric Failure Detection for GaN Power Devices

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***Abstract*—Despite promising figure of merits, as emerging wide bandgap devices, gallium nitride (GaN) power devices face significant reliability challenges. This article presents an on-chip condition monitoring (CM) approach addressing these challenges by seamlessly integrating device aging prognosis and dielectric failure detection into a unified circuit platform. Specifically, leveraging the device turn-ON transient time (t_{on}) as a reliable aging precursor, we propose a closed-loop t_{on} sensing scheme with self-regulated sampling to enhance precursor readout accuracy while mitigating sensing delays. Furthermore, we improve CM accuracy through junction temperature (T_J) calibration, effectively eliminating temperature-induced effects on precursor measurements. Concurrently, we develop a gate leakage current (I_{GSS}) based sensing scheme for dielectric failure detection, sharing the same circuitry of T_J calibration. Leveraging a proposed reconfigurable tri-mode gate driver, this CM approach minimizes impact on normal system operation. A power IC prototype was implemented on a 180-nm BCD process. Demonstrated on a GaN half-bridge power converter, the proposed CM exhibits the precise detection of both device aging and dielectric failure.**

***Index Terms*—Aging precursor, device reliability, dielectric failure, gallium nitride (GaN), gate leakage current, power device condition monitoring (CM), turn-ON transient delay.**

I. Introduction

As THE power electronics industry advances rapidly, reliability emerges as a critical imperative in face of escalating demands for high power density and high performance. Power semiconductor devices, tasked with handling substantial voltage and current stress during energy conversion and power delivery, encounter formidable challenges in terms of reliability. These challenges are underscored by the significant aging and wear-out effects experienced by these devices, accounting for approximately 40% of power system failures [1]. Meanwhile, GaN high electron mobility transistors have garnered recognition for their exceptional switching characteristics, facilitating superior performance in modern power electronics [2]. However, their high-frequency operations in switching power circuits pose additional reliability concerns due to significantly elevated *dv/dt* and *di/dt* [3], [4], [5].

To enhance device reliability, condition monitoring (CM) has emerged as a cost-effective solution in modern power electronics [6]. This approach often involves evaluating aging precursors—measurable characteristics that consistently change as devices degrade, thereby indicating their health conditions. Notably, *in situ* CM approaches [7], [8] have been developed to perform precursor measurements during system start-up to assess device health. However, the test conditions of *in situ* CM may significantly differ from actual operating conditions, leading to discrepancies in precursor readouts that could misrepresent the device's health status, thereby reducing monitoring accuracy. Moreover, this approach fails to address potential failures during regular system operation since evaluations are limited to system start-up. To overcome these challenges, online CM approaches [9], [10] are increasingly favored, offering real-time precursor measurements without interrupting system operation and thus providing higher precision in health assessment. However, implementing such systems introduces significant design overheads to enable accurate precursor detection. Furthermore, design complexity increases when considering multiple failure mechanisms such as device aging and dielectric failure, necessitating the integration of multiple precursors for health assessment.

Among the various approaches to monitoring device aging, the threshold voltage (V_{TH}) exhibits a gradual increase during gate oxidate degradation [11], [12], rendering it a viable aging precursor. However, V_{TH} measurements in [12] require the gate driver to be disabled. Therefore, the power converter must be shut down for precursor measurements, leading to system interruption. Conversely, the ON-resistance ($r_{\mathrm{DS(ON)}}$) of power devices emerges as a favorable precursor for online CM. Unfortunately, the unique dynamic $r_{\mathrm{DS(ON)}}$ phenomenon [13], [14] in GaN devices necessitates highly sophisticated circuits for precise measurement. Chen and Ma [10] employs synchronized voltage and current sensors to detect the device's V_{DS} and I_{DS} simultaneously, followed by a division operation to compute $r_{\mathrm{DS(ON)}}$. However, both sensing and computational operations are susceptible to signal processing errors.

Recently, the turn-ON transient delay (t_{on}) in silicon carbide MOSFETs has been reported as a promising aging precursor [8]. However, the accuracy of switching transient measurements is highly susceptible to any delay effects in the detection circuits.

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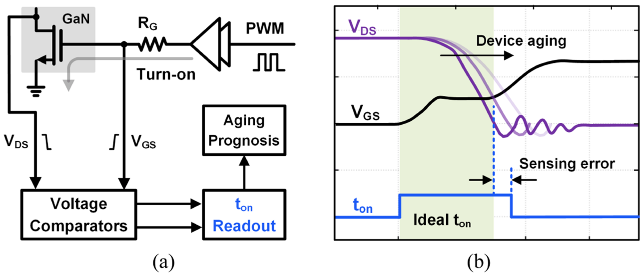


Fig. 1. (a) Conventional turn-ON transient delay t_{on} sensing approach, and (b) illustration of large t_{on} readout error due to circuit propagation delays.

Such delays can be comparable to changes in t_{on} over aging, resulting in significant errors in device health evaluation, as depicted in Fig. 1. Furthermore, these inherent delay errors vary significantly due to process variations and temperature fluctuations. Subtracting the actual sensing delays from the measured t_{on} during post-data processing can be quite challenging. If applied to GaN devices, the high-frequency operation would make t_{on} detection even more challenging due to the fast *dv/dt* switching. Furthermore, GaN power transistors often have tighter gate voltage margins compared to silicon counterparts, thus facing a higher risk of dielectric breakdown [2]. Therefore, an online dielectric failure detection scheme is highly preferable to prevent short circuit faults.

On the other hand, aging precursors are highly affected by the device junction temperature (T_J). If precursor measurements are conducted at different T_J without compensation, they will yield inaccurate assessments of device health. Therefore, an effective T_J calibration mechanism must be developed to mitigate the temperature effect and reveal the actual device aging condition. Shi et al. [15] adopts the delay time of impulse signal as a T_J sensing parameter. However, similar to t_{on} detection, the propagation delays resulting from analog circuits lead to large sensing errors. Shi et al. [16] employs the device transconductance (g_m) to estimate T_J. However, g_m measurement is converted into a digital pulse with analog buffers, introducing delay errors. Chen and Ma [10] utilizes the gate leakage current (I_{GSS}) to conduct T_J calibration. To fulfill the I_{GSS} sensing, an additional switch must be inserted between the gate driver and the GaN power device. This switch is exposed to high *di/dt* stress and requires bootstrapping driving technique, degrading the system reliability.

To address the aforementioned design concerns, this article presents an online CM approach that seamlessly integrates device aging monitoring and dielectric failure detection on a single chip. For device degradation, a closed-loop t_{on} sensing scheme is developed to achieve precise precursor readout. Furthermore, a T_J calibration process is implemented to mitigate temperature effects on the precursor t_{on}, thereby enhancing the accuracy of device health assessment. Concurrently, to address potential dielectric breakdown, a gate leakage current (I_{GSS}) based CM approach is proposed for dielectric failure detection. Notably, I_{GSS} also serves as a temperature-sensitive electrical parameter for T_J calibration, enabling both T_J sensing and dielectric failure detection to utilize the same circuitry and reducing design overheads.

The rest of this article is organized as follows. Following this introduction, Section II discusses the T_J-independent device aging monitoring scheme. Section III introduces the dielectric failure monitoring scheme. Then, the system architecture and detailed circuit implementations are presented in Section IV. To validate the proposed on-chip CM approach, a power IC prototype is implemented with experimental results presented in Section V. Finally, Section VI concludes this article.

II. T_{J}-Independent T_{ON}-Based Device Aging Monitoring

For GaN device degradation, the turn-ON transient time t_{on} is selected as an aging precursor. To understand the t_{on} behavior over device aging, we first review the analytical model of t_{on} based on the device's electrical characteristics. In a typical switching transition, the turn-ON behavior of a power switch can be divided into four phases. First, as the gate driver circuit starts charging the gate capacitance, the device gate-to-source voltage V_{GS} increases. Second, once V_{GS} reaches the threshold voltage V_{TH}, the drain-to-source current I_{DS} will be conducted in the device channel. So far, the time duration for the first two phases can be expressed as [17]

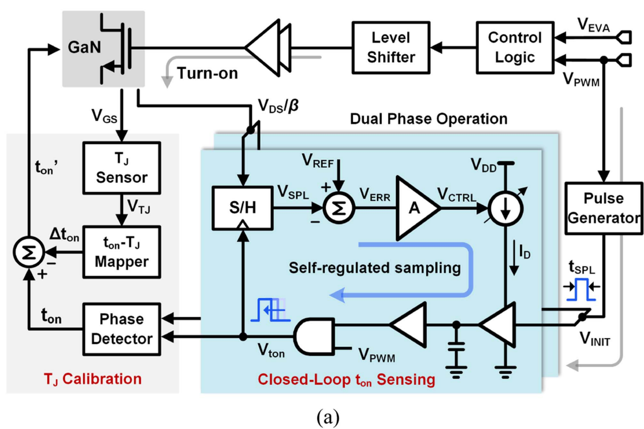
$$t_{1\&2} = R_G\, C_{\text{ISS}} \ln\left[V_{DD}/\left(V_{DD} - V_{\text{MP}}\right)\right] \tag{1}$$

where R_G and C_{ISS} are the total gate resistance and gate capacitance, respectively. V_{DD} is the supply voltage of the gate driver circuit and V_{MP} is the Miller Plateau voltage. Third, when V_{GS} reaches the Miller Plateau region, it remains almost constant. The gate driving current will flow through the gate-to-drain capacitance C_{GD}, causing the drain-to-source voltage V_{DS} to decrease from the input voltage V_{IN}. Therefore, the falling time of V_{DS} can be estimated as [17]

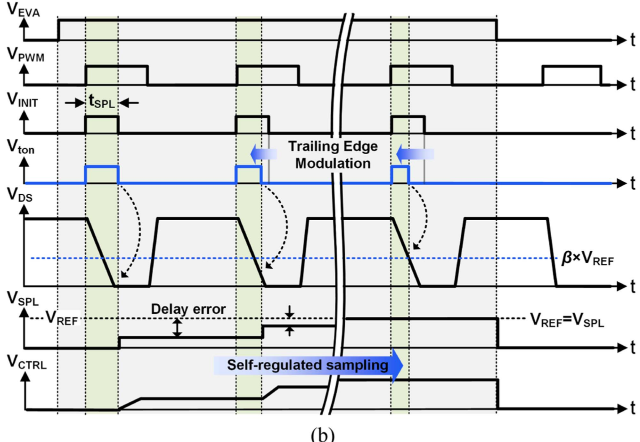
$$t_3 = R_G\, C_{\text{GD}} V_{IN}/\left(V_{DD} - V_{\text{MP}}\right). \tag{2}$$

As the device becomes aged, the gate capacitance including C_{GS} and C_{GD} remains almost unchanged [11]. However, a significant shift over aging is observed on the threshold voltage V_{TH} and transconductance g_m. Due to the traps under the device gate over aging process [18], V_{TH} increases while g_m decreases, resulting in an elevation of V_{MP}. In fact, the Miller Plateau voltage has been employed as the aging precursor for power MOSFETS [9]. Accordingly, the turn-ON transients $t_{1\&2}$ and t_3 both increase due to the rise in V_{MP} over aging process, which validates the effectiveness of t_{on} as an aging precursor.

Contrary to static characteristics such as V_{TH} and $r_{\text{DS(ON)}}$, the dynamic switching transient cannot be directly measured using voltage or current sensors. Prior works [7], [8] propose a method to detect the turn-ON transient delay by comparing the filtered V_{GS} or V_{DS} with a reference to generate the pulse signal. However, the inherent bandwidth limitations in the analog buffer and comparator circuits cause significant propagation delays and response times, leading to substantial errors in t_{on} readout. Even nanosecond-level delays can result in considerable inaccuracy in precursor measurements.



(a)



(b)

Fig. 2. (a) Block diagram of proposed T_J-independent t_{on}-based device aging monitoring scheme and (b) key operation waveforms.

To overcome this challenge, this article proposes a closed-loop t_{on} sensing approach to eliminate propagation delays for improved precursor readout accuracy. This method predicts the V_{DS} trailing edge through an on-chip delay modulation process to capture the precise turn-ON transition. Fig. 2(a) shows the block diagram of the proposed t_{on}-based device aging monitoring scheme. Before enabling the t_{on} sensing, the aging evaluator first sends the commands V_{EVA} to the gate driver. The turn-ON transition is thus extended for device health evaluation phase. The voltage V_{DS} is scaled down by a factor of β to fit into the operation voltage region of the on-chip sensor. Such voltage scaling is realized by a frequency-compensated voltage divider to capture the high-frequency characteristics of V_{DS}. The scaled V_{DS} is then sampled by a sample/hold (S/H) circuit with an initial delay time defined by t_{SPL}. By comparing the sampled result V_{SPL} with the predefined reference V_{REF}, the delay error is evaluated as a voltage signal V_{ERR}, which is further amplified to a control voltage V_{CTRL} with a voltage gain of A_0. To compensate for the delay error, the trailing edge of the initial sampling control signal V_{INIT} is modulated adaptively. By modulating the supply current I_D of the downstream logic circuit via V_{CTRL}, V_{INIT}'s trailing edge is adjusted accordingly as V_{ton}, which controls the S/H circuit to shift the sampling window until the ultimate sampled value V_{SPL} equals V_{REF}, as shown in Fig. 2(b).

By performing such self-regulated sampling mechanism, the proposed t_{on} sensing calibrates out the delay effect. For example, if V_{SPL} is lower than V_{REF}, V_{CTRL} will increase due to the positive delay error, leading to a large driving current I_D. This elevation in I_D reduces the charging duration for the capacitor, resulting in an earlier activation of the logic circuit. Therefore, V_{SPL}'s trailing edge is modulated backward and the sampled result will be lower in the next switching cycle. Such adaptive error correction will continue until the sampling window is aligned with the predefined reference. If the control-to-delay coefficient D_V is defined as the delay time change of V_{ton}'s trialing edge relative to variations in V_{CTRL}, and the slew rate of V_{DS} is represented as V_{SR}, the loop dc gain L_{G0} of this feedback system can be expressed as

$$L_{G0} = \frac{A_0 D_V V_{SR}}{\beta}. \tag{3}$$

Therefore, the feedback error voltage V_{ERR} in Fig. 2(a) can be computed using the loop gain as

$$V_{\text{ERR}} = \frac{V_{\text{REF}}}{1 + L_{G0}} \approx \frac{V_{\text{REF}}}{L_{G0}}. \tag{4}$$

With a scaled slew rate of V_{SR}/β in V_{DS}, this error voltage can be converted into the time domain. Correspondingly, the closed-loop delay error is described as

$$t_{\text{on,err}} = \frac{V_{\text{ERR}}}{V_{\text{SR}}/\beta} \approx \frac{\beta^2 V_{\text{REF}}}{A_0 D_V V_{\text{SR}}^2}. \tag{5}$$

Therefore, by selecting the parameters within the feedback system, delay errors can be significantly reduced. Furthermore, we apply two closed-loop schemes that operate simultaneously with different sampling references. The phase difference signal V_{ton} is analyzed by a phase detector. Any delay mismatches due to circuit layouts are avoided, further improving the precursor readout accuracy.

On the other hand, the turn-ON transient delay t_{on} exhibits dependency on the junction temperature T_J, as V_{MP} is determined by V_{TH} and g_m, both of which are highly influenced by temperature variations. If t_{on} is measured at different T_J without compensating for the temperature effects, the precursor readout might result in false monitoring of the device health. Therefore, a temperature calibration mechanism is employed to remove t_{on} readout error caused by T_J variation. The T_J-dependent Δ t_{on} is calculated using a t_{on} -T_J lookup table, which is built based on the corresponding t_{on} and T_J data. The temperature-induced Δt_{on} will be then subtracted from the measured t_{on}, resulting in a T_J-independent precursor t_{on}'. The junction temperature is obtained by a gate leakage current sensor, which also plays a role in the dielectric failure detection discussed in Section III.

III. I_{GSS}-Based Dielectric Failure Monitoring

For the dielectric failure in GaN device, the gate leakage current I_{GSS} is chosen as the failure indicator. I_{GSS} shows little variation during accelerated aging tests [11], [19], [20], as shown in Fig. 3(a). However, as the device is near dielectric breakdown, a considerable increase in I_{GSS} can be observed [11], [21]. Meanwhile, I_{GSS} demonstrates a significant dependency on the

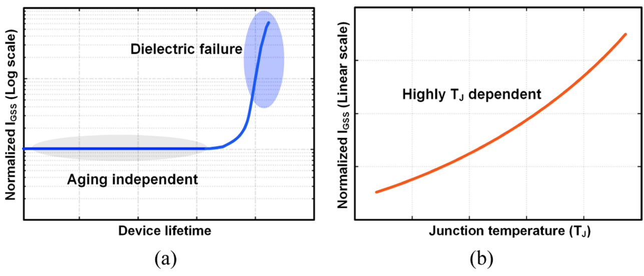


Fig. 3. Illustrations of (a) $I_{\rm GSS}$ characteristics with device aging/failure and (b) $I_{\rm GSS}$ temperature dependence.

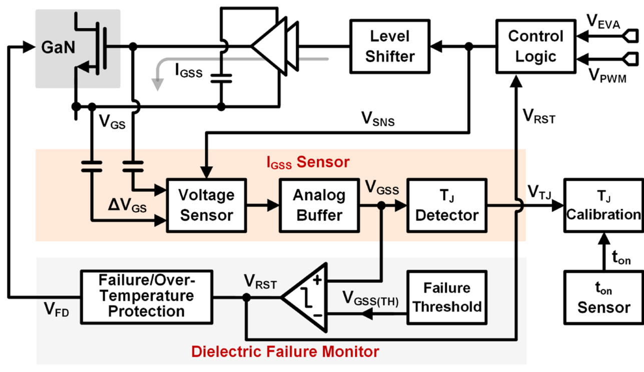
junction temperature T_J in GaN devices, as shown in Fig. 3(b). This characteristic enables the utilization of I_{GSS} as an indirect indicator of T_J, thereby obviating the necessity for an on-die temperature sensor.

Conventional methods for $I_{\rm GSS}$ sensing require a large gate resistance to increase sensing resolution. As $I_{\rm GSS}$ flows when the switch is fully turned ON, the voltage drop across the gate resistance can be measured with a differential amplifier. Even though $I_{\rm GSS}$ in a GaN device is much higher than that of a Si MOSFET, the gate resistance R_G must still be elevated to a level where the amplifier can reliably detect the voltage drop [21]. However, introducing such significant R_G inevitably leads to increased switching loss. Note that the proposed $t_{\rm on}$ sensor in Section II also requires slow switching transition for high sensing resolution. However, such operation is only activated in the device evaluation phase for a few switching cycles. Furthermore, the gate driver can be reconfigured into the fast-switching mode once the evaluation process is completed, which will be discussed in Section IV.

To detect the dielectric failure and junction temperature simultaneously, the $I_{\rm GSS}$-based failure monitoring with gate leakage current sensing is proposed as shown in Fig. 4(a). During the device evaluation phase, as $V_{\rm PMM}$ goes high, the power switch will be turned ON. After a blanking time of $t_{\rm BLK}$, the voltage $V_{\rm GS}$ reaches the gate driving supply voltage V_{DD}. The gate driver is then disabled temporarily for a short period of $t_{\rm SNS}$. Therefore, the output impedance of gate driver is high, allowing $I_{\rm GSS}$ to slightly discharge the gate capacitance $C_{\rm ISS}$. $V_{\rm GS}$ decreases during the discharge period. According to the charge conservation, the gate leakage current $I_{\rm GSS}$ can be computed as

$$I_{\rm GSS} = C_{\rm ISS}\Delta V_{\rm GS}/t_{\rm SNS} \tag{6}$$

where $\Delta V_{\rm GS}$ is the voltage drop for $V_{\rm GS}$. Since $t_{\rm SNS}$ is constant and $C_{\rm ISS}$ does not change over aging, $I_{\rm GSS}$ can be sensed by $\Delta V_{\rm GS}$ linearly as shown in Fig. 4(b). The voltage drop $\Delta V_{\rm GS}$ is capacitively coupled to a differential amplifier for voltage sensing. Once the output of amplifier $V_{\rm GSS}$ exceeds the failure threshold voltage $V_{{\rm GSS}(TH)}$, it indicates that the GaN device is near dielectric breakdown. A failure detection signal V_{FD} will be generated to warn the user that the device is facing potential failure and needs to be replaced. Meanwhile, it generates a reset signal $V_{\rm RST}$ to enable the gate driver, preventing $V_{\rm GS}$ over-discharge. As we have discussed, $I_{\rm GSS}$ is also highly



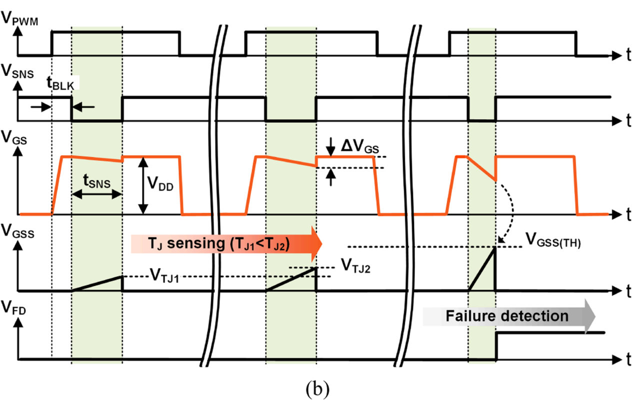


Fig. 4. (a) Circuit block diagram of proposed $I_{\rm GSS}$-based dielectric failure monitoring scheme and (b) key operation waveforms.

associated with T_J. Therefore, the peak value of $V_{\rm GSS}$ is captured as V_{TJ} to estimate the device junction temperature. Similar to dielectric failure detection, over-temperature protection can also be implemented by setting a threshold voltage for $V_{\rm GSS}$. And T_J information is further provided to $t_{\rm on}$ sensor for temperature calibration. It is noteworthy that both T_J increase and dielectric failure can cause elevated $I_{\rm GSS}$. However, dielectric failure is characterized by an exponential increase in $I_{\rm GSS}$, as shown in Fig. 3(a). As a result, the failure threshold $V_{{\rm GSS}(TH)}$ is set to be much higher than V_{TJ} at the maximum device operating temperature. Therefore, by taking advantage of the sensed $I_{\rm GSS}$, the dielectric failure monitoring and junction temperature sensing can be performed simultaneously, reducing design overheads.

IV. System Architecture and Circuit Implementation

A. System Architecture

The proposed CM approach is demonstrated on a GaN-based switching power converter, as shown in Fig. 5(a). The proposed closed-loop $t_{\rm on}$ sensing approach can enhance the precursor readout accuracy by compensating for propagation delays in the analog circuits. In addition, since the switching transients are impacted by the device junction temperature, a T_J calibration mechanism is developed to remove the temperature effect on $t_{\rm on}$. Therefore, a T_J-independent precursor $t_{\rm on}$' is measured with high precision for device aging prognosis. On the other hand,

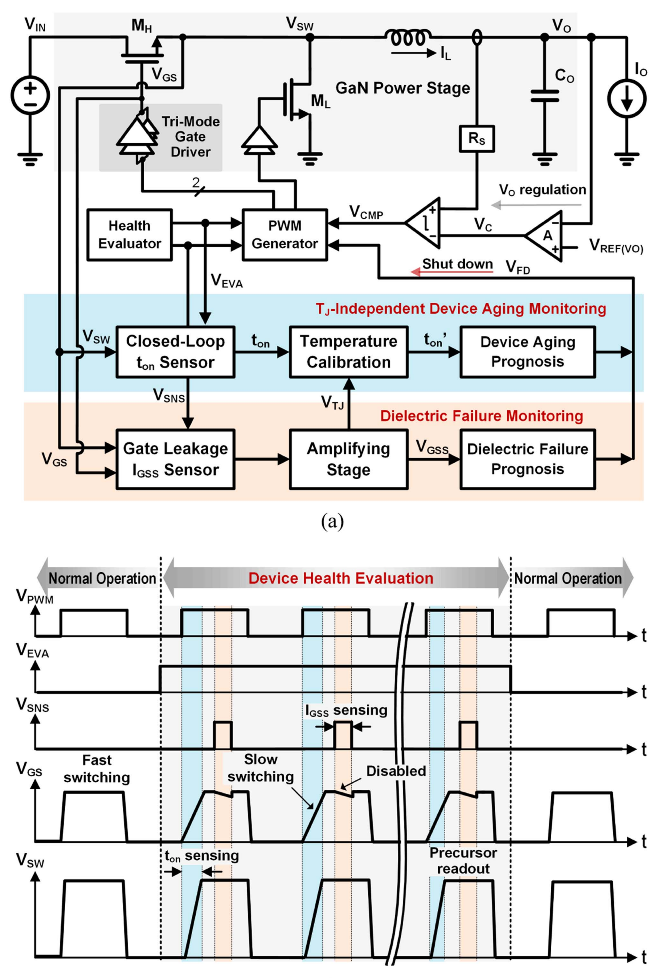
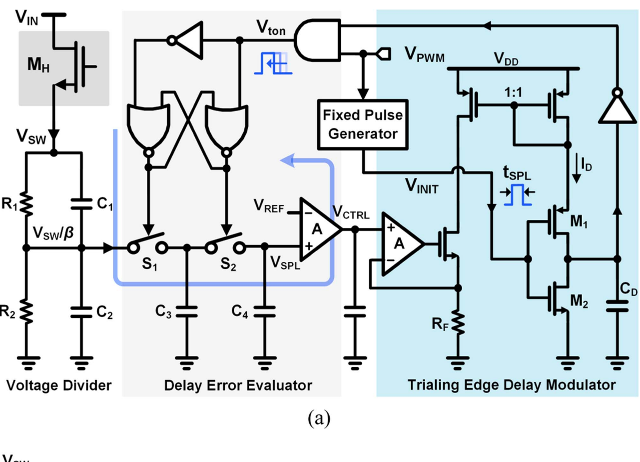


Fig. 5. (a) System block diagram of proposed CM approach demonstrated on a GaN power converter. (b) Key operation waveforms.

a gate leakage current I_{GSS}-based sensing scheme is designed to detect potential dielectric breakdown. Furthermore, I_{GSS} is also employed to estimate T_J simultaneously due to its highly T_J-dependent characteristic. Only the health status of high-side switch M_H is monitored since it operates in hard-switching condition and thus faces high voltage and current stresses. A conventional PWM controller is adopted for output regulation.

In addition to the proposed CM approach, a reconfigurable trimode gate driver is implemented to mitigate the system impact associated with aging evaluations. As shown in Fig. 5(b), the GaN device can be switched at different conditions for precursor readout. During the high-performance mode, the device operates at high switching speed to ensure optimal efficiency. Conversely, during the device health evaluation phase activated by V_{EVA}, the gate driver is adjusted to the slow-switching mode, offering better t_{on} sensing resolution. Simultaneously, V_{SNS} temporarily disables the gate driver for I_{GSS} sensing scheme to detect the dielectric breakdown and estimate the device junction temperature. Because device aging and temperature variations generally occur at a significantly slower pace compared to the



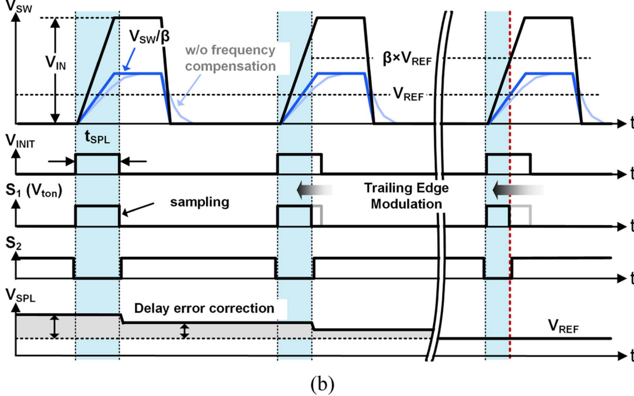


Fig. 6. Closed-loop t_{on} sensing mechanism. (a) Circuit schematic. (b) Key operation waveforms.

switching frequency, it is unnecessary to initiate device assessments frequently. Therefore, by reconfiguring the gate driver, the proposed CM method exhibits a minimal impact on the overall normal operation of the power converter.

B. *Closed-Loop* t_{on} *Sensing Mechanism*

Fig. 6(a) shows the detailed circuit schematic of the proposed closed-loop t_{on} sensor. Since the switching node voltage V_{SW} can be as high as the input voltage, it will be first scaled down to a 5-V domain for the on-chip sensors. Due to the high *dv/dt* nature of GaN power transistors, the frequency characteristic of V_{SW} waveform has a wide bandwidth, containing a large number of harmonics. To prevent distortion after V_{SW} scaling, a frequency-compensated voltage divider formed by R_1, C_1, and R_2, C_2 is adopted. By matching the impedances in *RC* network [22], it achieves a wide frequency range of voltage attenuation. The impedance matching can be described as

$$\frac{1}{\beta} = \frac{R_2}{R_1 + R_2} = \frac{C_1}{C_1 + C_2}. \tag{7}$$

During the turn-ON transient, V_{PWM} goes high and triggers an initial sampling control signal V_{SPL} with a pulse width of t_{SPL}. With a nonoverlapping clock generator, the switch S_1 is turned ON and V_{SW} is sampled at the capacitor C_3. As S_1 turns OFF and S_2 turns ON, the sampled result V_{SPL} is further stored in

the capacitor C_4 for signal processing. By comparing V_{SPL} with a predefined reference voltage V_{REF} through an error amplifier, the delay error is captured as V_{CTRL}. Such control voltage is converted linearly into a current flowing into a resistor R_F by a V-to-I converter. Then, it is copied to a driving current I_D by a current mirror. As M_1 and M_2 form a basic inverter, the pull-up driving strength is controlled by I_D while the pull-down strength is fixed. During the falling edge of the initial pulse V_{INIT}, the time spent to charge C_D can be modulated by I_D. Therefore, as V_{INIT} is fed to the gate of M_1 and M_2, its trailing edge can be adaptively adjusted by V_{CTRL} to generate V_{ton}. The modulated signal V_{ton} controls the S/H circuit to shift the sampling window until V_{SPL} equals V_{REF}, as shown in Fig. 6(b). For example, if V_{SPL} is higher than V_{REF} after the S/H circuit, it indicates that the sampling phase has been enabled earlier than desired so that V_{SW} hits $\beta\times V_{\mathrm{REF}}$ before V_{ton} goes low. In this case, V_{CTRL} increases, and so does I_D. As M_1 turns ON during V_{INIT}'s falling edge, larger I_D causes less delay to charge C_D in order to trigger the following logic. As a result, the pulse width of V_{ton} is reduced to sample V_{SW} in the next switching cycle. When it reaches the steady state, the trailing edge of V_{ton} is aligned with the instant where V_{SW} crosses $\beta\times V_{\mathrm{REF}}$. By performing such a negative feedback loop, the turn-ON transient delay is captured with high precision, eliminating any propagation delays. Note that the input polarity of the error amplifier in Fig. 6(a) is flipped compared to that in Fig. 2(a), as V_{SW} is sensed in real implementation to represent V_{DS}.

To estimate the accuracy of the proposed t_{on} sensing method, the pulse width of V_{ton} can be described as

$$t_{\mathrm{on}} = t_{\mathrm{SPL}} + \frac{R_F C_D V_{\mathrm{TP}}}{V_{\mathrm{CTRL}}} \tag{8}$$

where V_{TP} is the trip point voltage of the inverter followed by transistors M_1 and M_2 in Fig. 6(a). The simulated results indicate a control-to-delay coefficient D_V of 8 ns/V. The error amplifier is designed with a voltage gain A_0 of 60 dB. With a β of 5, V_{SR} of 0.4 V/ns, and V_{REF} of 2 V, the delay error of this close-loop t_{on} sensing is computed as 39 ps according to (5).

C. Gate-Leakage I_{GSS} Sensing Mechanism

Fig. 7 shows the circuit schematic of I_{GSS} sensor. The sensing period is enabled after a blanking time once M_H turns ON. The gate driver is first disabled to provide high impedance, causing V_{GS} drop due to I_{GSS}. When V_{SNS} is high, both switches S_3 and S_4 are ON, which connect the differential input of the amplifier to the common mode voltage V_{CM}. This will make the transistors in the amplifier operate in saturation region, ensuring the correct function of amplification in the next phase. Meanwhile, ΔV_{GS} is sampled on the capacitors C_5 and C_6. Once V_{SNS} becomes low, the bottom plates of capacitors are switched to the amplifier's input. ΔV_{GS} is then ac coupled through the capacitors for amplification. With a fixed pulse width generator, V_{SNS} has a fixed sensing period of t_{SNS}. To reduce the ON-resistance and prevent false turn-OFF of the GaN device, ΔV_{GS} must be much lower than the gate driver supply voltage V_{DD}. Furthermore, t_{SNS} must be designed to allow sufficient ΔV_{GS} to meet the

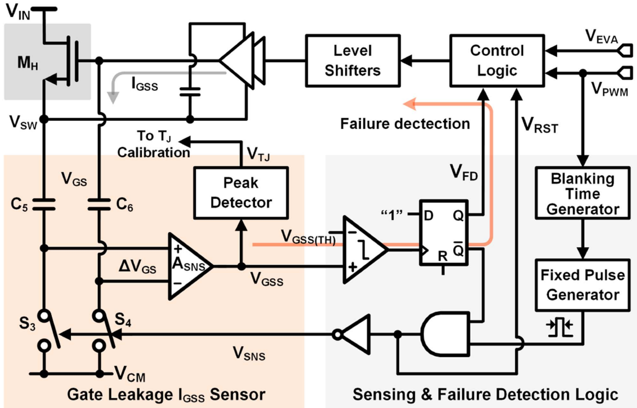


Fig. 7. Circuit schematic of I_{GSS}-based failure detection module.

minimum differential input voltage $V_{\mathrm{in,min}}$ requirement of the following sensing amplifier A_{SNS} in Fig. 7. Therefore, the t_{SNS} should satisfy

$$V_{\mathrm{in,min}} < \frac{I_{\mathrm{GSS}} t_{\mathrm{SNS}}}{C_{\mathrm{ISS}}} \ll V_{DD}. \tag{9}$$

To enhance the readout resolution, the sensing amplifier A_{SNS} magnifies the ΔV_{GS} into V_{GSS}. The A_{SNS} is designed with a programmable voltage gain, which is set by the on-chip resistor ratio [10]. Hence, the value of the voltage gain can be well controlled by layout techniques to minimize the impact of process variations. The sensing amplifier has a $V_{\mathrm{in,min}}$ of 10 mV. After the voltage amplification, a peak detector is used to extract the peak value of V_{GSS} as V_{TJ}, which is given to the t_{on} readout for temperature calibration. Meanwhile, V_{GSS} is compared to a failure threshold voltage $V_{\mathrm{GSS}(TH)}$. Once it exceeds this threshold, the comparator output becomes high, which triggers the D flip-flop to generate a warning signal V_{FD}. It also resets the sensing control signal V_{SNS}, re-enabling the gate driver to prevent over-discharge of V_{GS}.

D. Tri-Mode Gate Driving and Circuitry

Fig. 8(a) shows the circuit schematic of the reconfigurable trimode gate driver. Two pull-up transistors and one pull-down transistor are adopted in the buffer stage. By splitting the control signal for each transistor, the gate driver can be reconfigured into three modes to fulfill the needs for device health evaluation, as shown in Fig. 8(b). Specifically, when V_{EVA} is low, the gate driver exhibits strong driving strength for switch M_H. The large pull-up transistor M_{P1} and pull-down transistor M_{N1} will be turned ON alternatively with a small dead time to prevent the shoot-through. This will ensure high-performance operation for the GaN power converter, which is applied for normal system operations. Conversely, as V_{EVA} goes high, M_{P1} is disabled. Instead, the smaller transistor M_{P2} is enabled in the pull-up path, which achieves a weak gate driving strength for low *dv/dt* operation. This mode is designed to improve the readout resolution for closed-loop t_{on} sensing. Third, as V_{SNS} becomes high for a short period, all three driving paths comprising M_{P1}, M_{P2} and M_{N1} are OFF, allowing the gate leakage current to

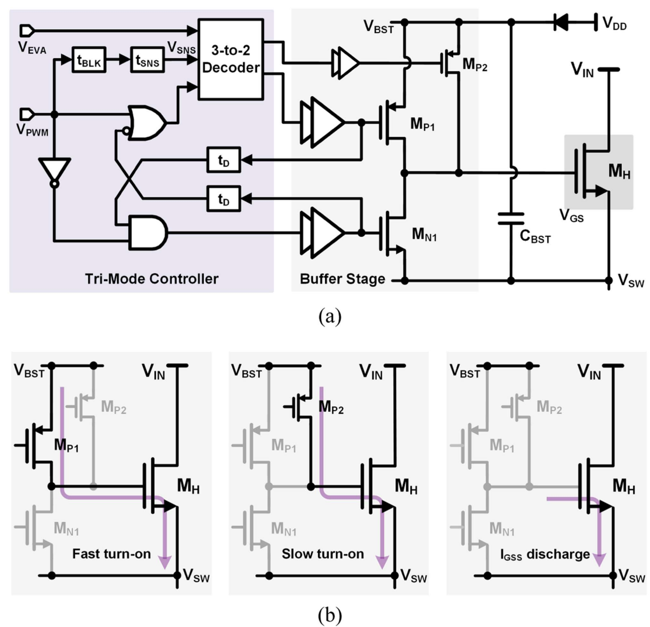


Fig. 8. Reconfigurable trimode gate driving. (a) Circuit implementation. (b) Operation modes.

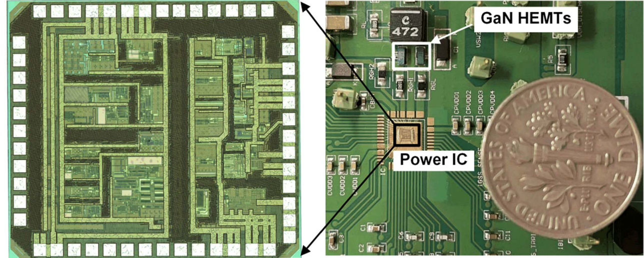


Fig. 9. Photographs of IC die and test PCB.

discharge the gate capacitance for I_{GSS} sensing. As a result, the three gate driving modes will be reconfigured based on the demands of system operation and device health evaluation. Note that the level shifters for signal isolations of V_{PWM} and V_{EVA} are omitted in the schematic.

V. Experimental Verification

To validate the on-chip CM approach, an IC prototype is implemented by a 180-nm high-voltage BCD process [23]. The closed-loop t_{on} sensor, I_{GSS} sensor, gate driver, and PWM controller are integrated on chip with an active area of 1.3 mm^2, as shown in Fig. 9. Adopting two enhancement-mode GaN power transistors as the power switches, the half-bridge power converter is used to evaluate the effectiveness of the proposed CM method. The GaN converter operates in an input voltage ranging from 5 to 24 V with a switching frequency of 1 MHz while delivering a maximum power of 5 W.

To verify the closed-loop t_{on} sensing method, Fig. 10 shows the measured V_{SW} and V_{ton} waveforms at 1 MHz. The voltage scaling factor of β is set to 5 for the 12-V input voltage. During the rising edge of switching node V_{SW}, the S/H circuit is

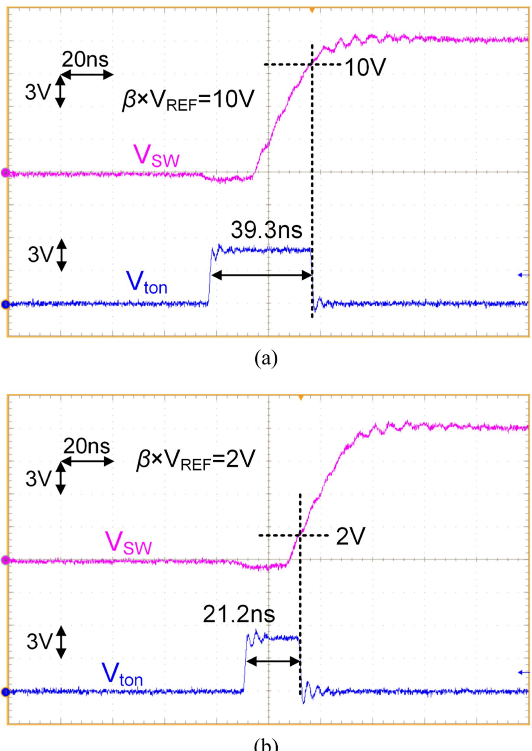


Fig. 10. Closed-loop t_{on} sensing real-time measurement results with (a) 10-V V_{SW} reference and (b) 2-V V_{SW} reference.

enabled to sample the moment when V_{SW} crosses the predefined reference voltage through a self-regulated sampling mechanism. For example, as shown in Fig. 10(a), when the reference with respect to V_{SW} is set to 10 V, the falling edge of sampling control signal V_{ton} is aligned to the point where V_{SW} hits 10 V. And V_{ton} in this case is measured as 39.3 ns without any propagation delay. Similarly, V_{ton} for a reference of 2 V is measured as 21.2 ns, as shown in Fig. 10(b).

To validate the proposed I_{GSS}-based failure monitoring, Fig. 11 shows the measured V_{GS} and V_{GSS} waveforms. During the on-time of the high-side power switch, the gate driver is disabled for a short duration, allowing the gate leakage current to slightly discharge the gate capacitance. As shown in Fig. 11(a), for a fresh health device, the voltage drop on V_{GS} is negligible and only causes a 160 mV increase on amplifier's output V_{GSS}. However, as device is near dielectric failure, a significant increase in I_{GSS} leads to a noticeable voltage drop in V_{GS}. As shown in Fig. 11(b), V_{GSS} in this condition quickly increases to 860 mV, which triggers the failure detection signal V_{FD} in the dielectric failure monitoring. Meanwhile, the gate driver is re-enabled to ensure that V_{GS} will not be discharged below the device threshold voltage.

Fig. 12(a) shows the measured V_{GS} and V_{SW} waveform under the high-performance mode. The proposed gate driver can accommodate a common mode transient immunity (CMTI) of 10 V/ns. During the aging evaluation phase, the gate driver is reconfigured to achieve a lower *dv/dt* of 0.4 V/ns, as shown in Fig. 12(b).

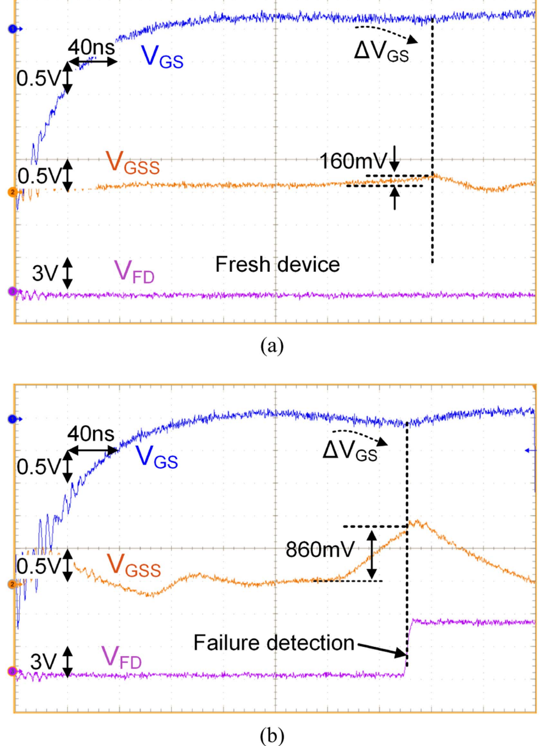


Fig. 11. I_{GSS} sensing measurement waveforms of (a) fresh device and (b) device near dielectric failure.

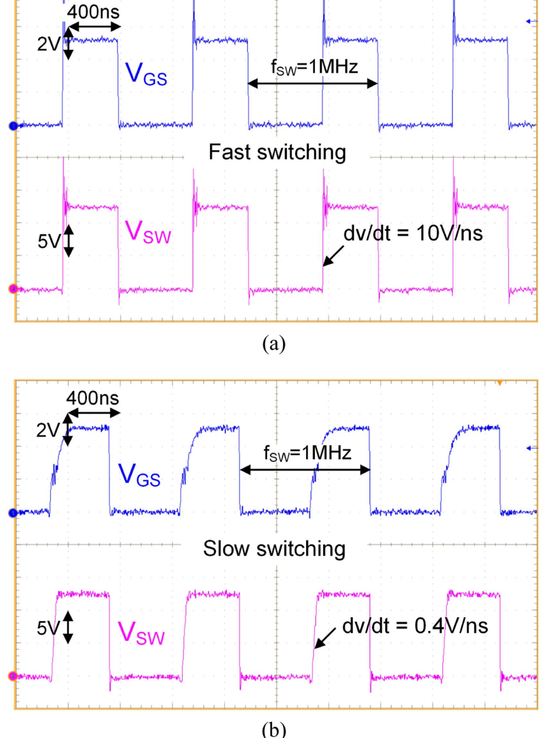


Fig. 12. Power converter measured key operation waveforms in (a) fast switching mode and (b) slow switching mode.

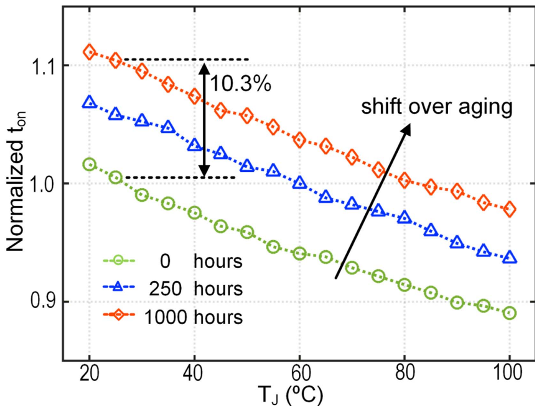


Fig. 13. Measured precursor t_{on} at different junction temperatures over accelerated aging test.

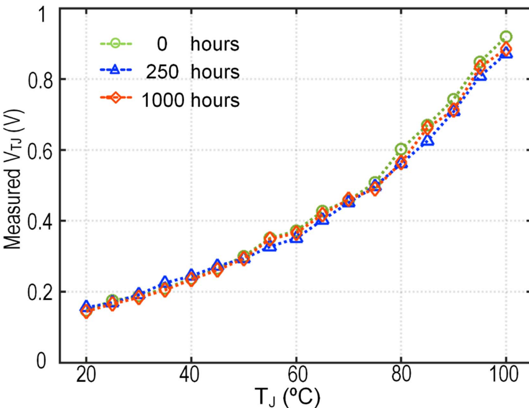


Fig. 14. Measured V_{TJ} for I_{GSS} sensing at different junction temperatures over accelerated aging test.

To validate the effectiveness of t_{on} as an aging precursor, the measured t_{on} over accelerated aging test is shown in Fig. 13. The high-temperature gate bias (HTGB) test is performed to accelerate the device gate oxide degradation due to high electric field and high temperature simultaneously [18], [20]. The measured precursor t_{on} is normalized at different junction temperatures for comparison. A positive shift of 10.3% of t_{on} after HTGB test has been observed, which is consistent to the theoretical analysis in Section II. Meanwhile, as temperature increases, t_{on} decreases as shown in Fig. 13. Therefore, the temperature effect on precursor t_{on} must be decoupled from aging effect to avoid false alarms.

To detect the device junction temperature, V_{TJ} is read from the peak value of V_{GSS}. Fig. 14 shows the measured V_{TJ} from 20 °C to 100 °C based on the I_{GSS} sensor. V_{TJ} is highly dependent on junction temperature but has negligible change over HTGB test, which validates the effectiveness of I_{GSS} as a temperature sensing parameter.

Finally, T_J data is correlated to precursor t_{on} to remove the temperature effect, leading to T_J-independent t_{on}'. As shown in Fig. 15, the temperature dependency of aging precursor is reduced from 13% to 2.3% thanks to the T_J calibration effort.

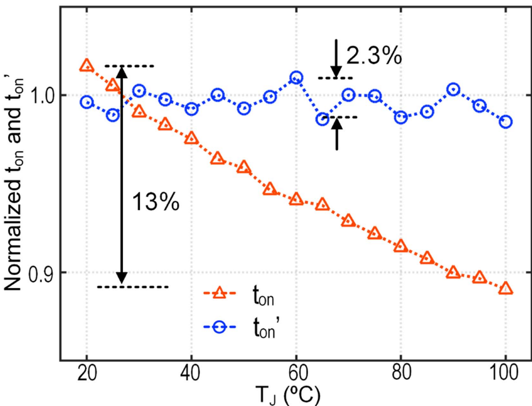


Fig. 15. Measured temperature independence of precursor t_{on}' by T_J calibration.

VI. Conclusion

In this article, an on-chip CM approach for concurrent GaN device aging prognosis and dielectric failure detection is presented. The approach utilizes a closed-loop sensing scheme to measure the turn-ON transient delay t_{on}, effectively mitigating precursor readout inaccuracy attributed to propagation delays. To further enhance monitoring precision, a junction temperature T_J calibration mechanism is implemented to remove the temperature dependence of precursor t_{on}, achieving temperature-independent aging prognosis. Meanwhile, dielectric failure detection is facilitated through a gate leakage current I_{GSS} sensing scheme, efficiently sharing the same circuitry with the T_J sensor, thus reducing design overheads significantly. Additionally, a reconfigurable tri-mode gate driver is developed to enable flexible switching conditions, accommodating both device aging evaluation and standard system operation. Validated successfully by experimental results on a GaN half-bridge power converter, the design ideas and circuits demonstrate their effectiveness.

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