Investigation on Single Pulse Failure of Avalanche Transistors Triggered by Voltage Ramps in Marx Bank Circuits

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***Abstract*—Although the Marx bank circuit (MBC) based on the avalanche bipolar junction transistor (ABJT) is widely used in the field of pulse power generators, the main trouble that ABJT triggered by voltage ramp is prone to failure still exists. To explain the obvious reliability differences of ABJTs triggered by voltage ramps of different *dV/dt* in MBC, the degradation and failure features under a single switching event are analyzed. The normal current path and the leakage current path of the failed device are compared by optical visualization to determine the failure point. A three-dimensional model is established to summarize the voltage ramp triggering conditions and the influence factors. The variations of the current path and the temperature distributions are analyzed by corresponding physical models. The results show that the current path triggered by the slow voltage ramp is easily confined to the device edge due to the insufficient displacement current. The formation of the current filament is related to the way of electron injection and causes the local overheating to damage the main junction. The degraded device completely fails during turning off due to the repeated formations of current filament leading to thermal runaway. The consistency between experimental results and simulations verifies the validity of the explanations. A reference is provided for the optimization of MBC based on ABJT.**

***Index Terms*—Avalanche transistor, dynamic avalanche, failure analysis, filamentation, Marx-bank generator, semiconductor device modeling.**

I. Introduction

HIGH voltage repetitive pulses are used in multiple applications, such as biomedical treatment [1], ultra-wideband radar [2], material modification [3], pseudospark switch [4], and underwater electrical discharge [5]. The applied pulses require a high repetitive rate, nanosecond or subnanosecond rising edge, narrow pulsewidth, and high output amplitude [6], [7]. These properties bring considerable challenges to the design of the pulse generator and the adopted power switch, which is the key component. As a pulse power semiconductor switch, the avalanche bipolar junction transistor (ABJT) has the advantages of ultrafast switching speed [8], high current density [9], low residual voltage [10], compact size [11], and commercial availability [12], which attract much attention in the field of pulse power technology.

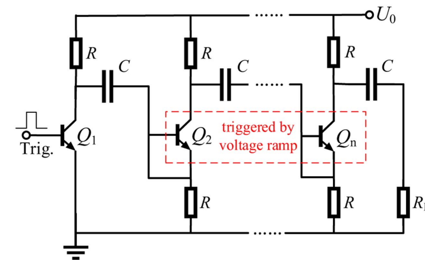

Fig. 1. $1\times N$-stage MBC with $Q_{2\text{-}n}$ triggered by voltage ramp.

To improve the output amplitude and the peak power, the Marx bank circuits (MBCs) based on ABJTs are constructed, which is a promising solution for generating pulses in the nanosecond range due to the advantages of compact structure, good scalability, and low input voltage requirements [13], [14]. As shown in Fig. 1, the most typical $1\times N$-stage MBC has N stages of capacitors and switches. The capacitors are discharged in series by triggering the switches step by step to achieve the pulse amplitude multiplication on the load. Different topologies are further developed based on the $1\times N$-stage MBC to increase the output voltage and current amplitude. The $M\times N$-stage MBC connects M ABJTs in series at each stage and balances the simplicity of structure and the high-voltage output, which is mainly used to generate relatively high-voltage (>5 kV) pulses [15]. The pulse amplitude has an evident saturation tendency by further increasing N or M due to the limited current capacity, limited power dissipation capacity, and the presence of conducting resistance of ABJTs [16]. Therefore, several multiplex power synthesis topologies adopting the pulse generating units $M\times N$-stage MBCs (including $1\times N$-stage MBCs) have realized for generating higher amplitude, such as direct pulse adding [17], MBC with microstrip power combiner [18], MBC with transmission line transformer [19], MBC with linear transformer driver (LTD) [20], spatial radiation power combining [21], and the hybrid pulse combining topologies based on the above [22].

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Although the hybrid topology with MBC as a superposition unit is relatively simple because of multiple ABJTs operating in voltage ramp triggering mode, the problem of low reliability of this triggering mode also comes out. That is, the device reliability is still the main trouble in these types of MBCs based on ABJTs. Take $1\times N$-stage MBC as an example, as shown in Fig. 1, except that the first device is triggered through base, the rest of the devices with base-emitter shorted are triggered by voltage ramps. Various research works show that ABJTs triggered by voltage ramps are highly susceptible to failure [23], [24], [25], [26], which greatly reduces the reliability of MBC and limits the applications of high pulse repetition frequency (PRF). The most vulnerable device to failure generally located at the second stage of $1\times N$-stage MBC where it is first triggered by a voltage ramp [27]. Moreover, the failure of ABJTs at the first stage of $M\times N$-stage MBC is similar to and more serious than the failure of second-stage ABJT in $1\times N$-stage MBC [28]. Although some topologies are adopted to improve the reliability of ABJT [28], [29], [30], [31], the rising edge, the time delay, and the amplitude of the output pulses are also affected in different degrees [23], [28], [32]. The causes of device failure are still controversial, such as the heat accumulation under high PRF conditions [33], the strong electrical stress during the switching transients [26], and the variation in the width of the current path [27], [34]. Besides, the devices always fail one after another in MBC under high PRF conditions [28], and the failure causes are still unclear.

So far, there are few systematic studies on the failure mechanism of ABJT triggered by voltage ramp in MBC. The characteristics and the possible causes of the device failure deserve further study. Previous studies show that the base-triggered ABJT can switch multiple times in the avalanche region [35], [36], with nondestructive current distribution and three-dimensional (3-D) variations of the width of the current path [37], [38], [39], [40]. The mechanism of ABJT triggered by a voltage ramp with faster switching speed is explained [34], but the current density distribution is considered to be quasi-uniform. The 3-D transient characteristics of the current path are closely related to the device failure, which has not been investigated. This work shows that the *dV/dt* of voltage ramp triggering ABJTs in MBC is obviously different. It makes the second stage most prone to failure and has the properties of degradation and failure in a single switching event. The current filamentation appears obviously in both the turning ON and turning OFF phases, and it is closely related to the *dV/dt* of the triggering voltage ramp. The current filamentation means that most of the current path concentrates in a small area and is associated with local overheating [41], [42].

To explain the causes of ABJT failure in MBC, this work is organized as follows. In Section II, the working principles of MBC and ABJT are analyzed. The switching transients and static characteristics of the degraded and failed devices are tested. The reasons for the progressive failure of devices in MBC are explained. The normal current path, the failure leakage current path, and the failure point of the device are observed, respectively. In Section III, the simulation is established according to the device structure. The voltage ramp triggering conditions and the influence factors are analyzed. In Section IV, the degradation and failure caused during the turning ON and turning OFF phases are analyzed, respectively. Section V concludes this article.

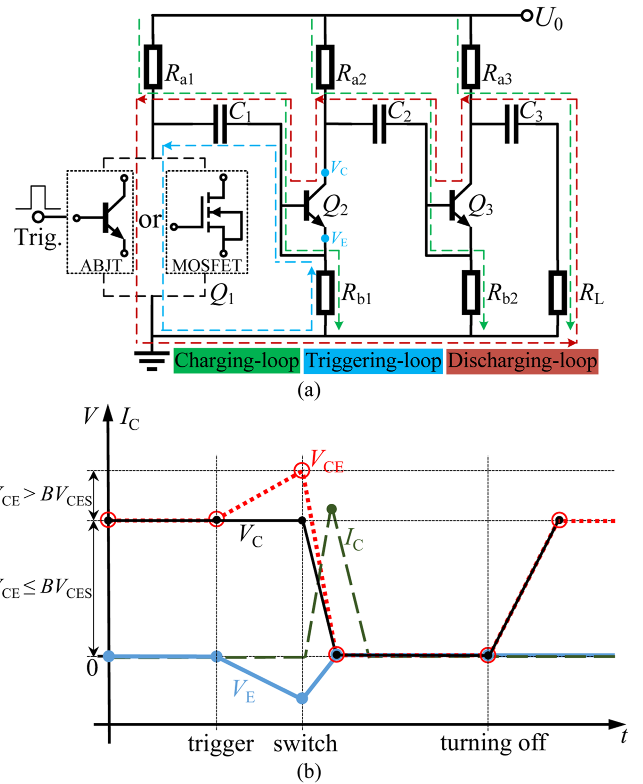

Fig. 2. (a) 1×3-stage MBC. (b) Switching and turning off waveform of ABJT (as Q_2) triggered by voltage ramp.

II. Experimental Observation of Thermal Failure

A. Experimental Setup and Switching Waveforms of ABJT

The tests applying voltage ramps of different *dV/dt* to ABJTs are carried out by the 1×3-stage MBC. Fig. 2(a) shows the schematic of the test circuit, which consists of switching devices Q_1–Q_3, capacitors C_1–C_3, and resistors R_{a1}–R_{a3}, R_{b1}–R_{b2}, R_L. Q_2–Q_3 are 320 V/180 V/60 A (V_{CES}/V_{CEO}/peak collector current) ABJTs (FMMT417) manufactured by Diodes [12]. Q_1 is an ABJT or a 500 V/24 A/0.14 Ω ($V_{DSS}/I_D/ R_{DS(ON)}$) MOSFET (SW24N50D) manufactured by Samwin to generate two different switching speeds [43]. Fig. 2(b) shows the switching and turning OFF waveform of ABJT triggered by the voltage ramp. The main parameters of the circuit elements are shown in Table I. The test platform is shown in Fig. 3. The test circuit is connected to the dc power supply and driving module to generate voltage pulses, which are observed by the high-voltage probe and oscilloscope. The main parameters of the hardware setups are in reference [44].

The working principle of the test circuit is explained below. At the charging state, Q_1–Q_3 are turned OFF and C_1–C_3 are charged along the charging loops and keep the voltage constant at U_0. At the triggering state, a drive signal is input to the base of Q_1 to turn ON it. C_1 discharges along the triggering loop and

TABLE I
MAIN PARAMETERS OF THE CIRCUIT ELEMENTS

Circuit elements	Parameters
DC power supply (U_0)	300 V
ABJT (Q_1, Q_2 - Q_3)	FMMT417
MOSFET (Q_1)	SW24N50D
Main capacitors (C_1 - C_3)	680 pF
Charging resistors (R_{a1} - R_{a3})	10 kΩ
Triggering resistors (R_{b1} - R_{b2})	10 kΩ
Load (R_L)	50 Ω

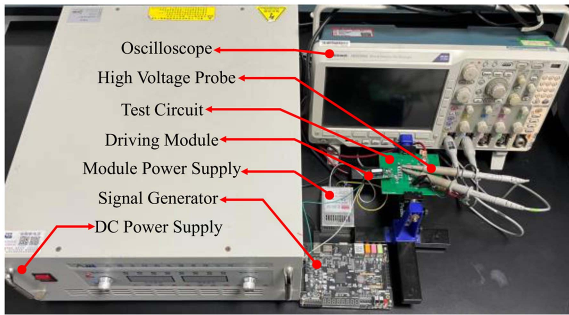

Fig. 3. Hardware setup and test platform.

produces a negative pulse on R_{b1}. As shown in Fig. 2(b), the emitter potential V_{E} of Q_2 changes from ground to negative, and the collector-emitter voltage V_{CE} rises and exceeds V_{CES}. Q_2 is turned ON due to the overvoltage. C_1–C_2 discharge in series to trigger Q_3, which is turned ON in the same way as Q_2. At the discharging state, C_1–C_3 discharge along the discharging loop with Q_1–Q_3 in series and produce a voltage pulse on the load R_{L}.

Fig. 4 shows the switching waveforms of ABJT triggered through base (Q_1) and triggered by voltage ramps of different *dV/dt* (Q_2 and Q_3). Q_1–Q_3 maintain voltage U_0 (300 V) before being triggered. When Q_1 is triggered through the base, V_{CE} decreases from U_0, as shown in Fig. 4(a). When Q_2–Q_3 are triggered by voltage ramps, V_{CE} increases from U_0 (300 V) to overvoltage (~400 V), and then V_{CE} quickly decreases to ~30 V accompanied by the device turned ON, as shown in Fig. 4(b) and (c). A current pulse with the amplitude of ~20 A is generated on R_{L}. Obviously, the switching speed of ABJT triggered through the base as Q_1 is much lower than that of Q_2 triggered by the voltage ramp. This results in a voltage ramp of 6 V/ns triggering Q_2, which is lower than the 100 V/ns voltage ramp triggering Q_3. The failure of Q_2 due to slower voltage ramp triggering is inevitable in a conventional $1\times N$-stage MBC. The avalanche process of ABJT triggered through the base (as Q_1) is negatively affected by the insufficient base injection current component and the insufficient total current passing through the device [10]. The possibility of a slower turning-ON speed of Q_1 results in a voltage ramp of lower *dV/dt* than 6 V/ns provided in Fig. 4(b). Moreover, the phenomenon that ABJT is triggered by a slower voltage ramp is more pronounced in the first stage of $M\times N$-stage MBC [28]. Therefore, considering the extreme conditions of slow voltage ramp triggering, the MOSFET is used as Q_1 to adjust the *dV/dt* of the voltage ramp that triggers Q_2 to be 1 V/ns, by changing the gate resistance on the driver module, as shown in Fig. 4(d). The experimental results show that the risk of device failure increases sharply with the decrease of *dV/dt* under the voltage ramp triggering condition. ABJT under the 1 V/ns triggering condition usually fails after a single switching event. The survival rate of ABJT under the 6 V/ns triggering condition is a little higher, but its normal switching times are often below $\sim 10^5$ times, far lower than the normal lifetime (4×10^{11} times) in the product manual [12].

B. Failure Determination of Single Switching Event

The degradation and failure of Q_2 triggered by 1 V/ns voltage ramp during a single switching event are tested as follows. Fig. 5(a) shows the waveform of the last test before degradation. The single switching period is ~40 μs. After Q_2 completes a switching and the test circuit generates a current pulse (~20 A) on the load R_{L}, C_1–C_3 are recharged along the charging loop. V_{CE} of Q_2 rises again to U_0 (300 V) in the turning OFF and recharging phase. The emitter potential V_{E} is 0 V and the collector potential V_{C} is 300 V. The leakage current ($I_{\mathrm{C(leakage)}} \approx V_{\mathrm{E}}/R_{\mathrm{b1}} \approx (U_0 - V_{\mathrm{C}})/R_{\mathrm{a2}} \approx 0$) passing through Q_2 is not significant. The "leakage current" refers to the current that passes through the device when it is at OFF-state. Fig. 5(b) shows the typical degradation waveform of Q_2 subjected to thermal damage in a single switching event. V_{E} is about 10 V and V_{C} is about 290 V in the turning OFF and recharging phase. V_{CE} cannot return to U_0 (300 V) and is reduced to ~280 V. Therefore, a leakage current ($I_{\mathrm{C(leakage)}} \approx V_{\mathrm{E}}/R_{\mathrm{b1}} \approx (U_0 - V_{\mathrm{C}})/R_{\mathrm{a2}} \approx 1$ mA) passes through the loop of U_0–R_{a2}–Q_2–R_{b1}–GND. Fig. 5(c) shows the waveform of Q_2 from degradation to complete failure after a single switching event. V_{CE} of the degraded Q_2 cannot rise to 400 V when it is triggered by the same voltage ramp. Q_2 repeatedly fails to turn off in the recharging phase until Q_2 cannot withstand voltage. When Q_2 is shorted out, a current path is formed between the collector and emitter and U_0 is mainly applied to R_{a2} and R_{b1}. Meanwhile, Q_3 triggered by 100 V/ns voltage ramp does not show any degradation features in the single switching event, with relatively high reliability.

The degradation and failure characteristics are evident in the junction blocking voltage. Fig. 6 shows the blocking voltage curves of collector-base (c-b) junction V_{CBO} and emitter-base (e-b) junction V_{EBO}. The results show that the c-b junction has obvious degradation and finally fails. The failure mode is due to the increase of the leakage current of c-b junction making the blocking voltage drop close to zero. While the e-b junction remains intact before and after the device failure.

V_{CBO} of failed c-b junction at repeated pulse condition is lower than that at a single pulse condition, presenting a more complete failure. This is due to the fact that the $1\times N$-stage MBC continues to work after the failure of Q_2, which also leads to the failure of the subsequent stages Q_3–Q_{n}. As shown in Fig. 7, when Q_2 is damaged and shorted out, C_2 cannot be charged due to the equal potentials at both ends. When the next trigger signal

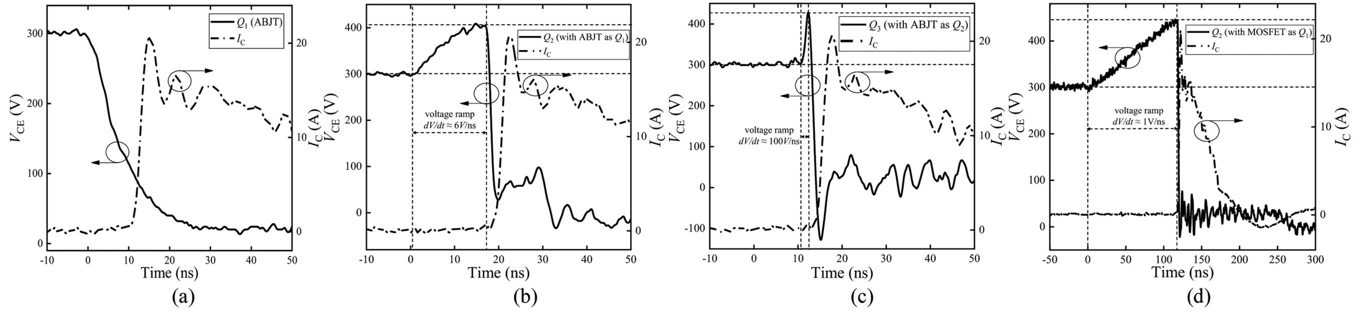

Fig. 4. (a) Switching waveform of ABJT triggered through base as Q_1. (b) Switching waveform of Q_2 is triggered by Q_1 (ABJT). (c) Switching waveform of Q_3. (d) Switching waveform of Q_2 is triggered by Q_1 (MOSFET).

turns Q_1 ON, C_1 discharges and produces negative pulses on both R_{b1} and R_{b2}. The initially damaged c-b junction of Q_2 is again subjected to the thermal effect of pulse current, resulting in more complete failure. Meanwhile, the slower switching speed of Q_1 results in a slower voltage ramp to trigger Q_3, as shown in Fig. 7(b). Q_3 is in a vulnerable switching state.

C. Observation and Comparison of Current Paths

The actual failure characteristics are determined by observing the leakage current distribution of the device. The formation of the current path is observed by the photon emission microscope (PEM), which captures the photons radiated from the electron-hole recombination. Fig. 8(a) shows the e-b junction interface of ABJT without package under the optical microscope (OM). Those small shadow spots on the chip surface are impurities after the package is dissected. The test circuit in Fig. 2(a) is used to generate repeated current pulses with an amplitude of $\sim$20 A. Our work [45] shows the current path distribution of the device triggered by the voltage ramp and successfully turned ON, as shown in Fig. 8(b). The current path in Fig. 8(b) is concentrated in the center of the device and around the p-base short-circuit point.

The failed device is further investigated by the OM and the PEM. The e-b junction and the surface contact layer of the chip have no obvious failure point. The c-b junction in the failed device is unable to withstand voltage due to the existence of leakage current. As shown in Fig. 8(c), the leakage current path is presented under PEM by applying stable 30 mA direct current to the c-b junction of the failed device. The failure point is located at the corner of the e-b and c-b junctions. Furthermore, the ion milling system is used to grind the chip surface and show the c-b junction to find the exact failure point, as shown in Fig. 8(d). The failure point with the diameter of 10–20 μm is located at the corner of c-b junction, which is small enough compared with the entire c-b junction interface. The leakage current paths of devices which are failed under the 6 V/ns voltage ramp triggering and repeated pulse condition, and under the 1 V/ns voltage ramp triggering and single pulse condition are observed, respectively. Surprisingly, both of them show similar failure phenomena, which means that the devices triggered by slow voltage ramps in MBC have similar failure properties.

As shown in Fig. 8(b), the opinion that the concentration of current paths in the center of the device in the successful switching events may cause heat accumulation under the repeated pulse conditions is reasonable. However, the leakage current path of the failed device is different from the conductive current path under the successful switching event. It indicates that the failure mode triggered by a low *dV/dt* voltage ramp is more serious. The current density and temperature rise at the failure point must be dramatic, which causes the device damaged in a single switching event. This is why Q_2 is always damaged first in the 1×3 stage MBC. To explore the failure mechanism, the simulation analyses of the transient avalanche process triggered by the voltage ramp are carried out in the following sections.

III. Simulation Setup

A. Device Model and Simulation Circuit Setup

Fig. 9 shows the doping structure and the cross-sectional structure, which are obtained from the actual device and used for Sentaurus TCAD simulations. As shown in Fig. 9(b), the model block containing the normal current path and the leakage current path is intercepted to simulate the variations of the current path under the different *dV/dt* voltage ramp triggering conditions. The simulation model emphasizes the actual doping distribution of e-b-c junctions, the relative position and size of the p-base short-circuit point, and the improvement of electric field distribution on c-b junction by terminal design. The voltage ramp with adjustable *dV/dt* is used as the triggering pulse and the existence of the bonding wire and other packaged inductors is represented by inductance L, which are combined with the actual conditions. The physical models include mobility, recombination, bandgap narrowing, thermodynamic, and impact ionization in simulation. The emitter and base interfaces, which are linked to the bonding wires, are set to adiabatic. The collector interface, which is connected to the copper substrate, is set to diabatic.

B. Influence Factors of Voltage Ramp Triggering

The mechanism of ABJT triggered by voltage ramp with base-emitter shorted is that the *dV/dt* effect creates a displacement current to pass across the c-b junction capacitance, and the nonequilibrium holes are formed in p-base region to cause electrons injection from the emitter to initiate the avalanche

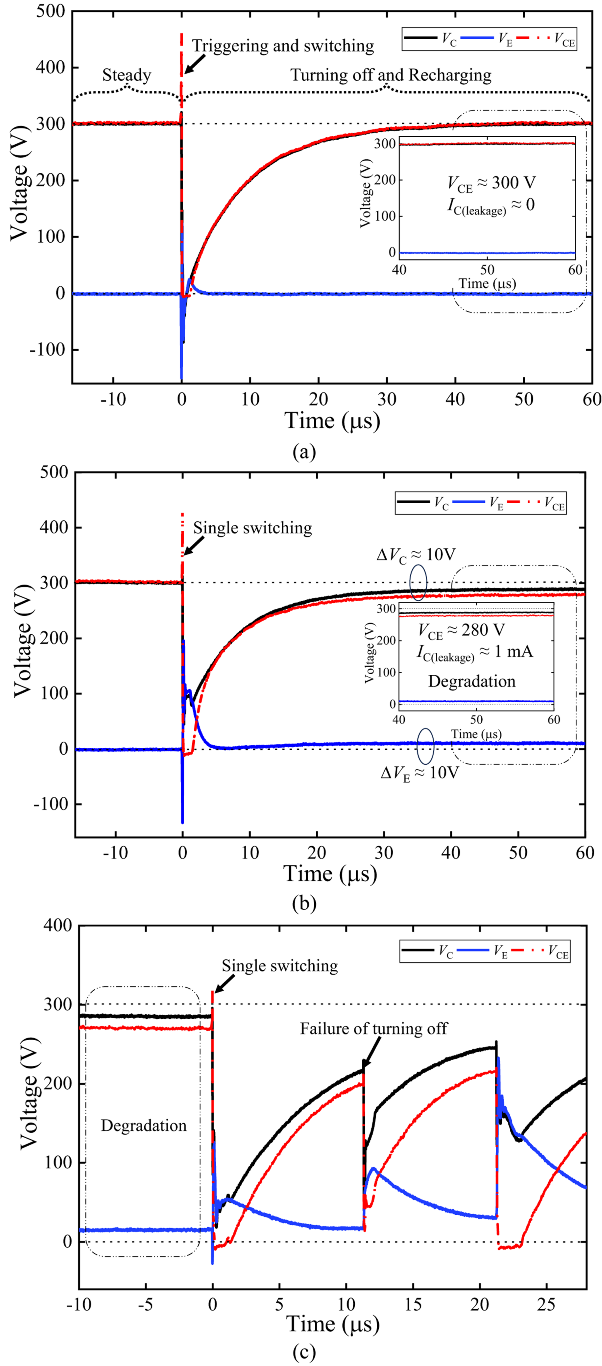

Fig. 5. Measured typical single switching waveforms of ABJT. (a) Last test before failure. (b) Degradation of ABJT after a switching event. (c) Degraded ABJT fails after a switching event.

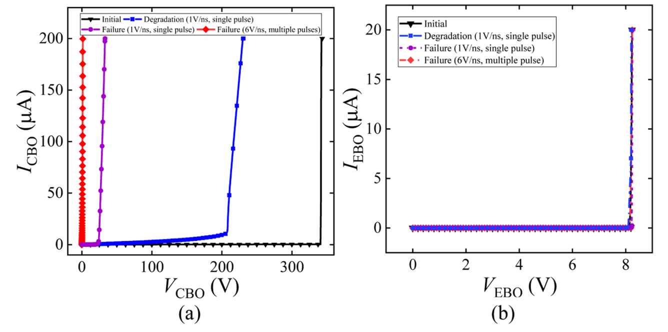

Fig. 6. Comparison of blocking voltage curve traces of ABJTs in the normal state, degraded state, and the failed state. (a) Curve traces of V_{CBO}. (b) Curve traces of V_{EBO}.

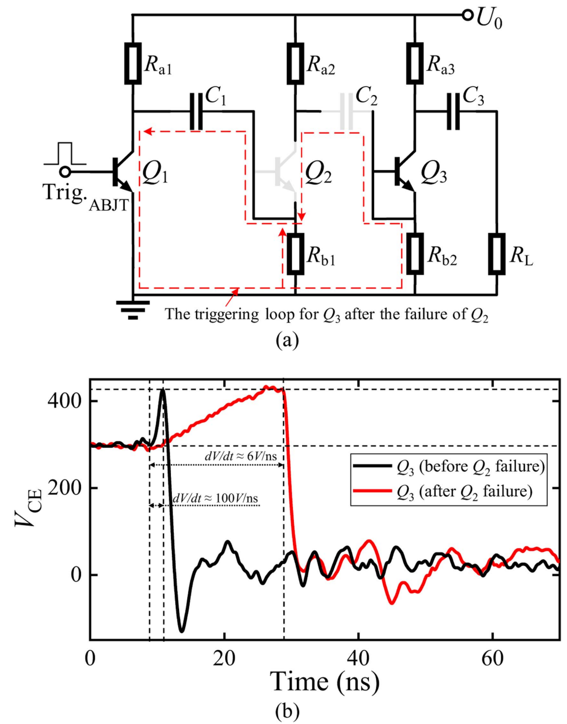

Fig. 7. (a) Triggering-loop for Q_3 after the failure of Q_2 in 1×3-stage MBC. (b) Switching waveform of Q_3 before and after the failure of Q_2.

process [34]. The leakage current path in the failed device is different from the normal current path, which means that the emitter electron injection path is affected by *dV/dt* effect and is related to the actual 3-D doping structure. As shown in Fig. 9(b), it is worth noting that the base electrode contacts the p-base region through both the short-circuit point and the e-b junction edge, which means that the collection path of nonequilibrium holes flow has two branches. Fig. 10 shows the distribution of nonequilibrium hole flow in the p-base region of 3-D model with equal scale and its schematic. The arrows in the figure represent the holes flow direction, and there is a clear dividing line along the paths of the nonequilibrium holes to the short-circuit point and the e-b junction edge. It means that the high potential at the dividing line makes it easy for emitter electrons to be injected around the p-base short-circuit point, which is consistent with the phenomenon in Fig. 8(b) that the normal current path concentrates in the device center.

In Fig. 9(b), r_{s} and r_{e} represent the base resistance distribution along the nonequilibrium hole flow paths to the short-circuit point and e-b junction edge, respectively. $r_{\mathrm{s}}/r_{\mathrm{e}}$ is composed of $r_{\mathrm{con(s)}}/r_{\mathrm{con(e)}}$, $r_{\mathrm{cb(s)}}/r_{\mathrm{cb(e)}}$, and $r_{\mathrm{b(s)}}/r_{\mathrm{b(e)}}$, which are shown in Fig. 9(b), and the items are described in Table II. r_{s} and r_{e} are

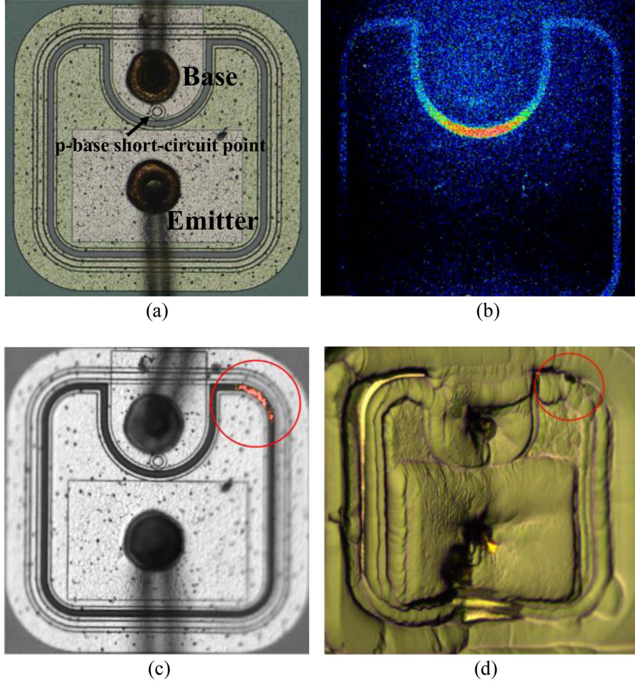

Fig. 8. (a) Chip top view of e-b interface. (b) Visualization of current path triggered by voltage ramp [40]. (c) e-b interface after the device failure and the leakage current path. (d) Chip top view of c-b interface and the location of the failure point.

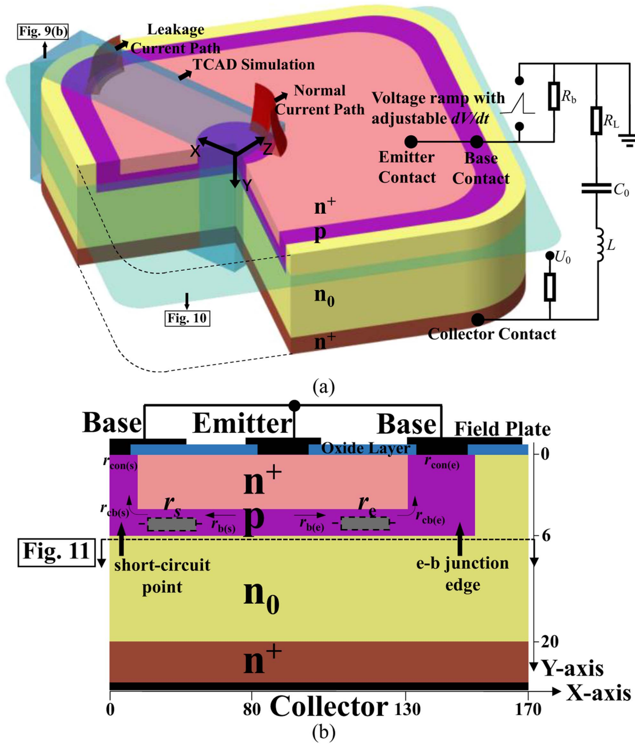

Fig. 9. (a) Three-dimensional doping structure of ABJT with the external circuit setup for TCAD simulation. (b) Cross-section of ABJT with p-base short-circuit point and e-b junction edge.

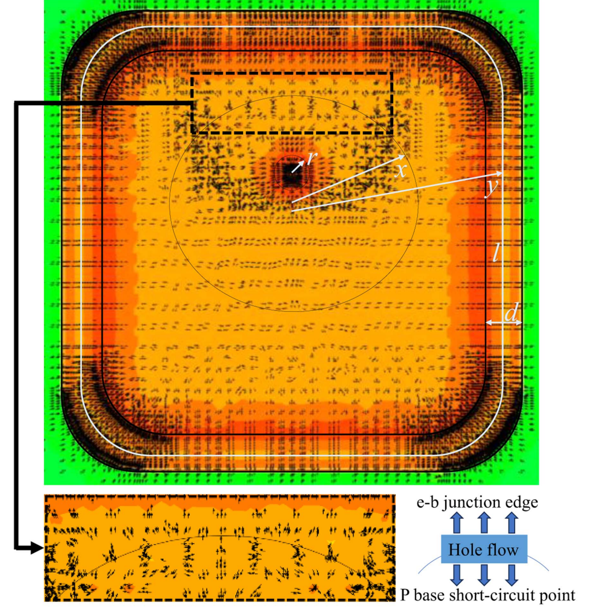

Fig. 10. Nonequilibrium hole flow distribution and its schematic. The interception surface is shown in Fig. 9(a). The *dV/dt* of the voltage ramp in trigger condition is set to 100 V/ns.

TABLE II
MAIN PARAMETERS IN FORMULA

Item abbreviation	Parameters
$r_{\mathrm{con(s)}}$, $r_{\mathrm{con(e)}}$	Ohm-contact resistance
$r_{\mathrm{cb(s)}}$, $r_{\mathrm{cb(e)}}$	Resistance under the base electrode contact area
$r_{\mathrm{b(s)}}$, $r_{\mathrm{b(e)}}$	Resistance under the active base region
C_Ω	Ohmic contact coefficient
$R_{\square\mathrm{cbs}}$, $R_{\square\mathrm{bs}}$, $R_{\square\mathrm{cbe}}$, $R_{\square\mathrm{be}}$	Square resistance of $r_{\mathrm{cb(s)}}$, $r_{\mathrm{b(s)}}$, $r_{\mathrm{cb(e)}}$, and $r_{\mathrm{b(e)}}$
S	Contact surface of c-b junction
$N_{\mathrm{Dn+}}$, N_{A}, N_{Dn0}	Impurity concentration of n_0-collector, p-base, and n^+-emitter

expressed as follows:

$$r_{\mathrm{s}} = \frac{C_\Omega}{\pi r^2} + \frac{R_{\square\mathrm{cbs}}}{8\pi} + \frac{R_{\square\mathrm{bs}}}{2\pi} ln\frac{x}{r} \quad (1)$$

$$r_{\mathrm{e}} = \frac{C_\Omega}{ld} + \frac{R_{\square\mathrm{cbe}}d}{3l} + \frac{R_{\square\mathrm{be}}}{2\pi} ln\frac{y}{x}. \quad (2)$$

As shown in Fig. 10, the results of r_{s} and r_{e} are based on the premise that the holes flow passing through the short-circuit point is simplified into a circular distribution, and the holes flow passing through the e-b junction edge is simplified into a hollow circular distribution. I_{s} and I_{e} represent the displacement current leading to the short-circuit point and the e-b junction edge, respectively, and are expressed as follows:

$$I = I_{\mathrm{s}} + I_{\mathrm{e}} = S\sqrt{\frac{\varepsilon_{\mathrm{s}} q N_{\mathrm{Dn_0}}}{2V_{\mathrm{CE}}}}\frac{dV}{dt}. \quad (3)$$

The c-b junction capacitance is nonlinear and varies with the applied voltage V_{CE}. The voltage ramp triggering condition to

initiate the avalanche process is that the transverse voltage drop generated by the displacement current is greater than the built-in potential of e-b junction V_{bi}, which is given by

$$V_{\text{bi}} = \frac{kT}{q}\, ln\left(\frac{N_{\text{A}} N_{\text{Dn+}}}{n_{\text{i}}^2}\right). \tag{4}$$

Therefore, the demand for *dV/dt* of voltage ramp is expressed by combining (1)–(4) as follows:

$$\frac{dV}{dt} > \frac{kT\,(r_{\text{e}}+r_{\text{s}})\,\sqrt{2V_{\text{CE}}}}{Sqr_{\text{e}}r_{\text{s}}\sqrt{\varepsilon_{\text{s}} q N_{\text{Dn}_0}}}\, ln\left(\frac{N_{\text{A}} N_{\text{Dn+}}}{n_{\text{i}}^2}\right). \tag{5}$$

The results show that the factors mainly affecting the *dV/dt* triggering efficiency are the location and relative size of the short-circuit point, the transient voltage V_{CE}, the doping concentration and area of bipolar junctions, and the temperature. According to the following parameters of device: V_{bi} (0.7–0.9 V), S ($\sim$1.6 $\times$ 10^{-5} cm^2), $N_{\text{Dn+}}$ ($\sim$1 $\times$ 10^{20} cm^{-3}), N_{A} ($\sim$1 $\times$ 10^{17} cm^{-3}), N_{Dn0} ($\sim$1 $\times$ 10^{14} cm^{-3}), and $V_{\text{CE(max)}}$ ($\sim$400 V), the critical *dV/dt* is approaching 100 V/ns. In the experiment results so far, there is no fixed critical *dV/dt* value for ABJT to distinguish the boundary between its accurate survival and failure. The ABJT triggered by a voltage ramp of 100 V/ns shows no significant damage after a single switching event, which means that 100 V/ns can be a reference value to ensure that the current path is formed normally in the device center and the device survives.

Previous research works did not consider the existence of the short-circuit point and the inhomogeneity of the overshot electric field when simulating the switching processes of ABJT triggered by a voltage ramp. Under the premise that the device structure and the environment temperature are determined, the most relevant factor that affects the *dV/dt* triggering efficiency and leads to the single switching failure is the transient voltage V_{CE}. When *dV/dt* is insufficient to enable emitter electron injection in the device center, V_{CE} increases. Since the device is triggered to overvoltage and V_{CE} ($\sim$400 V) exceeds V_{CES} temporarily, the blocking voltage of the c-b junction is largely dependent on the terminal efficiency. Fig. 11 shows the peak electric field distribution at the c-b junction edge and the improvement of the peak electric field by the terminal. The V_{CES} of device is $\sim$350 V, and the average electric field at c-b junction is $\sim$2.6 $\times$ 10^5 V/cm. The peak electric field at the junction edge is reduced after using the field plate as the terminal. However, the slightly protruding electric field spike at the c-b junction edge still has the possibility of causing leakage current before the triggering *dV/dt* makes the emitter electron injection when ABJT is triggered to overvoltage.

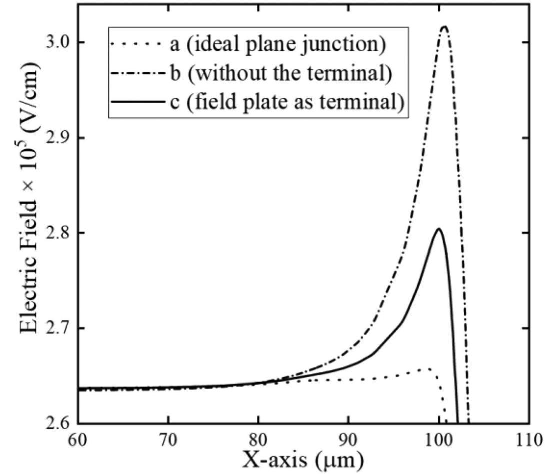

Fig. 11. Electric field distribution without considering the terminal (curve a), approaching the near-ideal breakdown of a plane junction (curve b), and taking the field plate as terminal (curve c). The interception surface is shown in Fig. 9(b).

IV. Results Discussion

A. Switching Transients Comparison of Different Dv/Dt

The ABJT triggered by 1 V/ns voltage ramp (as Q_2 in MBC) has degradation and failure features in a single switching event with the destructive current filament at the device edge, while the reliability of ABJT triggered by 100 V/ns voltage ramp (as Q_3) is much higher with current path located in the device center. The critical *dV/dt* in formula (5) making the device switch normally and the influence of actual electric field distribution are both taken into account. The model in Fig. 9(b) is captured from the 3-D model in Fig. 9(a) according to the actual distributions of current paths and is used to compare and analyze the switching transients under the 1 and 100 V/ns triggering conditions, respectively. As shown in Fig. 12, the simulated voltage and current waveforms in different *dV/dt* voltage ramp triggering conditions are matched with the measured waveforms. The measured waveforms are obtained from the test circuit in Fig. 2(a). Different moments in the simulation are captured to observe the switching transients, as shown in Fig. 13.

Fig. 13(a) and (b) shows the switching schematics of the device at 1 and 100 V/ns conditions, respectively. Time points t_1–t_5 in Fig. 13(c) and (d) show the process of device failure under the 1 V/ns condition, and points t'_1–t'_5 in Fig. 13(e) and (f) show the process of current path concentrated in the device center under the 100 V/ns condition. The current path formation and the temperature distributions and variations are explained as follows. The switching transients are divided into three phases.

At phase 1 (t_1, t'_1), the leakage current is formed at the c-b junction edge due to the device triggered by voltage ramp to the overvoltage ($\sim$400 V), which exceeds V_{CES} ($\sim$350 V) and the uneven distribution of electric field at the c-b junction edge. The initial carrier source of leakage current is attributed to the trap emission at the high electric field. The strength of leakage current at this phase is too weak to turn on the device.

At phase 2 (t_1–t_3, t'_1–t'_3), at the beginning of the switching, the current passing through the device increases and the current density distribution is different. The premises for the switching of ABJT triggered by the voltage ramp are the emitter electron injection and the impact ionization. For the device under 1 V/ns triggering condition (t_1–t_3), the displacement current effect is not enough to make the emitter electron injection due to the small *dV/dt*, which does not satisfy formula (5). The leakage current at the c-b junction edge is increasing and has the ability to cause the emitter electron injection. Our work [45] shows that this

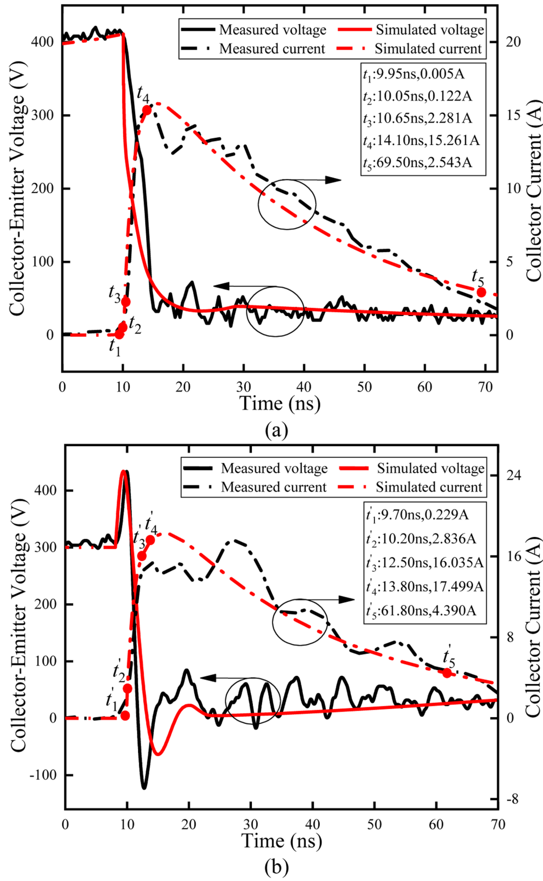

Fig. 12. Simulated voltage and current waveforms are compared with measured waveforms under the (a) 1 V/ns voltage ramp triggering condition, and (b) 100 V/ns voltage ramp triggering condition.

leakage current triggering mode makes the location of emitter electron injection competitive. It means the leakage current can be converted into the conductive current and concentrated in the device center without obvious damage after a single switching event, as shown in Fig. 5(a). The instability of the leakage current can cause the failure of emitter electron injection, keeping the device in the overvoltage state until the voltage ramp triggering ends. Moreover, points t_1–t_3 in this work show that the failure of the device in a single switching event is due to the fact that the leakage current triggers electron injection at the e-b junction edge, and the current path is not formed at the center of the device in the subsequent process. In contrast, points t'_1–t'_3 show that the emitter electrons are successfully injected by the displacement current, and the conductive path is located in the device center under the 100 V/ns triggering condition.

At phase 3 (t_3–t_5, t'_3–t'_5), these two current paths cause the differences in temperature distribution. The current path is confined to the e-b junction edge where a heat spot with the temperature of ∼1100 K is formed under the 1 V/ns triggering condition. The intrinsic carrier concentration in Si at such a lattice temperature is significantly higher than the doping in the p-base and the n_0-collector. It means that the current path is easily concentrated at the hot spot, forming a current filament and causing irreversible damage to the c-b junction in an actual single switching event. Literature [46] shows that the thermal effect of the current filament reduces the local impact ionization rate and induces a filament movement to counteract a strong local heating. As shown in Fig. 13(a) at t_4–t_5, although the filament has a tendency to move towards the center of the device during its formation, the thermally induced motion speed is much lower than that of local temperature rise, thus the formation of local overheating spot cannot be avoided. While the current path triggered by 100 V/ns voltage ramp is concentrated in the device center with a conductive width of ∼100 μm. The highest temperature of ∼850 K within ∼100 μm is located at the n_0-n^+ interface due to the dynamic reconstruction of the electric field. The intrinsic carrier concentration at this time has not exceeded n^+-collector doping. Under the high PRF conditions, there is a process of heat accumulation and the device with the temperature above 850 K is also prone to thermal failure. However, considering the actual operation scenarios of 1×N-stage MBC with Q_2 (1 V/ns) and Q_3 (100 V/ns) discharged in series, before the failure of Q_3 due to heat accumulation in repetitive current pulses, the failure of Q_2 under a single switching event occurs first, which makes Q_3 triggered by 1 V/ns voltage ramp and converted to the state of failure in a single switching event, passively.

The mechanisms of the current path confined at the e-b junction edge with the fatal local overheating (1 V/ns) and the current path in the device center (100 V/ns) with the ability to expand are explained below. First, the injection modes of emitter electrons are different. Our work [45] shows that the device can be turned on when $V_{\rm CE}$ rises to 370 V under the 100 V/ns triggering condition, which does not occur under the 1 V/ns triggering condition. It means that the emitter electrons are injected by the strong displacement current during $V_{\rm CE}$ rising, the injection intensity and width are much larger at the switching beginning compared with the leakage current triggering mode. Second, the expansion modes of the current path are different, which is caused by the dynamic reconstruction of an electric field during the process of $V_{\rm CE}$ drop. Fig. 14 shows the electric field distribution under the 1 and 100 V/ns triggering conditions. The high electric field is reconstructed at the n_0-n^+ interface during the turning-ON process. The electric field in the current path is modulated by the carriers and slightly weaker than the electric field outside the current path, thus a transverse electric field with the positive direction as the current path center is formed. The electrons at the n_0-n^+ interface are partially sucked in the transverse electric field and generate impact ionization to broaden the current path. Obviously, the current path at the center is broadened to both sides under the 100 V/ns triggering condition. In contrast, the current path located at the e-b junction edge is only widened from one side to the center, and the broadening capacity is limited due to the narrow reconstruction area of the electric field. Even though the device has two mechanisms (ambipolar carrier diffusion and hole drift) to broaden the current path along the p-base region, the spreading speed in the above-mentioned two mechanisms is much lower than the expansion speed of electrons absorbed by the transverse electric field at the n_0-n^+ interface. The intuitive evidence is that the current path with the expansion mechanism along the p-base region is distributed in a

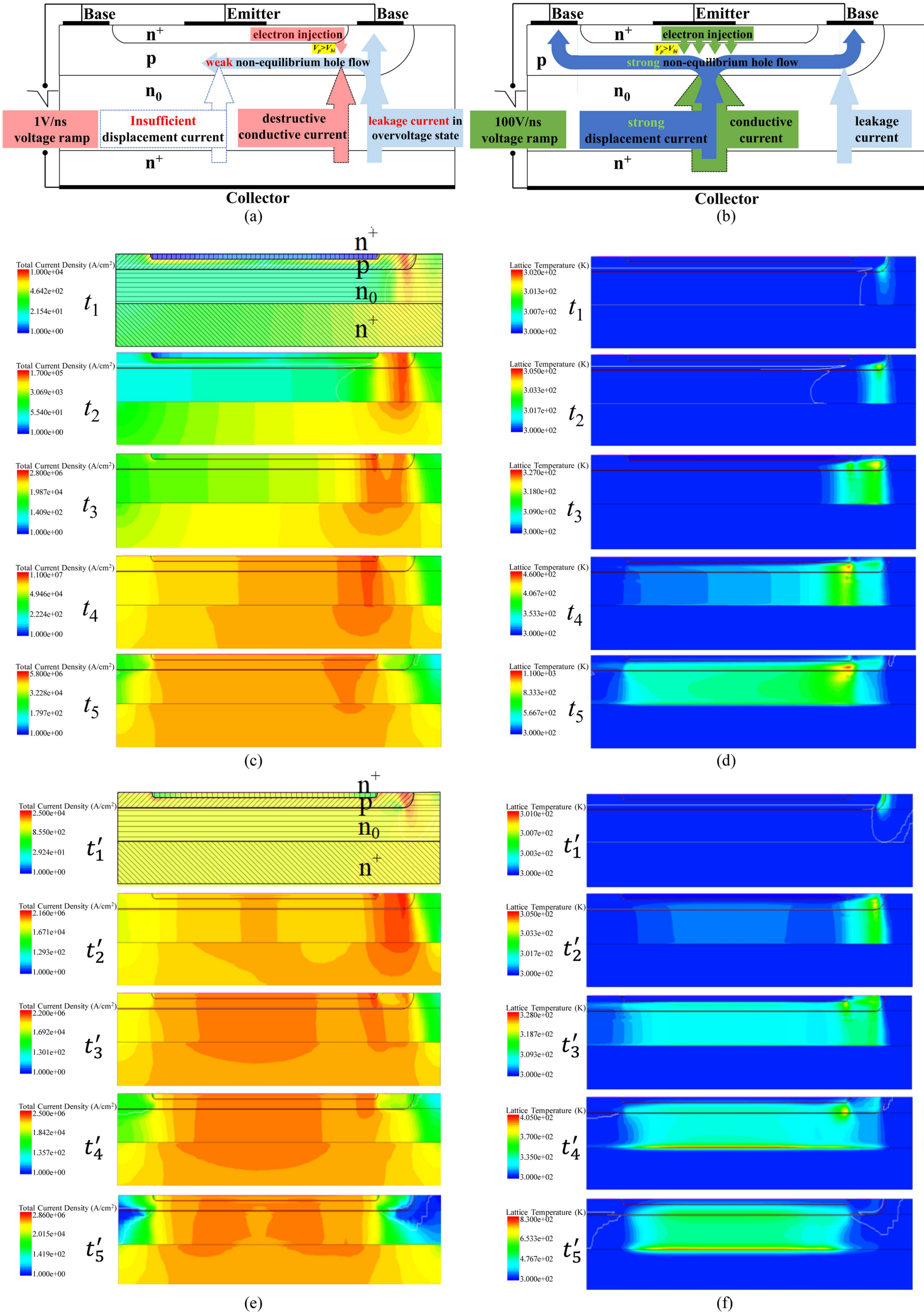

Fig. 13. Switching schematics with (a) 1 V/ns voltage ramp and a destructive current formation at the device edge, with (b) 100 V/ns voltage ramp and a conductive current formation at the device center. The formations of current paths and temperature distributions under the (c) and (d) 1 V/ns voltage ramp condition, and the (e) and (f) 100 V/ns voltage ramp condition.

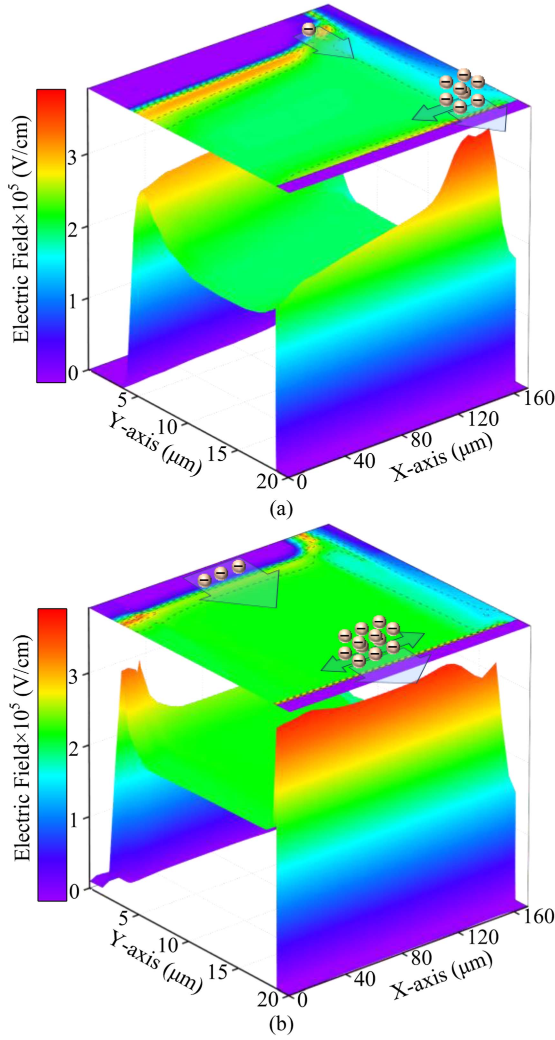

Fig. 14. Cross-sectional electric field distribution from Fig. 9(b) and the expansion mechanism of current paths under the (a) 1 V/ns voltage ramp triggering condition at $V_{\mathrm{CE}} = 320$ V, and the (b) 100 V/ns voltage ramp triggering condition at $V_{\mathrm{CE}} = 380$ V.

funnel shape along the Y-axis under 1 V/ns condition, as shown in Fig. 13(a) at t_5. While the current path with the expansion mechanism at the n_0-n^+ interface is distributed in a cone shape along the Y-axis under 100 V/ns condition, as shown in Fig. 13(b) at t'_5.

B. Current Filamentation During Turning OFF

The degraded device fails to turn OFF and loses the ability of blocking voltage during the recharging phase, as explained below. As shown in Fig. 15(a), the device subjected to thermal damage during the switching phase is simulated turning OFF and matched with the experimental waveforms. The simulated leakage current starts to increase without limit as V_{CE} approaches the breakdown point, which is an obvious thermal runaway. The sudden voltage drop without external triggering during the general voltage rising occurs simultaneously with the current filamentation at the failure point. This is different from the

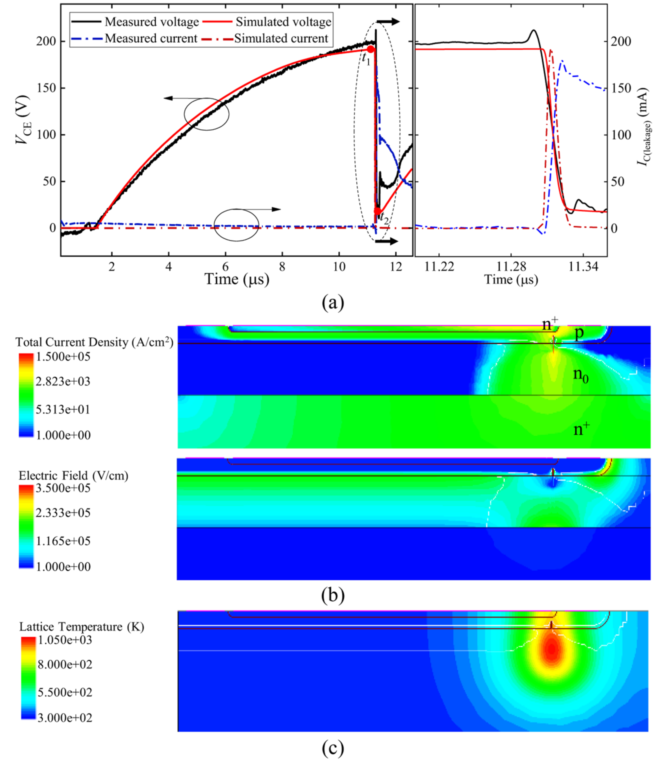

Fig. 15. (a) Simulated voltage and current waveforms during turning OFF are compared with measured waveforms. (b) Current density and electric field distribution at moment t_1 before voltage drop. (c) Temperature distribution at moment t_2 after voltage drop.

fully controlled devices, which are forcibly controlled off during conductive current passing, and the voltage rising causes the current concentrated to form a current filament. Fig. 15(b) shows the current density and electric field distribution intercepted at the moment t_1 before the sudden voltage drop in Fig. 15(a). The heating effect at the failure point causes a hole or channel of molten silicon located at the c-b junction with a local increase of impurity and trap concentration. As a result, the electric field spikes are prone to be concentrated at the failure point during turning OFF, which leads to the increase of the impact ionization rate and leakage current. And the local temperature increases strongly due to the high leakage current density. The avalanche-generated current filament is converted to be generated by the thermal effect. Fig. 15(c) shows the moment t_2 that the local temperature (∼1050 K) far exceeds the critical value where the inherent carrier concentration is greater than the doping concentration. The device enters a positive thermal feedback mode, which helps to form a stable current filament and leads to the thermal runaway and failure of turning OFF. More seriously, V_{CE} will rise again until the same thermal runaway phenomenon occurs at the failure point the next time, and the whole process stops when c-b junction completely fails.

V. Conclusion

To sum up, those ABJTs triggered by slow voltage ramps are the most prone to thermal failure and there is a problem

of step-by-step failure of devices in MBC due to the topology features. The complete failure of ABJT is caused by the current filamentation that exists in the switching period and the turning off phase. When the device is triggered by the leakage current in the overvoltage state and the emitter electron is injected at the e-b junction edge, the current path is formed and confined to the device edge, where the normal current path does not exist here. The formation of local overheating spot is accompanied by the degradation of c-b junction in a single switching event. The current filament is easily formed at the failure point during the turning off and recharging process, which causes the avalanche process to be triggered repeatedly and finally to the thermal runaway, forming a leakage current path at the c-b junction.

In principle, it is inevitable for ABJTs to be triggered by voltage ramps of different *dV/dt* in the typical MBC. The features of the ABJT triggered by slower voltage ramps are more significant in the first stage of M×N-stage MBC due to the uneven distribution of voltage ramps between the series ABJTs and the insufficient ability to trigger the series ABJTs to overvoltage. This investigation on the single pulse failure of device triggered by slow voltage ramp provides a reference for the new MBC topology with high reliability. For example, the triggering speed of MBC can be optimized by replacing the base-triggered ABJT with a fast-triggering circuit. For improving the device reliability under the voltage ramp triggering condition, the critical *dV/dt* can be reduced by adjusting the distribution of short-circuit points and reducing the peak electric field at the edge of device.

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